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COMMENTS AND CORRECTIONS

Comments on "High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits"

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I. INTRODUCTION

In the above article [1], R. A. Jaber *et al.* present the designs of ternary logic circuits based on CNTFET technology. The motivation for designing ternary gates is based on the following assumption quoted in the abstract: "Moreover, multi-valued logic (MVL) circuits provide notable improvements over binary circuits in terms of interconnect complexity, chip area, propagation delay, and energy consumption."

In the article, no comparison has been done between the proposed ternary circuits and the corresponding binary circuits that would confirm or disprove the supposed advantages of MVL circuits. The missing comparison is done in the following section.

II. COMPARING THE TERNARY CIRCUITS AND THE BINARY ONES

A. METHODOLOGY

CNTFET technology is widely used by MVL researchers. It has some advantages. The circuit styles are the same as for CMOS (and FinFET) technology. However, defining the different threshold levels that are needed between levels 0 and 1, or levels 1 and 2 is easier: they are defined according to the inverse function of the transistor diameter, while different masks are needed to get different threshold voltages with CMOS technologies. There is no need for further discussion of that point as we consider that the corresponding binary circuits are implemented in the same CNTFET technology.

According to Shannon's theory of information, when N events have the same probability to occur, the corresponding amount of information is $I=\log_2(N)$ bits (or Shannon). When N=2, I=1 bit. When N=3, I=1.585 bits. A ternary wire carries 1.585 times the amount of information of a binary one. This 1.585 information ratio must be used to compare binary and ternary circuits. For instance, an 8-bit binary adder can be compared to a 5-trit ternary adder as they process approximately the same amount of information; 8/5 is close to 1.585. The difference results from rounding issues.

A ternary circuit will be more efficient than the corresponding binary one if the ratio of complexity is smaller than 1.585. How to define circuit complexity? Many parameters should be considered:

- Number of transistors
- Chip area
- Propagation delays
- Power dissipation
- Etc.

In this comment, we use transistor count to compare binary and ternary circuits. If the transistor count ratio between a ternary circuit and the corresponding binary one is close to 1.585, the comparison would be inconclusive. However, if a huge difference exists in disfavor of the ternary circuit, some conclusion can be derived as it is very doubtful that far more transistors could lead to

- Less interconnects
- Reduced chip area
- Reduced power dissipation
- Reduced propagation delays

B. COMPARING THE DIFFERENT CIRCUITS

The ternary proposed circuits are

- The ternary inverter (STI)
- The ternary Nand (TNand)
- A ternary Half Adder (THA)
- A ternary 1-trit multiplier (TMul)

1) INVERTERS AND NAND GATES

Using the same circuit style, the comparison for inverters and NAND gates is presented in Table 1.

TABLE 1. Comparing elementary gates.

	Ternary	Binary	Ratio
Inverter (STI)	5 T	2 T	2.5
Nand (TNand)	10 T	4 T	2.5

The transistor count ratio is greater than 1.585. Moreover, the ternary circuits have two power supplies instead of one for the binary ones.

2) HALF ADDERS

The proposed ternary half adder has 85 T. In reference [2], a 66 T ternary half adder is used for the comparison, which means that the proposed ternary half adder is not the most efficient one. A conventional binary half adder that has been defined for a CMOS standard cell library [3] is presented in Figure 1. Using a standard cell design guarantees that the circuit has been simulated, fabricated, and tested. This half-adder has 14 T. The transistor count ratio with the ternary half adder presented in [1] is $85/14 \approx 6$! With the ternary half adder presented in [2], the ratio is $66/14 \approx 4.7$.

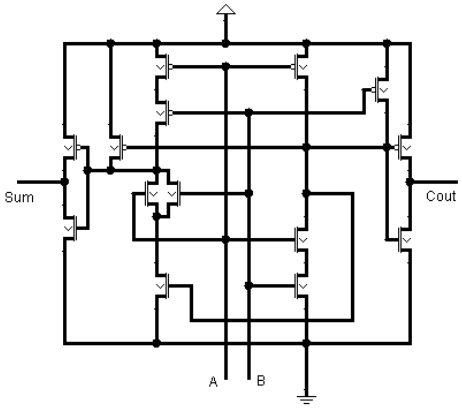

FIGURE 1. 14 T Binary Half Adder.

It could be noticed that the conventional implementation of a binary full adder is 28 T (Figure 2), which means three times fewer transistors than the proposed half adder. Many designs of full adders have been published using less than the 28 T implementation. Discussion of these designs is out of the scope of this comment. Even with the conventional implementation of binary circuits, the transistor count ratio between the proposed ternary half-adder and the binary full adder is greater than the information ratio.

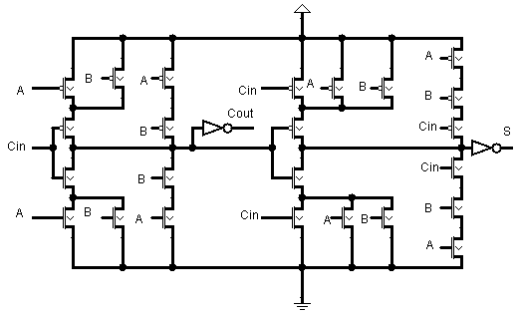

FIGURE 2. 28 T Binary Full Adder.

3) 1-TRIT MULTIPLIER

The proposed ternary 1-trit multiplier has 61 T. The corresponding 1-bit multiplier is implemented by an AND gate (6 T). The transistor count ratio is now 10! It should be noticed that a 1-trit multiplier has two outputs (product and carry terms) as $2*2 = 11$, which is not a good technique for reducing interconnects.

4) COMPARISON RESULT

The transistor count comparison is clearly in disfavor of ternary circuits. The difference becomes huge when implementing elementary 1-trit arithmetic circuits.

C. CONSIDERING ACTUAL ARITHMETIC CIRCUITS

The paper does not consider more significant arithmetic circuits such as M-trit adders or M∗M trit multiplier. A detailed comparison can be found in [3]. The results show the same disadvantage for ternary circuits.

III. CONCLUSION

The transistor count ratio between the proposed ternary circuits and the corresponding ones is always greater or far greater than the information ratio (1.585). Without any doubt, the proposed ternary circuits use more transistors, more chip area, and dissipate more than the corresponding binary ones, disproving the assumption quoted in the abstract of the paper.

In a paper published in IEEE Computer in 1988 [4], we were writing in the conclusion:

"For a long time, researchers in the m-valued area have tried to prove the possible advantages of m-valued circuits compared to two-valued circuits. M-valued circuits and two-valued circuits must not be seen as competitors. If they are seen as such, then two-valued circuits have already won. The key objective is to carefully examine the domains, the applications where m-valued circuits can be useful in the two-valued world." Has the position of ternary and multivalued circuits changed since then?

MVL circuits are restricted to a small niche for fundamental reasons that were detailed in [5]. The only significant use of these circuits is memorization, specifically in flash memories, for which chip area is more important than speed: flash memories store two bits per cell. 8-valued (TLC) memories store 3 bits per cell. In 2018, ADATA, Intel, Micron, and Samsung have launched some SSD products using QLD NAND-memory with 4 bits per cell. While binary flash memories have the advantage of faster write speeds, lower power consumption, and higher cell endurance, M-valued flash memories provide higher data density and lower costs.

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