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A Four-Phase Passive Mixer-First Receiver With a Low-Power Complementary Common-Gate TIA

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ABSTRACT This paper presents a four-phase passive mixer-first receiver using a common-gate (CG) trans-impedance amplifier (TIA), instead of a conventional shunt-feedback amplifier. The four-transistor TIA used in this work combines current-reuse with cross-coupled g_m-boosting to achieve a reduced noise figure (NF) at low power levels. Moreover, complementary derivative-superposition (CDS) linearization within the TIA helps to improve the linearity with no additional power overhead. A prototype receiver is implemented in a 180 nm CMOS technology. The receiver operates from 0.3 to 1.3 GHz with a conversion gain of 21.9 dB. In measurements, the receiver achieved a noise figure of 5.8 dB and an in-band (IB) IIP3 of +7.2 dBm while consuming 0.34 mW power per TIA at 1 GHz. The measured spurious-free dynamic range (SFDR) at 1 GHz is 76.9 dB.

INDEX TERMS Common-gate trans-impedance amplifier (TIA), current-reuse, g_m-boosting, low-power, mixer-first, N-path filter, passive mixer, tunable, wideband.

I. INTRODUCTION

Several new wireless communication standards are being proposed to satisfy the ever-increasing user requirements. In order to support more than one communication standard (existing or new), modern-day radio receivers need to be frequency agile. Since most of these receiver front-ends are used in portable devices, reducing the power consumption is necessary to increase battery life. Typically, two types of power consumption are associated with a receiver [1]–[7]: dynamic and static. The dynamic power consumption is due to the clock buffers driving the mixer switches, while the static power consumption is due to the radio frequency (RF) low noise amplifier (LNA) [8]–[11] and the baseband (BB) trans-impedance amplifier (TIA). In recent years, [12]–[39] have employed a passive mixer as the first block of the receiver instead of an LNA. Mixer-first receivers [12]–[39] offer many advantages over traditional LNA-first receiver architectures [1]–[3], [5], [6], making them suitable for next-generation software-defined radios (SDRs). Some of these advantages include frequency tunability, high linearity, and blocker resilience. A typical four-phase passive mixer-first receiver is shown in Fig. 1(a). In a mixer-first receiver, the TIA provides the input-match and has a major

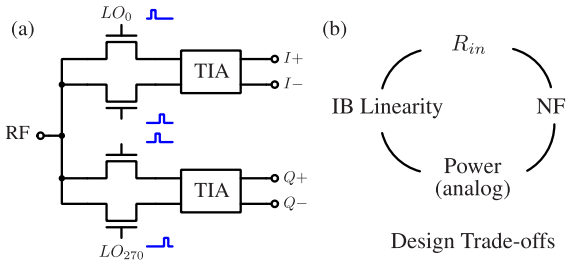

FIGURE 1. (a) A typical four-phase passive mixer-first receiver. (b) Trade-offs in the design of the TIA for a mixer-first receiver [40].

effect on the overall noise and linearity performance of the receiver. Typical trade-offs involved in the design of the TIA for a mixer-first receiver are shown in Fig. 1(b) [40]. In high-linearity mixer-first receivers presented in [20], [23], [24], the BB TIAs consume a significant portion of the total power budget.

Various techniques are proposed in [13]–[15], [34]–[36] to reduce the power consumption in passive mixer-first receivers. The mixer-first receiver in [15] uses a noise-power optimized multi-path current-reused baseband amplifier. An RF-to-BB current-reuse technique is proposed in [34] to reduce the power consumption in N-phase mixer-first receivers. [14] proposed a low-power blocker-tolerant receiver with a gain-boosted mixer-first topology.

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An optimized supply voltage is used to reduce the power consumption in the mixer-first receiver that is demonstrated in [35]. [13] proposed a low-power gain-boosted N-path mixer-first receiver with switched BB extraction. [36] proposed a passive mixer-first low-power wake-up-receiver using a ring-based local oscillator (LO). Overall, the in-band (IB) linearity of low-power mixer-first receivers demonstrated in [13]–[15], [34]–[36] is lower than that of the high-linearity mixer-first receivers [20], [23], [24]. Similarly, the power consumption of the high-linearity mixer-first receivers demonstrated in the literature is higher than that of the low power mixer-first receivers. The objective of the current work is to investigate a TIA topology that is suitable for a high-linearity and low power mixer-first receiver.

The shunt-feedback topology is the most commonly used TIA in mixer-first receivers. Opamp (or OTA) based shunt-feedback TIAs usually exhibit poor linearity and require an additional linearization technique, such as noise-and-distortion cancellation [40], to improve the in-band linearity. The noise-and-distortion canceling technique, which is also frequently used in the design of RF LNAs [10], [11], requires significantly high power to be dissipated in the auxiliary stage. There are not many low power linearization techniques available in the literature [41]. One particular linearization technique that requires zero additional power is the complementary derivative superposition (CDS) [41]. In this work, a capacitor-cross-coupled (CCC) complementary-common-gate (CCG) amplifier is used as a TIA. The four-transistor-TIA presented in this work achieves a high transconductance efficiency. The CDS technique is used to improve the IB linearity with no additional power overhead. The combination of CCC-CCG topology with CDS is not explored previously, even in RF low noise amplifiers [42]–[44]. In this work, the proposed TIA is used to design a frequency-agile receiver front-end working in the frequency range $0.3 - 1.3$ GHz.

The rest of the paper is organized as follows. Section II presents the receiver architecture and describes the proposed baseband TIA. Analysis and design details of the implemented receiver are presented in section III and section IV, respectively. Measurement results are presented in section V. Section VI summarizes the work and concludes the paper.

II. PROPOSED RECEIVER ARCHITECTURE

Fig. 2 shows the block diagram of the implemented four-phase mixer-first receiver using the CCC-CCG TIA in the baseband. In Fig. 2, R_s denotes the source resistance, C_{sh} is the shunt capacitance at the input of the TIA, and C_b is an off-chip dc blocking capacitor at the RF input. The mixer switches are implemented using nMOS transistors. The mixer is dc-coupled to the TIA. The gates of the mixer transistors are biased to resolve the dc-offset problem caused by the dc-coupling. An on-chip frequency divider (/2) and a set of combinational logic circuits are used to generate the four non-overlapping LO signals ($p_1 - p_4$) required for the mixer. The design details of each of these blocks are discussed in section IV. In the next subsection, we present the analysis and working principle of the proposed baseband TIA.

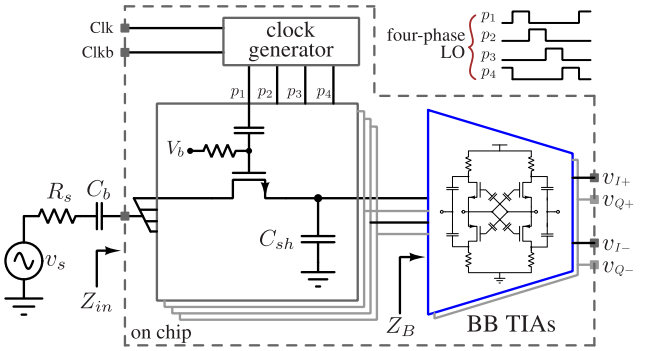

FIGURE 2. Block diagram of the implemented four-phase mixer-first receiver.

A. TIA ARCHITECTURE

The low-power fully-differential complementary common gate TIA used in this work, is shown in Fig. 3(a). The four transistors $M_{1p,n}$ and $M_{2p,n}$ act both as common gate (CG) as well as common source (CS) amplifiers. The two nMOS transistors (M_{1n}, M_{2n}) in Fig. 3(a) form a capacitor-cross-coupled CG pair and enhances the effective g_m of each transistor by a factor of two [45]–[49]. Similarly, the two pMOS transistors (M_{1p}, M_{2p}) form another cross-coupled CG pair. These two cross-coupled CG pairs are vertically stacked so that the dc current is reused. The pMOS and nMOS drain voltages are combined using two output capacitors C_o. The output is taken differentially, as shown in Fig. 3(a). Fig. 3(b) shows the component values used in the implementation of the TIA. Let g_{mp} and g_{mn} represent the transconductances of pMOS and nMOS transistors, respectively. Similarly, r_{op} and r_{on} represent the drain-to-source resistances of pMOS and nMOS transistors, respectively. For a given differential input ($v_{ip} - v_{in}$), the effective transconductance of the circuit can be shown to be equal to $2(g_{mp} + g_{mn})$, which is approximately four times more than the transconductance of a single CG amplifier biased at the same current.

For the purpose of analysis, the circuit can be folded along either the x-axis or the y-axis. Fig. 3(c) shows a reduced circuit obtained by folding the circuit along the x-axis. The transistors M_{1n} and M_{1p} from Fig. 3(a) are combined into a single transistor M_1 in Fig. 3(c), such that the transconductance of M_1 is $g_1 = (g_{mp} + g_{mn})$. Similarly, M_{2n} and M_{2p} are combined into a single transistor M_2. The effective load resistance at each output node of the equivalent circuit is $R_L/2$. C_x represents the effective capacitance present at the output node, where $C_x = (2C_oC_L)/(2C_o + C_L)$ and C_L is the load capacitance. The bias network, consisting of resistor R_c and capacitor C_c, is also scaled, as shown in Fig. 3(c). One can reduce the circuit in Fig. 3(c) further to get the single-ended equivalent version shown in Fig. 3(d). The effective transconductance of the circuit in Fig. 3(d) is

$$G_{m,eff} \approx \frac{1 + s2R_cC_c}{1 + sR_cC_c}(g_{mp} + g_{mn}). \quad (1)$$

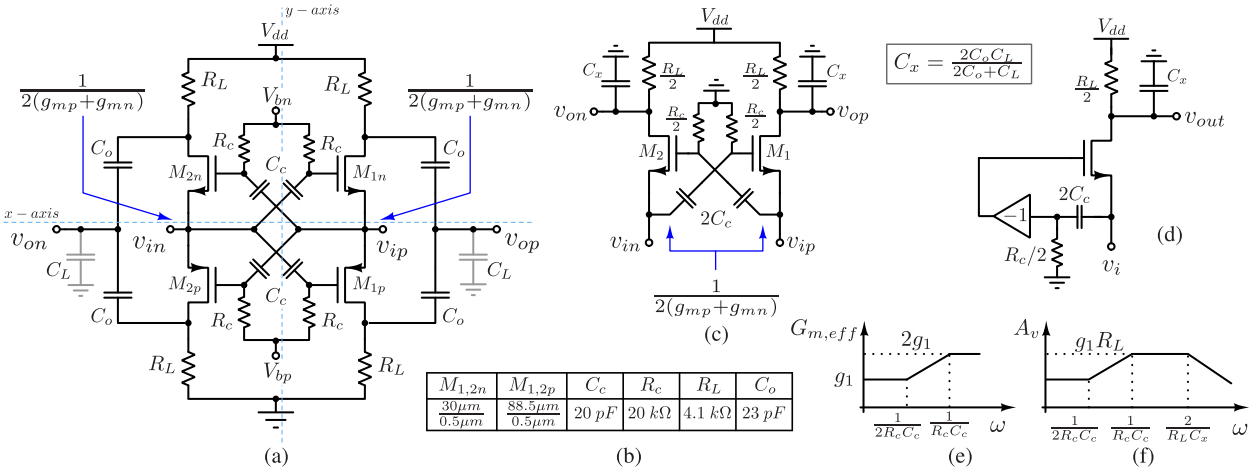

FIGURE 3. (a) Proposed fully-differential low-power baseband TIA, (b) component values used in the implementation of the TIA, (c) simplified differential equivalent circuit of the proposed TIA, (d) single-ended equivalent circuit of the proposed TIA, (e) variation of the effective transconductance of the TIA with frequency, and (f) typical magnitude plot of the TIA with frequency.

Fig. 3(e) shows the typical variation of the effective transconductance with frequency. After the pole frequency $1/(R_cC_c)$, the effective transconductance is $\approx 2(g_{mp}+g_{mn})$. The voltage gain of the circuit in Fig. 3(d) can be obtained as

$$A_v = \frac{(1+s2R_cC_c)(R_L/2)}{(1+sR_cC_c)(1+s(R_LC_x/2))}(g_{mp}+g_{mn}). \quad (2)$$

A magnitude Bode plot of the voltage gain is shown in Fig. 3(f). The mid-band voltage gain of the circuit is $\approx g_1R_L = (g_{mp}+g_{mn})R_L$. Assuming $r_{op}, r_{on} \gg R_L$, the input impedance of the circuit in the passband can be shown to be as follows.

$$Z_B \approx \frac{1}{2(g_{mp}+g_{mn})} \quad (3)$$

From equation (3), for a given input impedance, the CCC-CCG TIA requires approximately four-times smaller current compared to a single CG amplifier. This current is also much smaller than what is typically needed in a shunt-feedback TIA [23], [24].

One key advantage of the CCC-CCG TIA is the inherent linearization possibility using complementary derivative superposition [41], [43]. In the proposed TIA, the distortion is mainly caused by the nonlinear transconductance of the MOS transistors. Considering up to a third-order nonlinearity, the small-signal drain current of a MOS transistor is [50]:

$$i_{ds} = g_m v_{gs} + \frac{g'_m}{2!}{v_{gs}}^2 + \frac{g''_m}{3!}{v_{gs}}^3,$$

where $g_m = \frac{\partial i_{ds}}{\partial v_{gs}}$, $g'_m = \frac{\partial^2 i_{ds}}{\partial {v_{gs}}^2}$ and $g''_m = \frac{\partial^3 i_{ds}}{\partial {v_{gs}}^3}$. The pMOS and nMOS drain currents are combined using two capacitors (C_o) to generate the output current as follows [41].

$$i_{out} = \left[2g_1v_i + 2g_2{v_i}^2 + \frac{4}{3}g_3{v_i}^3\right], \quad (4)$$

where $g_2 = (g'_{mp} - g'_{mn})$ and $g_3 = (g''_{mp} + g''_{mn})$. From the output-current expression in (4), the second-order nonlinear terms can be canceled if g'_{mp} and g'_{mn} are properly matched. Moreover, the intrinsic third-order nonlinearity of the TIA can be reduced by biasing the pMOS and nMOS transistors near the zero-crossings of g''_{mp} and g''_{mn}, respectively. More discussion on the linearization technique is presented during the linearity analysis of the receiver in section III.

III. RECEIVER ANALYSIS

In this section, we present the theoretical analysis of the receiver. Fig. 4 shows an LTI model of the proposed mixer-first receiver [25]. In Fig. 4, R_{sw} is the on-resistance of the mixer switches, and R_{sh} accounts for the power loss due to the up-conversion by harmonics of the LO. In the model, the shunt capacitance (C_{sh}) and the baseband input-impedance (Z_B) are scaled by a factor γ [25], which is topology dependent. For a four-path mixer-first receiver, $\gamma \approx 0.203$ and $R_{sh} \approx 4.3(R_s + R_{sw})$ [25]. The LTI model shown in Fig. 4 is used in the following subsections to derive different performance parameters of the proposed mixer-first receiver.

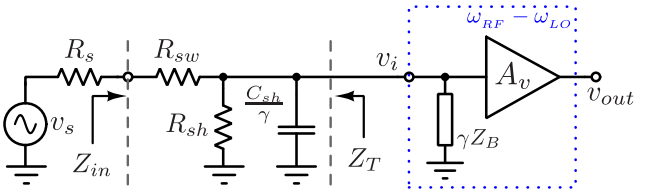

FIGURE 4. An LTI model of the receiver [25].

A. INPUT IMPEDANCE

The input impedance of the TIA is γZ_B, where $Z_B = 1/(2g_1)$ (from equation (3)). Hence, the input impedance of the receiver is

$$Z_{in} = R_{sw} + \left(\frac{1}{\frac{1}{R_{sh}} + j\omega\frac{C_{sh}}{\gamma} + \frac{2g_1}{\gamma}}\right), \quad (5)$$

where $\omega = (\omega_{RF} - \omega_{LO})$. Typically a low resistance is chosen for the mixer switches to achieve a low noise figure. Leaving R_{sw} aside, the designers can vary the transconductance g_1 to achieve impedance matching at the RF input. Fig. 5(a) shows a comparison of analytical (Eq. (5)) and simulated real part of Z_{in} with varying g_1. In this simulation, all ideal components are used, with their values being those corresponding to the actual implementation. From Fig. 5(a), we need a transconductance of around 2 m℧ for a $\approx$ 50 Ω input impedance. Fig. 5(b) and 5(c) show a comparison of analytical (Eq. (5)) and simulated real and imaginary parts of the input impedance at 1 GHz LO frequency for three different g_1 values.

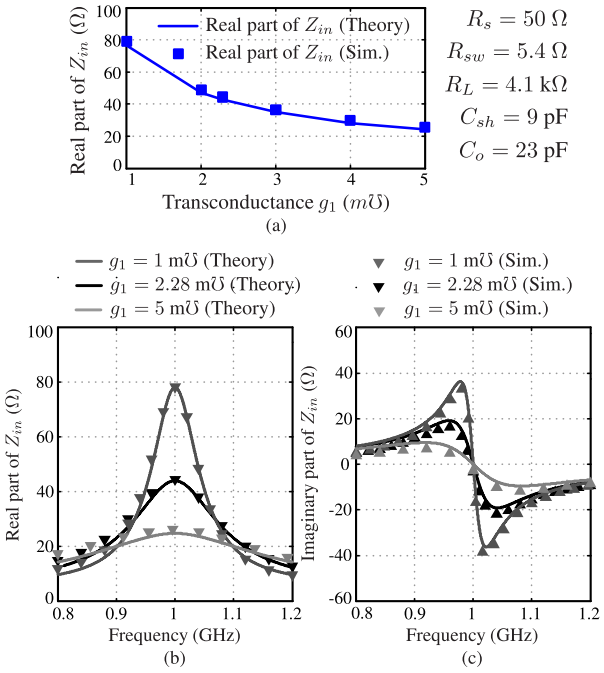

FIGURE 5. (a) Real part of Z_{in} of the receiver with varying baseband transconductance (g_1) for f_{LO} = 1 GHz. Comparison of analytical (Eq. (5)) and simulated values of (b) real and (c) imaginary parts of Z_{in} for f_{LO} = 1 GHz. Ideal transconductors are used to realize the baseband stage in these simulations.

B. CONVERSION GAIN

Let $R_a = (R_s + R_{sw})$. The impedance seen from the baseband input node towards the mixer is

$$Z_T = R_a \,||\, R_{sh} \,||\, \frac{\gamma}{j\omega C_{sh}}.$$

From Fig. 4, the voltage at the input of the baseband TIA (v_i) can be represented as

$$v_i = \frac{1}{1+T_o}\left[\frac{Z_T}{R_a}\right]v_s,$$

where $T_o = 2(g_1/\gamma)Z_T$. The conversion gain of a single-path of the receiver (including the source resistance) is

$$G = \frac{v_{out}}{v_s} = \frac{1}{1+T_o}\left[\frac{Z_T}{R_a}\right]A_v, \tag{6}$$

where A_v is the gain of the baseband TIA and is given by (2). Fig. 6 shows a comparison of the analytical (Eq. (6)) and simulated conversion gain of the receiver with varying g_1.

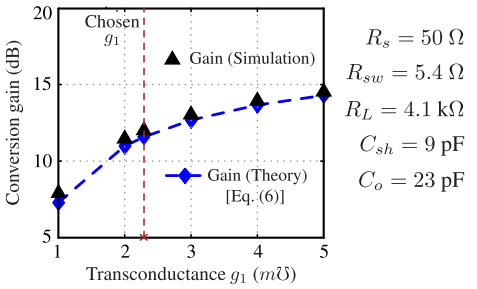

FIGURE 6. Comparison of analytical and simulated conversion gain of a single-path of the receiver (including the source resistance) with varying baseband transconductance (g_1) for f_{LO} = 1 GHz.

C. NOISE

Fig. 7 shows all the noise sources present in the proposed mixer-first receiver. As per the receiver LTI model [25], we need to scale all the baseband components, including g_1, by the factor γ. In Fig. 7, $\overline{i_{n1}}$ represents the instantaneous noise current of the baseband transconductor. $\overline{i_{n1}^2} = 4kT\gamma_m(g_1/\gamma)$, where γ_m is the thermal noise coefficient of a MOS transistor. The instantaneous noise voltage at the output due to $\overline{i_{n1}}$ is

$$\overline{v_{n,out}^2} = \left[\frac{1}{1+T_o}\right]^2\left(\frac{\gamma R_L}{2}\right)^2\overline{i_{n1}^2}$$

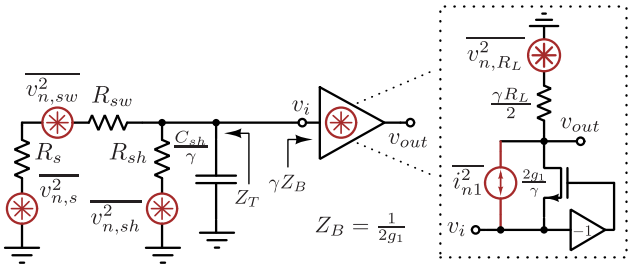

FIGURE 7. LTI model of the mixer-first receiver with all the noise contributing components.

The total noise voltage at the TIA output is

$$\begin{aligned}\overline{v_{n,b}^2} &= \overline{v_{n,out}^2} + \overline{v_{n,R_L}^2} \\ &= \left[\frac{1}{1+T_o}\right]^2\left(\frac{\gamma R_L}{2}\right)^2\left[4kT\gamma_m\frac{g_1}{\gamma}\right] + 2kT\gamma R_L \end{aligned} \tag{7}$$

Let $\overline{v_{n,s}^2} = 4kTR_s$, $\overline{v_{n,sw}^2} = 4kTR_{sw}$ and $\overline{v_{n,sh}^2} = 4kTR_{sh}$ represent the mean square thermal noise voltage densities of the resistors R_s, R_{sw} and R_{sh} respectively. The output noise voltage of the receiver is

$$\overline{v_{n,Rx}^2} = G^2\left[\overline{v_{n,s}^2} + \overline{v_{n,sw}^2} + \left(\frac{R_a}{R_{sh}}\right)^2\overline{v_{n,sh}^2}\right] + \overline{v_{n,b}^2} \tag{8}$$

From (8), the noise factor of the receiver can be derived as

$$\begin{aligned} F &= 1+\frac{R_{sw}}{R_s}+\frac{R_{sh}}{R_s}\left(\frac{R_a}{R_{sh}}\right)^2+\frac{\overline{v_{n,b}^2}}{(G)^2 4kTR_s} \\ &= 1+\frac{R_{sw}}{R_s}+\frac{R_{sh}}{R_s}\left(\frac{R_a}{R_{sh}}\right)^2+\frac{\gamma\gamma_m}{4g_1R_s}\left(\frac{R_a}{Z_T}\right)^2 \\ &\quad +\frac{\gamma(1+T_o)^2}{2{g_1}^2R_sR_L}\left(\frac{R_a}{Z_T}\right)^2 \end{aligned} \tag{9}$$

Fig. 8 shows a comparison of analytical (Eq. (9)) and simulated noise figures for different values of g_1. In this work, a g_1 of 2.28 m℧ is chosen for the implementation. This design choice ensures a good input match, a single-path conversion gain of $\approx$ 12 dB (including the source resistance), and an estimated NF < 4 dB.

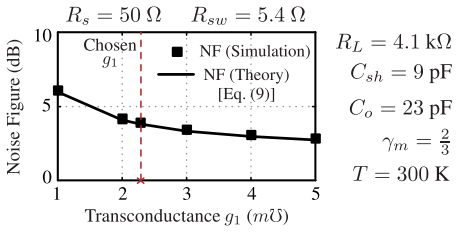

FIGURE 8. Comparison of analytical and simulated noise figure of the receiver with varying baseband transconductance (g_1) for f_{LO} = 1 GHz. Ideal transconductors with noise current-sources are used in the baseband stage for these simulations.

D. LINEARITY

In general, the mixer-switches are highly linear [17], and the overall in-band linearity of a mixer-first receiver is dominated by the linearity of the baseband TIA. In the present analysis, it is assumed that the mixer switches are completely linear, and distortion is caused by the baseband transconductors only.

Fig. 9 shows an in-band LTI model of the mixer-first receiver, including the nonlinear current components in the TIA. The following equation can be written using the nodal analysis on the circuit shown in Fig. 9.

$$\frac{v_i-v_s}{R_a}+\frac{v_i}{R_{sh}}+2\frac{g_1}{\gamma}v_i+2\frac{g_2}{\gamma}{v_i}^2+\frac{4}{3}\frac{g_3}{\gamma}{v_i}^3=0 \tag{10}$$

Using the output current equation in (4), the output voltage can be represented as

$$v_{out}=\frac{\gamma R_L}{2}\left[2\frac{g_1}{\gamma}v_i+2\frac{g_2}{\gamma}{v_i}^2+\frac{4}{3}\frac{g_3}{\gamma}{v_i}^3\right] \tag{11}$$

Using equations (10) and (11), the fundamental and third harmonic coefficients of the gain are

$$A_1=\frac{g_1R_L}{(1+T_o)}\left[\frac{Z_T}{R_a}\right],$$

$$A_3=\frac{2}{3}\frac{g_3R_L}{(1+T_o)^4}\left[1-\frac{3{g_2}^2}{g_1g_3}\frac{T_o}{(1+T_o)}\right]\left[\frac{Z_T}{R_a}\right]^3.$$

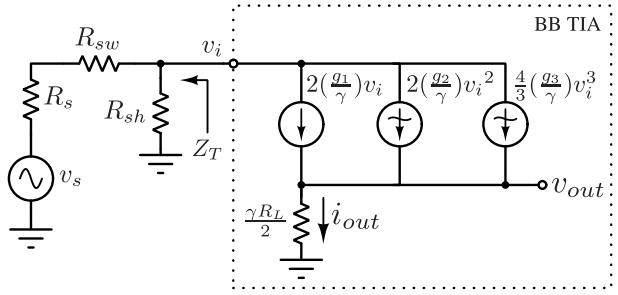

FIGURE 9. An in-band LTI model of the mixer-first receiver showing the distortion currents of the baseband TIA.

Hence, the in-band input third-order intercept point (IIP3) of the receiver is

$$\begin{aligned} A_{IIP3,IB} &= \sqrt{\frac{4}{3}.\left|\frac{A_1}{A_3}\right|} \\ &= \sqrt{2\left|\frac{g_1}{g_3}.\frac{(1+T_o)^3}{\left[1-\frac{3{g_2}^2}{g_1g_3}\frac{T_o}{(1+T_o)}\right]}.\left[\frac{R_a}{Z_T}\right]^2\right|} \end{aligned} \tag{12}$$

In the above expression, the term $\left[\frac{3{g_2}^2}{g_1g_3}\frac{T_o}{(1+T_o)}\right]$ in the denominator is due to the second-order interaction [41], [43]. The even-order harmonics, due to feedback, gets multiplied by the input tones to generate this distortion term. This term degrades the IIP3 because g_1 and g_3 usually have opposite signs. However, if g'_{mp} and g'_{mn} are properly matched, then g_2 is almost equal to zero. g_3 can be reduced if pMOS and nMOS transistors are appropriately biased, such that both g''_{mp} and g''_{mn} have near-zero values. Fig. 10(a) shows a comparison of simulated and analytical (Eq. (12)) IB-IIP3 of the receiver with varying g_3. The second-order distortion coefficient (g_2) is assumed to be zero in the analysis shown in Fig. 10(a). Fig. 10(b) shows the effect of second-order distortion on the receiver IIP3. It is observed that the IB-IIP3 of the receiver decreases with an increase in second-order distortion.

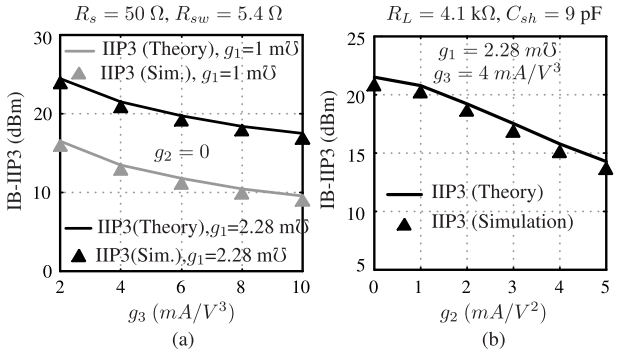

FIGURE 10. (a) Comparison of simulated and analytical (Eq. (12)) IB-IIP3 of the receiver at f_{LO} = 1 GHz with varying g_3. g_2 is considered zero for this analysis. (b) Effect of second-order distortion on the IB-IIP3 of the receiver at f_{LO} = 1 GHz for g_1 = 2.28 m℧ and $g_3 = 4\ mA/V^3$. Ideal transconductors with nonlinear current source models are used in the baseband stage for these simulations.

The CDS linearization technique is not effective in improving the out-of-band (OOB) IIP3 of the receiver. One can set

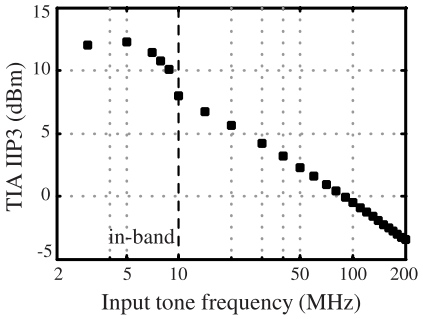

FIGURE 11. Simulated IIP3 of the proposed TIA with the varying input tone frequency. The component values used in the implementation of the TIA are shown in Fig. 3(b).

$|g_2| \approx 0$ (by proper design of the transconductors) at low frequencies, but $|g_2|$ increases with frequency due to parasitic feedback paths [41]. Also, the optimum gate-bias voltage for a MOS transistor changes with varying input-tone frequency [51]. Hence, for a specific gate-bias voltage, the linearity improvement may not be uniform with varying input tone frequencies. Fig. 11 shows the simulated IIP3 of the designed TIA with varying input-tone frequency. The component values and the bias-voltages used in the TIA implementation are given in the following section. From Fig. 11, it is observed that the linearity performance of the TIA degrades beyond its bandwidth (which is 10 MHz in the current design).

In order to understand the effect of input tone frequency on the IIP3 of the baseband TIA, the linear $\{P_{f_1}, P_{f_2}\}$ and IM3 $\{P_{(2f_1-f_2)}, P_{(2f_2-f_1)}\}$ output components are plotted in Fig. 12 with varying input power and for different input tone combinations. The magnitudes of the two IM3 components are completely identical when the two input tones are in-band, as shown in Fig. 12(a) and 12(b). Even when the tones are just outside the bandwidth of the TIA, the IM3 components show good symmetry (as shown in Fig. 12(c)). However, as the tones move further away from the TIA-bandwidth, some IM3 mismatch starts to appear, as shown in Fig. 12(d). When the two input tones are within the bandwidth of the system, the even-order terms go through identical responses, and good symmetry can be observed between the higher $(2f_2 - f_1)$ and lower $(2f_1 - f_2)$ IM3 components [52]. However, when the input tones are out-of-band, the different even-order terms experience different amplitude and phase responses, eventually leading to the asymmetry in the IM3 components [52]. This asymmetry becomes larger as the offset between the two input tones increases [52].

IV. RECEIVER DESIGN

A. DESIGN OF NON-OVERLAPPING CLOCK GENERATOR

An on-chip clock divider and a set of combinational logic circuits are used to generate the four non-overlapping clock signals $p_1 - p_4$. Fig. 13 shows the gate-level schematic of the non-overlapping clock generator. An external clock signal is converted to a differential clock using an off-chip splitter

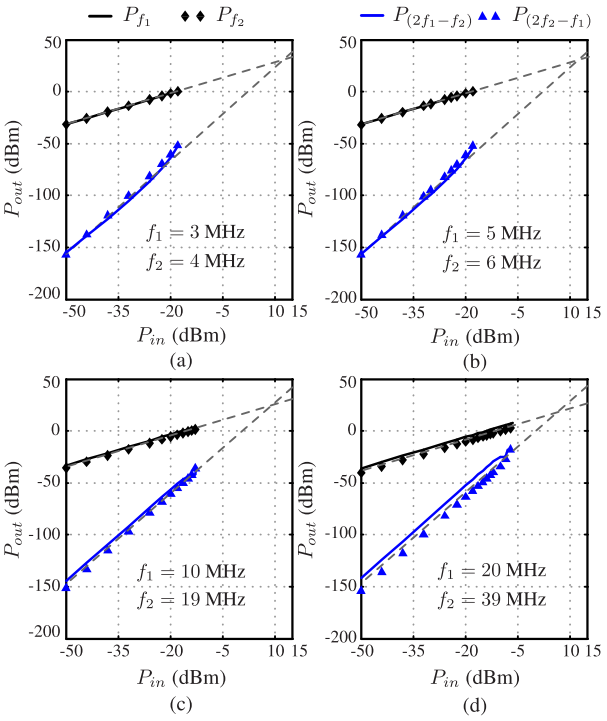

FIGURE 12. Simulated output power levels P_{f_1}, P_{f_2}, $P_{(2f_1-f_2)}$, $P_{(2f_2-f_1)}$ of the designed TIA with varying P_{in} for the following input tone frequencies: (a) $f_1 = 3$ MHz, $f_2 = 4$ MHz, (b) $f_1 = 5$ MHz, $f_2 = 6$ MHz, (c) $f_1 = 10$ MHz, $f_2 = 19$ MHz and (d) $f_1 = 20$ MHz, $f_2 = 39$ MHz.

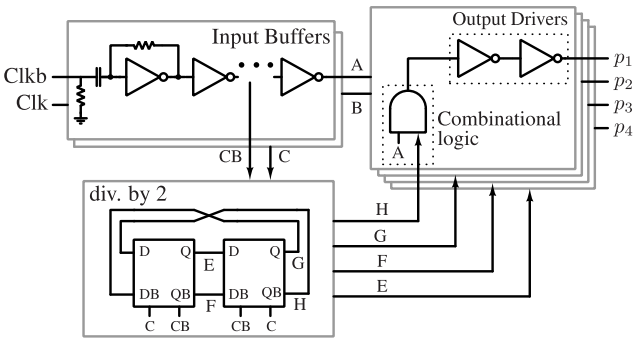

FIGURE 13. Schematic of the non-overlapping clock generator.

(SYPJ-2-33+) and then fed to the non-overlapping clock generating circuit. The first stage of the non-overlapping clock generator is a shunt-feedback LNA that provides a broadband input match. The high-frequency clock (at $2f_{LO}$) is then converted to a square wave using a two-stage inverter chain and fed to the divide by two circuit. The frequency divider consists of back-to-back connected two D-latches, as shown in Fig. 13. The output of the divide by two circuit is a set of four 50% duty-cycled clocks at f_{LO}. These 50% duty-cycled clocks are combined with the $2f_{LO}$ clocks to generate the non-overlapping 25% duty-cycled clocks at f_{LO}. A chain of inverter is used at each output of the non-overlapping clock generator to drive the mixer switches.

B. MIXER DESIGN

Switches of the mixer are realized using nMOS transistors. Separate biasing is applied at the gates of the nMOS transistors using a resistor of 11 kΩ and a capacitor of 3.3 pF, as shown in Fig. 2. The gate biasing helps to overcome the dc offset present at the source nodes of mixer-switches. The size of the switches pose a trade-off between the dynamic power consumption and the noise figure of the receiver. The IIP3 of the receiver is also a strong function of the switch width below a threshold value. Fig. 14 shows the variation of noise figure and IIP3 of the mixer switches with varying gate-width in 180 nm CMOS process. Ideal TIAs are used in this simulation. A size of $120\mu m/0.18\mu m$ is chosen for the nMOS transistors in this implementation. From Fig. 14, the theoretical bounds defined by the mixer are NF $\geq$ 1.9 dB and an IIP3 of $\leq +18$ dBm. Each mixer switch is followed by a shunt capacitor (C_{sh}) of 9 pF in the current implementation.

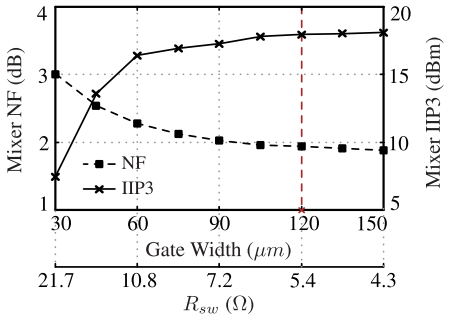

FIGURE 14. Simulated noise figure and IIP3 of the mixer switches with varying gate-width for a channel length of 180 nm.

C. BASEBAND TIA DESIGN

The baseband TIA is the only block that consumes the static power in a mixer-first receiver. Since the objective of the current work is to design a low power mixer-first receiver, the TIA is optimized for the smallest power consumption possible. For 50 Ω impedance matching at the RF input, we need a transconductance of $\approx$ 1.14 $m\mho$ per transistor (g_1 = 2.28 $m\mho$) in the TIA. The bias network (as shown in Fig. 3(a)) of the TIA is implemented using a resistor (R_c) of 20 kΩ and a capacitor (C_c) of 20 pF. The drain nodes of the MOS transistors are terminated with load resistances (R_L) of 4.1 $k\Omega$. The pMOS and nMOS drain voltages are combined using two output capacitors (C_o) of 23 pF.

The dimensions and the biasing voltages of the transistors are chosen to optimize the linearity. In this design, nMOS transistors of $(W/L)_n = 30\mu m/0.5\mu m$ and pMOS transistors of $(W/L)_p = 88.5\mu m/0.5\mu m$ are used. Fig. 15(a), 15(b), and 15(c) show the first-order, second-order, and third-order transconductances of the nMOS and pMOS transistors used in this design. For best linearity, one has to operate the nMOS and pMOS transistors at bias voltages, which results in $g''_{mn} \approx g''_{mp} \approx 0$. One also has to ensure $g'_{mn} \approx g'_{mp}$ to mitigate the second-order interaction induced third-order nonlinearity.

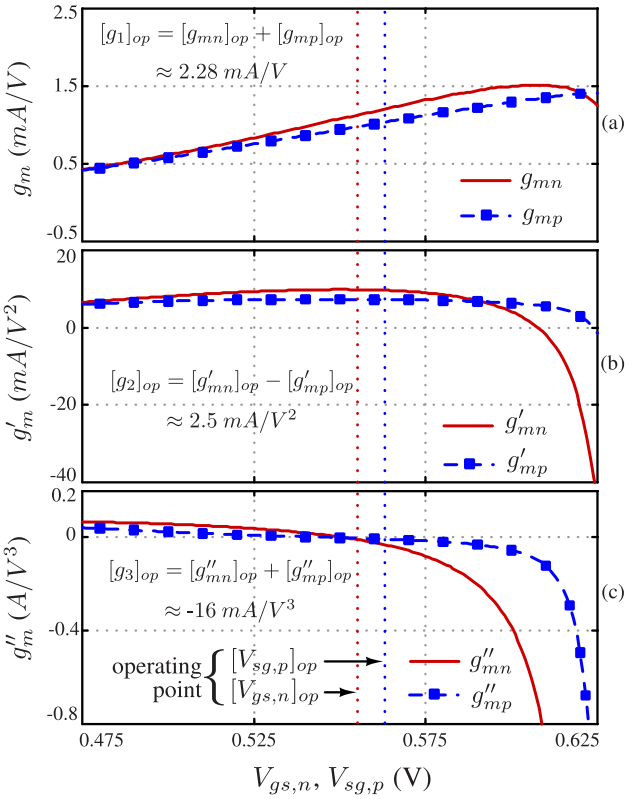

FIGURE 15. Simulated (a) transconductance, (b) second-order distortion coefficients and (c) third-order distortion coefficients of the pMOS and nMOS transistors with varying gate-to-source voltage. Selected transistor dimensions are: $(W/L)_n = 30\mu m/0.5\mu m = 60$, $(W/L)_p = 88.5\mu m/0.5\mu m = 177$.

From Fig. 15, the optimum gate-to-source voltages are found to be $\approx$ 555 mV for nMOS and $\approx$ 563 mV for pMOS transistors.

The optimum gate-to-source voltage for best linearity also depends on the channel length of the transistors. Let, $V_{zc,n}$ and $V_{zc,p}$ represent the g''_m-zero-crossing gate-to-source voltage of the nMOS and pMOS transistor, respectively. Fig. 16(a), 16(b) shows the typical variations of g''_m-zero-

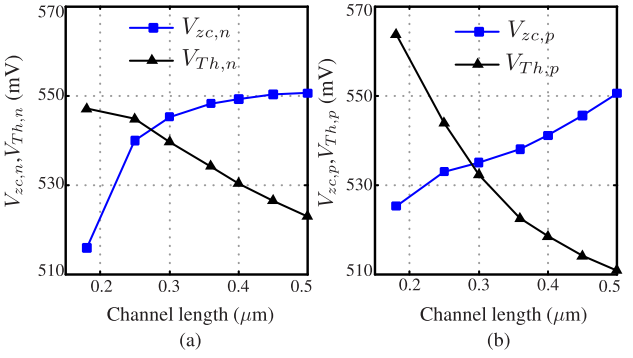

FIGURE 16. Variation of g''_m-zero-crossing gate-to-source voltage and threshold voltage of an (a) nMOS, (b) pMOS transistor with channel length. $(W/L)_n = 60$ and $(W/L)_p = 177$ is used in these simulations.

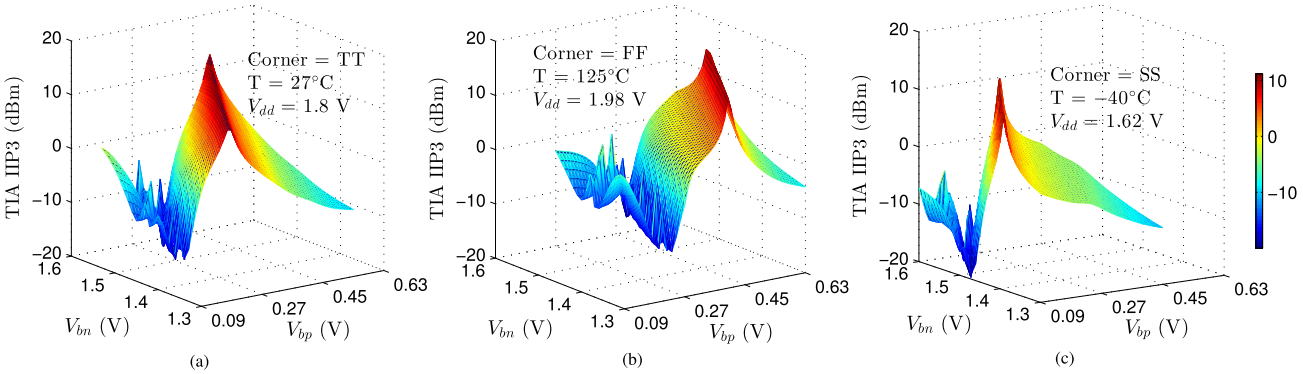

FIGURE 17. Simulated IIP3 of the proposed TIA with varying bias voltages V_{bp} and V_{bn} at the following three PVT settings: (a) corner = TT, V_{dd} = 1.8 V, T = 27° C, (b) corner = FF, V_{dd} = 1.98 V, T = 125° C and (c) corner = SS, V_{dd} = 1.62 V, T = −40° C.

crossing voltage and threshold voltage with varying channel length. From Fig. 16, it can be observed that $V_{zc,n}$ (or $V_{zc,p}$) is lower than the threshold voltage $V_{Th,n}$ (or $V_{Th,p}$) for small channel length devices. Therefore, one has to operate the transistors in sub-threshold in small channel-length designs for the CDS linearization technique to be effective. In general, sub-threshold operation leads to reduced bandwidth and increased noise. As a result, the implementation of the CDS linearization technique in advanced technology nodes while maintaining the required bandwidth and noise performance is a challenging task. In the present implementation, 0.5 μm channel length is chosen to avoid sub-threshold operation, and also to reduce the flicker noise.

In the proposed TIA, one can set $V_{gs,n} \approx 555$ mV and $V_{sg,p} \approx 563$ mV by different combinations of V_{bn} and V_{bp} values. Fig. 17(a) shows the variation of TIA IIP3 with bias voltages V_{bn} and V_{bp}. In the present implementation, we have chosen $V_{bn} = 1.45$ V, and $V_{bp} = 0.33$ V. Fig. 17(b) and 17(c) show the IIP3 variation at extreme PVT corners. From Fig. 17, the TIA can achieve high linearity performance at any given PVT condition subject to the proper selection of the bias voltages. The automatic setting of bias voltages for high IIP3 requires further research and is not explored in this work.

Fig. 18 shows the distribution of TIA IIP3 under the statistical variation of process and device mismatches. The obtained

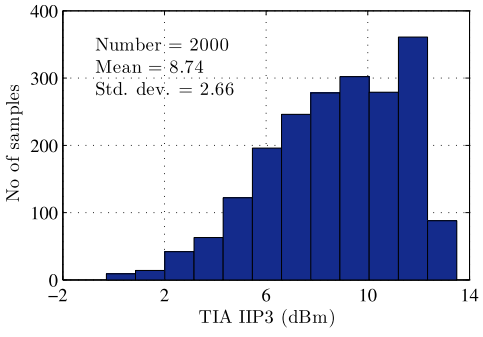

FIGURE 18. Variation of TIA IIP3 from Monte-Carlo simulation.

samples have a statistical mean of 8.74 dBm with a standard deviation (σ) of 2.66 dBm. Around 64.2% of the total samples lie within $\pm$ 1σ of the mean value.

V. MEASUREMENTS

A prototype receiver is implemented in a standard 180 nm CMOS technology. The chip is enclosed in a 56-pin QFN package and mounted on an FR-4 PCB for testing. The testing PCB and the chip micrograph is shown in Fig. 19(a) and 19(b), respectively. All bias voltages (for switches and transconductors) are supplied externally. If not mentioned otherwise, the following TIA bias voltages are used in all the measurements: $V_{bn} = 1.45$ V and $V_{bp} = 0.33$ V.

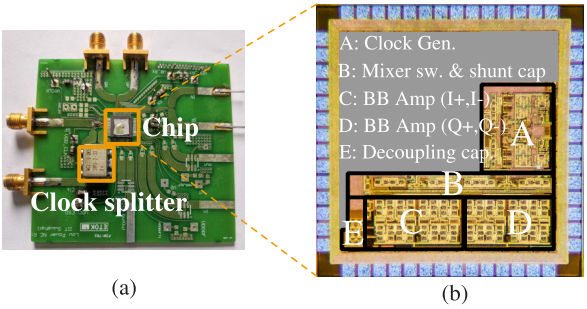

FIGURE 19. Photographs of the (a) testing board and (b) chip.

The receiver is tunable from 0.3 GHz to 1.3 GHz. Depending on the frequency of operation, the clock path consumes 21.6-75 mA of current from a 1.8 V supply voltage. Each baseband TIA consumes around 188.9 μA from a 1.8 V power supply resulting in a 0.68 mW of power consumption for the receiver (Rx). The non-overlapping clock generator consumes $\approx$ 100 mW/GHz from a 1.8 V supply voltage. Table 1 shows the dynamic power distribution of the non-overlapping clock generator at 1 GHz.

Fig. 20 shows the measured $|S11|$ of the receiver. The receiver has an $|S11| < -15$ dB and a conversion gain greater than 20 dB over the frequency range 0.3-to-1.3 GHz. Fig. 21 shows the measured conversion gain and noise figure of

TABLE 1. Dynamic Power Distribution of the Clock Generator at 1 GHz.

Block	Power (mW)
Input buffers	44.6
div. by 2	13
Combinational logic	14.7
Output drivers	27.7
Total	100

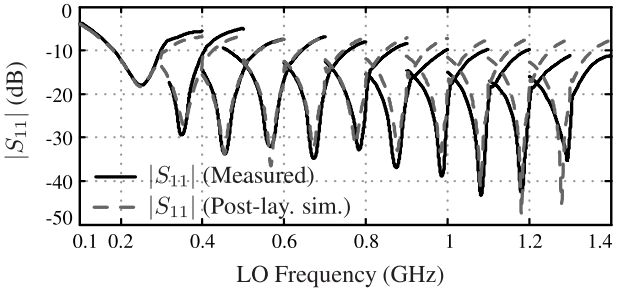

FIGURE 20. Measured $|S_{11}|$ plot of the receiver at different LO frequencies.

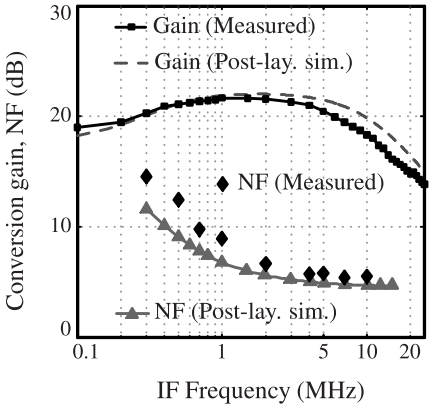

FIGURE 21. Measured conversion gain and noise figure of the receiver at 1 GHz LO with varying IF frequency.

the receiver at 1 GHz LO with varying IF frequency. The measured BB bandwidth is ≈ 10 MHz. The designed receiver has an almost flat noise figure for > 3 MHz IF frequency. The measured conversion gain and NF of the receiver at different LO frequencies are shown in Fig. 22. The measured NF varies from 5.7 dB to 6.3 dB over the LO frequency range 0.3-to-1.3 GHz for an IF frequency of 4 MHz. Fig. 23 shows the simulated NF of the receiver at 1 GHz LO frequency in the presence of a blocker at two different offset frequencies: $\Delta f/BW = 5$ and $\Delta f/BW = 10$. Fig. 24(a) and 24(b) show the measured receiver gain with varying bias voltage V_{bp} and V_{bn}, respectively.

The imbalance between the in-phase (I) and the quadrature-phase (Q) output paths are characterized using the test setup shown in Fig. 25(a). The gain and phase mismatches are estimated from the time-domain waveforms of the output signals using an oscilloscope. Fig. 25(b) shows the four output signals ($I+, I-, Q+, Q-$) when the LO is at 500 MHz, and the RF input is at 498 MHz. For 500 MHz LO,

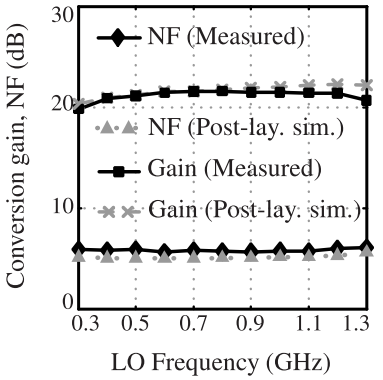

FIGURE 22. Measured conversion gain and noise figure of the receiver at different LO frequencies.

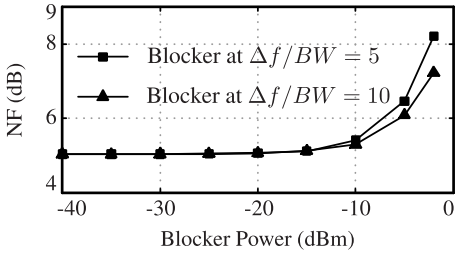

FIGURE 23. Simulated noise figure of the receiver at 1 GHz LO frequency in the presence of a blocker.

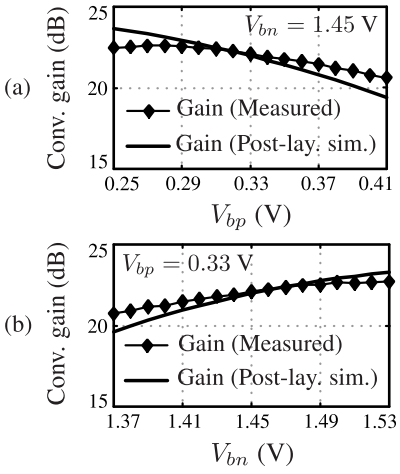

FIGURE 24. Measured conversion gain of the receiver at 1 GHz LO frequency with varying bias voltage (a) V_{bp} and (b) V_{bn}.

the measured gain and phase errors are ≈ 0.1 dB and ≈ 3.6°, respectively, which leads to an estimated image rejection of ≈ 30 dB [53]. Fig. 26(a) and 26(b) show the measured I/Q gain and phase errors at different LO frequencies, respectively. Between 0.4-1.1 GHz, the gain error is ≤0.5 dB, and the phase error is ≤ 5.5°. The current implementation of the receiver does not have an I/Q calibration circuitry, which, if present, can reduce the I/Q mismatches.

Fig. 27 shows the measured IB-IIP3 of the receiver at different LO frequencies. The receiver has ≈ +7.2 dBm

TABLE 2. Performance Comparison with Recent Mixer-First Receivers.

		Tech. (nm)	Gain (dB)	f_{RF} (GHz)	BB BW (MHz)	NF (dB)	IB-IIP3 (dBm)	IB-SFDR (dB)‡	OOB-IIP3 (dBm @ $\Delta f/BW$)	Supply (V)	Power (mW)		Area (mm^2)
											Rx	Clock	
This Work		180	21.9	0.3-1.3	10	5.7-6.3	+7.2	76.9	4.5 @ 2	1.8	**0.68**	100$^{\diamond}$	0.728
High Linearity	JSSC20 [40]	180	31.4	0.2-1.2	18	3.4-4	+14.5	83.2	39.8	1.8	19.8	45-135	0.54
	SSCL19 [27]	28	32.4	0.5-2	130	5.5$^{\clubsuit}$	$-12^{\boxplus}$	64.3	21 @ 3	1.8/1.2	21.6	7.8$^{\diamond}$	0.16
	JSSC19 [23]	28	16	0.1-2	6.5	4.1-10.3	$+5^{\dagger}$	76.6	44 @ 12.3	1.2/1	30	33$^{\diamond}$	0.49
	JSSC18 [24]	45^{π}	21	0.2-8	10	2.3-5.4	$0^{\dagger}$	73.4	39 @ 8	1.2	50	30$^{\diamond}$	0.8
	ISSCC17 [21]	65	23	0.1-1	1.25-20	$7^{\in}$	+8	76.7	21 @ 1.2	1.2/1	$64-84$ mA$^{\perp}$		2.3
	TMTT16 [28]	28	35	0.4-3.5	50	2.4-2.6	$+8^{\dagger}$	79.7	20.5 @ 3.3	1.1/1.5$^{\theta}$	38-75*		0.23
	ESSCIRC15 [37]	65	40	0.8-3	–	5.5-7.8	–	–	17	–	$32-38$		0.5
	JSSC14 [33]	65	26.5	0.2-2.6	12	7.5	+21	85	18 @ 37.5	1.2	13.9	3.4-22.8	< 0.2
Low Power	RFIC18 [38]	45^{π}	$14-40$	0.1-3	20-165	3-6	–	–	–	0.9/1.8	16$^{\odot}$		1.95
	JSSC17 [13]	65	36	0.84-1.88	9	3.2^{ξ}	−12	65.9	8 @ 8.88	1	13	3.3-7	0.038$^{\nabla}$
	ISSCC15 [14]	65	38	0.1-1.5	2	1.5-2.9	–	–	13	0.7/1.2	11$^{\ominus}$		0.028
	JSSC14 [34]	65	51 ± 1	0.15-0.85	9	4.6 ± 0.9	−12	65.5	17.4	1.2/2.5	7.5	3.1-8.7	0.55
	JSSC13 [15]	65	37	0.7-3.2	$0.1-20$	7-16	$-43^{\dagger}$	42.7	6	1.3	1.8	8.2-10.2$^{\bullet}$	2.9
	RFIC13 [32]	65	20-36	0.1-0.8	$5^{\dagger}$	3.6$^{\square}$	–	–	7$^{\square}$	1.2/1.6	23$^{\times}$		0.33
RF Noise Canceling	JSSC15 [12]	65	42	0.7-3.8	10	$1.6-3.2$	$-10^{\dagger}$	68.3	1 @ $5^{\dagger}$	1.2	7.44-20.4	12-26.4	0.15
	JSSC12 [20]	40	72	0.08-2.7	2	1.9	–	–	13.5 @ 40	1.3	31.2	3.9-46.8	1.2
Discrete Time	JSSC19 [22]	22^{β}	13-14	0.6-1.3	16	5-6	–	–	25 @ 10	0.8	$0^{\heartsuit}$	0.4-0.78	0.23
	JSSC18 [16]	65	35	0.1-0.6	–	4.6-9	–	–	31	1.1/1.25	24	9.5-55.8	1.63

‡ IB-SFDR = $\frac{2}{3}$[IB-IIP3+174-10log(1MHz)-NF]; ♣ At $f_{LO} = 2$ GHz; ◇ per 1 GHz; † Estimated from figures; π SOI; θ 1.5 V for LDO; ⊞ Two-tones test with the first tone near center band and the second one near band edge; ⋆ Total power (includes on-chip LDOs); ξ At 1.88 GHz; ∈ Excludes balun loss; ⊥ Total current; ∇ Includes transmitter (Tx) area; • Includes VCO power; ⊙ At 1 GHz; ⊖ At 1.5 GHz; □ At maximum gain setting; × At 800 MHz LO; β FDSOI; ♡ No integrated baseband.

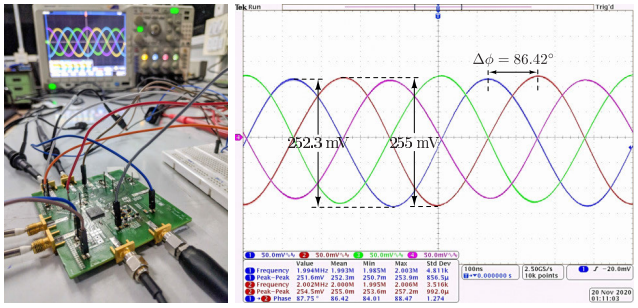

FIGURE 25. (a) Photograph of the test setup for the measurement of I/Q gain and phase errors. (b) The four output waveforms ($I+$, $I-$, $Q+$, $Q-$) for −23 dBm 498 MHz RF input with 500 MHz LO.

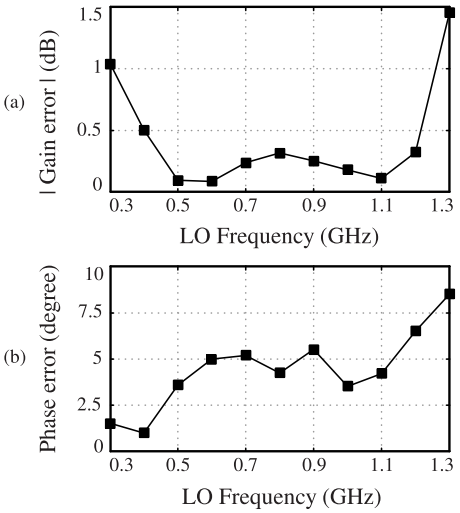

FIGURE 26. Measured I/Q (a) gain error and (b) phase error of the receiver at different LO frequencies.

measured IB-IIP3 at 1 GHz LO frequency. Bias voltages of the baseband TIA play an important role in the obtained IIP3 of the receiver. Fig. 28(a) and 28(b) show the measured IB-IIP3 of the receiver with varying V_{bp} and V_{bn}, respectively. Out-of-band (OOB) IIP3 measurements are carried out using two tones at $f_1 = f_{LO} - \Delta f$ and $f_2 = f_{LO} - 2\Delta f + 1$ MHz, where f_{LO} is the LO frequency and Δf is the frequency offset from the LO frequency. The receiver has an OOB-IIP3 of 4.5 dBm at an offset of twice the band-

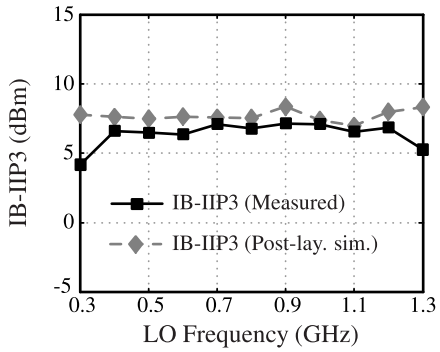

FIGURE 27. Measured IB-IIP3 of the receiver at different LO frequencies.

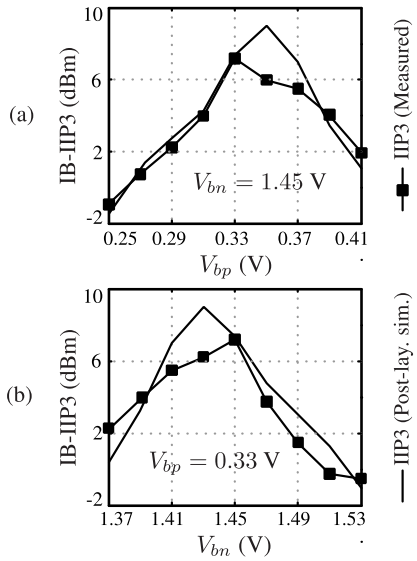

FIGURE 28. Measured IB-IIP3 of the receiver at 1 GHz LO frequency with varying TIA bias voltage (a) V_{bp} and (b) V_{bn}.

width. Fig. 29 shows the measured OOB-IIP3 of the receiver at 1 GHz LO frequency for varying $\Delta f/BW$. Similarly, OOB-IIP3 points are measured at various LO frequencies for a fixed frequency offset $\Delta f/BW = 2$. Fig. 30 shows the variation of OOB-IIP3 across the LO frequency range (for a $\Delta f/BW = 2$).

Table 2 shows a comparison of this work with different mixer-first receivers reported in the literature. The IB-IIP3 of the proposed receiver is on par with the high-linearity mixer-first receivers and much better than the low-power mixer-first receivers or noise-canceling mixer-first receivers. The clock power consumption of the proposed receiver is slightly on a higher side, but can be significantly reduced if implemented in an advanced CMOS process (because of reduced parasitic capacitances in an advanced CMOS process). Although [12], [20] achieve a better noise figure by employing the RF noise-canceling technique, their Rx power consumption is much higher than the proposed work. The proposed receiver has achieved a wider frequency tuning range with similar noise performance as compared to

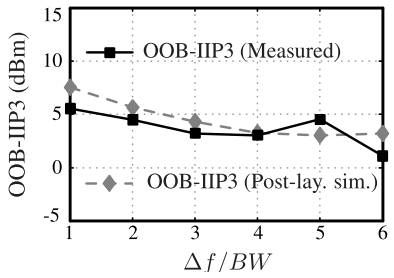

FIGURE 29. Measured OOB-IIP3 of the receiver for varying $\Delta f/BW$ at 1 GHz LO frequency.

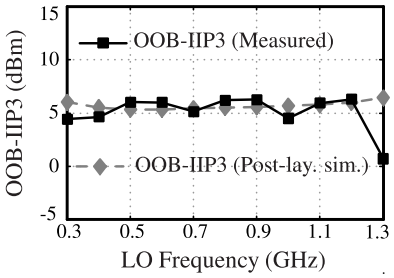

FIGURE 30. Measured OOB-IIP3 of the receiver at different LO frequencies for $\Delta f/BW = 2$.

recent discrete-time mixer-first receivers [16], [22]. Overall, the mixer-first receiver presented in this work achieved a good in-band SFDR while consuming the lowest Rx power.

VI. CONCLUSION

In this paper, we have demonstrated a four-phase passive mixer-first receiver with a low-power complementary common-gate TIA. The TIA is designed to exploit cross-coupled g_m-boosting along with complementary derivative superposition linearization. The receiver presented in this work has achieved an NF of 5.8 dB and an IB-IIP3 of +7.2 dBm with the lowest power consumption of 0.68 mW for baseband circuitry. Overall, the receiver achieved a measured IB-SFDR of 76.9 dB at 1 GHz.

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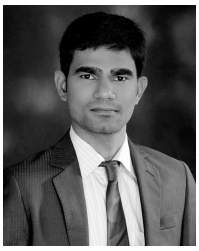

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