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CMOS Plasmon Detector With Three Different Body-Biasing MOSFETs

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ABSTRACT A complementary metal–oxide–semiconductor (CMOS) plasmon detector using metal–oxide–semiconductor field–effect transistors (MOSFETs) biased at three different body voltages is proposed for high sensitivity and a wide dynamic range. The detection core consists of three differential MOSFET detectors biased at different body voltages based on the photoresponse variation depending on the body potential. The sensitivity of the proposed detector is improved through an increase in the nonlinearity owing to the uses of transistors biased by negative body voltages, and the dynamic range of the detector is widened through the parallel-connected detectors individually biased at different body voltages. A 200-GHz signal is simultaneously incident to the detection cores configured in-parallel through the integrated differential antenna, and DC voltages converted using the different photoresponsivity of the cores are current-combined at the preamplifier and amplified with a three-stage folded-cascode operational amplifier. Simulation and measurement results of the proposed detector designed using TSMC 0.25-μm CMOS technology show that the negative body-biasing (set to 0, -0.2, and -0.4 V), in the MOSFET can improve the voltage responsivity of 2.63 times, the sensitivity by 2.9-fold compared to zero body-biasing, reaching a dynamic range of 11.1% in the CMOS plasmon detector. Raster-scanned imaging for 60-μm thick copper tapes with a line width of $6-12$ mm attached to 10-mm thick Styrofoam demonstrates that the signal-to-noise ratio of 200-GHz images can be improved from 25.5 dB to 30.6 dB when using the proposed detector with three different body-biased MOSFETs.

INDEX TERMS Body biasing, CMOS plasmon detector, high sensitivity, image SNR, negative body potential, subthreshold slope, terahertz imaging, wide dynamic range.

I. INTRODUCTION

Since Dyakonov and Shur first introduced the mechanism of plasma-wave detection in a field-effect transistor, plasmon detectors have been an attractive technology for measuring the magnitude of high-frequency signals above the cut-off frequency of the transistor when implemented using a low-cost semiconductor process [1]–[5]. Complementary metal − oxide − semiconductor (CMOS) detectors based on the plasmon-wave theory have had limited applicability in imaging applications within the terahertz band owing to low sensitivity and a narrow dynamic range compared to conventional compound semiconductor-based detectors, despite the many advantages in the implementation of the focal-plane array (FPA), such as a room-temperature operation, fast response time, and easy integration with readout, control, and bias circuits [6]–[9]. Other CMOS-based detectors fabricated using a nanometer-scale semiconductor process have shown a competitive performance, particularly in terms of the voltage responsivity (R_V) and noise-equivalent power (NEP) within the frequency band of 100 GHz or higher. However, the manufacturing cost of these detectors is expensive compared to the cost of CMOS plasmon detectors manufactured through a low-cost process with a high yield during mass production [4], [9]–[11]. The sensitivity and dynamic range of the CMOS plasmon detector in the terahertz

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band should be improved to obtain real-time images with a high signal-to-noise ratio (SNR) using a low-cost CMOS process [12], [13].

A common source configuration with control of the body bias voltage has been reported in the CMOS amplifier design [14]–[16]. Previous studies have presented amplifier designs with improved performances by applying a body-bias voltage, which is not the same as the source bias or ground, and utilizing the characteristics of a metal − oxide − semiconductor field − effect transistor (MOSFET) depending on the change in threshold voltage through the body bias. A reverse bias voltage by which the amplifier efficiency can increase as the turn-off speed increases in the switching operation and the sub-threshold current decreases to reduce the power consumption has been studied [14]. The efficiency of the amplifier can be improved using a forward body bias because the turn-on speed and the on-resistance of the switching transistor are increased by decreasing the threshold voltage [16]. In addition, it has been reported that the performance of the square-law detector implemented using the HEMT can be improved by changing the sub-threshold slope owing to the body bias control [17]. As indicated in previous studies, it can be predicted that the R_V and *NEP* of the CMOS plasmon detector are increased by the nonlinearity increase owing to the body-bias control. However, to the best of the authors' knowledge, it has yet to be reported that the sensitivity, dynamic range, and image SNR, which are important factors for the performance of the THz imaging system, can be improved by the body-bias control of the detection core transistor. Moreover, it is not known whether the body voltage should be biased with forward or reverse voltages to improve the performance of the CMOS plasmon detector. It is necessary to conduct the study on the design configuration of the CMOS plasmon detector IC including the detection core transistors controlled with body-bias voltages from the perspective of a performance improvement in THz imaging.

In this paper, a CMOS plasmon detector IC in which each detector core in a differential configuration is composed of three parallel-connected transistors having different body voltages is proposed to improve the performance of a THz imaging system. The proposed detector IC consists of an integrated patch antenna with differential ports, a differential detector core individually biased at three different body voltages, a pre-amplifier operating at the sub-threshold region, and a main amplifier with a high voltage gain. The sensitivity of the detector can be improved by a nonlinearity increase owing to the negative body biasing at the detector core, and the dynamic range of the detector IC can be expanded using parallel-connected detector core transistors with different threshold voltages caused by body biasing. The simulation and measurement results of the proposed detector IC implemented with the TSMC 0.25-μm CMOS process show that the body-bias voltage of the detection core affects the detection performances for 200-GHz incident signals, and the optimum bias condition becomes three negative voltages spaced with equal intervals. Section II provides the operating mechanism of the CMOS plasmon detector depending on the body bias. The circuit design and implementation including the simulation results are shown in Section III. Section IV presents the measurement results of the photoresponse of the detector IC and raster-scanned imaging and discusses the improvement of the performance of the proposed detector IC in THz imaging. Some concluding remarks are presented in Section V.

This paper is an expanded version of a manuscript presented at the 45th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz 2020) with the following contents added [18]. A detailed explanation has been added indicating that the performance of the CMOS plasmon detector can be improved by controlling the body voltage of the detection core. The measurement results and their analysis depending on the different body voltages are presented in detail. Raster-scanned images using the proposed detector IC have been provided to show the improvement of the quality of the THz imaging by the detector.

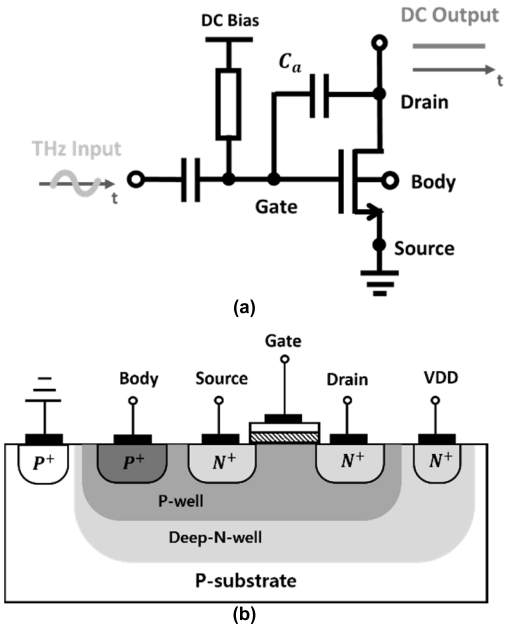

FIGURE 1. Configuration of the detection core in the proposed CMOS plasmon detector. (a) Schematic of the detection core and (b) a vertical layer structure of the device in the detector core.

II. BODY-BIASING IN CMOS PLASMON DETECTORS

A. THEORETICAL ANALYSIS

The core configuration of the proposed detector is based on a CMOS plasmon detector with a common-source stage as shown in Fig. 1. DC output voltages are generated at the drain node owing to the accumulation of electrons supplied into the source node, the concentration of which depends on the input signal power at the gate node having an operating frequency above that of the core transistor [19]. Here, R_v can be improved by increasing the coupling by adding the capacitance between the gate and drain nodes [20]. The detection

core transistor is implemented using a triple-well device to prevent a performance degradation by external noise flowing into the channel, and the configuration of the detection core is the same regardless of the body-biasing control because the body potential in the device is separated from the source.

Previous studies on an amplifier design show that the body biasing control can affect the speed of the turn-on or turn-off of the core transistor in the amplifier based on the change in the threshold voltage depending on the bias voltage [14], [16]. The results of the previous studies cannot be applied to the case of the detector core because the detector core responds to the low-powered input signal, which is higher than the maximum operating frequency (f_{max}) of the device. The analysis by the body biasing control in the square-law detectors can explain that the nonlinear characteristics of the core transistor in the CMOS plasmon detector are changed through body-biasing [17]. Based on the analysis results, the detection performances may be increased by using the dynamic threshold voltage MOSFET (DTMOS) in the CMOS plasmon detector. However, the previous study has a limitation in fully describing the effect of the body biasing in the CMOS plasmon detector because the DC voltage generated at the drain node in the plasmon detector is not considered.

Because it can be assumed that the diffusion current owing to electrons accumulated in the channel near the source is a dominant factor in the operation of the CMOS plasmon detector, the drain-source current i_{ds} is expressed as follows:

$$i_{ds} = -qD_n W \frac{dn}{dx} \tag{1}$$

where D_n is the diffusion constant, W is the gate width, and n and x are the carrier density and position in the channel, respectively [21]. The channel carrier density n can be expressed in both weak and strong inversion regions of a FET as follows:

$$n = \frac{C_{ox}\eta k_B T}{e^2} \ln\left[1 + \exp\left(\frac{e(V_{gs} - V_{th})}{\eta k_B T}\right)\right] \tag{2}$$

where C_{ox} is the oxide capacitance per unit area at the gate, e is the electron charge, k_B is the Boltzmann constant, T is the temperature of the transistor, and η is related to the subthreshold slope S as in [22] and [23]:

$$\eta = \frac{e}{k_B T}\frac{S}{\ln 10}. \tag{3}$$

The gate-source $v_{gs}(t)$ and drain-source $v_{ds}(t)$ voltages can be described using the input signal $v_{in}(t)$, the gate bias voltage V_G, and the DC output voltage V_{OUT} as follows:

$$v_{gs}(t) = v_{in}(t) + V_G = V_{THz}\cos(2\pi ft) + V_G, \tag{4}$$
$$v_{ds}(t) = v_{in}(t) + V_{OUT}(t). \tag{5}$$

Under a steady-state, the V_{OUT} of the detector core whose gate voltage is biased near the threshold voltage can be expressed as a function of $V_{in}(t)$ in [24] as follows:

$$V_{OUT}|_{Steady-state} = \frac{\eta k_B T}{e} \ln\left[I_0\left(\frac{e(V_{THz})}{\eta k_B T}\right)\right], \tag{6}$$

where I_0 is the Bessel function of the imaginary argument. Using (2)−(5), $i_{ds}(t)$ can be expressed as follows:

$$i_{ds}(t) = D_n C_{ox}\frac{W}{L}\frac{\exp\left(\frac{\ln 10\cdot(V_G - V_{th})}{S}\right)}{1+\exp\left(\frac{\ln 10\cdot(V_G - V_{th})}{S}\right)} \times\left[V_{OUT} - v_{in}(t) + \frac{\ln 10}{S}\frac{v_{in}^2(t) - V_{OUT}^2}{2\left\{1+\exp\left(\frac{\ln 10\cdot(V_G - V_{th})}{S}\right)\right\}}\right]. \tag{7}$$

In addition, the DC current of the $i_{ds}(t)$ can be expressed as

$$I_{DS} = D_n C_{ox}\frac{W}{L}\frac{K}{1+K}\left[V_{OUT} + \frac{\ln 10}{S}\frac{0.5V_{THz}^2 - V_{OUT}^2}{2\{1+K\}}\right], \tag{8}$$

$$K = \exp\left(\frac{\ln 10}{S}(V_G - V_{th})\right). \tag{9}$$

The output voltage V_{OUT} at $t + \Delta t$ can be described using V_{OUT} at t as follows:

$$\begin{aligned} &V_{OUT}(t+\Delta t)\\ &= V_{OUT}(t) + \frac{\ln 10}{2S(1+K)}\left(0.5V_{THz}^2 - V_{OUT}^2(t)\right)\\ &= V_{OUT}|_{INIT} + V_{OUT}(t)\left(1 - \frac{\ln 10}{2S(1+K)}V_{OUT}(t)\right). \end{aligned} \tag{10}$$

Substituting (6) into $V_{OUT}(t)$, the output voltage can be presented as

$$V_{OUT} = \frac{\ln 10}{S}\frac{v_{THz}^2}{4(1+K)} + \frac{S}{\ln 10}\ln\left[I_0\left(\frac{\ln 10}{S}v_{THz}\right)\right] \times\left\{1 - \frac{1}{2(1+K)}\ln\left[I_0\left(\frac{\ln 10}{S}v_{THz}\right)\right]\right\} \tag{11}$$

Equation (11) can be approximated as the same formula as the square-law detector when the input signal power is quite small [17]. It is shown that the output voltage of the CMOS plasmon detector is generally smaller than that of the square-law detector because the second term of (11) has a negative sign based on the Bessel and logarithm functions. The value of R_V can be expressed using the input power of V_{THz}^2/R_{in} as

$$R_V = \frac{\ln 10}{S}\frac{R_{in}}{4(1+K)} + \frac{R_{in}}{V_{THz}^2}\frac{S}{\ln 10}\ln\left[I_0\left(\frac{\ln 10}{S}v_{THz}\right)\right] \times\left\{1 - \frac{1}{2(1+K)}\ln\left[I_0\left(\frac{\ln 10}{S}v_{THz}\right)\right]\right\} \tag{12}$$

where R_{in} is the input resistance of the detector core. As shown in (12), the value of R_V in the detector can slightly decrease as the input power increases because of the effect of the characteristics of the plasmon detection. The theoretical analysis shows that the voltage responsivity varies owing to the sub-threshold slope. The value of R_V in the CMOS plasmon detector can increase as the slope S becomes smaller, which is the same characteristic as the square-law detector. The body voltage affects the threshold voltage, which increases as the body is biased with the negative voltage [21].

The effect of R_V owing to the body biasing can be understood by the variation of the subthreshold slope S because the variation effect of the threshold voltage can be minimized by adjusting the gate bias.

B. QUALITATIVE ANALYSIS

The subthreshold slope S can be presented by the relational expression from the subthreshold swing as

$$S \propto \frac{1}{1 + C_{dep}/C_{ox}} \tag{13}$$

where C_{dep} is the depletion capacitance [23]. The slope generally decreases owing to the increase in the depletion region when the negative body voltage is biased [25].

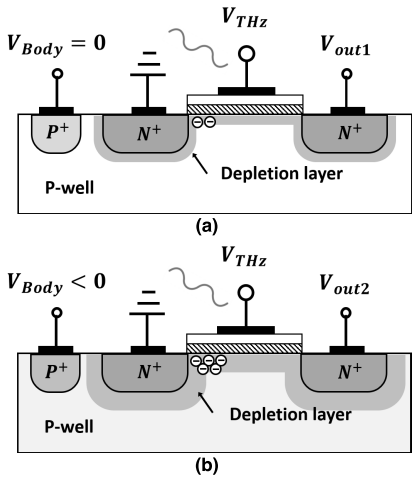

FIGURE 2. Charge profile and depletion layer depending on the body voltage in the proposed CMOS plasmon detector: (a) zero body biasing, and (b) negative body biasing.

However, the subthreshold slope in the CMOS plasmon detector cannot be exhibited only based on the effect of the depletion capacitance because the output signal is not generated by the channel transport modulated by the gate potential. The charge distribution by the body voltage can explain the variation of DC outputs depending on the body biasing. When the electron concentration in the channel increases owing to the negative body biasing, as shown in Fig. 2, the amount of the accumulated charge near the source in the CMOS plasmon operation increases. This phenomenon represents an increase in the subthreshold swing, which is inversely proportional to the subthreshold slope, and the increase in the potential difference between the drain and source. In addition, this characteristic can be acceptable as a decrease in the subthreshold slope in the plasmon detector owing to an increase in unstable charge by the negative body voltage [23], [25]. The simulation results of the CMOS plasmon detector shown in Fig. 3 indicate that the negative body biasing can increase the photoresponse compared to the zero and positive body biasing. The design parameters of the detector are detailed in Section III-A. The simulated photoresponse in Figs. 3 and 4 are obtained from the difference between the

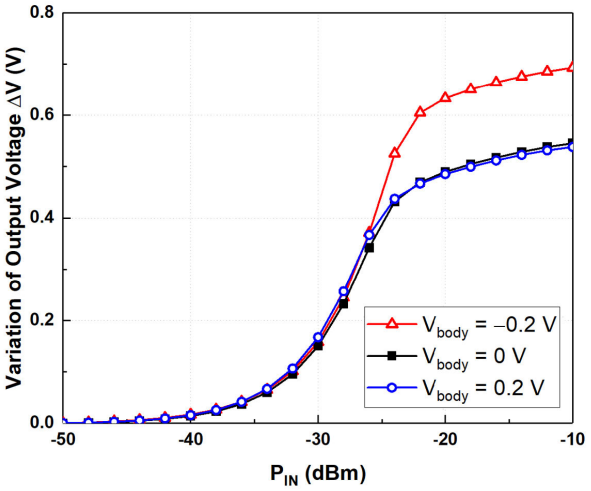

FIGURE 3. Simulated photoresponses in the CMOS plasmon detector depending on the input power level using the detector core transistor biased with negative, zero, and positive voltages at the body.

output and reference voltages. The reference voltage is set to the simulated output voltage when the input signal power of −60 dBm or less is incident to the detector.

An increase in the output voltage by the body biasing shows that an output DC voltage of a detectable level can be generated at a low power level of the input signal. In addition, the output voltage of the CMOS plasmon detector is gradually saturated to a constant as the input power increases because the amount of charge in the channel is determined by the doping concentration in the p-well. These characteristics show that the minimum sensitivity level and the dynamic range can be improved by the negative body biasing. The simulation results in Fig. 4 show the changes in the output voltage at the different body voltages of the detector core transistor depending on an input power level of 200 GHz. The minimum sensitivity level is defined as the input power level that generates the same output voltage as the arbitrary noise voltage. The dynamic range is defined by the input power range from the minimum sensitivity level to the input power level in which the output voltage does not change depending on the input power. Figure 4 shows that the detector with negative body biasing has a lower sensitivity level and a wider dynamic range than the detector without any biasing at the body.

III. INTEGRATED CIRCUIT DESIGN OF THE PROPOSED CMOS PLASMON DETECTOR

A. DETECTOR CORES AND PREAMPLIFIER

Fig. 5 shows the overall IC structure of the detector. The detector chain consists of a detector core, a preamplifier, and a folded cascode main amplifier. The characteristics of the DTMOS for increasing the effect of the subthreshold slope are implemented using three detector core transistors with different body biases in parallel. The differential patch antenna is integrated on a chip, and the gate bias with the same

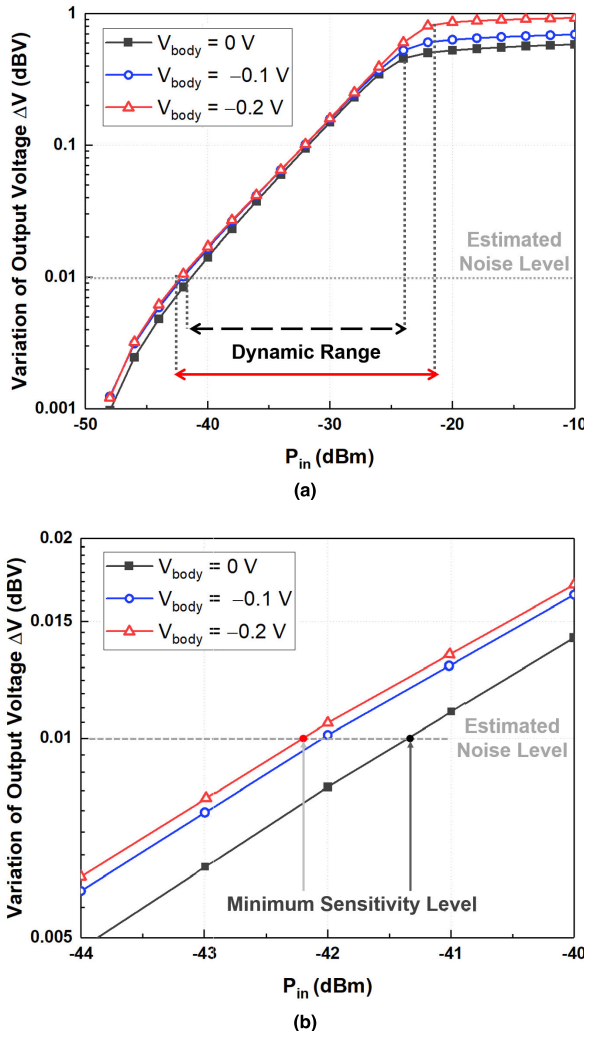

FIGURE 4. Simulation results of the CMOS plasmon detector with the different body biasing of zero, −0.1 V, and −0.2 V. (a) Photoresponse depending on the input signal power, and (b) an enlarged view to display the sensitivity depending on the body voltage.

voltage level is simultaneously applied to the detector cores by using the virtual node of the antenna. The transmission lines of a differential patch antenna are designed identically for the simultaneous incidence of the terahertz signal to each detector core. The gate-drain capacitance of 28.6 fF, which is the minimum-sized MIM capacitor supported by the process, is added to each detector core. The core transistor of the detector uses the minimum-sized transistor in the process. As shown in Fig. 6, the output at each core is delivered to a preamplifier and differentially combined as the drain-source current at the input transconductance stage in the preamplifier [26]. The input stage of the preamplifier is self-biased by the DC output of the detector core, and the self-biased operation reduces the noise from the detector cores and the preamplifier transmitted to the output of the detector IC when the input signal is not incident. The cascode structure functions as the isolator that reduces the deterioration of the characteristics owing to leakages between signals having

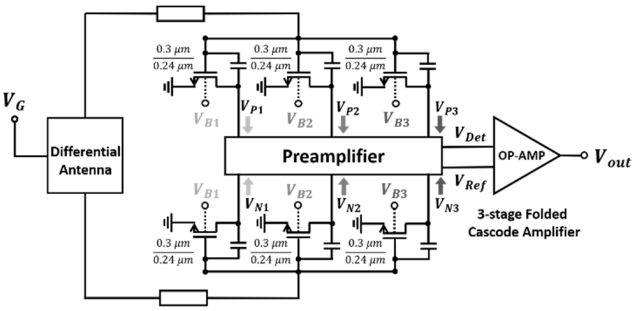

FIGURE 5. Schematic of the integrated circuit of the proposed CMOS plasmon detector.

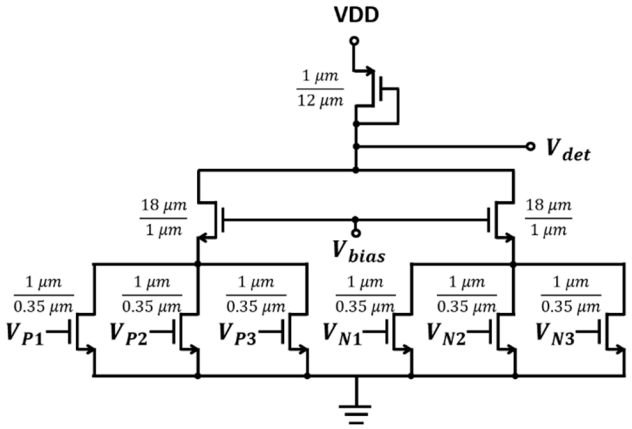

FIGURE 6. Schematic of the preamplifier for current combining and self-biasing in the proposed CMOS detector.

differential phases. A total of six core transistors are used in the proposed detector, and the dummy transistors in the preamplifier are designed to generate the reference voltage by using the same transistors for minimizing the effect of the DC offset of the preamplifier itself [26].

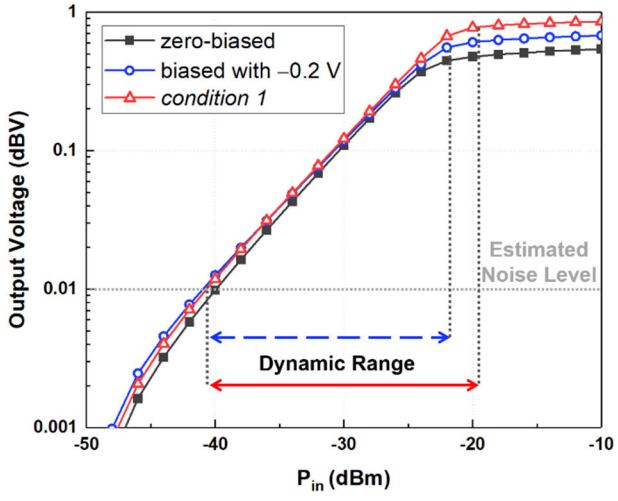

FIGURE 7. Simulation results of the output characteristics depending on the input power level of the proposed detector with three adjustable body voltages.

The simulation results in Fig. 7 depict the output voltages depending on the body biasing configuration of three detector core transistors. The output characteristics of the detector IC

in the simulation are compared among the conditions under which all body voltages are equally set to zero or −0.2 V and the condition under which the body voltages are set to the same interval of 0.2 V in the negative direction. The last condition biased with 0, −0.2, and −0.4V is called *condition 1*. The conditions biased with the same voltage present the same change in the characteristics as when adjusting a single body bias, as shown in Figs. 3 and 4. Fig. 7 shows that the detector biased with *condition 1* has a wide dynamic range, and that there is no significant difference in the sensitivity level between the detector in which all bodies are biased at −0.2V and the detector under *condition 1*. The dynamic range shown in Fig. 7 is only widened by approximately 3 dB by the detector biased with *condition 1* because the detector cores are connected in parallel to the antenna port and the photoresponse of the detector core is influenced by each other owing to the parallel configuration.

B. DIFFERENTIAL PATCH ANTENNA

The differential patch antenna is designed at the operating frequency of 200 GHz by using an ANSYS HFSS 3D electromagnetic wave simulation. The differential antenna is advantageous in the improvement of R_V by reducing the antenna area and in the reduction of the parasitic effect generated at the interconnection lines [27]. The input impedance at each port is designed to be 50 Ω by using the transmission line with a width of 6.5 μm, and the antenna (348 μm × 310 μm) is implemented on the top metal with a thickness of 3 μm. The pixel size shielded by the ground lines stacked by metal layers is 800 μm × 790 μm. An M1 layer, the lowest layer in the backend oxide layers, is used as the ground on the antenna design, and the simulation results in Fig. 8 show the −10 dB bandwidth of 5.4 GHz and an antenna gain of − 5.1 dBi.

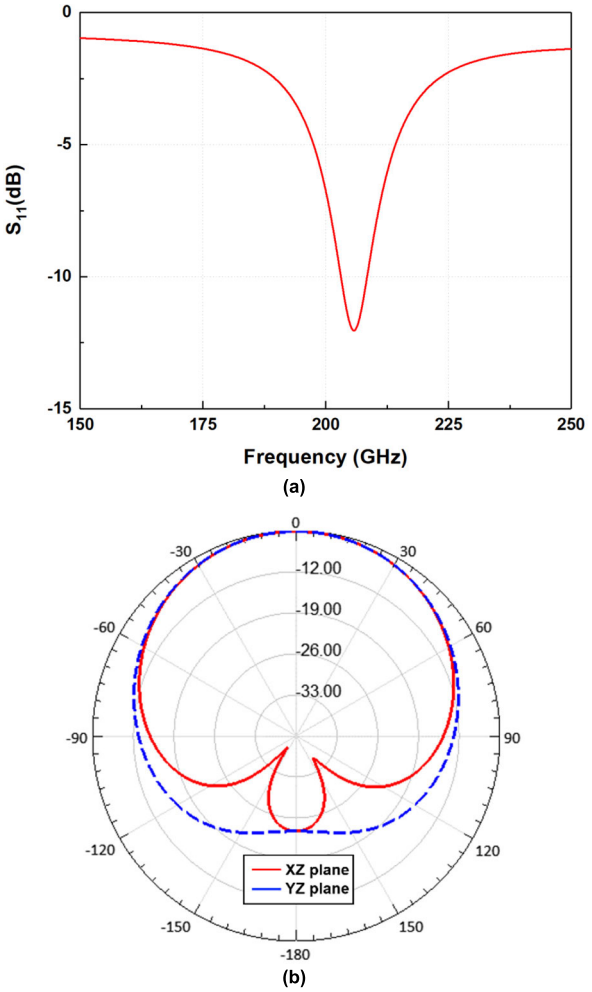

FIGURE 8. Simulation results of the differential patch antenna of the proposed CMOS plasmon detector: (a) Input matching using the differential port and (b) radiation patterns in the E- and H- planes.

C. IMPLEMENTATION

The proposed detector IC is implemented using a TSMC 0.25 μm mixed-signal CMOS process with 1-poly and 5-metal layers. The fabricated die area including the detector IC, a low-dropout (LDO) regulator, and a bias circuitry is 1.30 mm × 1.58 mm as shown in Fig. 9. The core supply voltage of the detector IC is designed to 1.8 V, which is converted from 2.5 V by the LDO regulator. The voltage difference between the DC detection voltage through the preamplifier and the reference voltage for a DC offset cancelation is amplified using a three-stage folded cascode main amplifier with a variable voltage gain from 36 to 44 dB and a differential-to- single-ended conversion, and the final output voltage of the proposed detector IC is transmitted to the single-ended pad. The total power consumption is 1.1 mA in the simulation results.

IV. RESULTS AND DISCUSSIONS

A. MEASUREMENT SETUP

Fig. 10 shows a block diagram indicating the measurement setup used to obtain the performance, including R_V and *NEP*, of the proposed detector IC itself. The 200-GHz signal generated by the gyrotron is focused on the detector by off-axis parabolic (OAP) mirrors [28]. An optical chopper operating at a frequency of 100 Hz is used to mechanically modulate the input signal to reduce the effect of the 1/*f* noise [5]. The linearly polarized signal generated from the gyrotron is transmitted to the integrated antenna of the detector by adjusting the power level based on the cosine value of the angle determined by the polarizer. The chopper is located at the focal position of the THz signal generated by OAP mirrors to minimize any disturbance by the blade blockage of the chopper, and the polarizer is placed to more minutely control the power of the well-polarized THz signal from the gyrotron. The control signals that adjust the supply voltage by the LDO regulator and the voltage gain of the main amplifier are transmitted to the detector IC using digital I/O terminals of the data-acquisition board (DAQ) manufactured by National Instruments Inc. (NI). The single-ended output voltage at the detector IC is conditioned to be amplified and filtered with the voltage gain of 2 and the passband from 3 to 300 Hz by

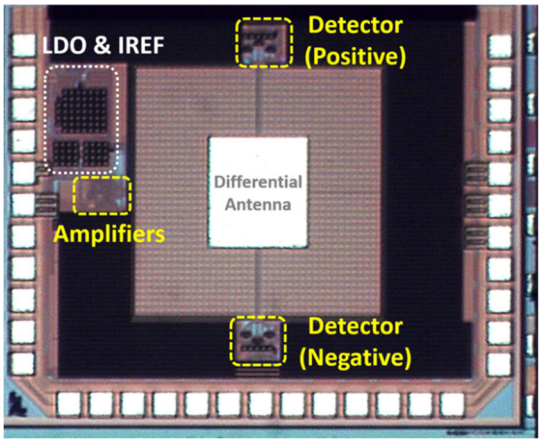

FIGURE 9. Die photograph of the detector IC fabricated using TSMC 0.25 μm mixed-signal CMOS process with a thick metal layer on top.

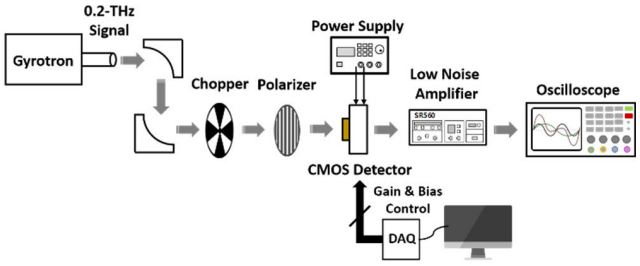

FIGURE 10. Measurement setup for obtaining the voltage responsivity and the noise-equivalent power of the proposed detector IC itself.

the SR560 low-noise voltage amplifier manufactured by Stanford Research Systems. The voltage gain of the SR560 amplifier is excluded in the calculation of the output performances of the detector IC. The noise spectral density for calculating the NEP is measured using a spectrum analyzer instead of an oscilloscope.

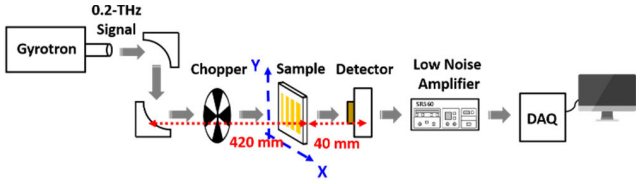

FIGURE 11. Measurement setup for obtaining the THz images with the proposed detector IC using the raster scanning.

The measurement setup for obtaining the 0.2-THz images is configured as shown in Fig. 11, in which the output voltage at each position can be captured while moving the position of the target sample in the XY direction. The output voltage of the detector is obtained by using the analog input terminal of the NI DAQ instead of the oscilloscope, and the NI LabVIEW is used for implementing the program to store the output voltages in the data set and move the sample by controlling the step motors. THz images are produced through raster scanning with a movement interval of 1 mm. The measurement time at each position is set to 2 seconds to minimize the noise signal generated by vibrations in the movement of the sample. The sample is placed at the focal location where the polarizer is located, as shown in the measurement setup in Fig. 10, to irradiate a small-sized THz beam onto the sample. The mirror-to-sample and the sample-to-detector distances are 420 and 40 mm, respectively.

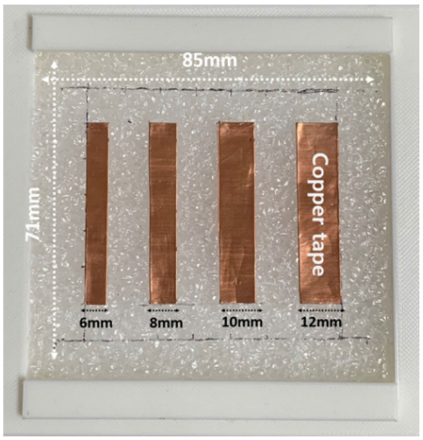

FIGURE 12. Photograph of a sample for THz imaging using the proposed detector IC.

A target sample is prepared by applying a copper tape with a thickness of 0.06 mm on Styrofoam with a thickness of 10 mm and a size of 85 mm $\times$ 71 mm. The line width of each piece of tape is 6, 8, 10, and 12 mm, with an equal distance spacing of 11 mm, as shown in Fig. 12. When the THz signals are covered by the pieces of a copper tape of the sample, the signal power level incident to the detector decreases. The THz images are obtained based on the variation of the output voltage of the detector IC at each position depending on the incident power.

B. R_V AND NEP OF THE PROPOSED DETECTOR IC

It is necessary to accurately obtain the signal power level incident to the integrated antenna for calculating the R_V and *NEP* of the detector. The power density of the 0.2-THz signal generated by the gyrotron and the effective antenna area by the antenna gain and the operating frequency are calculated as 0.5 W/m^2 and 5.53 $\times$ 10^{-8} m^2, respectively [4], [28]. The output of the detector IC is measured under each body bias condition to compare the detection performances depending on the body voltage configuration. In addition to *condition 1* defined in Section III, the other bias condition is defined as *condition 2*, where three different body voltages are biased with 0, -0.1, and -0.2 V, respectively.

Fig. 13 shows the detector outputs as a function of the decrease in the input signal power in proportion to $\cos^2\theta$, which is determined by the angle θ of the polarizer. The noise floor at the output of the detector at a gate voltage of 0.15 V is measured to be 15 mV based on the RMS value of the noise signal displayed on the oscilloscope in the absence of the input signal. Assuming that the same output as the noise floor

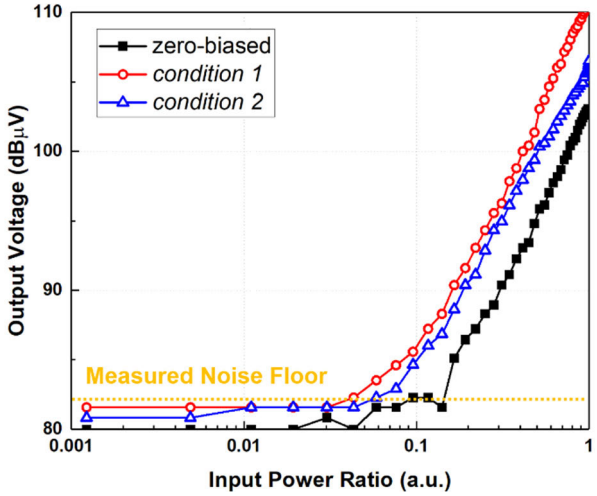

FIGURE 13. Measured photoresponses depending on the input signal power controlled by the angle of the polarizer.

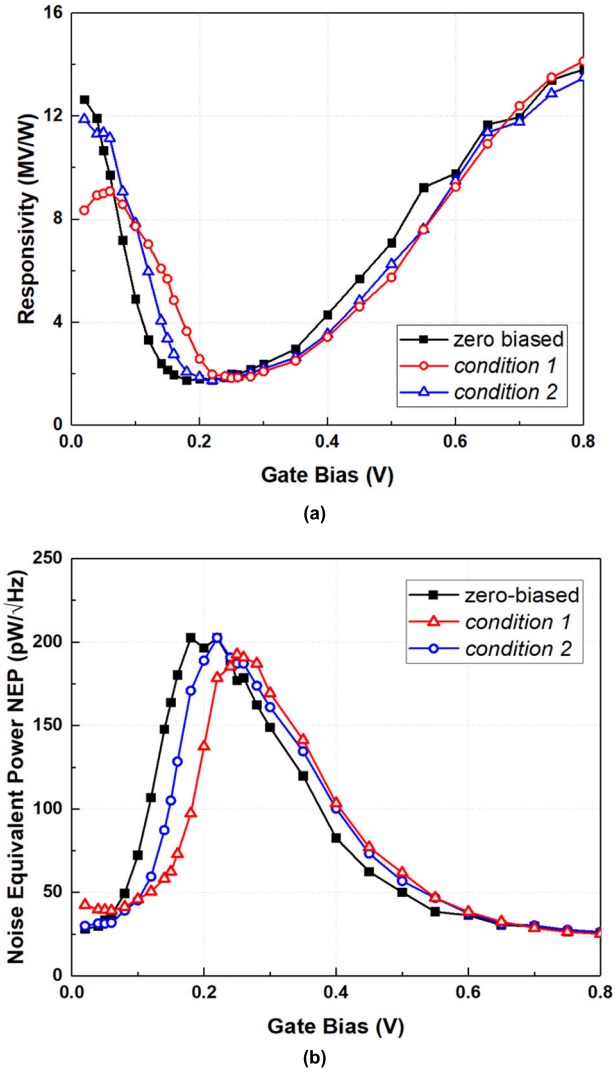

FIGURE 14. Measurement results of the proposed CMOS plasmon detector IC: (a) Voltage responsivity R_V and (b) noise-equivalent power *NEP*.

can be measured in the detector (SNR = 1), the minimum sensitivity of the detector calculated using the input power density and the effective antenna area is measured to be 3.73, 1.28, and 2.14 nV at the zero-bias and *condition 1* and *condition 2*, respectively. The results show that the proposed detector with *condition 1* in which three different body voltages are biased at the detector cores improves the sensitivity by 2.9-fold compared to the zero- biased detectors. The detector output in Fig. 13 is linearly increased with an increase in the input power because the input power does not reach the saturation level. Owing to the limit of the maximum input power below the saturation level, the increase in the dynamic range at a high input power level, which is shown in the simulation results of the proposed detector, cannot be demonstrated in the measurement results. However, the dynamic range of the detector biased as *condition 1* is increased by 11.1% compared to the zero-biased detectors simply by the improvement of the sensitivity.

Fig. 14 shows the measurement results of R_V and *NEP*, which are indicators of the detector performance depending on the gate voltage. The voltage gain of 36 dB in the main amplifier of the detector IC is not de-embedded in the results because the main amplifier is an important component constituting the detector IC. The results show that the detector biased with different body voltages exhibits a high R_V and low *NEP* within a gate voltage of 0.1 to 0.2 V. At a gate voltage of 0.15 V, the largest difference in the performance is shown depending on the body bias condition. The minimum R_V and maximum *NEP* are similar regardless of the gate bias voltage, which shows that the minimum R_V is presented at a gate voltage of approximately 0.25 V. In addition, the output performances are degraded because the gate voltage is gradually far from the 0.25 V. The minimum R_V at the gate bias near the threshold voltage is not a general characteristic in the CMOS plasmon detector, but it can be explained by using (12) in Section II. The value of R_V in (12) gradually increases at the gate biasing voltage below the threshold voltage because of the decreases in the magnitude of the exponential function of (9). The increase of R_V at the gate biasing voltage above the threshold voltage has been explained by the increase in the gain of the preamplifier by the self-biasing of the transconductance stage [26]. The tendencies of R_V to increase under the different gate voltages are because of the change in the threshold voltage by the body bias, and the results in Fig. 14 show that the detectors with negative body bias voltages have higher threshold voltages. The gate voltage of 0.15 V, at which the detector has the best performance improvement when adjusting the body bias voltages, is set to the optimal operating bias because R_V increased at a gate bias of 0.25 V or more has a low correlation with the detector characteristics. The values of R_V at a gate bias of 0.15 V are measured to be 2.170, 5.696, and 3.382 MV/W under the zero biasing and under *condition 1* and *condition 2*, respectively. In addition, *NEPs* at the gate bias are calculated

TABLE 1. Comparisons of CMOS plasmon detectors.

	Freq. [GHz]	Detector Core Configuration[a]	Process [μm]	R_V[b] [kV/W]	NEP [pW/√Hz]
[4]	856	CS	0.065	140	100
[8]	860	CG	0.18	3.3	106
[19]	200	CS	0.25	482	39.3
[20]	200	CS	0.065	1.5	15
[26]	200	CS	0.25	2,020	76
[29]	290	CS	0.18	0.7	261
[30]	365	CS + CG	0.09	1,200	200
This work	200	CS	0.25	5,696[c]	62.4[c]

[a]CS and CG indicate common-source and common-gate configurations, respectively.
[b]The voltage responsivity includes the voltage gain of the integrated amplifier.
[c]These are obtained from body bias *condition 1* and a gate voltage of 0.15V where the change in the responsivity depending on the body biasing becomes maximum.

to 163.7, 62.4, and 105.1 pW/√Hz under zero biasing and under *condition 1* and *condition 2*, respectively. The proposed detector IC with three different body biasing shows the 2.63-fold improvement of R_V and *NEP* when compared to the detector with zero body biasing. Table 1 summarizes the performance comparison of the proposed CMOS plasmon detector from previous studies at similar operating frequencies.

C. 200-GHz IMAGES USING THE DETECTOR IC

THz images for the sample are obtained using the proposed detector, as shown in Figs. 15−17. Fig. 15 shows 200-GHz images obtained at the different distances between the sample and detector for a partial area of the sample, which displays pieces of a copper tape with widths of 6- and 8-mm. White-dotted squares in Fig. 15 indicate the width of the copper tape with widths of 6 and 8 mm. The images measured at different distances show the diffraction of the 200-GHz signals. The image in Fig. 15a measured at a distance of 25 mm shows the shape of the copper tape, but the boundary is not clear because of blurring, whereas the image in Fig. 15b measured at a distance of 40 mm has a relatively clear boundary and a high SNR. The image measured at 25 mm shows a general characteristic owing to the incident power level of the THz signal, and the area obscured by the copper tape displays a low output voltage and the uncovered area displays a high voltage. The blurring at the boundary can be understood to be a characteristic of the scattering of the input signal generated at the boundary of the copper tape. By contrast, the image measured at a distance of 40 mm shows that the minimum power is incident at the boundary and the output at the part covered by the copper tape is higher than the minimum output voltage. This phenomenon indicates that the diffraction of the 200 GHz input signal is

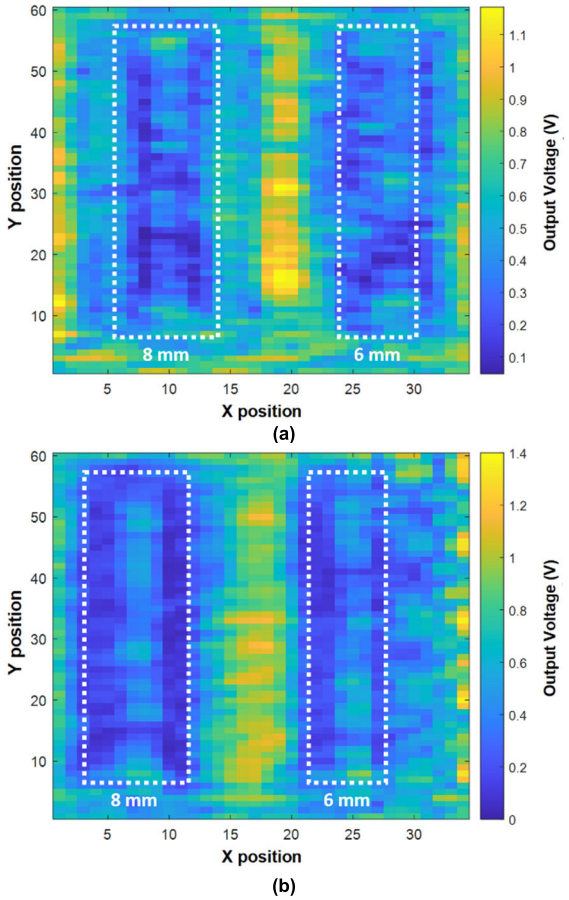

FIGURE 15. Measured THz images depending on the distance from the sample to the detector: at (a) 25 and (b) 40 mm.

generated. The images measured at a distance of 25 mm are appropriate for use as THz images, although the purpose of presenting THz images in the experiment is to verify whether the proposed detector can achieve a better dynamic range and image SNR. Thus, the THz image for each body bias condition is purposely measured at a fixed distance of 40 mm between the sample and the detector.

Fig. 16 shows the result of 200-GHz images measured using a zero-biased detector and the detector with three different body voltages under *condition 1*. Both images in Fig. 16 show a sufficient quality to distinguish the pieces of a copper tape with line widths of 6−12 mm. It is demonstrated that the detector under *condition 1* has a higher SNR than the zero-biased detector from the ratio between the minimum and maximum output voltages in the images. Despite the images in Fig. 16 being normalized with each maximum and minimum voltage, the boundary of the tape is clearly observed in the images obtained by the detector biased under *condition 1* as compared to the zero-biased detector. The improvement in the dynamic range and the SNR of the detector when adjusting the body bias voltages is effectively pronounced in Fig. 17, which shows normalized images at the same voltage level. The SNR in the image of Fig. 17 is measured to be 25.5 dB in the zero-biased detector and

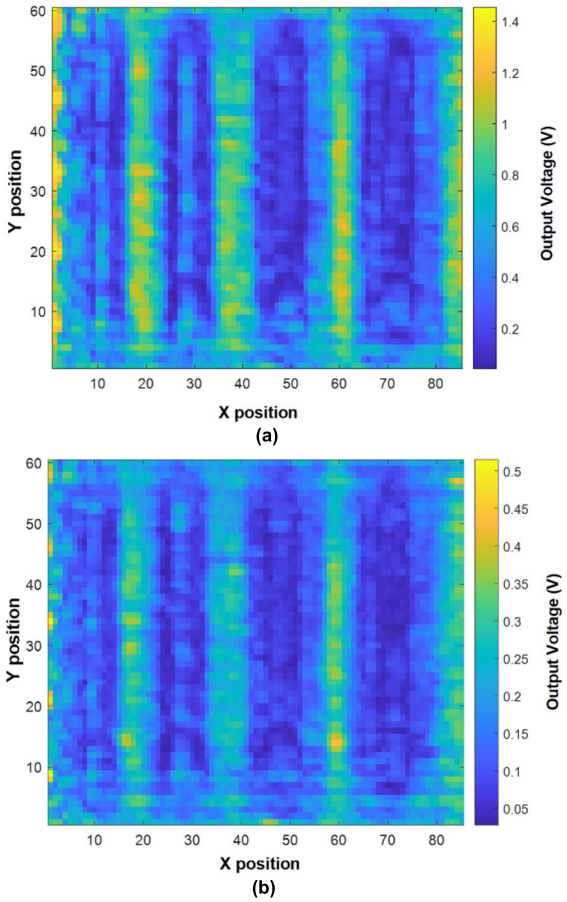

FIGURE 16. Measured THz images in the different body-biasing of the detector cores: biased (a) under *condition 1* and (b) at zero voltage.

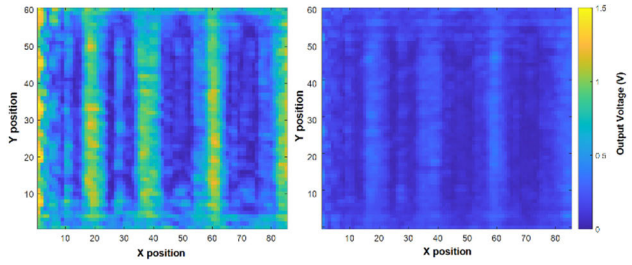

FIGURE 17. Normalized THz images to compare the performances of the detector biased at the three different body voltages to those of the zero-biased detector.

30.6 dB in the detector biased under *condition 1*, showing that the image SNR of 5.1 dB is improved by adjusting the body voltages. The image resolution is 6 mm or less because the width of 6 mm can be effectively distinguished from the background. The image resolution of the CMOS plasmon detector is determined by the detector movement interval in the raster scanning.

V. CONCLUSION

A CMOS plasmon detector composed of detector core transistors with three different body voltages is proposed for a performance improvement in a THz imaging system. The theoretical and quantitative analysis of the effect of the body biasing in the CMOS plasmon detector shows that the proposed detector operates by applying a negative body voltage to reduce the sub-threshold slope owing to an increase in the electron in the channel based on the body potential. A detector IC consisting of a differential on-chip antenna, three-pair differential detector cores, a pre-amplifier that combines the outputs of the cores as a current, and the main amplifier with a voltage gain of 36 dB is designed and fabricated using a TSMC 0.25-μm CMOS process. The voltage responsivity and noise-equivalent power of the proposed detector to 200-GHz incident signals are 5,696 kV/W and 62.4 pW/$\sqrt{}$Hz at a gate bias of 0.15V, where the performance improvement by body biasing is effectively presented. The performance of the detector with three different body voltages is improved 2.63-fold compared to the zero-biased detector. The minimum sensitivity is improved by 2.9-fold from 3.73 to 1.28 nV, and the dynamic range is increased by 11.1% even though the dynamic range improvement at a high input power cannot be measured. In addition, 200-GHz images of a sample composed of copper tapes placed on a Styrofoam substrate show that the detector with three different types of body biasing has an image SNR of 30.6 dB, which is 5.1 dB better than a zero biased detector.

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