Arithmetic Tracking Adaptive SAR ADC for Signals With Low-Activity Periods

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ABSTRACT This paper introduces a novel arithmetic tracking algorithm for successive approximation ADCs, and presents its analysis. The algorithm utilizes low activity signal periods to cut the ADC energy dissipation by reducing the number of required bit-cycles. The approach determines the required step size, and bypasses conversion cycles when signal activity is low, without compromising the precision or sampling rate. The required first-order predictions and boundary checkings are performed with simple digital circuits. A lowered number of cycles paired with reduced voltage variations across DAC capacitors yields power savings. The solution has been simulated in a 90 nm CMOS process using HSPICE, demonstrating a 10-bit tracking SAR ADC. The proposed ADC was examined with low activity signals such as EEG, ECG, etc. The results predict from 5.8 μW to 27.6 μW dissipation when the sampling rates range from 32 kHz to 800 kHz, respectively.

INDEX TERMS Successive approximation register, predicting ADC, bio-medical signals, Internet-of-Things, IoT, sensors.

I. INTRODUCTION

With the advent of the Internet-of-Things (IoT), minimizing instantaneous and average power consumptions of sensor nodes has attracted much attention[1]. This is particularly important when aiming at ultra-low power [1] energy scavenging based solutions. While the energy efficiency of digital logic has been improving due to reducing operation voltages and smaller line-widths, the power share of Analog to Digital Converters (ADCs) in sensor nodes can no longer be considered insignificant [2]. For example, the ultra-low power MCU ARM M0+ implementation by ST Microelectronics [3] draws 88 μA/MHz, while the ADC requires 40 μA at 10kS/s and 200 μA at 1MS/s. For wireless communications, long range backscatter technology has been demonstrated to dissipate only 70 μW at 868 MHz with 2.9 kbit/s [4], a low rate that may require exploiting sparse sampling as a low energy compression scheme, if feasible for the signal of inter-

est [5]. With the aim being deep-sub-mW devices, multiple approaches have been proposed to improve the energy efficiency of the ADC, ranging from device and process improvements to circuit level and architectural innovations [5]–[7].

ADCs in microcontrollers are often designed with a broad range of application uses in mind, however, the software in ultra-low power designs regularly exploits the characteristics of the signals to maximize endurance. Periods of low activity are often less important, enabling savings in computations and lowering the clock frequency and voltage. For ADCs similar approaches have been proposed, e.g. [8], [9], to cut energy dissipation during the times of low activity. Such opportunities exist with biomedical signals such as EEG and ECG when measuring temperature and pressure. Even image capture by digital camera could be considered to belong to this category [8].

SAR ADCs match such needs in medium resolution applications, 10-12 bits, with sampling rates of up to a few MS/s [10]. The major energy sinks in SAR ADCs are digital logic, the Digital-to-Analog Convertor (DAC) and the comparator [11]. If the activity of the comparator and DAC components can be reduced during slow signal change periods, the power dissipation is lowered [12], [13].

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[1]The low power ADC simulation model and software for the approach proposed in this paper are available from Github at https://github.com/NeuroFan/Algorithmic-SAR-ADC-simulation-files

Two categories of low activity period energy saving schemes exist for SAR ADCs. A lossy scheme demonstrated by Chiang *et al.* [14] employs an SAR bit cycle bypassing approach that skips resolving the Most Significant Bit (MSB), saving around 12% of power with only 0.017% incorrect conversions. Ignoring conversion cycles of two MSBs resulted in only 0.3% conversion error, while saving 25% of the power. The signal sampled at 25 kS/s was a 4-channel EEG from rat brains.

Lossless approaches aim at improving the predictions, but may lose cycles in the case of misses. For instance, Chen *et al.* [9] proposed an SAR ADC that does not reset all capacitors in the DAC. The solution proposed for mispredictions requires modifications to the DAC analog section. The authors report best case 75% conversion cycle savings, while a misprediction always results in twice the regular SAR cycles - 20 cycles for a 10 bit SAR.

In this paper, we propose a novel lossless energy saving approach for predictive SAR ADC that requires changes only to the digital part. With the used set of diverse signals, the average energy and cycle savings are 30%. In the case of misprediction, only an extra 10 SAR cycles are needed. Subjected to the worst case, every second sample at maximum, and every second at zero, the solution dissipates twice the unmodified SAR ADC.

In next section, a review of related works is presented. In section III, the proposed approach is described in detail, and section IV presents the behavioral and circuit level simulations for the different types of signals used in the analysis. Section V discusses the challenges, followed by conclusions in section VI.

II. PRIOR RESULTS AND THE NOVEL APPROACH

The principle of an SAR ADC is to convert a sampled charge, V_{in}, by comparing it against the output of a DAC (commonly a capacitive type) controlled by SAR logic, as illustrated in Figure 1. At least N cycles are required for resolving N bits. Starting from the first cycle, the SAR logic sets the MSB to "1" and the remaining bits to "0" (e.g. for 5-bit ADC, the code will be "10000"). Based on the result from the comparator, the MSB bit is either kept or reset to zero in the next cycle. The process is repeated for the next lower bit, the SAR logic approximating the sampled charge by digital logic and DAC.
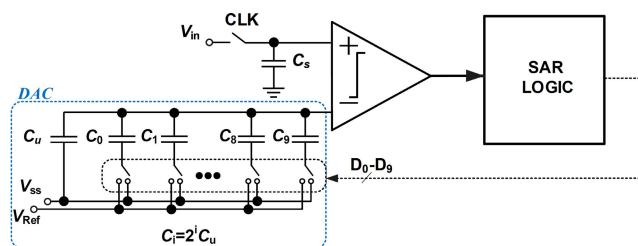

FIGURE 1. The basic SAR ADC structure.

Different methods have been proposed in the literature to reduce the number of conversion cycles of SAR ADCs for low activity signals. In this section, we review relevant prior contributions. We have categorized the approaches into those that are useful with slowly changing signals, such as temperature and humidity measurements, and schemes that can be used in cases in which the signals exhibit periodical higher activity. Many biosignals such as ECG belong to the latter class.

A. SAR ADC APPROACHES FOR SLOWLY CHANGING SIGNALS

Designs such as [6] and [15] aim at reducing SAR ADC conversion bit-cycles by converting only sample-to-sample variations. This necessitates analog subtraction of consecutive samples, and is familiar from Delta-Sigma ADCs [16]. The method rests on the assumption that the input signal is guaranteed to have limited sample-to-sample differences, i.e., the signal bandwidth is relatively low. Analog subtraction adds extra design constraints and prevents employing bottom plate sampling, increasing the impact of the charge injection problem [6].

Zhang *et al.* [12] propose a highly oversampling dynamic tracking SAR ADC to limit the sample-to-sample variations. Changes to the analog section are needed, while predictions are made based on two previous samples. In the case of mispredictions, only $N + 3$ bit cycles are needed. The targeted application is bio-signals.

Lee [15] has proposed a 10 bit SAR ADC that needs only the number of cycles of a 6 bit converter by avoiding MSB conversions. Once again, in many applications, such as ECG acquisition, the signals are bursty and their changes cannot be guaranteed to be bounded to a small range. Yim *et al.* [17] propose performing a 10 bit conversion at full-range, while continuously monitoring the signal activity. During low activity periods, the DAC subtracts each new sampled charge from the summed charge in 5 DAC MSB capacitors, leaving 5 LSBs to be resolved through an SAR binary search. The solution assumes limited sample-to-sample changes.

A "LSB-first" SAR ADC method that aims to avoid MSB conversions has been presented by Yaul and Chandrakasan [18]. The idea is to start stepping from the LSB and successively test toward the MSB, in contrast to the conventional MSB-first approach. If the rate of change of the signal is slow, the MSB bits change relatively rarely, enabling substantial energy savings. For very low activity periods (almost DC), an N-bit LSB-first SAR ADC requires only a single bit cycle. However, in the worst case it might require up to $2 \times N + 1$ cycles for every sample during the times of high-activity. It has been shown in [19] that the energy efficiency of the LSB-first SAR ADC loses against the conventional MSB first approach when the signal activity increases even slightly.

In this category, the underlying assumptions necessitate either a limited signal bandwidth relative to the sampling frequency, or rather a restricted signal amplitude, or both.

As for small bandwidth signals, other efficient techniques such as Noise Shaping SAR (NS-SAR) ADCs [20], [21] are a competing rival. On the other hand, if the oversampling ratio and the signal bandwidth are known, the maximum sample-to-sample variations can be determined analytically. Rather than a predictive approach, this priori information can be leveraged into reducing SAR bit-cycles as was shown previously in [22].

B. SAR ADC APPROACHES FOR SIGNALS WITH PERIODIC HIGHER ACTIVITY

Signals with periodic higher activity can be sampled in an energy conserving manner using SAR ADCs that adapt to changes with precision compromises. An example of this principle has been proposed by Nasserian *et al.* [23] who change the ADC resolution based on signal activity, switching between 5 and 10 bits to save conversion cycles. This scheme is feasible when the low-activity parts of the signal are less important than the higher activity ones. An additional advantage is the automatically provided low to medium ratio signal compression. However, while the energy consumption is reduced, the resolution during low activity periods is sacrificed. A similar approach by Chen *et al.* [24] adaptively adjusts the sampling rate of SAR ADC based on signal activity. This approach also suffers from precision loss.

In [25] Van Rethy *et al.* propose a signal tracking method to reduce the average number of SAR ADC bit cycles per conversion. Predictor logic feeds the DAC and and performs a linear binary search restricted to a part of the full dynamic range. For some of the signals used in their experiments up to a 50% reduction in power consumption was achieved. The downside of the approach is its worst case bit cycle count that equals 2^K bit cycles, where K is the number of bits in the subrange. This is due to the linear search employed at the final conversion stage.

Resembling the approach of [25], Van Rethy *et al.* propose an N bit algorithmic SAR ADC that avoids resetting all the DAC capacitors. The electrical charge in the K MSB capacitors is retained based on signal prediction, and the $(N - K)$ LSB bits are resolved [9]. The value of K is adjusted based on signal activity. The outcome is an SAR ADC that requires $(K + 1) + 2$ bit cycles per conversion when the prediction is correct, and $(N + 1) + 2$ bit-cycles otherwise [26]. In [9] a solution is proposed to improve the predictions, but it would require modifications to the DAC structure.

C. NOVEL TRACKING SAR ADC APPROACH

The previous predictive approaches either lose in precision, or the bit cycles increase disproportionately with prediction errors, unless changes to the analog part are made. Our proposed approach keeps the precision, pays a lower bit cycle penalty in the case of prediction misses, and requires modification only to the digital section of the SAR ADC.

We propose using an arithmetic successive approximation scheme instead of the conventional successive approximation approach. For instance, methods such as [9], [17], and [18]

and assume that the next sample shares the same MSBs with the current one. Otherwise, their advantages are lost. In contrast, our method does not require the consecutive samples to have the same MSBs. Furthermore, the approach is competitive both with slowly changing and periodically highly active signals.

The proposal in [9] is to perform two extra cycles at the beginning of each conversion to compare the analog sample with the upper and lower bounds of the predicted range. However, this introduces a relatively large overhead due to two extra DAC resets. Instead, we employ simple digital logic to check whether the sampled signal falls inside the predicted range, without the involvement of the DAC and the comparator.

Earlier works suggest setting the prediction range for next sample based on the rate of change [26]. However, due to complexity of such digital logic, simple counting based approaches have been used [9], [27]. We propose calculating the difference between two consecutive converted samples, rounding the result up to the nearest power of 2. This improves the prediction performance with minimal digital overhead. Furthermore, as in [9], [17], and [18] the solution is fully digital.

III. ARITHMETIC TRACKING FOR SAR ADC

The following subsections describe the proposed SAR ADC structure in a top-down manner from system to circuit levels.

A. SYSTEM LEVEL SOLUTION

Fig. 2 shows the system level implementation of the proposed arithmetic tracking SAR ADC. The structure is very similar to the conventional SAR ADC, except for additional delay blocks in the digital part. Unlike the conventional design, the proposed arithmetic SAR ADC adds or subtracts a digital step value from the digital input of the DAC. While this solution is not optimal for full dynamic range conversion, it facilitates implementing signal tracking without extra analog circuit components or modifying existing ones.
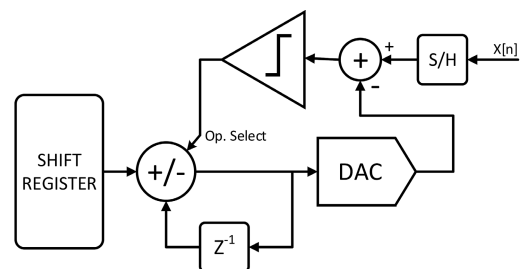

FIGURE 2. A basic conceptual representation of the arithmetic tracking ADC.

In the conversion algorithm depicted in Fig. 3, digital code D from the preceding bit cycle is the input to the DAC. In each cycle, a step value is added or subtracted from D, based on the result of comparison in the previous cycle, and the step value is shifted to the right.
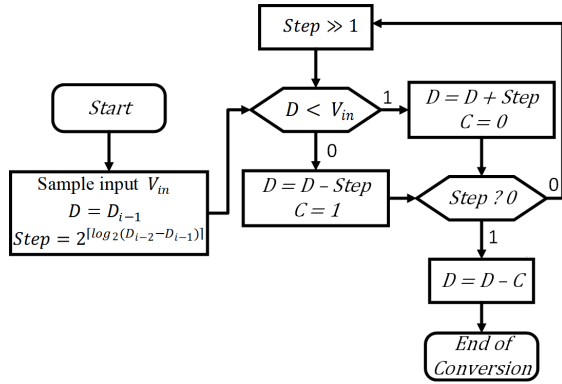
FIGURE 3. The Adaptive Arithmetic Tracking SAR algorithm.

For tracking purposes, and to limit the number of bit cycles, the first step value is determined based on the rate of change. For example, if the starting step value in a 5-bit arithmetic tracking SAR ADC is "01000", the next cycles will add or subtract "01000", "00100", "00010" and "00001". The conversion ends when all bits in the step value have been shifted out. To illustrate the process Figure 4 is a cycle-by-cycle example of the DAC output. By setting the step register MSB to 1 and the other bits to 0, the proposed design operates as a conventional SAR ADC, consuming one cycle per converted bit. However, this is uneconomical due to the extra energy dissipation of the digital logic intended for periodically high active signals. Based on our simulations, the total energy consumption at Nyquist rate is higher than with a conventional SAR ADC implemented with the same component technology. This gap can be narrowed using power and clock gating, but not fully.
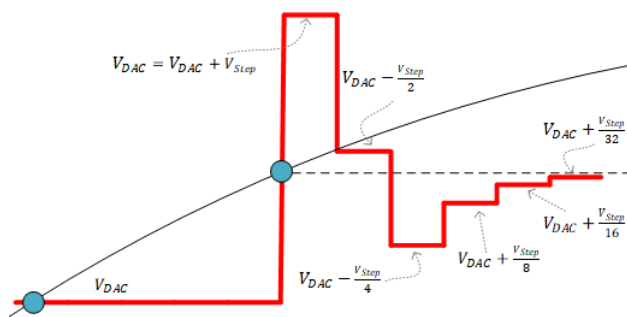

FIGURE 4. Illustration of conversion bit cycles of the arithmetic tracking SAR ADC.

To determine whether the sampled signal was in the predicted range, the outputs of the comparator from all cycles are used. If all those outputs for sample V_{in} are '1', e.g. "111...1", the sample value overshot the prediction range, i.e.

$$D_{i-1} + step + \frac{step}{2} + \ldots + 1 < D_i \qquad (1)$$

In a case where all the comparison results are '0', e.g. "000...0", the sample value undershot the prediction range:

$$D_{i-1} - step - \frac{step}{2} - \ldots - 1 > D_i \qquad (2)$$

Similar to other tracking ADCs, it takes a few samples before the ADC settles and captures the signal. In the worse case, i.e. having the maximum gap between the current random initial value and the actual sample value, it takes 2 conversions to catch up with the input signal due to the employment of a simplified first order predictor (Fig. 7).

If a misprediction occurs, the conversion starts over with the initial step of the regular SAR i.e. setting the MSB to '1' and the other bits to '0'.

The prediction misses can be detected with simple logic checking only the output of the comparator. The functionality of the solution is presented by the state-machine diagram in Fig. 5.
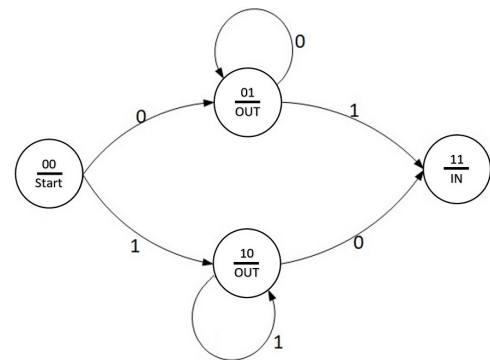

FIGURE 5. Binary output of comparator is input to the state-machine. The "OUT" and "IN" states indicate out of range and in-range conversions, respectively. The diagram can be realized using simple logic as a mealy machine.

To determine the prediction window for the next sample, the two previous consecutive conversions are subtracted and rounded up to the next highest power of 2 value, as shown by equation (3).

$$Step = 2^{\lceil log2(D_{(i-2)} - D_{(i-1)}) \rceil} \qquad (3)$$

B. CIRCUIT LEVEL SOLUTION

Figure 6 presents the structure of the proposed 10 bit SAR ADC, consisting of an S/H circuit, a binary weighted capacitor array for digital to analog conversion (DAC), a dynamic comparator [21], and a digital section. The digital logic includes an adder/subtractor, the necessary delay elements, a subrange extractor and a shift register. Three clocks are employed: the external master clock CLKM, and the internally generated CLKS and CLKSA.

The ADC operates as follows: the predicted conversion range window for the next sample is calculated with the subrange extractor. Before each sample time, the bits A_0 to A_9 of the previous conversion are clocked by CLKSA to the delay elements, generating A_{0D}-A_{9D}. When the sampling clock CLKS goes high, the input signal is sampled to capacitor
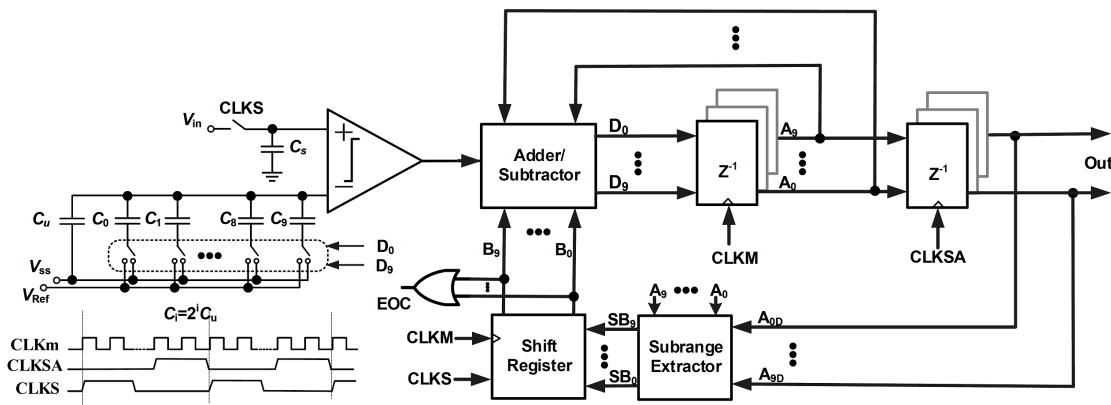
FIGURE 6. The proposed arithmetic tracking SAR ADC. The step Value (B0..B9) is added to and subtracted from value generated in the previous cycle (A0..A9).
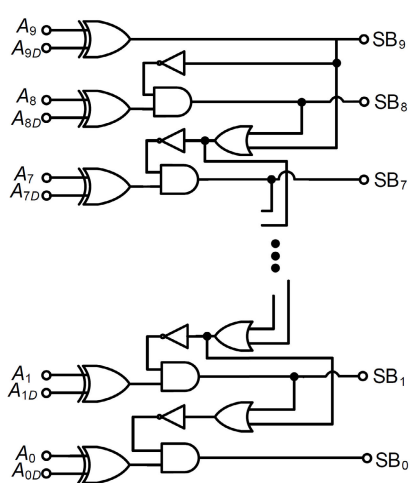

FIGURE 7. The subrange extractor circuit.

C_S, and the difference of A_0-A_9 and A_{0D}-A_{9D} (i.e. subrange SB_0-SB_9) is calculated by the energy efficient asynchronous subrange extractor in Fig. 7 implementing Eq. 3, and loaded to the shift register.

During the conversion cycles, the shift register shifts right bit by bit with CLKM so the output of the adder/subtractor is updated. As the subrange extractor continuously re-calculates the window size, the out of range cases are automatically handled.

As shown in Table 1, on average, only a few conversion cycles per sample are needed for low-activity signals. This provides an opportunity to use power gating and clock gating techniques to save energy. The components without memory, e.g. the comparator, the arithmetic unit, etc., can be safely power gated and the rest can be clock gated through utilization of the End of Conversion (EOC) Signal. That is generated when all the bits in the shift register have been shifted out.

IV. SIMULATION RESULTS
A. BEHAVIORAL SIMULATION

As a proof-of-concept of the conversion algorithm, a 10 bit version of the proposed SAR ADC was simulated due to

challenges of the analog section with higher resolutions. The initial behavioral study of the design was carried out using MATLAB. The objective was to determine the average bit cycle counts per sample in selected application cases.

The mean number of conversion cycles and the misprediction rates for the test signals are shown in Table 1. Biomedical and industrial signals with periodic low activity regions, including ECG, EEG, and image signals were used.

TABLE 1. The average number of bit cycles and miss-rates of the proposed arithmetic SAR and the conventional SAR for different signals.

		ECG	EEG	Image	15kHz sine	10kHz pulses
Mean bit cycles	Prop.	4.0	7.7	3.3	4.4	3.3
	Conv.	10				
Miss rate	Prop.	1%	12%	0.9%	1.5%	1%
	Conv.	0%				
Sampling rate (Hz)		1024	256	N/A	1M	100k

The EEG signals were adopted from [28], while the ECG signals were synthesized using the ECGsyn toolbox [29]. The mean heart rate was set to 60 beats per minute (standard deviation 1 bpm), and was sampled at 1024Hz. The image signal was a gray scale "Lenna" image [30], fed as a 1-D pixel-to-pixel array. Also a 10 kHz 50% duty cycle pulse train and a 15*kHz* sinusoid were used. The former was sampled at a 100kHz and the latter at a 1MHz rate. Except for the EEG signal, the number of bit cycles was cut to less than half.

The conversion cycles were compared with two previous works, i.e [9] and [31] in Fig. 8 with the same test signal. The comparison demonstrates reduced bit cycle counts.

It should be noted that each misprediction requires extra *N* conversion cycles for correction. This is an explanation for the small, below 30% conversion cycle savings in the case of the EEG signal that may not be characterized as a low activity signal. Fig. 9 shows that in the case of abrupt change, the number of bit cycles required to cover the rate of change between samples is quite high.

Figure 10 compares the prediction rates of the proposed approach against the dynamic tracking scheme of [12].
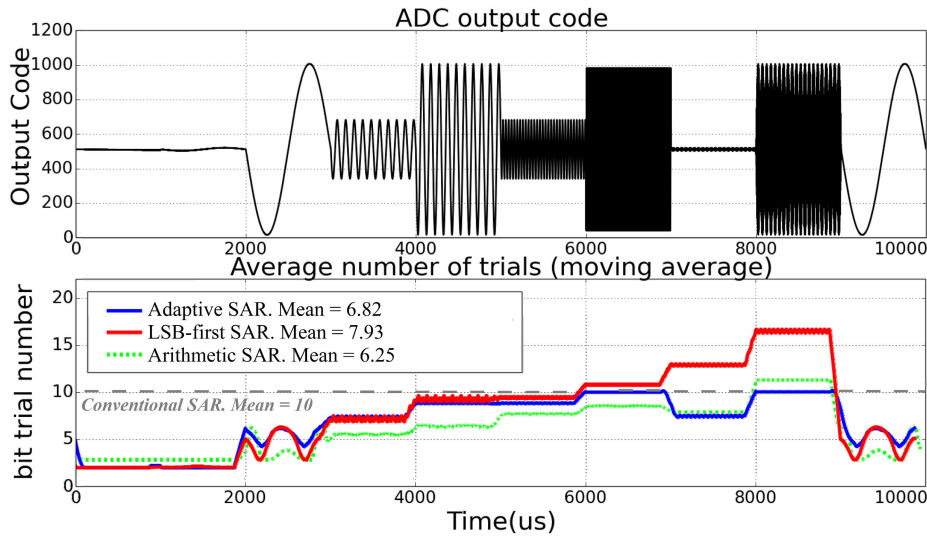
FIGURE 8. The adaptivity of arithmetic SAR ADC versus similar ADCs, "Adaptive SAR" [9], [27] and "LSB-first" [18], [31], to inputs (adapted from [9]).
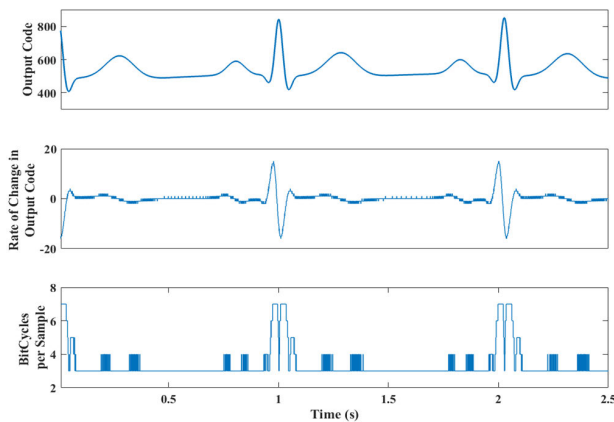

FIGURE 9. Samplewise rate of change and the number of consumed bit cycles for an ECG signal.
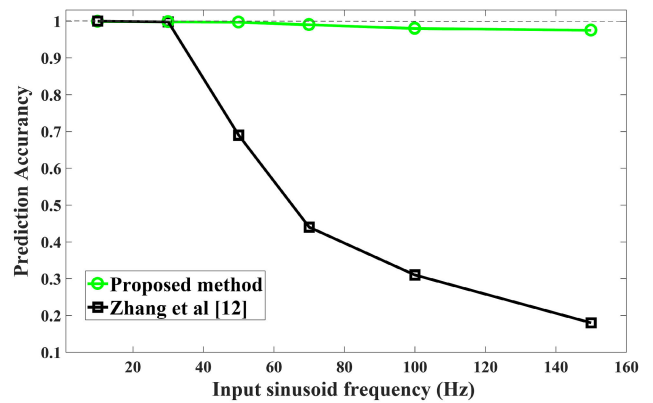

FIGURE 10. Comparison of the prediction performance against the approach of [12] at 10kHz sampling rate.

The latter works well with highly oversampled cases, and has an attractive worst case misprediction cycle count $N + 3$. Unfortunately, the average cycle counts have not been provided. The currently proposed approach achieves better prediction rates at higher signal activity levels.

B. THE TRANSISTOR LEVEL SIMULATION

The proposed SAR ADC approach was simulated using a 90 nm CMOS process to study the energy dissipation. The analog section was powered from 1V and the digital logic from 0.6V. The spectrum of a 1 kHz, -1.03 dbFS sinusoidal input after sampling at 32 kHz is presented in Fig. 11. In the simulations, the circuit noise was not considered. However, to overcome the overall kT/C noise of the ADC, the unit capacitance in the capacitor array (DAC) as well as the sampling capacitor were chosen large enough, $C_u = 20$fF and $C_s = 1$pF, respectively.

With the input signal, the signal-to-noise and distortion ratio (SNDR) of the simulated proposed ADC was found to be 56.4 dB, translating into 9.07 Effective Number Of Bits (ENOB). According to Fig. 11, the spurious-free dynamic range (SFDR) is 56.8 dB, indicating high linearity of the proposed ADC. Based on the simulations at different frequencies the mean and standard deviation of SFDR are 56.1 dB and 0.56 dB, respectively. For SNDR they are 51.6 dB and 0.33 dB.

Due to the negligible power of kT/C noise of the DAC capacitive array and S/H circuit which were calculated according to [20] compared to the signal and quantization noise power, it was omitted from the SNDR calculations.

Table 2 presents a summary of SAR ADCs with signal-specific designs. For comparability, the simulations of the currently proposed approach were carried out using the same parametrizations as in [18]. The circuit level simulations verified the functionality of the proposed scheme, and

TABLE 2. Comparison summary with similar signal specific SAR ADCs.

	[18] [Chip]	[12] [Sim.]	[23] [Sim.]	[32] [Chip]	This Work [Sim.]	
Lossy	No	No	Yes	No	No	
Technology	180nm	130nm	180nm	180nm	90nm	
Unit Cap (fF)	72	51	N/A	63	20	
Supply Voltage(V)	1	0.6	1	1.8	1.0 (analog), 0.6(digital)	0.7(analog), 0.55(digital)
Test input frequency(Hz)	16k	41.5	2k	10k	10k	500
Sampling rate(Hz)	450k	10k	5k	200k	800k	32k
ENOB	9.82	11.7	9.3	10.62	9.07	9
Power (μW)	13	0.96	0.42	40.2	27.6	5.8
FoM (fJ/C-S)	35	28	126.9	127	59	34
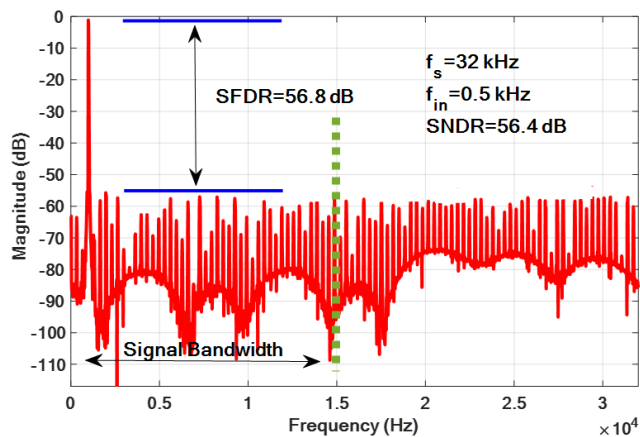
FIGURE 11. Output spectrum of a sampled 1kHz signal by the proposed ADC at a 32kHz sampling rate.

FIGURE 12. Power break down of the proposed ADC.

demonstrated Figure-of-Merit (FoM), i.e. ($\frac{Power}{f_{sampling} \times 2^{ENOB}}$), in the range of the earlier proposals. [2] The main objective of the current contribution has been to demonstrate the functionality and effectiveness of the first-order arithmetic tracking scheme without further optimizations. However, by adopting more advanced circuit techniques, as used in [31], the FoM could be improved further. An example of the potential of optimizations in a signal specific ADC, e.g., by using low-leakage components is [12]. Yaul's circuit design [31] results in less power dissipation than the one used in our simulations; however, as demonstrated by behavioral simulations, our algorithm converges in less cycles.

For the currently proposed SAR ADC, the simulations predict an average power consumption of about 5.8 μW for a 0.5 kHz sinusoidal input at a 32 kHz sampling rate, and 27.6 μW for a 10 kHz sinusoidal at an 800 kHz sampling rate. While the digital logic is supplied from near-threshold 0.6V, it dominates in power dissipation. This also means that advances in digital logic processes would benefit the proposed scheme.

As is seen in Fig. 12, the digital section of the proposed design consumes more energy than that in a conventional

SAR ADC, while the opposite takes place with the analog sections that are the same. The outcome is lower total energy dissipation. Optimization of the digital components would result in larger absolute energy savings with the new design due to its higher gate count.

Monte Carlo simulations were carried out to investigate the impacts of the non-ideality of the DAC and comparator offset. In this simulation $\sigma(\Delta C/C)$ was set to 1% according to the process specifications, and 200 iterations were performed. The SNDR reduced to 55.54 dB from the ideal 56.4 dB. The offset voltage of the simulated comparator is about 21.69 mV, reducing the SNR by 0.38 dB (0.064 ENOB). Considering both the capacitors mismatch and the comparator offset effects, the achieved SNDR is about 55 dB. It should be noted that the power dissipation estimates reported in Table 2 may need up to a 10% increase due to RC parasitic effects addressed in [7], and not explicitly included in current simulations.

V. DISCUSSION AND FUTURE DEVELOPMENT

The proposed arithmetic SAR ADC scheme tackles misprediction detections using digital logic that implements a simple first order predictor. The majority of power is dissipated in the digital logic section as the number of cycles and voltage variations across the DAC are reduced in comparison to a basic SAR ADC. This contributes to power savings both in the comparator and the DAC. Furthermore, as the delay paths in the digital logic are shallow, voltage scaling could be quite safely exploited, providing potential energy savings at lower sampling rates.

As the proposed arithmetic SAR ADC avoids checking the input voltage against the prediction boundary, it optimally

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[2] Notice that the commonly used FoM can be misleading with signal specific ADCs, as it can be boosted by choosing artificially high oversampling factors.

requires performing only $K + 1$ comparisons rather than the $K + 3$ cycles of [9]. Here K is the prediction subrange size. The misprediction penalty for the proposed designs is $(N + K + 1)$, while it is $(N + 1) + 2$ in the case of [9] where it appears to be lower. However, with the proposed approach, the actual misprediction rate was found to be smaller. The worst case bit cycle count of [12] is $N + 3$, but it requires a high oversampling factor to be competitive.

The authors envision that integrating the current solutions to the earlier tracking SAR ADCs, in particular [9], [27], could be most fruitful. The outcome of removing two extra cycles from the out of range detection, and better predictions would together provide significant further energy savings.

Overall, due to added overheads or simplifications in the design, the signal specific ADCs may lose their advantages in applications that do not match the assumptions behind the energy saving schemes.

VI. CONCLUSION

Depending on the characteristics of the input signal, the proposed arithmetic tracking SAR ADC can be more energy efficient than a respective conventional SAR ADC. With its novel digital misprediction detection scheme, the bit cycle efficiency is better than with previous tracking SAR ADC designs. While the analog power dissipation has been reduced, the share of digital logic has increased, but this can be expected to benefit more from circuit technology advances.

ACKNOWLEDGMENT

REFERENCES

[1] P. Harpe, "Ultra-low power analog-digital converters for IoT," in *Enabling the Internet of Things*. Cham, Switzerland: Springer, 2017, pp. 361–383.

[2] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Sel. Areas Commun.*, vol. 17, no. 4, pp. 539–550, Apr. 1999.

[3] *STM32L063C8 Reference Manual*, ST Microelectron., Geneva, Switzerland, 2016.

[4] A. Varshney, O. Harms, C. Pérez-Penichet, C. Rohner, F. Hermans, and T. Voigt, "LoRea: A backscatter architecture that achieves a long communication range," in *Proc. 15th ACM Conf. Embedded Netw. Sensor Syst.*, Nov. 2017, pp. 1–14.

[5] M. Safarpour, R. Inanlou, M. Charmi, O. Shoaei, and O. Silven, "ADC-assisted random sampler architecture for efficient sparse signal acquisition," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 8, pp. 1590–1594, Aug. 2018.

[6] B.-G. Lee and S.-G. Lee, "Input-tracking DAC for low-power high-linearity SAR ADC," *Electron. Lett.*, vol. 47, no. 16, pp. 911–913, 2011.

[7] R. Inanlou and M. Yavari, "A 10-bit 0.5 V 100 kS/s SAR ADC with a new rail-to-rail comparator for energy limited applications," *J. Circuits, Syst., Comput.*, vol. 23, no. 2, 2014, Art. no. 1450026.

[8] E. Rahiminejad, M. Saberi, and R. Lotfi, "A power-efficient signal-specific ADC for sensor-interface applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 9, pp. 1032–1036, Sep. 2017.

[9] B. Chen, F. Yaul, Z. Tan, and L. Fernando, "An adaptive SAR ADC for DC to Nyquist rate signals," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[10] B. Razavi, "A tale of two ADCs: Pipelined versus SAR," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 3, pp. 38–46, Sep. 2015.

[11] B. Razavi, *Principles of Data Conversion System Design*, vol. 126. New York, NY, USA: IEEE Press, 1995.

[12] Z. Zhang, J. Li, Q. Zhang, K. Wu, N. Ning, and Q. Yu, "A dynamic tracking algorithm based SAR ADC in bio-related applications," *IEEE Access*, vol. 6, pp. 62166–62173, 2018.

[13] H.-W. Lu, X.-P. Yu, Z.-H. Lu, K.-S. Yeo, and J.-M. Chen, "A data-dependent energy reduction algorithm for SAR ADC using self-adaptive window," *Microelectron. J.*, vol. 100, Jun. 2020, Art. no. 104754.

[14] K. C.-H. Chiang, N. S. Artan, and H. J. Chao, "A signal-specific approach for reducing SAR-ADC power consumption," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, Oct. 2013, pp. 278–281.

[15] B.-G. Lee, "Power and bandwidth scalable 10-b 30-MS/s SAR ADC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 6, pp. 1103–1110, Jun. 2015.

[16] B. Razavi, "The delta-sigma modulator [a circuit for all seasons]," *IEEE Solid State Circuits Mag.*, vol. 8, no. 2, pp. 10–15, Jun. 2016.

[17] S. Yim, Y. Park, H. Yang, and S. Kim, "Power efficient SAR ADC adaptive to input activity for ECG monitoring applications," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[18] F. M. Yaul and A. P. Chandrakasan, "A 10b 0.6 nW SAR ADC with data-dependent energy savings using LSB-first successive approximation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 198–199.

[19] A. Waters, J. Leung, and U.-K. Moon, "LSB-first SAR ADC with bit-repeating for reduced energy consumption," in *Proc. 21st IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2014, pp. 203–206.

[20] R. Inanlou and M. Yavari, "A simple structure for noise-shaping SAR ADC in 90 nm CMOS technology," *AEU-Int. J. Electron. Commun.*, vol. 69, no. 8, pp. 1085–1093, Aug. 2015.

[21] M. Shahghasemi, R. Inanlou, and M. Yavari, "An error-feedback noise-shaping SAR ADC in 90 nm CMOS," *Anal. Integr. Circuits Signal Process.*, vol. 81, no. 3, pp. 805–814, Dec. 2014.

[22] M. Safarpour, R. Inanlou, O. Silven, T. Rahkonen, and O. Shoaei, "A reconfigurable dual-mode tracking SAR ADC without analog subtraction," in *Proc. Signal Process., Algorithms, Archit., Arrangements, Appl. (SPA)*, Sep. 2019, pp. 28–32.

[23] M. Nasserian, A. Peiravi, and F. Moradi, "An adaptive-resolution signal-specific ADC for sensor-interface applications," *Anal. Integr. Circuits Signal Process.*, vol. 98, no. 1, pp. 125–135, Jan. 2019.

[24] S.-L. Chen, J. F. Villaverde, H.-Y. Lee, D. W.-Y. Chung, T.-L. Lin, C.-H. Tseng, and K.-A. Lo, "A power-efficient mixed-signal smart ADC design with adaptive resolution and variable sampling rate for low-power applications," *IEEE Sensors J.*, vol. 17, no. 11, pp. 3461–3469, Jun. 2017.

[25] J. Van Rethy, M. De Smedt, M. Verhelst, and G. Gielen, "Predictive sensing in analog-to-digital converters for biomedical applications," in *Proc. Int. Symp. Signals, Circuits Syst. (ISSCS)*, Jul. 2013, pp. 1–4.

[26] N. Wood and N. Sun, "Predicting ADC: A new approach for low power ADC design," in *Proc. IEEE Dallas Circuits Syst. Conf. (DCAS)*, Oct. 2014, pp. 1–4.

[27] B. Chen, E. C. Guthrie, M. C. Coln, and M. D. Maddox, "Incremental preloading in an analog-to-digital converter," U.S. Patent 10 038 452, Jul. 31, 2018.

[28] F. Aloise, P. Aricò, F. Schettini, A. Riccio, S. Salinari, D. Mattia, F. Babiloni, and F. Cincotti, "A covert attention P300-based brain–computer interface: Geospell," *Ergonomics*, vol. 55, no. 5, pp. 538–551, May 2012.

[29] P. E. McSharry, G. D. Clifford, L. Tarassenko, and L. A. Smith, "A dynamical model for generating synthetic electrocardiogram signals," *IEEE Trans. Biomed. Eng.*, vol. 50, no. 3, pp. 289–294, Mar. 2003.

[30] R. C. Gonzalez, R. E. Woods, and S. L. Eddins, *Digital Image Processing Using MATLAB*. London, U.K.: Pearson Education India, 2004.

[31] F. M. Yaul and A. P. Chandrakasan, "A 10 bit SAR ADC with data-dependent energy reduction using LSB-first successive approximation," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2825–2834, Dec. 2014.

[32] H.-W. Chang, H.-Y. Huang, Y.-H. Juan, W.-S. Wang, and C.-H. Luo, "Adaptive successive approximation ADC for biomedical acquisition system," *Microelectron. J.*, vol. 44, no. 9, pp. 729–735, Sep. 2013.
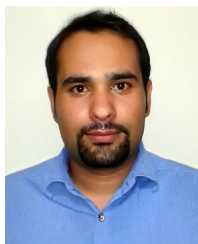
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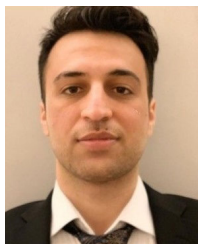
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