IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 28, 2020, accepted November 17, 2020, date of publication November 20, 2020,
date of current version December 9, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3039343

Evaluation Model of Loop Stray Parameters for Energy Storage Converter of Hybrid Electric Locomotive

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This work was supported by the Key Project of the State Key Laboratory of Heavy Duty AC Drive Electric Locomotive Systems Integration under Grant 172195100750.

ABSTRACT When the silicon carbide (SiC) power module is applied to the energy storage converter of a hybrid locomotive, under the action of di/dt and loop stray inductance, it is easy to produce excessively high voltage overshoot, which affects the battery life and stimulates high-frequency oscillations, causing power devices to withstand greater electrical stress. In order to optimize the system layout and improve system performance, it is extremely necessary to accurately extract and evaluate the loop inductance. This paper takes the typical high-frequency converter structure as the object, establishes an equivalent model of the circuit, and quantitatively analyzes the loop inductance from a mathematical point of view. For the circuit after the parallel of absorption capacitor, the small signal model is used to analyze and reveal the role and influence of the absorption capacitor. Finally, the calculation results of the model are compared through a double-pulse experiment. The results show that the error between the model and the experimental results is about 1%, and the effect of evaluating the stray parameters of the converter circuit is good, and it can provide a theoretical support for the selection and design of the absorption capacitor.

INDEX TERMS SiC module, commutation circuit, stray inductance, extraction and evaluation.

I. INTRODUCTION

Bidirectional DC/DC converters are widely used in energy storage converters of hybrid locomotive, connecting power batteries or super capacitors as auxiliary power [1], [2]. With the development of power electronic devices, reducing volume, reducing cost and improving reliability have become research hotspots. Silicon carbide (SiC) devices have the characteristics of high thermal conductivity, fast switching speed and high blocking voltage [3]. Power electronic devices based on SiC modules solve the contradiction between high converter operating voltage and low power module withstand voltage, and also greatly increase the switching frequency of the converter and reduce the volume of the output filter devic [4], [5], which has extremely broad potential in the application of energy storage converters for hybrid locomotives.

The associate editor coordinating the review of this manuscript and approving it for publication was Yijie Wang.

Under the high-frequency and high-voltage working environment, the action of SiC MOSFET switching momentary excessive di/dt and loop inductance will induce higher electrical stress and reduce battery life. In addition, high-order harmonics are generated, which affects the performance of the system, and may also cause problems such as switching losses [6], electromagnetic interference [7], and noise pollution [8], and even endanger the normal operation of the system in severe cases. In order to implement targeted suppression measures, it is extremely necessary to accurately extract and evaluate the stray inductance of the power loop.

Loop inductance mainly includes device parasitic inductance, stray inductance of connecting parts and bus capacitance parasitic inductance [9]–[11], etc. Existing literature researches on the extraction method of stray inductance are mostly for laminated busbars. Literature [12] sorts out the transient process of turn-on and turn-off, and finds the most favorable stage for the extraction of stray inductance, combining the method of integral operation to extract the stray

inductance. Literature [13] studies the laminated busbar of the five-level converter module, and tests the proposed method by comparing simulation and experiment. Reference [14] improves the traditional integration method by considering stray resistance and measurement offset, and improves the calculation accuracy. Literature [15] proposes to use the oscillation frequency during the turn-on and turn-off process to extract the loop inductance by analyzing the switching transient process of SiC MOSFET, which improves the accuracy. Although many literatures have proposed the optimization of the extraction method of stray inductance, most of the analysis is to improve the accuracy of the experimental extraction method from the analysis of the transient process of the device switching. The mathematical quantitative analysis of the power loop stray parameter model is not performed.

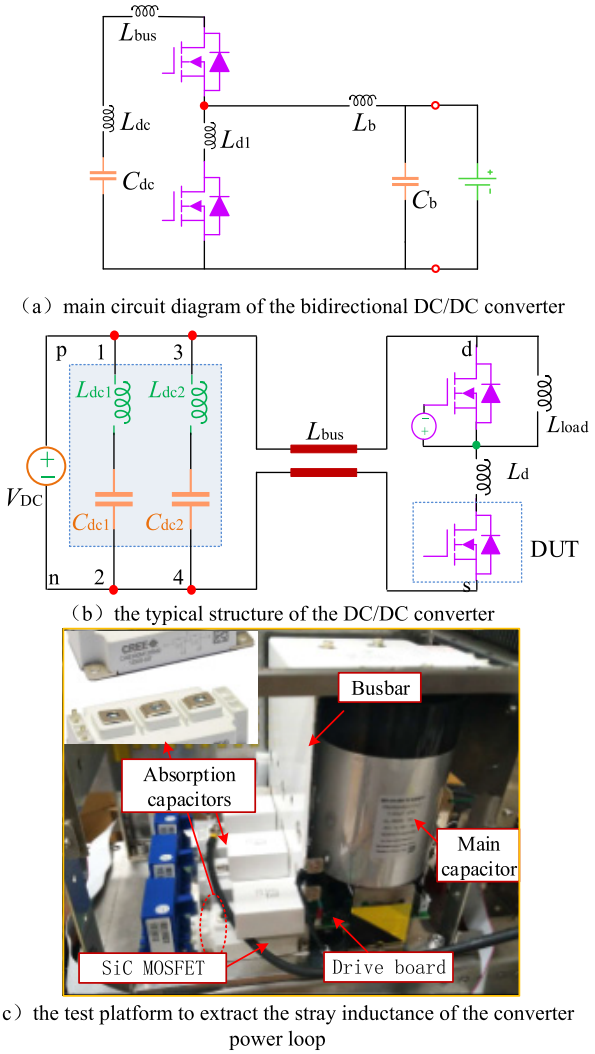
In order to enrich the theoretical basis and reduce the test cost, based on the previous research, this paper takes the bidirectional DC/DC converter based on SiC power module as the object, and establishes the stray parameter mathematical model of the power loop in sections. We quantitatively calculate the stray inductance of each part of the loop, and evaluate the proportion and influence of each section of stray parameters in the power loop. Finally, a double-pulse experiment is conducted to verify the accuracy of the theoretical analysis and the applicability of the evaluation model.

II. EXPERIMENTAL PLATFORM BASED ON SiC MOSFET

Figure 1(a) is the main circuit diagram of the bidirectional DC/DC converter, including support capacitor C_{dc}, support capacitor parasitic inductance L_{dc}, stacked bus bar L_{bus}, parallel SiC power module, filter inductor L_b and filter capacitor C_b, L_{d1} is SiC module parasitic inductance. This article takes the typical structure of the DC/DC converter shown in Figure 1(b) as the object, and builds the test platform shown in Figure 1(c) to extract the stray inductance of the converter power loop. Including DC voltage V_{DC}, support capacitance C_{dc1}, C_{dc2}, support capacitance parasitic inductance L_{dc1}, L_{dc2}, laminated bus bar L_{bus}, load inductance L_{load} and DUT.

The device under test is selected from Cree's CAS300M17BM2 half-bridge power module. The support capacitor and the power module are connected by a busbar. The busbar adopts a laminated structure, and the current between the positive and negative plates is reversed, which makes the magnetic field cancel and the busbar inductance reduced. In order to further reduce the loop inductance, absorption capacitors can be connected in parallel at the positive and negative ports of the power device. The absorption capacitor, the support capacitor and the power device are connected to the bus bar through bolts. The DC input terminal is supported by two supporting capacitors in parallel; during the test, the two ends of the upper tube gate source are turned off by applying negative pressure.

The test method is the traditional double-pulse test method. Figure 2 shows the timing diagram of the double-pulse test.



(a) main circuit diagram of the bidirectional DC/DC converter

(b) the typical structure of the DC/DC converter

(c) the test platform to extract the stray inductance of the converter power loop

FIGURE 1. SiC module test platform.

After the device under test is pressurized to stability, at time t_0, the SiC MOSFET is turned on for the first time, and the drain current rises; At the first turn-off at time t_1, the current change rate di/dt acts on the loop stray inductance and forms a voltage spike at both ends of the device after being superimposed with the bus voltage; At time t_2, the device is turned on for the second time, and the reverse parallel diode of the upper tube reversely recovers, resulting in an overshoot of the drain current; at t_3, the device is turned off, and a large voltage overshoot is formed again across the device under test. At this moment, the current change rate changes significantly, and the SiC junction capacitance has little effect, which is suitable for the extraction of stray parameters.

III. MODEL OF CONVERTER CIRCUIT CONSIDERING PARASITIC PARAMETERS

The converter circuit includes four parts as shown in Figure 3: support capacitor, laminated busbar, absorption capacitor and power module. The parasitic inductance of the power module can be obtained from the data sheet. This article mainly analyzes the other three parts.

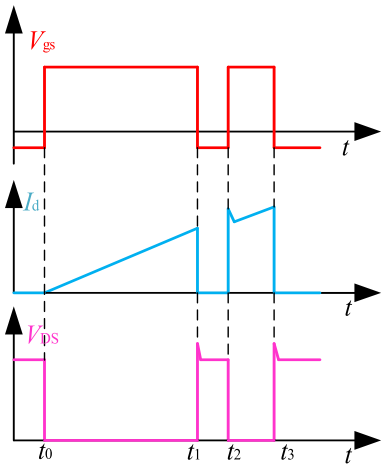


FIGURE 2. Double pulse signal timing diagram.

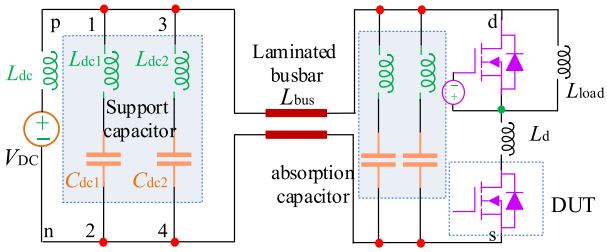


FIGURE 3. Complete parasitic parameters model.

A. SUPPORT CAPACITANCE PARASITIC INDUCTANCE

The wide-band characteristic of the support capacitor is characterized by an RLC circuit, where R_{dc1}, C_{dc1}, and L_{dc1} are the stray resistance, main capacitance, and parasitic inductance of the support capacitor, respectively. Single support capacitors are directly connected in series by RLC. In this paper, two support capacitors are connected in parallel as an example for analysis. The equivalent circuit is shown in Figure 4.

Before the test process, first charge the supporting capacitor. Therefore, the positive electrodes of C_{dc1} and C_{dc2} are equipotential points. Equations (1)∼(3) give the parameter values of each element in the process of equivalent transformation.

$$\begin{cases} G_{dc1} = \dfrac{R_{dc1}}{R_{dc1}^2 + (\omega L_{dc1})^2} \\ G_{dc2} = \dfrac{R_{dc2}}{R_{dc2}^2 + (\omega L_{dc2})^2} \\ B_{dc1} = -\dfrac{\omega L_{dc1}}{R_{dc1}^2 + (\omega L_{dc1})^2} \\ B_{dc2} = -\dfrac{\omega L_{dc2}}{R_{dc2}^2 + (\omega L_{dc2})^2} \\ C_{dc} = C_{dc1} + C_{dc2} \end{cases} \tag{1}$$

$$\begin{cases} G_{dc} = G_{dc1} + G_{dc2} \\ B_{dc} = B_{dc1} + B_{dc2} \end{cases} \tag{2}$$

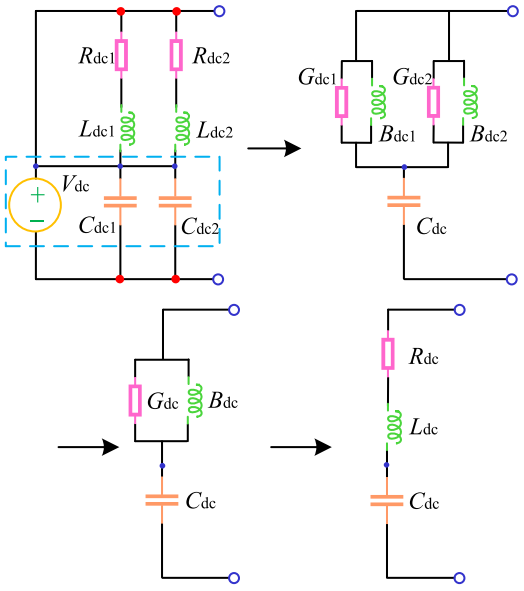


FIGURE 4. Main capacitors equivalent circuit.

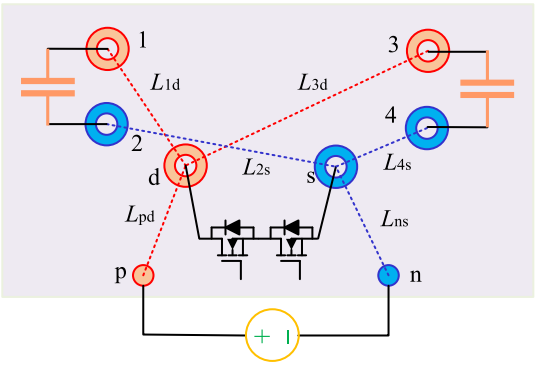


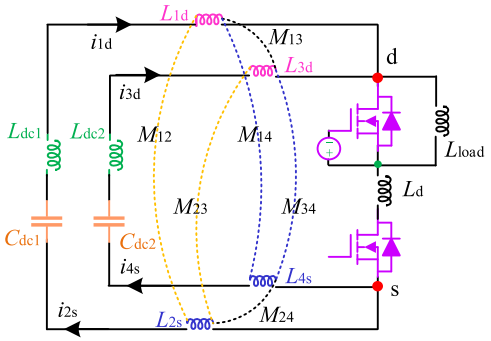
FIGURE 5. Schematic diagram of stray inductance distribution of laminated busbars.

$$\begin{cases} R_{dc} = \dfrac{G_{dc}}{G_{dc}^2 + B_{dc}^2} \\ L_{dc} = -\dfrac{B_{dc}}{\omega(G_{dc}^2 + B_{dc}^2)} \end{cases} \tag{3}$$

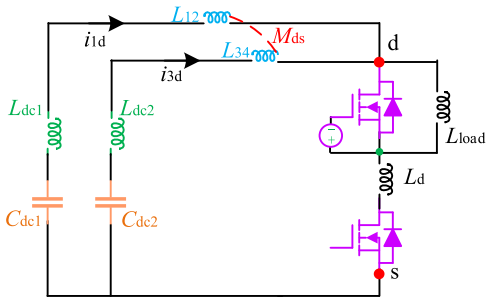
B. STRAY INDUCTANCE OF LAMINATED BUSBAR

According to the circuit structure of FIG. 1, FIG. 5 draws a schematic diagram of each stray inductance branch in the bus bar. In the figure, L_{1d}, L_{2s}, L_{3d}, L_{4s}, L_{pd} and L_{ns} are the inductance from C_{dc1} to SiC MOSFET positive electrode, from C_{dc1} to SiC MOSFET negative electrode, from C_{dc2} to SiC MOSFET positive electrode, from C_{dc2} to SiC MOSFET negative electrode, from DC power supply to SiC MOSFET positive electrode, from DC power supply to SiC MOSFET negative, respectively.

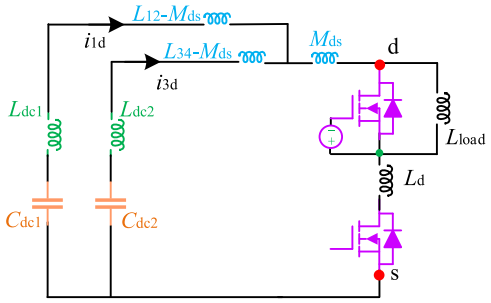
There is direct mutual inductance in each branch inductance. Figure 6 shows the topology of the double-pulse test circuit. v_{1d}, v_{3d}, v_{s4}, v_{s2} are the terminal voltages of L_{1d}, L_{3d}, L_{2s}, L_{4s}, respectively. The volt-ampere characteristic formula of the stacked busbar with two supporting capacitors



（a）consider the circuit diagram of mutual inductance of laminated bus branches



（b）equivalent circuit diagram



（c）decoupling equivalent circuit diagram

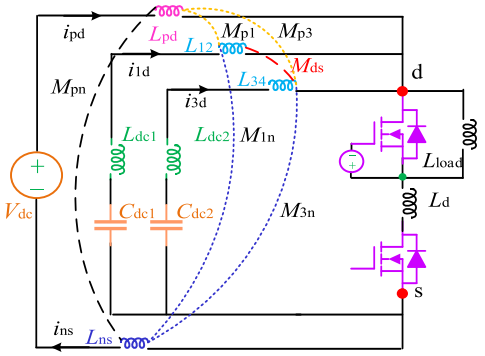
FIGURE 6. Topology of a stacked busbar considering mutual inductance.

in parallel is shown in equation (4).

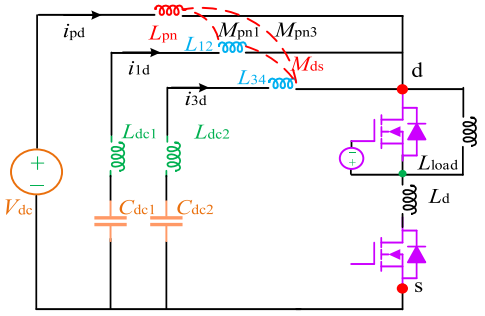
$$V_{bus} = j\omega L I_{bus}$$
$$L_{bus} = \begin{bmatrix} L_{1d} & M_{13} & M_{14} & M_{12} \\ M_{31} & L_{3d} & M_{34} & M_{32} \\ M_{41} & M_{43} & L_{4s} & M_{42} \\ M_{21} & M_{23} & M_{24} & L_{2s} \end{bmatrix}$$
$$V_{bus} = \begin{bmatrix} v_{1d} \\ v_{3d} \\ v_{s4} \\ v_{s2} \end{bmatrix} \quad I_{bus} = \begin{bmatrix} i_{1d} \\ i_{3d} \\ i_{s4} \\ i_{s2} \end{bmatrix} \tag{4}$$

In equation (4), L_{bus} is a 4×4 inductance matrix, and the inductance in FIG. 6(b) can be expressed using equation (5).

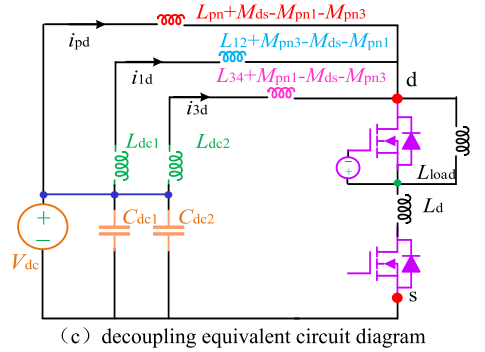
$$\begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{1d} \\ v_{3d} \\ v_{s4} \\ v_{s2} \end{bmatrix} = j\omega \begin{bmatrix} L_{12} & M_{ds} \\ M_{sd} & L_{34} \end{bmatrix} \begin{bmatrix} i_{1d} \\ i_{3d} \end{bmatrix} \tag{5}$$



（a）Consider the circuit diagram of mutual inductance of laminated bus branches



（b）equivalent circuit diagram



（c）decoupling equivalent circuit diagram

FIGURE 7. Topology of inverter commutation circuit when 2 supporting capacitors are connected in parallel.

Decouple the two parallel coupled inductors to obtain a structure in which L_{12}-M_{ds} and L_{34}-M_{ds} are connected in parallel and then in series with M_{ds}. The calculation formula of the two parallel coupled inductors is shown in equation (6).

$$L_{bus} = \frac{(L_{12} - M_{ds}) \cdot (L_{34} - M_{ds})}{L_{12} + L_{34} - 2M_{ds}} + M_{ds} \tag{6}$$

For a single support capacitor loop, the model calculation formula is:

$$L_{12} = L_{1d} + L_{2s} + 2M_{12} \tag{7}$$

In the inverter commutation circuit, the branches L_{pd} and L_{ns} between the DC power supply and the busbar should also be considered. Figure 7 shows the distribution of the stray inductance of each branch of the inverter commutation

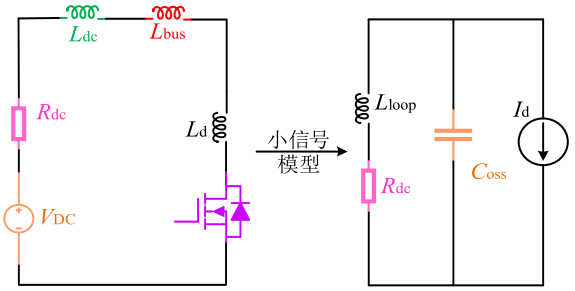


FIGURE 8. Small-signal equivalent model of the test platform.

circuit. The analysis method is the same as that of the test platform with double supporting capacitors in parallel. According to equation (8), the inductance of the power supply branch can be obtained:

$$L_{pn} = L_{pd} + L_{ns} + 2M_{pn} \tag{8}$$

For the coupled inductance of three branches in parallel, there is independence during decoupling conversion, and only one or a few of them can be decoupled. The circuit after decoupling the star-connected circuit is shown in Figure 7(c).

Due to the parasitic inductance of the supporting capacitor, the DC side ends of the three equivalent branch inductances are no longer equipotential points. The two branches connecting the support capacitor and the positive pole of the power module should be connected in series with the support capacitor first, and then in parallel with the equivalent inductance of the DC voltage branch in the laminated busbar. At this time, the equivalent inductance of the inverter commutation loop can be obtained as shown in equation (9).

$$\begin{aligned} L_{loop} &= L_o + L_d \\ &\begin{cases} L_o = \dfrac{L_aL_b + L_aL_c + L_bL_c}{L_aL_bL_c} \\ L_a = L_{pn} + M_{ds} - M_{pn1} - M_{pn3} \\ L_b = L_{12} + M_{pn3} - M_{ds} - M_{pn1} + L_{dc1} \\ L_c = L_{34} + M_{pn1} - M_{ds} - M_{pn3} + L_{dc2} \end{cases} \\ M_{pn1} &= \begin{bmatrix} M_{p1} & M_{p2} \\ M_{n1} & M_{n2} \end{bmatrix} \quad M_{pn3} = \begin{bmatrix} M_{p3} & M_{p4} \\ M_{n3} & M_{n4} \end{bmatrix} \end{aligned} \tag{9}$$

C. THE FUNCTION AND INFLUENCE OF ABSORPTION CAPACITOR

After absorbing capacitors in parallel, the overvoltage phenomenon caused by stray inductance can be suppressed, but at the same time, the circuit structure is changed, making the circuit into a higher-order system, and it is difficult to obtain an analytical expression using time-domain analysis. This paper analyzes the circuit using the small-signal model of SiC MOSFET in the complex frequency domain. SiC MOSFTE is approximately a constant current source with a certain increase. According to the principles of DC current source open circuit and voltage source short circuit, Figure 8 shows the small signal equivalent model of the test platform.

The expression of loop inductance is:

$$L_{loop} = L_{dc} + L_{bus} + L_d \tag{10}$$

According to the equivalent circuit, the input admittance of the circuit is:

$$\begin{aligned} Y &= j\omega C_{oss} + \frac{1}{R_{dc} + j\omega L_{loop}} \\ &= \frac{R_{dc}}{R_{dc}^2 + j\omega^2 L_{loop}^2} + j(\omega C_{oss} - \frac{\omega L_{loop}}{R_{dc}^2 + j\omega^2 L_{loop}^2}) \end{aligned} \tag{11}$$

When the imaginary part is 0, the circuit resonates. Therefore, the resonance condition of the circuit is:

$$\omega C_{oss} - \frac{\omega L_{loop}}{R_{dc}^2 + j\omega^2 L_{loop}^2} = 0 \tag{12}$$

The resonance frequency is:

$$\omega = \sqrt{\frac{L_{loop} - R_{dc}^2 C_{oss}}{L_{loop}^2 C_{oss}}} \tag{13}$$

In order to ensure that the circuit resonates, it should be guaranteed $R_{dc} < (L_{loop}/C_{oss})^{1/2}$. When $R_{dc} \ll (L_{loop}/C_{oss})^{1/2}$, the resonance frequency of the circuit is approximately:

$$\omega \approx \sqrt{\frac{1}{L_{loop}C_{oss}}} \tag{14}$$

At this time, the circuit is approximately GCL parallel, and its equivalent admittance is:

$$\begin{aligned} Y &= \frac{R_{dc}}{R_{dc}^2 + j\omega^2 L_{loop}^2} + j(\omega C_{oss} - \frac{\omega L_{loop}}{R_{dc}^2 + j\omega^2 L_{loop}^2} \\ &\approx \frac{R_{dc}}{\omega^2 L_{loop}^2} + j(\omega C_{oss} - \frac{1}{\omega L_{loop}}) \end{aligned} \tag{15}$$

The loop impedance is:

$$Z = \frac{L_{loop}}{R_{dc}C_{oss}} \tag{16}$$

The closer the absorption capacitor is to the SiC module, the better the absorption effect. Figure 9 is a test platform circuit and its equivalent model of parallel absorption capacitors.

After the parallel absorption capacitor, during the switching process, the support capacitor will first charge the absorption capacitor, and then the absorption capacitor will discharge to the power module, so Figure 9(a) can be equivalent to Figure 9(b). According to the foregoing, when the absorption capacitor is close to the port of the power module, selecting an absorption capacitor with a sufficient value can completely absorb the voltage spike introduced by the parasitic inductance of the support capacitor and the stray inductance of the busbar, but at the same time, it will introduce parasitic inductance of the absorption capacitor.

$$C_{snub} = \lambda \cdot C_{oss} \tag{17}$$

When the voltage spikes caused by L_{dc} and L_{bus} are completely absorbed, the resonance impedance of L_{dc}, L_{bus}

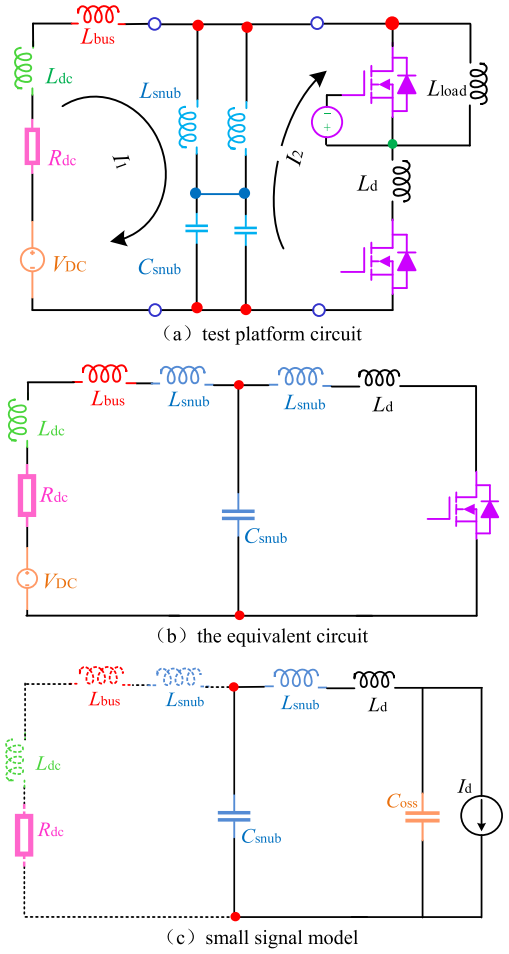


FIGURE 9. Circuit diagram of test platform for parallel absorption capacitors.

and the absorption capacitor is much smaller than the L_{stray} impedance at the resonance frequency.

$$Z_1 \ll j\omega(L_{stray} + L_{snub})$$
$$Z_1 = \frac{j\omega(L_{dc} + L_{bus} + L_{snub}) \cdot \frac{1}{j\omega C_{snub}}}{j\omega(L_{dc} + L_{bus} + L_{snub}) + \frac{1}{j\omega C_{snub}}} \quad (18)$$

Simultaneous (17) and (18):

$$\lambda \gg \frac{L_{loop}}{L_{dc} + L_{bus} + L_{snub}} + \frac{L_{loop}}{L_{stray} + L_{snub}} \quad (19)$$

In addition, the absorption capacitor is connected in parallel at both ends of the device. After complete absorption, only the absorption capacitor parasitic inductance L_{snub} and power device stray inductance L_{stray} are in the loop. Therefore, the selection of the absorption capacitor is based on the two principles of capacitance and parasitic inductance. When $L_{snub} < L_{stray}/10$, the influence of L_{snub} can be ignored, so the requirement for its parasitic inductance when selecting the absorption capacitor is

$$L_{snub} < \frac{n}{10} L_{stray} \quad (20)$$

$L_{sn} = nL_{snub}$, L_{sn} is the parasitic inductance of a single absorption capacitor, n is the number of parallel absorption capacitors.

At this time, the loop stray inductance is:

$$L_{loop} = L_{snub} + L_{stray} \quad (21)$$

IV. STRAY PARAMERER EXTRACTION BASED ON CALCULATION MODEL AND Q3D

The stray parameters include four parts: supporting capacitance parasitic inductance, stacked busbar stray inductance, absorption capacitance parasitic inductance and power module parasitic inductance. Two supporting capacitors are connected in parallel and three absorption capacitors are connected in parallel. The parameters in the analysis model are shown in Table 1.

TABLE 1. Parameters in the analysis model.

Model	Parameter	Numerical value
Support capacitance	C_{dc}/uF	1120
	L_{dc}/nH	40
	R_{dc}/mΩ	0.65
Absorption capacitance	C_{snub}/uF	1
	L_{snub}/nH	32
SiC MOSFET	C_{gd}/nF	0.12
	C_{gs}/nF	19.18
	C_{ds}/nF	2.45
	L_{stray}/nH	15
Load inductance	L_{load}/nH	70

According to formula (1) ∼ formula (3), the supporting capacitance parasitic inductance L_{dc} can be calculated as 20nH; The inductance of the laminated busbar is composed of mutual inductance and self-inductance. Figure 10 shows the busbar model built in Q3D software according to Figure (1)b. The principle of applying the excitation source is based on the actual test. For example, the supporting capacitor and power device are connected to the busbar with bolts, so the excitation source can be applied to the corresponding screw hole of the positive and negative busbars, and the simulation step and frequency are set according to the double pulse test time. After the inductance of each branch is obtained, calculation is performed according to equation (7), and the result is 25.1 nH. The parasitic inductance of the power device is obtained from the data sheet. According to equation (10), the loop inductance of the test platform can be obtained as 60.1nH.

V. EXPERIMENTAL EXTRACTION AND VERIFICATION OF STRAY PARAMETERS

Build a dual-pulse test platform based on the dual-pulse test schematic shown in Figure 1(b), and extract the stray

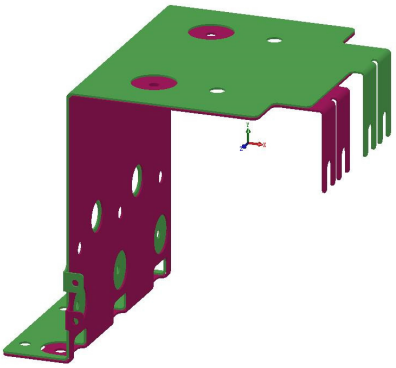
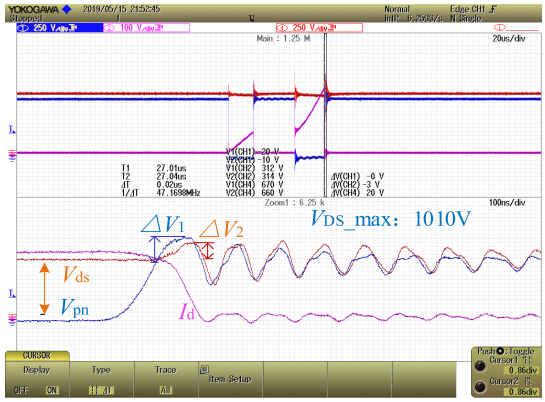


FIGURE 10. Busbar simulation model.



（a）both ends of power module

（b）supporting capacitance both ends

FIGURE 11. Experimental waveforms during shutdown.

inductance of each part of the power loop according to the waveform of the SiC MOSFET module off process.

A. STRAY PARAMETERS WITHOUT ABSORPTION CAPACITANCE

Select the positive-negative port, output-negative (down tube DS) and supporting capacitor port of the power module as the voltage test points to obtain the experiment waveform of voltage V_{DS} across the lower tube of the SiC MOSFET, the power module terminal voltage V_{pn}, the supporting capacitor terminal voltage V_{dc} and the drain current I_d, which is shown in Figure 11.

1) The stray inductance of the power loop is extracted according to the relationship between the volt-ampere characteristics of the inductor given by equation (22).

$$V_{ds} = V_{DC} - V_{Rdc} - L_{loop}\frac{di_d}{dt} \tag{22}$$

Among them, V_{Rdc} is the voltage drop of the stray resistance.

$$L_{loop} = \frac{\int_{t_1}^{t_2} \Delta V_1 dt}{|i_d(t_2) - i_d(t_1)|} \tag{23}$$

Similarly, equation (24) gives the calculation formulas for the supporting capacitance parasitic inductance and the stray inductance of the laminated busbar.

$$\begin{cases} L_{dc} = \dfrac{\int_{t_1}^{t_2} \Delta V_3 dt}{|i_d(t_2) - i_d(t_1)|} \\ L_{bus} = \dfrac{\int_{t_1}^{t_2} \Delta V_2 dt}{|i_d(t_2) - i_d(t_1)|} - L_{dc} \end{cases} \tag{24}$$

Table 2 summarizes the stray inductance of each part obtained by model calculation and experiment extraction.

TABLE 2. Inductance of each part.

	L_{dc}/nH	L_{bus}/nH	L_d/nH	L_{loop}/nH
Theoretical analysis	20	25.1	15	60.1
Experimental extraction	23.2	20.9	16.45	60.55

B. STRAY PARAMETERS AFTER PARALLEL ABSORPTION CAPACITORS

After the parallel absorption capacitors at the positive and negative ports of the power module, the experimental waveforms of the voltage V_{DS} across the lower tube of the SiC MOSFET, the voltage V_{pn} at the power module terminal, and the drain current I_d are shown in Figure 11. Table 3 statistics the inductance values of each part after theoretical analysis and experimental measurement after parallel absorption capacitors. After the parallel absorption capacitor, the absorption capacitor absorbs the overvoltage caused by the bus capacitor and the laminated bus bar, but at the same time introduces parasitic inductance. According to the experimental results, after a 1uF absorption capacitor is connected in parallel, the loop inductance is reduced by 21.95nH, and an absorption capacitance parasitic inductance of 13.6nH is introduced at the same time.

C. COMPARATIVE ANALYSIS OF EXPERIMENTAL RESULTS AND MODELS

When there is no parallel absorption capacitor, the measured loop inductance is basically consistent with the theoretical calculation. The parasitic inductance of the supporting capacitor and the parasitic inductance of the power device are

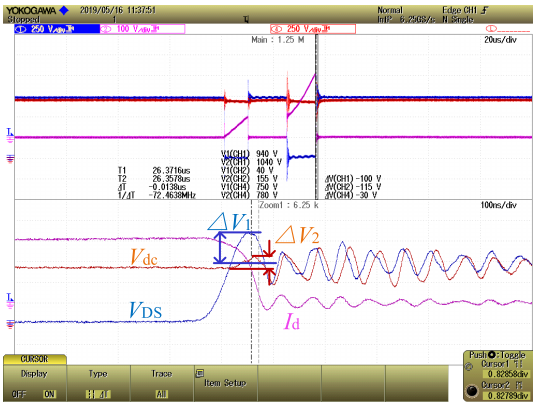


FIGURE 12. Experimental waveforms of the shutdown process when the absorption capacitors are connected in parallel.

TABLE 3. Inductance of each part after parallel absorption capacitor.

	L_{snub}/nH	L_d/nH	L_{loop}/nH
Theoretical analysis	10.7	15	25.7
Experimental extraction	13.6	25	38.6

slightly larger than the theoretical value. This is due to the fact that the voltage probe is clamped on the busbar and bolts are introduced during the experimental measurement, which causes the terminal voltage generated by the busbar inductance to be small and L_{dc} and L_d too large. The equivalent inductance of the bus capacitor and the stacked busbar series is 44.1nH. After the absorption capacitor absorbs it completely, the parasitic inductance of 13.6nH is introduced, which is close to the theoretical analysis. This error is caused by the position where the probe is clamped during the measurement. Because the actual structure uses bolt connection, the probe can only be clamped inside the busbar, causing the measured value of the voltage spike at both ends of the busbar inductance to be small, and the L_{dc} and L_d ends are measured The value is too large. This is an inherent measurement error. Combined with the ANSYS Q3D simulation results of the busbar, the analysis of the error is correct and reasonable, and the measured value of the total loop inductance is consistent with the theoretical analysis, which can prove the effectiveness of the method. The existence of this error can better prove the value of the calculation model proposed in this article, because it can compensate for the inherent error of the measurement. We have further analyzed the mechanism of this error in the updated article.

Table 4 makes statistics on the proportion of inductance of each part in the power loop inductance before and after the parallel absorption capacitor. The parasitic inductance of the power module is based on the measured value when there is no parallel absorption capacitor.

TABLE 4. Proportion of inductance value of each part.

	L_{dc}	L_{bus}	L_d	L_{snub}	L_{others}
Absorption capacitor not connected in parallel	38.3%	34.5%	27.2%	0	0
Parallel absorption capacitor	0	0	41.6%	35%	23.4%

Before the parallel absorption capacitor, the parasitic inductance of the supporting capacitor accounted for the highest proportion of 38.3%, followed by the laminated busbar, accounting for 34.5%, and the parasitic inductance of the SiC module depends on the manufacturing process. When the busbar structure is fixed, the more supporting capacitors are connected in parallel, the smaller the loop equivalent inductance value. Therefore, we can try to use more supporting capacitors in parallel to reduce the loop inductance.

After the parallel absorption capacitor, the parasitic inductance introduced by the absorption capacitor accounted for the highest proportion, and the extra stray parameters due to insufficient contact of the absorption capacitor pin and contact accounted for 23.4%. When installing the absorption capacitor, multiple capacitors with small parasitic inductance should be connected in parallel as much as possible, and the capacitor can be fully contacted with the SiC module. In addition, attention should be paid to the parasitic inductance of the capacitor pin when selecting.

VI. CONCLUSION

In this paper, based on the SiC module-based hybrid locomotive energy storage converter converter circuit, a loop stray parameter evaluation model is established, and the stray inductance of each part of the power circuit is quantitatively calculated from a mathematical point of view. Firstly, the distribution of loop stray inductance is analyzed, and then the mathematical model of supporting capacitance equivalent circuit and laminated busbar considering the self-inductance and mutual inductance of the branch is established, and the effect of the absorption capacitance on the converter circuit is revealed through the small signal model. And influence. Finally, the results of model calculation and experiment extraction are compared to verify the accuracy and practicability of the model. The model can be used to calculate the power loop inductance of the converter in sections, clarify the distribution of stray parameters in the loop, and provide strong support for further optimization of the system structure layout. The model is still applicable to other similar topologies.

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