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Comprehensive Analysis of Quantum Mechanical Effects of Interface Trap and Border Trap Densities of High-k $Al_2O_3/In_{0.53}Ga_{0.47}As$ on a 300-mm Si Substrate

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ABSTRACT We investigated the effects of quantum confinement in determining the interface traps (D_{it}) and border traps (N_{bt}) of ALD deposited Al_2O_3 with temperature variations onto $In_xGa_{1-x}As$ on a 300-mm Si (001) substrate. We also analysed the impact of these effects on the total gate capacitance of high-*k*/Si and high-*k*/$In_xGa_{1-x}As$ structures using 1D Poisson-Schrodinger solver simulation tool (Nextnano). While quantum confinement has no or very little impact on the gate capacitance of high-*k*/Si structure, it has a considerably high amount of impact on the high-*k*/$In_xGa_{1-x}As$ structures and substantially lowers the total gate capacitance. To reflect the actual thickness between the insulator-semiconductor interface and charge centroid, capacitance-equivalent-thickness was used to reflect the effects of quantum confinement in the $In_xGa_{1-x}As$ layer. The D_{it} and N_{bt} values extracted using capacitance-equivalent-thickness were observed to be around 10% and 25%, respectively, higher than the values of extraction with equivalent-oxide-thickness.

INDEX TERMS Interface trap density, border trap density, quantum mechanical effect, high-*k*, III-V substrate.

I. INTRODUCTION

Traditional Si/SiO_2 metal-oxide-semiconductor devices have reached the peak limit of scalability. Different high-*k* dielectrics as an insulator and III-V based materials as a channel have been widely researched for their scalability, which extensively increases speed with the help of high electron mobility and reduces power consumption of devices [1]–[5]. Whereas high-*k* materials and their nanolaminates such as Al_2O_3, HfO_2, La_2O_3, ZrO_2, and $HfAlO_x$ are under broad investigation as a substitute for SiO_2 [2], [6]–[10]. Recently, the $In_xGa_{1-x}As$ channel with high-*k* has been considered as a replacement of Si as a channel material with outstanding electron transport properties [2]–[5], [8], [10]. High-*k*/Si as well as high-*k*/III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs) have the prospective advantage of equivalent-oxide-thickness (EOT) scaling over SiO_2/Si devices. With EOT scaling, high-*k* dielectrics show low leakage current while maintaining high switching speed compared to silicone dielectrics. III-V materials such as $In_xGa_{1-x}As$ have higher electron velocities, which result in considerably better electron transport properties compared to Si [5], [11]. This high electron mobility can contribute to high on-state current and faster switching speed. However, this high electron mobility originates from the low effective mass of III-V channel material, which contributes to the lower density of states (DOS) to the channel layer [12]–[14]. Because of this low DOS, during the strong inversion, Fermi level (E_F) moves inside the conduction band (E_C) [15]. This phenomenon reduces the effective barrier height between the oxide and channel, which leads to the charging/discharging of the oxide traps with channel electrons via tunnelling [16], [17].

In MOSFETs, the charged defects that occur between the insulating layer and channel layer are mostly interface traps (D_{it}) and border traps (N_{bt}). The D_{it} is located at the

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interface of the insulator and channel [18], [19]. On the other hand, N_{bt} is positioned in the insulator near the interface of the insulator and channel interface with energy states inside the channel bandgap [20], [21] (Figure 1a). By exchanging carriers with the channel material, these traps can change charge states which significantly reduces devices performance. These traps can cause Fermi level pinning and lower the carrier generation in the channel, hence reducing the drive current and sub-threshold swing [22]. There are several prominent methods of extracting D_{it} and N_{bt}. Among these, the conductance method for the extraction of D_{it} and the distributed border trap model for N_{bt} extraction are well recognised [2], [23]–[26]. Both methods used the measured gate capacitance (C_m) and conductance (G_m) characteristics for the extraction of traps. The total gate capacitance (C_g) can be modelled as a series connection of insulator capacitance (C_{ins}) and inversion-layer capacitance (C_{inv}) [27]. Inversion-layer capacitance (C_{inv}) can be represented by two series capacitances known as quantum capacitance (C_q) and centroid capacitance (C_{cent}) [28], [29]. Quantum capacitance (C_q) originates due to the injection of Fermi level E_F inside the conduction band E_C, and centroid capacitance (C_{cent}) is related to the average charge distance from the interface of the insulator and channel [30], [31]. In conventional Si-based MOS devices, values of quantum capacitance (C_q) and centroid capacitance (C_{cent}) are comparatively large, so the total gate capacitance approaches the oxide capacitance (C_{ox}) [30], [32], [33]. However, in small scaled III-V based MOS devices these capacitances tend to be smaller and comparable to oxide capacitance (C_{ox}) and lead to a smaller total gate capacitance (C_g). In determining the oxide thickness, generally physical thickness (t_{ox}) or EOT is considered, but they do not provide a clear consideration of these mentioned effects for III-V based MOS devices. Capacitance-equivalent-thickness (CET) considers these effects and provides more accurate results for D_{it} and N_{bt} extraction. Figure 1b provides a clear illustration of these effects including quantum capacitance and centroid capacitance.

In previous works, comprehensive analysis or consideration of quantum mechanical effects while extracting D_{it} was not included [34]–[37], but another study included these effects in determining N_{bt} while comparing the values extracted based on physical oxide thickness t_{ox} [38]. In contrast, we endeavoured to show a comprehensive study of these effects in determining both D_{it} as well as N_{bt}, and made a comparison with the values acquired based on EOT. We also thoroughly analysed the effects of quantum mechanical confinements in Si and III-V structures.

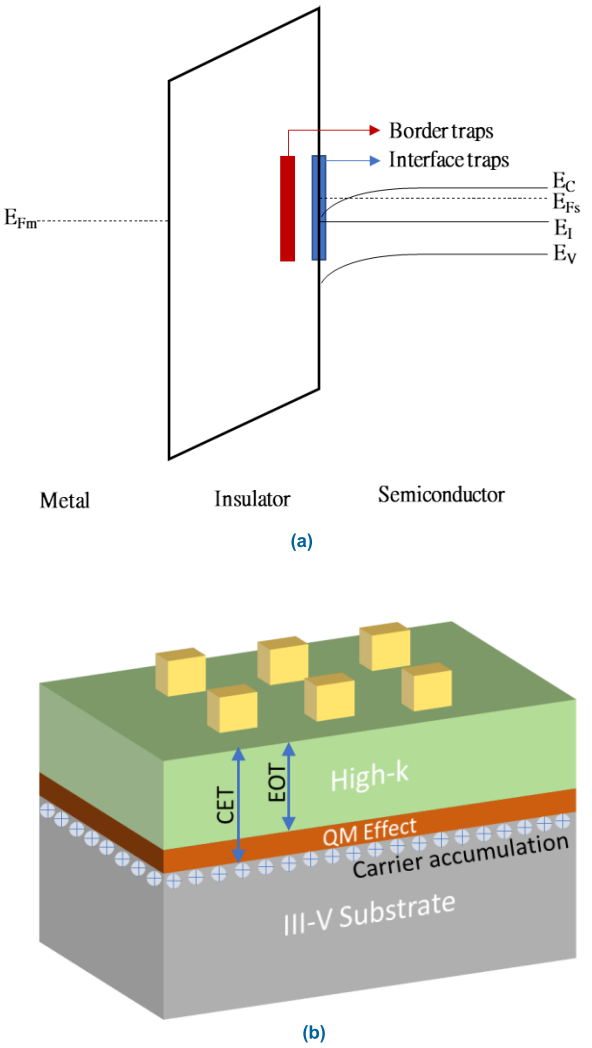

FIGURE 1. (a) Schematic band diagram of the metal/insulator/semiconductor structure showing interface traps (D_{it}) and border traps (N_{bt}). (b) Visual representation of quantum mechanical confinement in the III-V substrate.

II. MODEL DESCRIPTION

A. GATE CAPACITANCE MODEL

The total gate capacitance of $In_xGa_{1-x}As$ MOS devices can be represented as a series combination of two capacitances known as insulator capacitance (C_{ins}) and inversion-layer capacitance (C_{inv}) (Figure 2a), considering that beneath the channel, there is no doping level. Inversion-layer capacitance (C_{inv}) consists of several parallel combinations of quantum capacitance (C_{q_i}) and centroid capacitance (C_{cent_i}), which are connected in series and represent the contribution of each occupied electron sub-band in the channel. The total inversion-layer capacitance can be written as:

$$C_{inv\_i} = \frac{\partial(-Q_s)}{\partial \psi_s} = \frac{q\partial(-Q_s)}{\partial(E_F - E_C)} \tag{1}$$

Here, Q_s represents total electron charge in the channel, ψ_s represents surface potential, E_F is Fermi level and E_C is the conduction band edge, which is located at the insulator channel interface. Q_s, which is the summation of all sub-band charges, can be given as:

$$Q_s = \sum_i Q_i = \sum_i \int_{E_i}^{\infty} \frac{\frac{m^*_{||} q}{\pi \hbar^2}}{1 + e^{\left(\frac{E - E_F}{kT}\right)}} dE \tag{2}$$

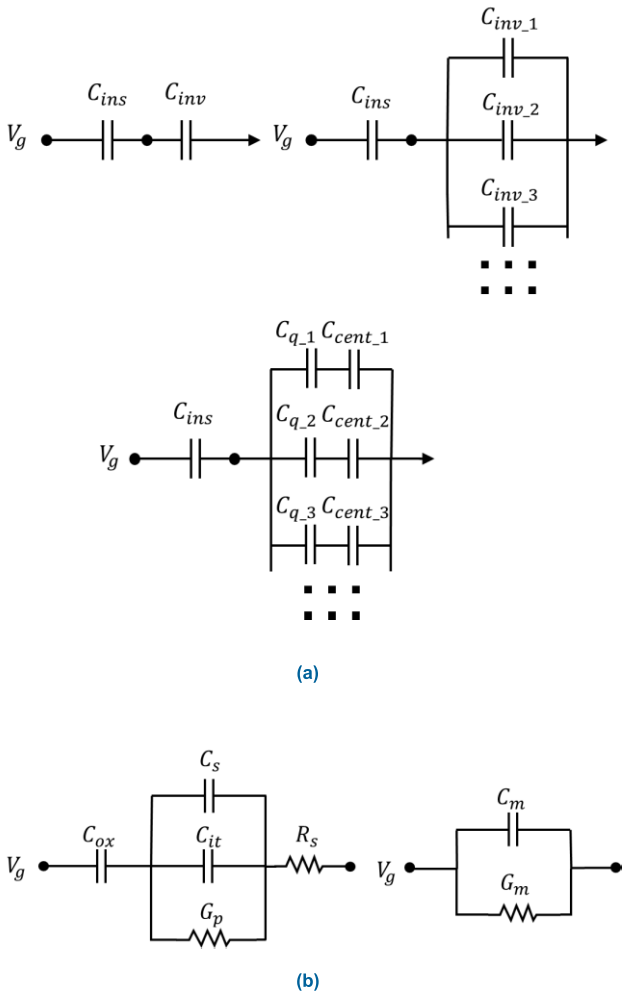

FIGURE 2. (a) Equivalent gate capacitance circuit diagram of an III-V field effect transistor. (b) Equivalent circuit of metal oxide semiconductor device in depletion mode.

Here, Q_i is the total electron charge of the sub-band i located at the channel, the energy level of the sub-band i is E_i, and $m^*_{||}$ denotes as the in-plane effective mass of the channel material, which can be calculated from the following equation [39]:

$$m^*_{||} = m^*_0(1 + \alpha E) = \frac{\hbar^2 k^2}{2E} \tag{3}$$

where, m^*_0 is referred to as the effective mass at $k = 0$, the energy and wave number of the charge carrier are E and k, respectively, $\hbar$ is the reduced Plank's constant, and α is referred to as the nonparabolicity parameter. The quantum capacitance (C_{q_i}) of any particular sub-band i can be mathematically extracted from the derivative of electron charge of that particular sub-band with respect to the difference of energy between E_F and E_i:

$$C_{q\_i} = \frac{q\partial(-Q_i)}{\partial(E_F - E_i)} = \frac{q\partial\left(-\int_{E_i}^{\infty} \frac{\frac{m^*_{||}q}{\pi\hbar^2}}{1+e^{\left(\frac{E-E_F}{kT}\right)}} dE\right)}{\partial(E_F - E_i)}$$

$$= \frac{\frac{m^*_{||}q^2}{\pi\hbar^2}}{1 + e^{\left(\frac{E_i - E_F}{kT}\right)}} \tag{4}$$

Likewise, the centroid capacitance (C_{cent_i}) is the derivative of electron charge of that particular sub-band i with respect to the difference of energy between E_F and E_C:

$$C_{cent\_i} = \frac{q\partial(-Q_i)}{\partial(E_F - E_C)} = C_{q\_i} \cdot \frac{\partial(E_F - E_i)}{\partial(E_F - E_C)} \tag{5}$$

From the above equations C_{inv_i} can be expressed as:

$$C_{inv\_i} = \sum_i \left(\frac{1}{C_{q\_i}} + \frac{1}{C_{cent\_i}}\right)^{-1} \tag{6}$$

Inversion-layer capacitance can be calculated if the location of each sub-band energy level (E_i) and Fermi level (E_F) are known with respect to the conduction band edge.

B. INTERFACE TRAP DENSITY EXTRACTION MODEL

We used the conductance method for the extraction of interface traps (D_{it}). The conductance method analyses the loss occurred by the change of the trap level charge state. With lower response time τ, traps with an energy level closer to the Fermi level (E_F) can change their occupancy. Figure 2b shows the equivalent circuit diagram of a MOS capacitor in depletion which contains interface traps. C_{ox} is the oxide capacitance, C_s is the semiconductor capacitance and R_s is a series resistance. Here, C_{it} and G_p represent the equivalent parallel interface trap capacitance and conductance, respectively, which are formed by interface traps [24], [40]. The interface trap capacitance is denoted as $C_{it} = qD_{it}$, where, q is the charge of the element and D_{it} is the interface trap density [24], [41]. When electrons are captured by the interface traps, a direct contribution is made to the formation of interface trap capacitance C_{it}. The trap response can be evaluated by the Shockley-Read-Hall statistics of capture and emission rates [2], [42]–[44]:

$$\tau = \frac{1}{2\pi f} = \frac{1}{\omega} = \frac{e^{\left(\frac{\Delta E}{K_B T}\right)}}{\sigma v_{th} D_{dos}} \tag{7}$$

Here, ΔE represents the difference of energy between the trap level E_T and the majority carrier band edge, either E_C or E_V, K_B is the Boltzmann constant and T is the temperature. The cross section of traps is represented by σ, v_{th} is the average thermal velocity of majority carriers, and D_{dos} is the effective density of states of the majority carrier band. Figure 2b represents the equivalent circuit for analysing the impedance with measured capacitance C_m and measured conductance G_m. These measured values must be corrected for series resistance R_s [45]:

$$R_s = \frac{G_{ma}}{G^2_{ma} + \omega^2 C^2_{ma}} \tag{8}$$

Here, C_{ma} and G_{ma} are measured capacitance and conductance in the accumulation respectively, and ω is the angular frequency.

For the correction of capacitance and parallel equivalent conductance, we can use the following equations [24]:

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{\left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]^2 + \omega^2 C_m^2} \tag{9}$$

$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) \left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]}{\left[G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s\right]^2 + \omega^2 C_m^2} \tag{10}$$

The equivalent parallel conductance can be measured from the following relation:

$$G_p = \frac{\omega^2 C_{ox} G_c}{G_c^2 + \omega^2 \left(C_{ox} - C_c\right)^2} \tag{11}$$

Here, C_{ox} is the insulator capacitance. So, D_{it} can be calculated from the normalized parallel conductance peak $(G_p/\omega)_{max}$ [45]:

$$D_{it} \approx \frac{2.5}{Aq} \left(\frac{G_p}{\omega}\right)_{\max} \tag{12}$$

Here, A is the device area.

We can use Eq. 7 to determine trap occupancy in the energy level where f is the frequency determined from the conductance peak $(G_p/\omega)_{max}$ [2].

C. BORDER TRAP DENSITY EXTRACTION MODEL

For border trap extraction, we used the distributed circuit model. Generally, the border traps in the insulator and the mobile carriers in semiconductor bands can exchange charge. Usually this charge exchange occurs through tunnelling [26]. The average time for an empty trap to capture electron is denoted by τ, which is exponentially proportional to the distance x between the trap and interface [46], [47].

$$\tau = \tau_0 e^{2kx} \tag{13}$$

where,

$$k = \frac{\sqrt{2m* \times E_b}}{\hbar}$$

Here, τ_0 represents capture/emission time constant and k is the attenuation coefficient. The effective mass of the insulator is denoted by m^*, E_b is the barrier height between the insulator and semiconductor conduction bands, and $\hbar$ is the reduced Plank's constant. Note that τ_0 can also be defined as:

$$\tau_0 = (n_s v_{th} \sigma)^{-1} \tag{14}$$

Here, n_s is the electron density of the semiconductor surface, v_{th} is the electron thermal velocity, and σ is the capture cross-section area of the border trap. When the device is in accumulation, the Fermi level is close to the conduction band. In this situation, n_s can become relatively equal to the density of states of the conduction band[48]. Assuming $\omega\tau = 1$, at any particular applied frequency (f) the probing depth of a border trap can be measured as:

$$X_p = \frac{1}{2k} \ln \frac{1}{2\pi f \tau_0} \tag{15}$$

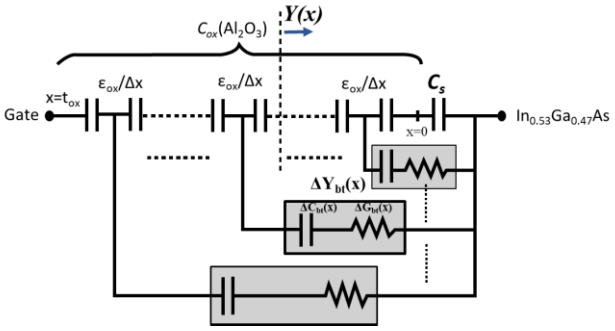

FIGURE 3. Equivalent circuit of distributed bulk oxide trap model representing a metal oxide semiconductor device [25], [26].

Figure 3 shows the equivalent circuit model for border trap extraction. To the extract border trap, this distributed border trap model analyses the dispersion of the frequencies in the accumulation region at any particular gate bias voltage. In this model, oxide capacitance is divided into small capacitive components, $\varepsilon_{ox}/\Delta x$, where ε_{ox} is the permittivity and Δx is the small portion of oxide thickness. Border trap induced charge and loss of energy is demonstrated by a series of admittance for a particular portion of thickness. Total admittance consists of series connected capacitance C_{bt} and conductance G_{bt} in parallel to the insulator capacitance. Semiconductor capacitance C_s is connected in series. This whole structure can be represented by a differential equation of first order:

$$\frac{\partial Y}{\partial x} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{q^2 N_{bt} \ln\left(1 + j\omega\tau\right)}{\tau} \tag{16}$$

Here, the boundary condition is x = 0, Y = j$\omega$$C_s$ (Y = Total admittance). ω is the angular frequency, q is the electron charge and N_{bt} represents the border trap density of the oxide layer.

III. EXPERIMENTAL DETAILS

We used metal organic chemical vapour deposition (MOCVD) to create a n-type $In_{0.53}Ga_{0.47}As$ heterostructure. Firstly, on top of a 300-mm n-type Si (001) substrate, we grew two strain relaxation buffer epitaxies of GaAs and InP. We followed the Volmer-Weber growth mode. The carrier concentration of GaAs and InP are 2×10^{17} cm^{-3} with thicknesses of 350 nm and 800 nm, respectively. Then two consecutive layers of Si-doped n- $In_{0.53}Ga_{0.47}As$ was formed. The first layer had 5×10^{17} cm^{-3} electron density and a 110-nm thickness, and the second layer has 1×10^{17} cm^{-3} electron density and a 160-nm thickness. We prepared a total of three samples with different ALD oxide deposition temperatures. The substrates were cleaned with isopropyl alcohol and acetone for several minutes. They were then immersed in a 1:10 solution of diluted hydrochloric acid and deionized water at room temperature for 30 seconds such that no native oxide could form. Then the substrates were removed from the solution and cleaned with deionized water. We used

ambient nitrogen (N_2) to remove any remaining water from the substrate surface. After the cleaning procedure, the substrates were separately placed in the ALD chamber for oxide deposition. The ALD chamber was pre-cleaned with 10 cycles of trimethyl aluminium (TMA). Then 30 cycles of Al_2O_3 was ALD deposited at 200°C, 250°C and 300°C growth temperature, respectively. TMA and water were used as the metal precursor and oxidant, respectively. Nitrogen (N_2) flowing at 300 sccm was used for the carrier and purge gas. A 5-nm layer of TiN was deposited by ALD. A 200-nm metal layer of Au was deposited both as the front as well as the back-side contact by E-beam evaporation. Before the front side metal deposition, the physical thickness of the samples was extracted using ellipsometry (incident angle = 70°). For the 200°C, 250°C and 300°C ALD-deposited samples, the physical thicknesses t_{ox} were evaluated to be 4.2006 nm, 3.867 nm and 3.5128 nm, respectively. For extracting the exact effective dielectric constant ε_{ox} of the samples, we prepared a metal insulator metal (MIM) capacitor. A 300-mm n-type Si (001) substrate was pre-cleaned using the same methods as above. Then the substrate was delivered into the thermal evaporator where Al was deposited using thermal evaporation as the bottom electrode. The substrate was then placed in the ALD chamber for oxide deposition for 100 cycles of Al_2O_3 at 250°C. TMA and water were used as the metal precursor and oxidant, respectively. For both the carrier as well as purge gas, we again used nitrogen (N_2) at 300 sccm. Al was deposited as the front side metal using thermal evaporation with a shadow mask. All capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were conducted using a Keysight B1500A semiconductor device analyser and an Agilent 4384A precision LCR meter. The measurement frequency range was between 10 KHz and 1 MHz. The effective relative permittivity ε_{ox} was determined using the following equation:

$$\varepsilon_{ox} = \frac{C_{mim} t_{mim}}{\varepsilon_0} \tag{17}$$

Here, C_{mim} is the measured capacitance, t_{mim} is the thickness of the MIM capacitor.

For EOT and CET extraction, we used the following equations:

$$EOT = \frac{3.9 \times t_{ox}}{\varepsilon_{ox}} \tag{18}$$

$$CET = \frac{3.9 \times \varepsilon_0}{C_{acc}} \tag{19}$$

Here, C_{acc} is the measured accumulation capacitance of the MOS capacitors.

IV. RESULT DISCUSSION

Using the Nextnano simulation tool, we resolved the self-consistent solution of the one-dimensional Poisson and Schrodinger equations [49]. We also extracted the total sheet charge density Q_s, values of sub-band energy E_i, conduction band energy E_C and Fermi level energy E_F with this same simulation tool. By differentiating the total sheet charge density with respect to the applied gate bias voltage, we calculated the capacitances of MOS devices. Figure 4a shows the C-V curves of simulated Al_2O_3/Si and Al_2O_3/$In_{0.53}Ga_{0.47}As$ structures as well as the measured C-V curves of Al_2O_3/$In_{0.53}Ga_{0.47}As$. Here, we considered the ideal dielectric constant ($k = 9$) and measured the thickness of Al_2O_3 to determine the insulator capacitance C_{ins}. From Figure 4a, we can see that the gate capacitance of the Si structure is very close to the insulator capacitance, which indicates no or very low inversion layer capacitance effect. On the other hand, the simulated as well as the measured capacitances of the $In_{0.53}Ga_{0.47}As$ devices were around 55-60% of the C_{ins}, showing the high impact of the inversion layer capacitance on scaled down III-V devices. Figure 4(b, d) shows the sub-band energy levels of Al_2O_3/Si and Al_2O_3/$In_{0.53}Ga_{0.47}As$ structures, respectively. For Si structure, the Fermi level penetrates only the first sub-band energy level (E_1), but for $In_{0.53}Ga_{0.47}As$ structure, it penetrates the first and second sub-band energy levels, and was very close to penetrating the third sub-band. To extract the inversion layer capacitance components, the conduction band effective mass of Si and $In_{0.53}Ga_{0.47}As$ were considered to be $0.98m_0$ and $0.043m_0$ (m_0 is the rest mass of electron) with the consideration of a non-parabolicity effect[50]. Figure 4(c, e) shows the inversion layer capacitances of Al_2O_3/Si and Al_2O_3/$In_{0.53}Ga_{0.47}As$ structures. Quantum capacitance (C_q) is related to the electron mobility, effective mass and density of states (DOS) of the channel material. $In_{0.53}Ga_{0.47}As$ has lower effective mass and density of states (DOS) compared to Si, which induces lower quantum capacitance in $In_{0.53}Ga_{0.47}As$. From Figure 4(c, e) we can see that C_q and C_{cent} of Si substrate is very large compared to the insulator capacitance (C_{ins}).

Because of this high amount of inversion layer capacitance, it has very little to no impact on the gate capacitance. On the contrary, we can see that C_{inv1} of the $In_{0.53}Ga_{0.47}As$ structure is close to the insulator capacitance, thus it has a greater effect on the gate capacitance. C_{inv2} is much smaller compared to C_{inv1} due to a lower electron density in the second sub-band energy level.

We used a MIM capacitor to extract the dielectric constant of Al_2O_3 used in our samples. The dielectric constant was found to be 7.19 using Eq. 17. The oxide capacitance C_{ox} was calculated by dividing the total oxide permittivity by EOT or CET for each case. EOT and CET were calculated according to the Eq. 18 and Eq. 19, respectively. For the CET calculation, C_{acc} was the capacitance value from 100 KHz frequency at 1 V gate voltage. To extract the density of interface traps (D_{it}) of the samples, the following procedure was used. Parallel conductance G_p was measured in accordance with Eq. 11 with corrected measured conductance G_c and corrected measured capacitance C_c. D_{it} was extracted using Eq. 12 with the help of the parallel conductance peak $(G_p/\omega)_{max}$. Table. 1 shows the values of different parameters used in the D_{it} extraction process. Figure 5a shows

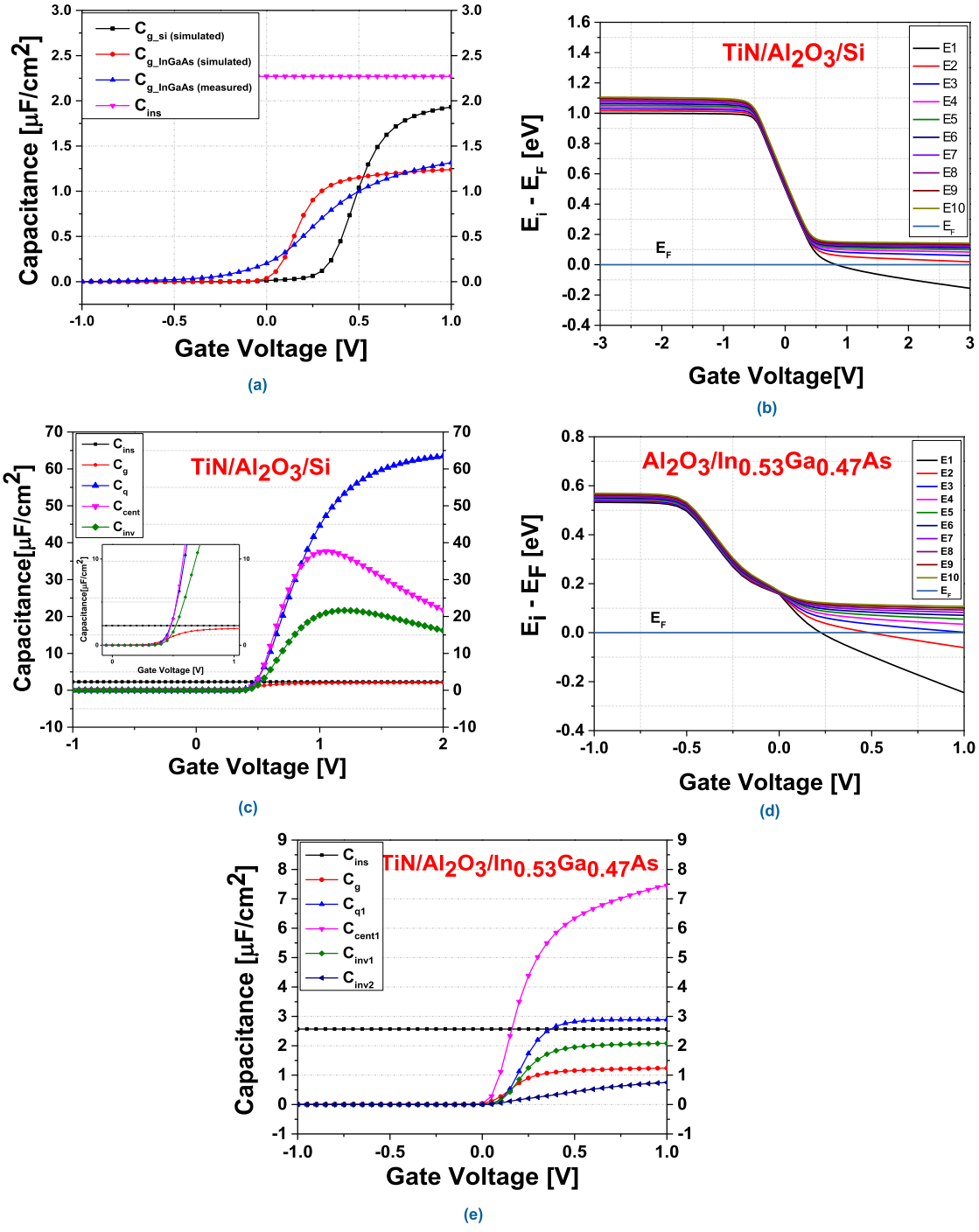

FIGURE 4. (a) Comparison of C-V characteristics between Al_2O_3/Si and $Al_2O_3/In_{0.53}Ga_{0.47}As$ structures. (b) Sub-band energy levels with respect to the Fermi level of Al_2O_3/Si structure. (c) Inversion-layer capacitances of Al_2O_3/Si structure. (d) Sub-band energy levels with respect to the Fermi level of $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure. (e) Inversion-layer capacitances of $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure.

the contour mapping of the normalized parallel conductance ($G_p/A\omega q$) as a function of applied gate biasing voltage and measured frequency. The white dashed lines show the movement of the parallel conductance peak $(G_p/\omega)_{max}$, which indicates the band bending efficiency and the degree of Fermi level pinning [24], [51], [52]. The steeper nature of the slope indicates less Fermi level pinning and efficient band bending. Figure 5b illustrates the interface trap states of a high-k/III-V device interface with respect to trap energy level. To allocate D_{it} band energy positions, we determined E_T from Eq. 7. It was calculated from the corresponding frequency of $(G_p/\omega)_{max}$. Average thermal velocity v_{th} and effective

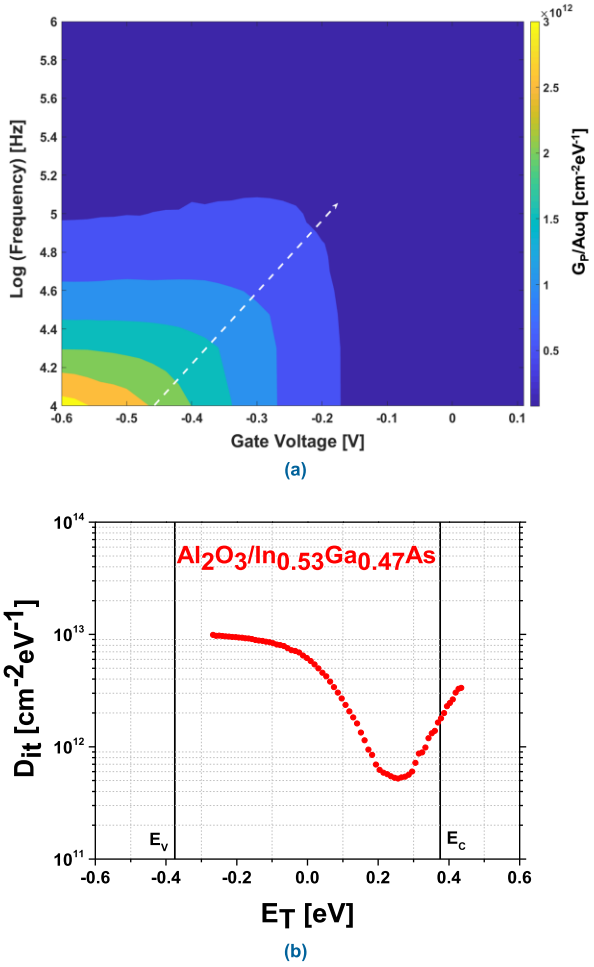

FIGURE 5. (a) Contour mapping of normalized parallel conductance ($G_P/A\omega q$) as a function of applied gate biasing voltage and frequency. (b) Interface trap distribution as a function of trap energy (E_T).

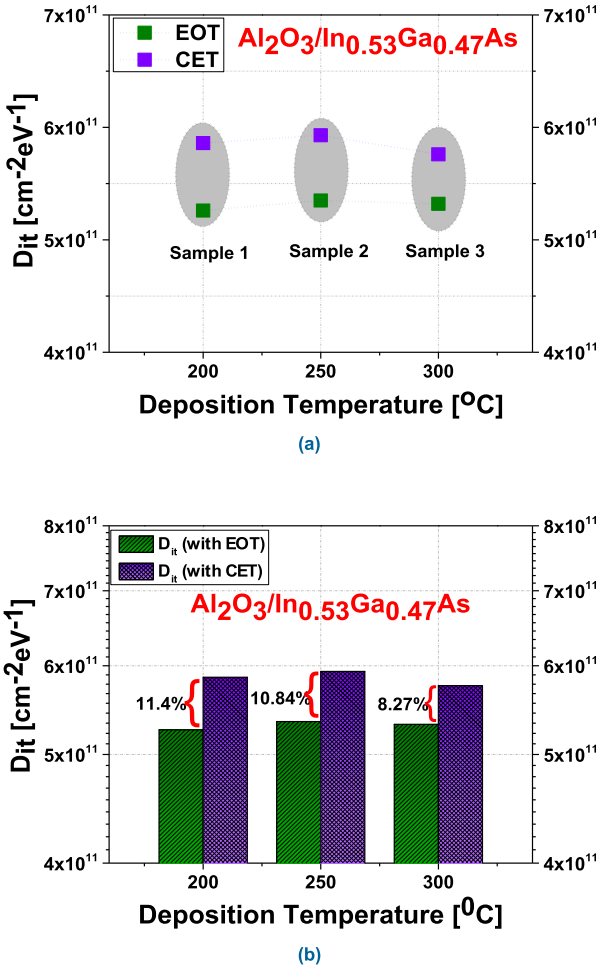

FIGURE 6. (a) Extracted interface trap density (D_{it}) between different ALD deposition temperatures. (b) Comparison between EOT and CET extracted values of interface trap density (D_{it}).

density of states D_{dos} of n-type $In_{0.53}Ga_{0.47}As$ at room temperature (300K) was considered to be $5.6 \times 10^7 cms^{-1}$ and $2.2 \times 10^{17} cm^{-3}$ respectively from literature [48]. Though the value of capture cross section of $In_{0.53}Ga_{0.47}As$ is still a matter of ongoing research, some reported values are between 7×10^{-15} and 5×10^{-17} cm^2 from deep level transient spectroscopy measurement [53]–[56]. As error in σ does not inflict any major impact on E_T, here we assumed it to be 1×10^{-16} cm^2 which is also in range from the reported values [24]. From literature it is evident that at room temperature E_T can vary up to 60 meV per decade change of σ which is very much insignificant [2]. D_{it} values appears to be high near the valance band (E_V) edge compared to the conduction band (E_C) edge. A similar drop of D_{it} values for high-k/III-V devices near the conduction band (E_C) edge using conductance method was also reported in the literature [44], [57]. Figure 6(a, b) shows the extracted values of interface trap densities (D_{it}). Using EOT, D_{it} values of 200°C, 250°C and 300°C deposited samples were $5.26 \times 10^{11} cm^{-2}eV^{-1}$, 5.35×10^{11} $cm^{-2}eV^{-1}$ and 5.32×10^{11} $cm^{-2}eV^{-1}$, respectively. To demonstrate the effects of quantum mechanical effects, we used CET instead of EOT to extract D_{it} and the other parameters were unchanged. In this case, D_{it} values of 200°C, 250°C and 300°C deposited samples were 5.86×10^{11} $cm^{-2}eV^{-1}$, 5.93×10^{11} $cm^{-2}eV^{-1}$ and 5.76×10^{11} $cm^{-2}eV^{-1}$, respectively. D_{it} values extracted using CET were found to be higher (∼10%) than the values extracted using EOT, which came from quantum mechanical confinement.

To extract density of border traps (N_{bt}), we calculated the parameters in Table 1. We considered the effective mass of Al_2O_3 to be 0.23 m_0 (m_0 is the electron mass at rest) to calculate the attenuation coefficient [58]. We used Nextnano simulation tool to calculate semiconductor capacitance C_s at 1 V (Border trap extraction voltage) by solving the one dimensional Poisson-Schrodinger equation considering quantum confinement [49]. We used Eq. 16 to generate the best fitting curve with the measured capacitances at 1 V, where N_{bt} and τ_0 were used as variable fitting parameters. Figure 7(a, b) shows border trap (N_{bt}) extraction fitting

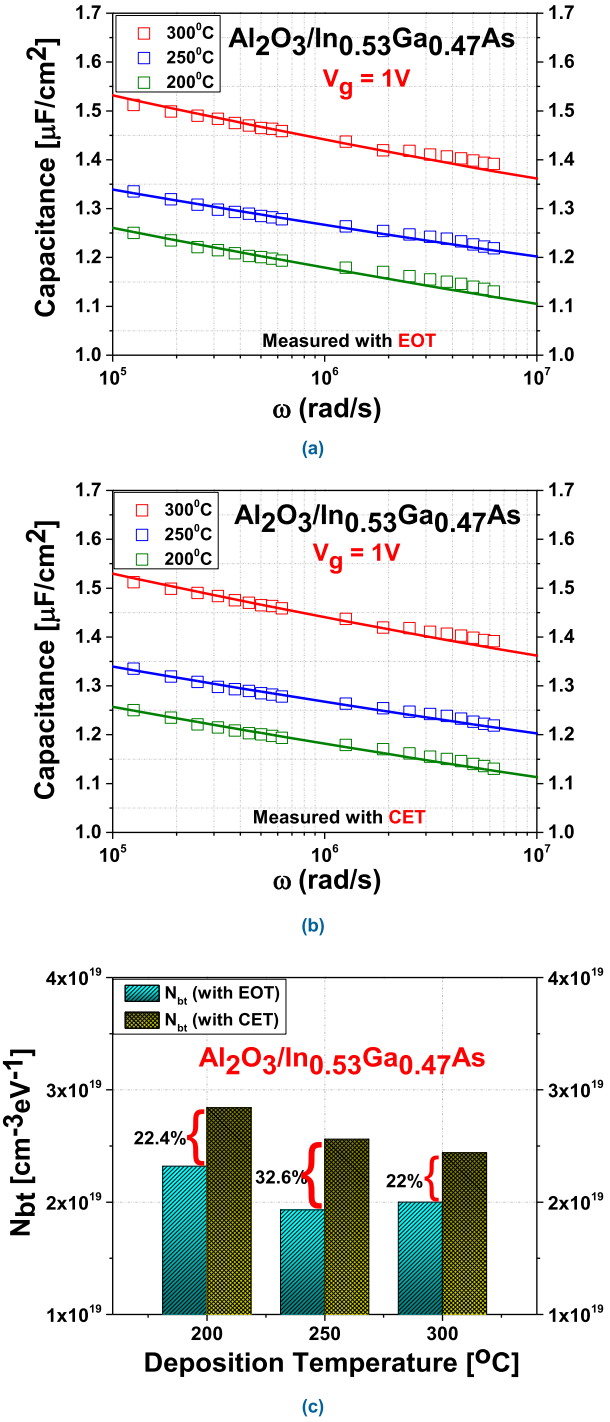

FIGURE 7. (a) Fitting curves for measured accumulation capacitances at 1 V gate voltage from the distributed border trap model using EOT and (b) CET. (c) Comparison between EOT and CET extracted values of border traps (N_{bt}).

curves using EOT and CET, respectively. Squares represents the measured capacitance values from different frequencies (10 KHz-1 MHz) at 1 V and the straight lines are fitting curves. Figure 7c shows the difference between the extracted N_{bt} values of different samples. Using EOT, the border trap (N_{bt}) values of 200°C, 250°C and 300°C deposited samples

TABLE 1. Parameters for the extraction process and extracted D_{it} and N_{bt} values.

Sample	$Al_2O_3/In_{0.53}Ga_{0.47}As$		
Parameters	200°C	250°C	300°C
t_{ox} [nm]	4.2006	3.867	3.5128
EOT [nm]	2.27	2.09	1.9
CET [nm]	2.89	2.7	2.36
ε_{ox}	7.19	7.19	7.19
m* [m_0] (Al_2O_3)	0.23	0.23	0.23
E_b [eV]	3.6	3.6	3.6
K [nm^{-1}]	4.5	4.5	4.5
C_S [$\mu f/cm^{-2}$]	1.1	1.14	1.2
τ_0 [s] (using EOT)	1×10^{-12}	1×10^{-12}	1×10^{-13}
τ_0 [s] (using CET)	1×10^{-12}	1×10^{-12}	1×10^{-13}
D_{it} [$cm^{-2}eV^{-1}$] (Using EOT)	5.26×10^{11}	5.35×10^{11}	5.32×10^{11}
D_{it} [$cm^{-2}eV^{-1}$] (Using CET)	5.86×10^{11}	5.93×10^{11}	5.76×10^{11}
N_{bt} [$cm^{-3}eV^{-1}$] (Using EOT)	2.32×10^{19}	1.93×10^{19}	2×10^{19}
N_{bt} [$cm^{-3}eV^{-1}$] (Using CET)	2.84×10^{19}	2.56×10^{19}	2.44×10^{19}

were $2.32 \times 10^{19} cm^{-3}eV^{-1}$, 1.93×10^{19} $cm^{-3}eV^{-1}$ and 2×10^{19} $cm^{-3}eV^{-1}$, respectively. In this case, the values of τ_0 were between $1 \times 10^{-13} \sim 1 \times 10^{-12}$. To consider the quantum mechanical effect, we used CET instead of EOT to extract N_{bt} without changing any other parameters except N_{bt} and τ_0, which were used as variable fitting parameters like before. In this case, the extracted N_{bt} values were $2.84 \times 10^{19} cm^{-3}eV^{-1}$, 2.56×10^{19} $cm^{-3}eV^{-1}$ and 2.44×10^{19} $cm^{-3}eV^{-1}$ for 200°C, 250°C and 300°C deposited samples, respectively, which are also higher (~25%) than the EOT extracted values like D_{it}. In this case, the values of τ_0 were also between 1×10^{-13}– 1×10^{-12}.

V. CONCLUSION

In this study, we attempted to show the impact of quantum mechanical confinement on interface trap density (D_{it}) as well as border traps (N_{bt}) for scaled down III-V metal oxide semiconductor devices. To show that the quantum confinement is more dominant in small scaled III-V devices, we made a comparison between Al_2O_3/Si and $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure using the Nextnano simulation tool. From the simulation, we found that inversion-layer capacitance is much larger compared to insulator capacitance in Si structure, thus having no or very low impact on total gate capacitance. On the contrary, the inversion-layer capacitance in $In_{0.53}Ga_{0.47}As$ structure was comparable to insulator capacitance and lowered the total gate capacitance. We made $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors with different oxide deposition temperatures on top of a 300-mm Si substrate. All devices went through a rapid thermal annealing (RTA)

process. We measured interface trap density (D_{it}) and border trap (N_{bt}) using both EOT and CET. The extracted D_{it} and N_{bt} values using CET were almost 10% and 25% higher than the values extracted using EOT, respectively. This underestimation of D_{it} as well as N_{bt} values using EOT is caused by the fact that additional inversion layer thickness due to quantum mechanical effect in the $In_{0.53}Ga_{0.47}As$ channel layer was not considered. For the additional thickness, the oxide-semiconductor interface is shifted more towards the channel and there may be some additional interface trap that could add to energy loss.

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