Stability Analysis and Efficiency Optimization of an Inductive Power Transfer System With a Constant Power Load

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ABSTRACT Series-series compensated inductive power transfer (SSIPT) systems have been widely studied and characterized for constant resistance loads (CRLs) and constant voltage loads (CVLs), but much less so for constant power loads (CPLs), although CPLs have numerous applications. In this work, we address some of the fundamental knowledge gaps for SSIPT/CPL systems that we believe have not been fully explored in the literature. First, we apply Middlebrook's stability criterion to derive a closed-form impedance-based stability condition for SSIPT/CPL systems. The derivation of the equilibrium solution is based on small-signal analysis and we show its consistency with intuitive results from perturbation-based arguments. Second, we show that the power transfer efficiency is minimum at the resonant frequency of the primary resonator. Third, the stability criterion is used to develop a straightforward approach for finding the operating frequency and input voltage that achieves near-maximum power transfer efficiency. This solution is useful as a starting point for a more meticulous parameter sweep to find the optimum input voltage and frequency values. Our analytical results are validated by performing frequency sweep measurements with two SSIPT experimental setups – one tuned to 165 kHz and the other to 6.78 MHz. We also provide an intuitive description and comparison of voltage-driven and current-driven CPLs. This topic is rarely treated in an intuitive manner and largely ignored, but we believe a solid conceptual understanding of voltage-driven and current-driven CPLs is beneficial for designers.
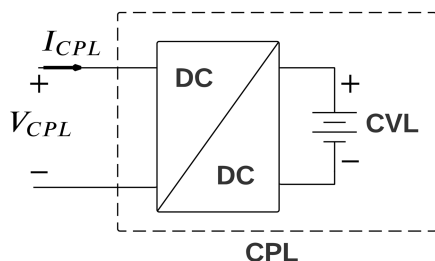
INDEX TERMS Constant power load (CPL), constant resistance load (CRL), power transfer, resonance, series-series compensated inductive power transfer (SSIPT).

I. INTRODUCTION

Inductive power transfer (IPT) systems have rapidly gained popularity as an efficient and practical means for wirelessly transferring power by magnetic induction over short distances. In the literature, IPT systems are routinely considered with constant resistance loads (CRLs) and constant voltage loads (CVLs), while constant power loads (CPLs) receive much less attention. Nevertheless, CPLs are important as they model the behavior of tightly regulated power converters and motor drives which are deployed in a number of applications like automotive systems [1]–[3], aircraft [4], [5],

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ships [6], [7], and microgrids [8]–[13]. In the area of DC distributed power systems, CPLs have traditionally been investigated for networks of classic switch-mode converters like buck, boost, and buck-boost converters [4], [8], [14]–[18]. In comparison, there have been significantly fewer detailed studies of IPT systems with CPLs. This work addresses some knowledge gaps for CPL-loaded IPT systems that we believe are fundamentally important but not yet sufficiently addressed. In particular, our study is focused on the stability and power transfer efficiency of series-series compensated IPT (SSIPT) systems. This SSIPT topology was chosen because of its popularity, simplicity, capability for high power transfer efficiency, load-independent output current, and k-independent tuning [19].

FIGURE 1. A DC-to-DC converter that maintains a tightly regulated current through a CVL behaves as a CPL.

A CPL maintains to consume a constant amount of power, i.e., the input and the output power remains always constant. Therefore, a CPL has negative incremental impedance, although the instantaneous impedance is positive. As mentioned above, tightly regulated DC-to-DC converters exhibit CPL behavior. As an example, Fig. 1 shows a block diagram of a DC-to-DC converter that maintains a tightly regulated current through a CVL. This may model, for example, a battery management system during a phase of the charging cycle. For simplicity, if we assume the DC-to-DC converter is lossless then the input power equals the output power delivered to the CVL. Let, V_{CPL}, I_{CPL}, and P_{CPL} represent the input voltage, current, and power, respectively. If the input voltage V_{CPL} is increased then the input current I_{CPL} must decrease in order to maintain the product $P_{CPL} = V_{CPL}I_{CPL}$ for a fixed output power (and vice versa). This means the CPL has a negative incremental resistance. In contrast, for ordinary CRLs if we increase the input voltage then the input current also increases.

From a design standpoint, CPLs are challenging because they have negative incremental resistances which can cause system instability. For analyzing stability of cascaded power electronic systems, it has proven effective to use the minor loop gain, which is the ratio of the source to load impedances at an interface between two converters. Middlebrook showed the minor loop gain plays an equivalent role in the stability analysis of cascaded power converters as the ordinary loop gain for feedback systems [20]. A necessary and sufficient condition for stability is that the minor loop gain satisfies the Nyquist stability criterion. This has been used to derive various impedance-based stability conditions [14], [20]–[24], each offering a unique balance between simplicity and conservatism of stability criteria. Originally, the minor loop gain was developed for voltage-source systems. Later the formation of the minor loop gain was generalized to handle current-source systems [25]–[27], and distributed power systems with arbitrary subsystems [28], [29]. Along with assessing stability, there are a number of techniques to improve stability which are reviewed and summarized in detail in [14].

As the large number of articles and attention on the topic indicates, stability of power systems is a critically important topic. However, the stability of IPT systems with CPLs is not fully explored. Particularly, we have not seen a rigorous derivation of an impedance-based stability criterion for

SSIPT/CPL systems. In previous works in this area, the equilibrium solution was reasoned using perturbation arguments applied to the power transfer curve [26], [30]. While intuitive, such arguments lack the rigor of a more formal stability analysis. In other works on IPTs, steady-state analytical solutions have been asserted and verified without a stability analysis (e.g., see [31]). Given the importance of stability and the rising adoption of IPT technology, in this work we firmly establish a closed-form stability criterion for the SSIPT/CPL system based on a rigorous small-signal stability analysis (Middlebrook's approach). Our stability analysis assumes a voltage-driven CPL. We suspect that a number of researchers focused on IPT system design may not be familiar with voltage-driven CPLs and current-driven CPLs. Therefore, in this work we also present an intuitive and simple description of these models.

Along with stability, the power transfer efficiency η is a key figure of merit for IPT systems. It is well-known that for ordinary CRLs, the efficiency η can be maximized at the resonant frequency for a tuned IPT system, provided the optimal choice of load impedance. On the contrary, it has been recently reported that η is poor for a tuned SSIPT/CPL operating on-resonance in stable equilibrium [30], [31]. However, to the best of the authors' knowledge, it has not been proven that the efficiency is minimum at resonance. We therefore prove here that the power transfer efficiency is indeed minimum at the resonant frequency of the primary series LC resonator for a SSIPT/CPL system.

A key question is: how does one increase η of a SSIPT/CPL system if η is minimum at resonance? Zhang *et al.* showed that η can be increased by operating off-resonance [31], and derived design equations for maximizing η for a given input voltage. While useful if the input voltage is fixed, these design equations do not yield the maximum possible efficiency. This leaves the need to perform a two-dimensional parameter sweep to find the optimal input voltage and optimal operating frequency to fully maximize efficiency. However, parameter searches can be computationally expensive, slow, and unintuitive. To address this, we present here analytical expressions for finding a near-optimal starting point to dramatically speed up the parameter search. Our method uses the impedance-based stability criterion and the known equation for the optimal load impedance.

The summary of the contributions of this article with some remarks regarding our motivation and novelty is presented below:

1) We firmly establish a closed-form stability criterion for the SSIPT/CPL system based on a rigorous small-signal stability analysis (Section II). This stability analysis has not been published before and provides a more formal and rigorous treatment of the subject compared to previous perturbation-based arguments [26], [30]. We were motivated to undertake this stability analysis because it was not clear the validity
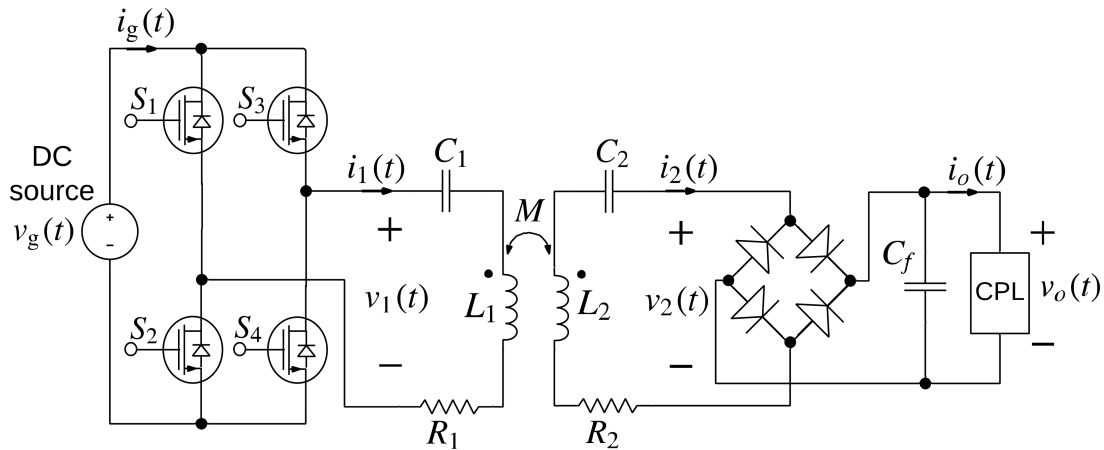
FIGURE 2. Schematic diagram of a SSIPT system driven by a DC voltage source and terminated in a CPL.

and assumptions made in the simple perturbation-based treatments.

2) We show that the efficiency of a SSIPT/CPL system is minimum at the resonant frequency of the primary resonator (Section III. A). This result is a defining feature of SSIPT/CPL systems, but it has not been explicitly stated or emphasized before in other works. This result is important because it may conflict with expectations gained from the widespread use of tuned SSIPT systems with ordinary CRLs and CVLs in which the maximum possible efficiency is achieved by operating at resonance with an optimum load impedance. In contrast, for tuned SSIPT/CPL systems, the efficiency is minimum at resonance and the designer must select a different operating frequency to improve efficiency.

3) We present a novel method for finding the optimal combination of operating frequency and input voltage to maximize the power transfer efficiency for a given set of SSIPT/CPL system parameters (Section III. B). The closest related works are [31] and [38]. In [31] the optimal operating frequency is found that maximizes efficiency for a given input voltage. Conversely, in [38] the optimal input voltage is found that maximizes efficiency for a given operating frequency. The limitation of both approaches is that they do not yield the maximum possible efficiency. In other words, they do not optimize both the input voltage and operating frequency, simultaneously. A two-dimensional parameter sweep over input voltage and operating frequency is therefore needed to find the optimal combination. Our method speeds up the search by providing a simple and intuitive analytical method for finding the near-optimal combination of operating frequency and input voltage.

II. IMPEDANCE STABILITY CRITERION FOR A SSIPT SYSTEM TERMINATED IN A CPL

Our focus is on achieving high efficiency for an IPT system that is stationary (i.e., the coil-to-coil orientation and
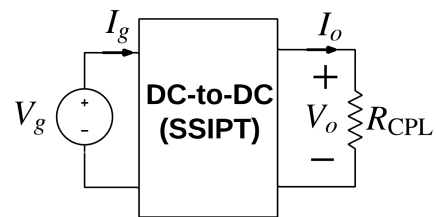

FIGURE 3. Simplified block diagram of the SSIPT system shown in Fig. 2 at steady state with the DC terminal voltages and currents shown.

distance are fixed) with a known, fixed output power in stable equilibrium. An example of a stationary application is an inductive charging system with magnetic alignment and attachment. An example of a fixed-power CPL model is a battery management system that maintains constant current through a battery during a phase of the charging cycle. Fig. 1 shows a schematic diagram of a SSIPT system terminated in a CPL. The system includes a power inverter, coupled resonant network, and rectifier. The primary (secondary) series resonator is composed of capacitor C_1(C_2), inductor L_1(L_2), and series resistor R_1(R_2). The mutual inductance between inductors L_1 and L_2 is $M = k\sqrt{L_1 L_2}$, where k is the coupling coefficient. The output of the rectifier connects to a low pass filter capacitor C_f in parallel with the CPL. Unless otherwise stated, this article assumes ideal lossless switches and diodes and ignores inverter switching losses. We assume no feedback or communication between the primary and secondary sides.

A. STEADY-STATE EQUIVALENT CIRCUIT MODEL

At steady state the terminal signals of the SSIPT system shown in Fig. 2 do not vary with time, i.e., $v_g(t) = V_g$, $v_o(t) = V_o$, $i_g(t) = I_g$, and $i_o(t) = I_o$. Under this condition, the CPL consumes constant load power $P_o = V_o I_o$ and has input resistance $R_{CPL} = V_o / I_o$. Fig. 3 presents a simplified block diagram of the system at steady state.

At steady state the coupled resonator section between the output of the inverter and input of the rectifier can be modeled
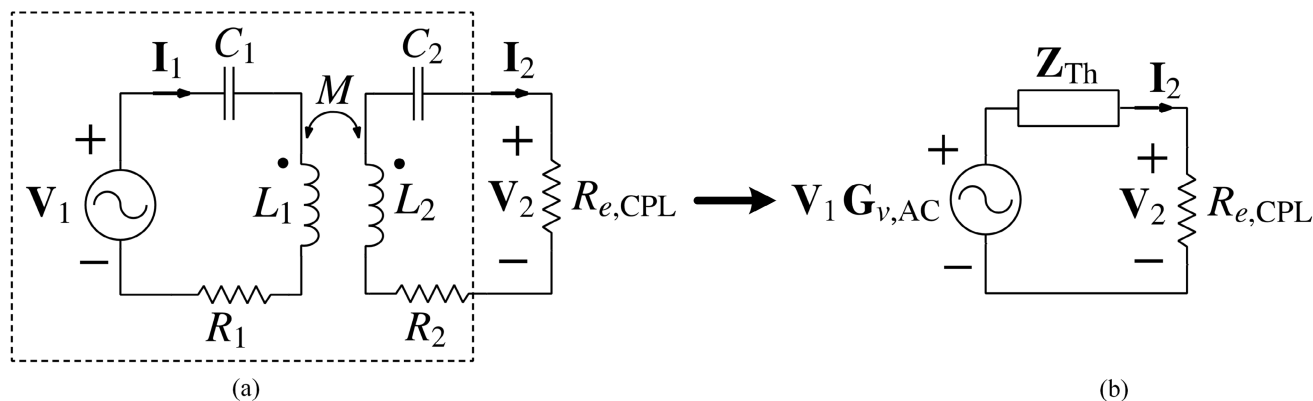
FIGURE 4. (a) AC equivalent circuit of the resonant section at steady state and (b) its corresponding AC Thevenin equivalent circuit connected to the equivalent load.

by the AC equivalent circuit shown in Fig. 4. Here we employ the sinusoidal approximation in which higher-order harmonics of the switching frequency are ignored, and the waveforms are assumed to be purely sinusoidal. Bold capital letters represent phasor quantities of the corresponding first-harmonic sinusoidal waveforms, e.g., $\mathbf{I}_1$ is the phasor representation of $i_1(t)$. The terminal AC voltages $\mathbf{V}_1$ and $\mathbf{V}_2$ relate to the terminal DC voltages V_g and V_0 as follows [32], [33]:

$$|\mathbf{V}_1| = V_g \frac{\sin(\pi D) 2c_{12}}{\pi}, \tag{1}$$

$$|\mathbf{V}_2| = V_o \frac{2d_{12}}{\pi}, \tag{2}$$

where D is the inverter's duty cycle $0 \leq D \leq 1$; coefficient $c_{12} = 1$ for a half-bridge inverter and 2 for a full-bridge inverter; and coefficient $d_{12} = 1$ for a half-bridge rectifier and 2 for a full-bridge rectifier. The terminal AC current $\mathbf{I}_2$ is related to the terminal DC current Io by:

$$|\mathbf{I}_2| = I_o \frac{\pi}{d_{12}}. \tag{3}$$

Additionally, $\mathbf{V}_2$ and $\mathbf{I}_2$ are in phase and their ratio is the effective AC CPL input resistance:

$$R_{e,CPL} = \frac{\mathbf{V}_2}{\mathbf{I}_2} = R_{CPL} \frac{2d_{12}^2}{\pi^2}. \tag{4}$$

The output impedance $\mathbf{Z}_{th}$ and open-circuit voltage gain $\mathbf{G}_{v,AC}$ of the AC Thevenin equivalent circuit shown in Fig. 4 can be obtained using ordinary AC circuit analysis, yielding the following expressions:

$$\mathbf{Z}_{th} = \left(R_2 + \frac{(\omega M)^2 R_1}{R_1^2 + X_1^2} \right) + j \left(X_2 - \frac{(\omega M)^2 X_1}{R_1^2 + X_1^2} \right), \tag{5}$$

$$\mathbf{G}_{v,AC} = \left(\frac{\omega M X_1}{R_1^2 + X_1^2} \right) + j \left(\frac{\omega M R_1}{R_1^2 + X_1^2} \right), \tag{6}$$

where ω is the switching frequency of the inverter, and $X_1 = \omega L_1 - 1/(\omega C_1)$ and $X_2 = \omega L_2 - 1/(\omega C_2)$ are the primary and secondary reactances, respectively. Since the rectifier is

assumed lossless, the output power P_o delivered to R_{CPL} is equal to the real power consumed by the effective AC load $R_{e,CPL}$. Therefore, the AC Thevenin equivalent circuit shown in Fig. 4 can be used to express output power P_0 consumed by the CPL in terms of $R_{e,CPL}$, V_1, $\mathbf{G}_{v,AC}$, and $\mathbf{Z}_{th}$:

$$P_o = \frac{R_{e,CPL} |\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{2|\mathbf{Z}_{th} + R_{e,CPL}|^2}. \tag{7}$$

According to the maximum power theorem, the AC circuit in Fig. 4 should be terminated in a load impedance that is conjugately matched to $\mathbf{Z}_{th}$ to obtain the maximum available power from the source P_{max}. However, in our AC circuit the CPL's effective AC resistance $R_{e,CPL}$ is real (no imaginary component). Under this constraint, maximum power transfer occurs for $R_{e,CPL} = |\mathbf{Z}_{th}|$ and P_{max} can be found by substituting $R_{e,CPL} = |\mathbf{Z}_{th}|$ into (7), yielding (after some algebraic simplifications):

$$P_{max} = \frac{|\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{4(|\mathbf{Z}_{th} + Re[\mathbf{Z}_{th}])}. \tag{8}$$

B. OUTPUT STEADY-STATE POWER CURVE
We do not have direct control of the CPL's input impedance R_{CPL}; instead, the CPL effectively regulates a constant power sink $P_o = V_o I_o$ by adjusting R_{CPL}. Assuming all other circuit parameters are fixed, the value of R_{CPL} sets the output power. Recall that the CPL's input resistance R_{CPL} is related to its effective AC input resistance $R_{e,CPL}$ by (4). If the CPL is programmed to sink output power $P_0 < P_{max}$, then we find that there are two possible values of $R_{e,CPL}$ that yield the same power P_0 at steady state. To find these values we rearrange terms in (7) to yield a quadratic equation in $R_{e,CPL}$ and solve for the roots, which we denote $R_{e,CPL,1}$ and $R_{e,CPL,2}$:

$$R_{e,CPL,1} = \left(\frac{|\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{4P_o} - Re[\mathbf{Z}_{th}] \right)$$

$$- \sqrt{\left(\frac{|\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{4P_o} - Re[\mathbf{Z}_{th}] \right)^2 - |\mathbf{Z}_{th}|^2}, \tag{9}$$

FIGURE 5. Normalized power transfer characteristic.

$$R_{e,CPL,2} = \left(\frac{|\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{4P_o} - Re[\mathbf{Z}_{th}] \right)$$
$$+ \sqrt{\left(\frac{|\mathbf{V}_1 \mathbf{G}_{v,AC}|^2}{4P_o} - Re[\mathbf{Z}_{th}] \right)^2 - |\mathbf{Z}_{th}|^2}. \quad (10)$$
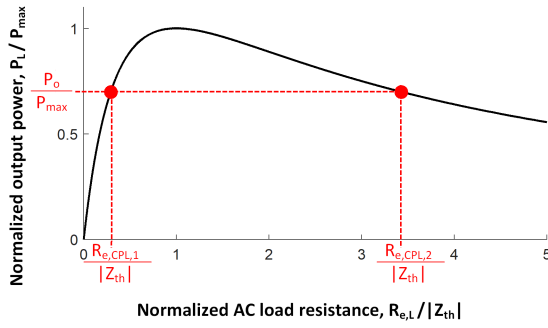
Fig. 5 shows a normalized power transfer characteristic curve generated by loading the AC Thevenin equivalent circuit in Fig. 4 with a variable AC load $R_{e,L}$, sweeping the load from $R_{e,L} = 0$ to $R_{e,L} = 5|\mathbf{Z}_{th}|$, and plotting the normalized load power P_L/P_{max}. As expected, the peak of the power curve P_{max} occurs for the load $R_{e,CPL} = |\mathbf{Z}_{th}|$. If the system is loaded with a CPL programmed to sink output power $P_0 < P_{max}$, then Fig. 5 confirms that there two solutions for the effective AC CPL input resistance, which we recognize as $R_{e,CPL,1}$ and $R_{e,CPL,2}$ given by (9, 10). Our first goal is to prove that the solution with the positive root $R_{e,CPL,2}$ is the stable equilibrium solution.

C. SMALL-SIGNAL TRANSFER FUNCTION
Here we use small-signal analysis to investigate the stability of the SSIPT system in Fig. 2. This is achieved by driving the system with a time-varying input voltage $v_g(t)$ in which the average of $v_g(t)$ is equal to a positive DC (quiescent) value V_g plus a superimposed small-signal AC variation $\widehat{v_g}(t)$:

$$\langle v_g(t) \rangle_{T_S} = \frac{1}{T_S} \int_{t-T_S/2}^{t+T_S/2} v_g(t) \, dt = V_g + \widehat{v_g}(t), \quad (11)$$

where $\langle v_g(t) \rangle_{T_s}$ denotes the average of $v_g(t)$ over the switching frequency T_s. In our notation, capital letters X denote DC steady-state values and lower-case terms $\widehat{x}(t)$ represent small-signal AC variations.

Fig. 6 presents a simplified block diagram of the SSIPT system showing the terminal signals decomposed into their steady-state DC and small-signal AC components. If we assume the system can be linearized at the quiescent operating point, then the system dynamics are characterized by the small-signal AC Thevenin equivalent circuit shown in Fig. 6, where $\widehat{v_g}(s)$, $\widehat{v_o}(s)$, and $\widehat{i_o}(s)$ are the Laplace transforms of $\widehat{v_g}(t)$, $\widehat{v_o}(t)$, and $\widehat{i_o}(t)$, respectively; $G_v(s)$ and $Z_g(s)$ are the system's small-signal open circuit voltage transfer function and source impedance, respectively; and $Z_{CPL}(s)$ is the CPL's small-signal input impedance. To assess stability, we consider
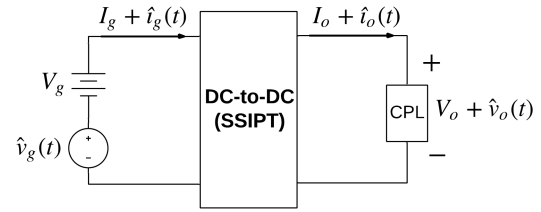

FIGURE 6. Simplified block diagram of the SSIPT system showing the terminal signals decomposed into their steady-state DC and small-signal AC components.
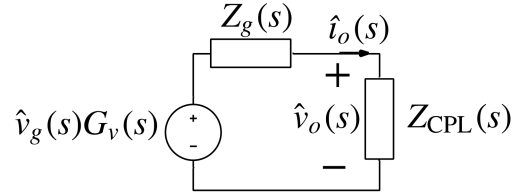

FIGURE 7. Small-signal AC Thevenin equivalent circuit in the s-domain.

the transfer function of the small-signal AC Thevenin equivalent circuit in Fig. 7, represented as $\widehat{i}_o(s)/(\widehat{v}_g(s)G_v(s))$:

$$\frac{\widehat{i_o}(s)}{\widehat{v_g}(s)G_v(s)} = \frac{1}{Z_g(s) + Z_{CPL}(s)}$$
$$= \left(\frac{1}{Z_{CPL}(s)} \right) \left(\frac{1}{1 + Z_g(s)/Z_{CPL}(s)} \right)$$
$$= \left(\frac{1}{Z_g(s)} \right) \left(\frac{1}{1 + Z_{CPL}(s)/Z_g(s)} \right). \quad (12)$$

The reason for expressing the transfer function $\widehat{i}_o(s)/(\widehat{v}_g(s)G_v(s))$ in three equivalent forms (12) is to highlight that one form may be more convenient to use over the others for stability analysis and that we are free to choose which form to use. Stability is clearly dependent on the pole and zero locations of $Z_g(s)$ and $Z_{CPL}(s)$. In the following sections we examine the properties of $Z_g(s)$ and $Z_{CPL}(s)$ individually, and then use this information along with (12) to develop our impedance-based stability criterion.

D. PROPERTIES OF THE SMALL-SIGNAL SOURCE IMPEDANCE
The small-signal source impedance $Z_g(s)$ characterizes the impedance of the SSIPT system. In general, the source impedance $Z_g(s)$ of a stable source converter has no RHP poles (called "open-circuit stable") and no RHP zeros (called "short-circuit stable") [34]. Since the SSIPT system shown in Fig. 2 is powered directly by the DC input voltage $v_g(t)$, operates in open loop without feedback, and contains only passive components and switching elements, we assume the SSIPT system is stable under all passive loading conditions (including open and short loads). We conclude $Z_g(s)$ has no RHP poles nor RHP zeros. Next, we evaluate the small-signal source impedance $Z_g(s)$ at the limits $s = 0$ and $s = \infty$. At $s = 0$ we have the following result (proven in the
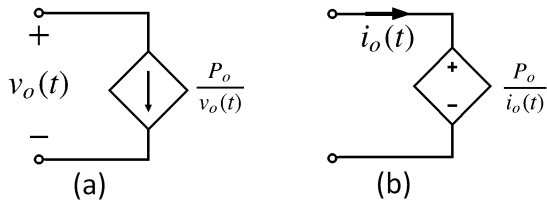
FIGURE 8. Ideal instantaneous CPL models implemented with a (a) VCCS and (b) CCVS.

FIGURE 9. Bandwidth-limited CPL models implemented with a modified (a) VCCS and (b) CCVS.

Appendix):

$$Z_g(0) = \left(\frac{\pi^2}{2d_{12}^2}\right)\left(\frac{|\mathbf{Z}_{th}|^2 + Re[\mathbf{Z}_{th}]R_{e,CPL}}{R_{e,CPL} + Re[\mathbf{Z}_{th}]}\right). \quad (13)$$

As $s \to \infty$ the large lowpass filter capacitor C_f (see Fig. 2) shorts out the circuit elements proceeding it; therefore,

$$\lim_{s \to \infty} Z_g(s) = 0. \quad (14)$$

In this work we assume that C_f is sufficiently large such that the magnitude $|Z_g(s)|$ decreases rapidly as s is increased from DC such that $max|Z_g(s)| = |Z_g(0)|$.

E. CPL MODEL

At DC steady state, the CPL consumes power $P_o = V_oI_o$ and has an input resistance $R_{CPL} = V_o/I_o$. Fig. 8 presents two ideal CPL models, one implemented with a voltage-controlled current source (VCCS) and the other with a current-controlled voltage source (CCVS), both of which react instantaneously to signal changes. The small-signal impedance of each model can be derived by linearizing about the DC (quiescent) operating point. The result is that both ideal CPLs exhibit the same negative small-signal resistance $Z_{CPL}(s) = -R_{CPL}$, where R_{CPL} is the large-signal DC resistance. This negative impedance characteristic is a well-known result used in numerous stability studies (e.g., see [4], [8], [15], [35]).

Despite the fact that the ideal VCCS and CCVS CPLs in Fig. 8 have the same small-signal impedance $Z_{CPL}(s) = -R_{CPL}$, we see that there is a clear difference between the two models. Namely, the VCCS CPL is not compatible with independent current-source inputs, while the CCVS CPL is not compatible with independent voltage-source inputs. This difference is not modeled in their small-signal impedances, which suggests that the ideal models in Fig. 8 are incapable of being realized with physical circuitry. Realistic CPLs, such as tightly regulated DC-to-DC converters, exhibit dynamic behavior and behave as CPLs only within the bandwidths of the converters' feedback loops [7], [36]. Even SPICE is not able to simulate the ideal CPL's instantaneous behavior, since the program's iterative algorithm includes a numerical delay of at least one time-step between input signal variations and output responses produced by the dependent sources. Therefore, to make the CPL models more realistic for our small-signal stability analysis, we shall slow their response times. The modified CPL models are shown in Fig. 9, where
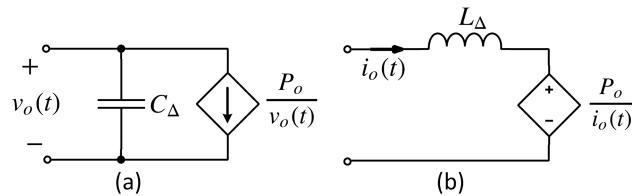
the equivalent circuit parameters $C_\triangle$ and $L_\triangle$ limit the bandwidth of the respective models to be consistent with a realistic controller design. The modified VCCS CPL in Fig. 9 (a) has small-signal impedance:

$$Z_{CPL}(s) = \frac{1/C_\triangle}{s - 1/(C_\triangle R_{CPL})}, \quad (15)$$

which has a RHP pole at $1/(C_\triangle R_{CPL})$. The modified CCVS CPL in Fig. 9 (b) has small-signal impedance:

$$Z_{CPL}(s) = L_\triangle\left(s - \frac{R_{CPL}}{L_\triangle}\right), \quad (16)$$

which has a RHP zero at $R_{CPL}/L_\triangle$. Because the small-signal impedance expressed in (15) for the VCCS CPL has a RHP pole, the CPL is stable when connected to an independent voltage source and unstable when connected to an independent current source. We refer to this type of CPL as "voltage-driven", since voltage changes across the CPL's input terminals drive the load to proportionately adjusts its current draw. Such voltage-driven CPLs are common and well-studied, going back to Middlebrook's original article on the minor loop gain [20]. In contrast, the small-signal impedance expressed in (16) for the CCVS CPL has a RHP zero, which means this "current-driven" CPL is stable when connected to an independent current source and is unstable when connected to an independent voltage source. Conceptually, a CPL is a self-adjusting variable resistor that continuously changes its input resistance to maintain a constant power sink.

With this impedance-based viewpoint, the difference between "voltage-driven" and "current-driven" CPLs relates to the way its input resistance is adjusted in the face of disturbances. Using a discrete-time approximation, we can imagine power transfer change requests are sent to the CPL when mismatches are detected between the target output power and the measured output power. Table 1 presents the reactions of voltage-driven and current-driven CPLs to such requests. A detailed transient analysis depends on the dynamics of the specific CPL implementation which is outside of the scope of this work. As will be shown, the CPL properties that are centrally important to stability include the DC value of the small-signal impedance $Z_{CPL}(0) = -R_{CPL}$ and the existence of RHP poles and RHP zeros of $Z_{CPL}(s)$. While our bandwidth-limited CPL models shown in Fig. 9 are simple, they are sufficiently broad in scope to feature both important properties.

TABLE 1. CPL reactions to power transfer change requests (discrete-time approximation).

Request	Voltage-driven reaction	Current driven reaction
Increase power transfer	Decrease resistance	Increase resistance
Decrease power transfer	Increase resistance	Decrease resistance

F. IMPEDANCE-BASED STABILITY CRITERION

As previously mentioned, the literature on power converter stability commonly assumes voltage-driven CPLs (note that in many articles this assumption is not explicitly stated but implied). Indeed, voltage-driven converters are much more common than current-driven converters, so most actual applications will be better matched to this model. In this work we follow suit and focus solely on SSIPT systems terminated in voltage-driven CPLs to simplify the scope of the analysis. For the remainder of this article, current-driven CPLs are not considered. We model the voltage-driven CPL using the VCCS CPL in Fig. 9 (a), which has a small signal impedance given by (15) with a RHP pole. The source impedance $Z_g(s)$, which characterizes the source impedance of the SSIPT system, has no RHP poles. Both $Z_g(s)$ and $Z_{CPL}(s)$ have no RHP zeros. It follows from the pole and zero placements of $Z_g(s)$ and $Z_{CPL}(s)$ that the minor loop gain $Z_g(s)/Z_{CPL}(s)$ in (12) is stable. We can therefore apply the Bode stability criterion [37] to this minor loop gain to determine the stability of the system as a whole. Note that the minor loop gain $Z_{CPL}(s)/Z_g(s)$ in (12) is unstable; therefore, we cannot directly apply the Bode stability criterion to this gain term. Using (13) and (15) we can express the minor loop gain $Z_g(s)/Z_{CPL}(s)$ in (12) at DC as:

$$\frac{Z_g(0)}{Z_{CPL}(0)} = \frac{-\pi^2(|\mathbf{Z}_{th}|^2 + Re[\mathbf{Z}_{th}]R_{e,CPL})}{2d_{12}^2 R_{CPL}(R_{e,CPL} + Re[\mathbf{Z}_{th}])}. \quad (17)$$

Since $R_{CPL} > 0$, $Re[\mathbf{Z}_{th}] > 0$, $R_{e,CPL} > 0$, and $|\mathbf{Z}_{th}| > 0$, the minor loop gain at DC must be negative; therefore, $Z_g(0)/Z_{CPL}(0) = -|Z_g(0)/Z_{CPL}(0)|$. Given a sufficiently large output capacitance C_f, we assume the amplitude of the minor loop gain decreases rapidly with s such that $max\{|Z_g(s)/Z_{CPL}(s)|\} = |Z_g(0)/Z_{CPL}(0)|$. Hence, to satisfy the Bode stability criterion it is necessary and sufficient that the amplitude of the minor loop gain is less than unity at DC, or

$$1 > \left(\frac{\pi^2}{2d_{12}^2}\right)\left(\frac{1}{R_{CPL}}\right)\left(\frac{|\mathbf{Z}_{th}|^2 + Re[\mathbf{Z}_{th}]R_{e,CPL}}{R_{e,CPL} + Re[\mathbf{Z}_{th}]}\right). \quad (18)$$

Simplifying (18) yields:

$$R_{e,CPL} > |\mathbf{Z}_{th}|, \quad (19)$$

which is our desired impedance-based stability criterion in terms of the AC equivalent circuit impedance. If the CPL's operating power P_0 is less than the maximum available power from the source ($P_0 < P_{max}$), we found that there are two solutions for $R_{e,CPL}$ which are denoted $R_{e,CPL,1}$ and $R_{e,CPL,2}$ in (9). We are now in a position to show that $R_{e,CPL,2}$ is the stable solution. First, it is straightforward to show from (9, 10)

that $R_{e,CPL,2} > |\mathbf{Z}_{th}|$ and $R_{e,CPL,1} < |\mathbf{Z}_{th}|$ (this is illustrated graphically in Fig. 5). Hence, $R_{e,CPL,2}$ satisfies the stability criterion (19) and is therefore the stable equilibrium solution for $R_{e,CPL}$. It is also straightforward to show from (7) that if (19) is satisfied then the following condition holds true:

$$\frac{\partial P_o}{\partial R_{e,CPL}} > 0, \quad (20)$$

which is an alternative form of the stability criterion. Substituting (5) into (19) yields another form of the stability criterion that is directly in terms of the CPL's large-signal DC resistance:

$$R_{CPL} > \frac{\pi^2}{2d_{12}^2}|\mathbf{Z}_{th}|. \quad (21)$$

Substituting (4) into (20) yields:

$$\frac{\partial P_o}{\partial R_{CPL}} > 0. \quad (22)$$

Equations (19)–(22) are four equivalent forms of the impedance stability criterion. They all give the same result that $R_{e,CPL,2}$ given in (10) is the CPL's stable equilibrium resistance for the SSIPT system, assuming a voltage-driven CPL. The form of the stability criterion in (22) matches that published by Narusue *et al.* who considered the special case of a perfectly-tuned resonant SSIPT system terminated in a CPL (see Section II in Ref. [30]). The derivation of Narusue *et al.* is based on reasoning how the rectifier output voltage would react to small disturbances at different operating points for a tuned-system operating at resonance. In contrast, our derivation here is based on classical small-signal analysis and the Bode stability criterion, and valid for both tuned and mistuned systems. We note again that our derivation assumes a voltage-driven CPL. Additional insights into the impedance stability criterion (19) are gained by looking at the system's trajectories of various initial conditions on the normalized power transfer characteristic curve, as shown in Fig. 10. This curve is the same as that shown in Fig. 5 except with the addition of five initial conditions (or states) labeled A, B, C, D and E with arrows that depict the system's trajectories. Each state is quantified by a single independent state variable: the CPL's effective AC input resistance $R_{e,CPL}$. The value of $R_{e,CPL}$ sets the instantaneous output power consumed by the CPL. The arrow directions are found by considering the CPL's response at each state As discussed previously, a CPL can be effectively modeled as a self-adjusting variable resistor that continuously changes its effective AC input resistance $R_{e,CPL}$ in pursuit of sinking a constant target output power P_0. A basic voltage-driven CPL achieves this through a simple algorithm: it decreases $R_{e,CPL}$ if the measured output power P_L is less than the target output power P_0 (i.e., $P_L < P_0$), and increases $R_{e,CPL}$ if the measured output power P_L is greater than the target output power P_0 (i.e., $P_L > P_0$). In sketching the trajectories shown in Fig. 10, we assume the system slowly moves toward equilibrium without overshoot due to the large output capacitor C_f. Note that all arrows in
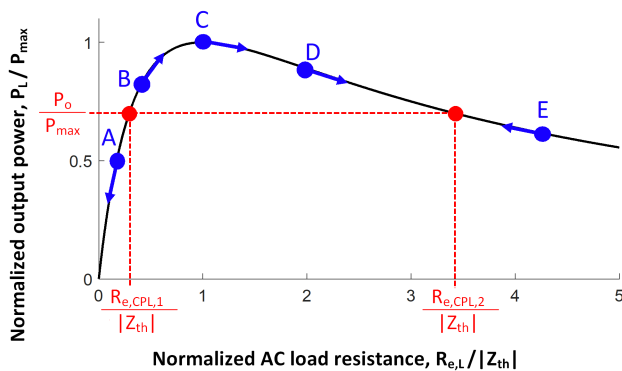
FIGURE 10. Normalized power transfer characteristic with initial condition states and their trajectories.

Fig. 10 diverge away from the state $R_{e,CPL} = R_{e,CPL,1}$ which indicates this is an unstable equilibrium state. On the other hand, $R_{e,CPL,2}$ is an attractor (or sink). Specifically, $R_{e,CPL,2}$ is a locally stable state for initial values of $R_{e,CPL}$ greater than $R_{e,CPL,1}$. Note that $R_{e,CPL}$ approaches zero if the initial value of $R_{e,CPL}$ is less than $R_{e,CPL,1}$.

For a stationary IPT system with a fixed output power, both the CPL's resistance and the system's power transfer efficiency remain fixed and stationary over time after the system reaches stable equilibrium.

III. POWER TRANSFER EFFICIENCY OF A SSIPT SYSTEM TERMINATED IN A CPL AT EQUILIBRIUM

A. EFFICIENCY LIMIT OF A TUNED RESONANT SYSTEM IN STABLE EQUILIBRIUM

An important figure of merit is the power transfer efficiency $\eta = P_o/P_s$ at the DC stable equilibrium state, where P_o is the power delivered to the CPL and P_s is the power produced by the source. In this section we consider the efficiency of a synchronously tuned SSIPT system ($\omega_0 = 1/\sqrt{L_1 C_1} = 1/\sqrt{L_2 C_2}$) operated at resonance in which the primary and secondary reactances are both zero ($X_1 = 0$ and $X_2 = 0$). This is a common assumption and operating condition for SSIPT systems in the literature. Unfortunately, a tuned SSIPT system terminated in a voltage-driven CPL has an efficiency less than the maximum in stable equilibrium. In fact, Narusue *et al.* showed that for a lossy system in stable equilibrium the efficiency is less than 50% ($\eta < 0.5$) [30]. We shall verify this result using the impedance stability criterion (19).

The efficiency η of a SSIPT system terminated in a general AC load resistance $R_{e,L}$ is [38]:

$$\eta = \frac{\omega^2 M^2 R_{e,L}}{[(R_2 + R_{e,L})^2 + X_2^2]R_1 + \omega^2 M^2 (R_2 + R_{e,L})}. \quad (23)$$

At resonance $X_2 = 0$, and (23) can be rewritten in terms of three terms $R_{e,L}, |\mathbf{Z}_{th}|$, and R_2:

$$\eta = \left(\frac{|\mathbf{Z}_{th}| - R_2}{R_2 + R_{e,L}}\right)\left(\frac{R_{e,L}/|\mathbf{Z}_{th}|}{1 + R_{e,L}/|\mathbf{Z}_{th}|}\right). \quad (24)$$

Inspecting (24) reveals that if $R_{e,L} > |\mathbf{Z}_{th}|$ then $\eta < 0.5$. Since, the voltage-driven CPL's input resistance $R_{e,CPL} > |\mathbf{Z}_{th}|$ in stable equilibrium according to the impedance stability criterion (19), we conclude the maximum efficiency for a resonant tuned SSIPT system terminated in a voltage-driven CPL is less than 50% in stable equilibrium. Furthermore, for practical cases with output power levels much less than the maximum available power of the source, the corresponding efficiency is much less than 50%. To graphically illustrate the efficiency limit concept, Fig. 10 presents a plot of the normalized power transfer characteristic and efficiency. These curves are generated by analyzing the AC equivalent circuit in Fig. 3 with a variable load $R_{e,L}$ in which the load resistance is swept from $R_{e,L} = 0$ to $R_{e,L} = 9|\mathbf{Z}_{Th}|$. The primary and secondary effective series resistances are $R_1 = R_2 = 0.039|\mathbf{Z}_{Th}|$. The shaded area in Fig. 10 corresponds to the region $R_{e,L} < |\mathbf{Z}_{th}|$, which is unstable for a voltage-driven CPL termination according to the stability criterion (19). Note that the efficiency η reaches values greater than 50% in the unstable (shaded) region; however, $\eta < 50\%$ in the stable (unshaded) region. The above analysis shows that, without modification, the tuned SSIPT system at resonance will converge to the operating point with reduced efficiency. Indeed, it can be shown from (23) that $\partial\eta/\partial X_1|_{X_1=0}$ for $R_{e,L} = R_{e,CPL,2}$ given by (10), which means the efficiency is minimum at stable equilibrium at the primary circuit's resonant frequency. This is an important result for SSIPT/CPL systems, which, to the best of the authors' knowledge, has not been stated explicitly in the literature before.

B. OPERATING OFF-RESONANCE TO STABILIZE THE SYSTEM AT A HIGH EFFICIENCY OPERATING POINT

In the previous section we showed that the efficiency of a resonant-tuned SSIPT system is minimum at resonance in stable equilibrium. To increase efficiency, Narusue *et al.* proposed adding a K-impedance inverter to the primary side which increases the optimum input resistance [30]. While effective, a K-impedance inverter introduces more components into the system, which adds complexity and increases loss. A simpler solution is to operate off-resonance. Zhang *et al.* showed how to find the optimal frequency to maximize efficiency for a given input voltage [31]. This is useful if the input voltage is fixed, but the method does not yield the maximum possible efficiency. A parameter sweep is required to find the optimal input voltage and operating frequency to maximize efficiency. To speed up search, it would be useful to select a starting point near the optimum point. In this section we show how to find such a starting point. The optimum AC load impedance $R_{e,L}$ required to maximize efficiency η is [38]:

$$R_{e,opt} = \sqrt{R_2^2 + X_2^2 + \frac{\omega^2 M^2 R_2}{R_1}}. \quad (25)$$

Substituting $R_{e,L} = R_{e,opt}$ into (23) yields the maximum efficiency at any given frequency. The maximum achievable
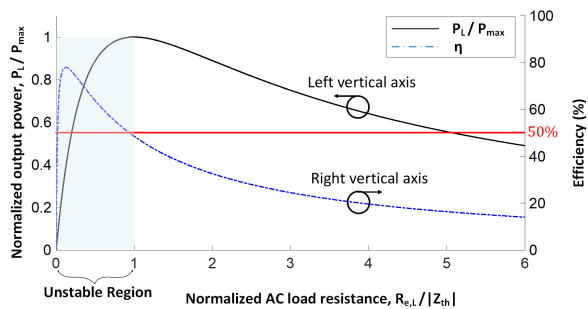
FIGURE 11. Power transfer characteristic and efficiency curve for a tuned SSIPT system operated at resonance.

FIGURE 12. Experimental setup (6.78 MHz system).

TABLE 2. System parameters of the experimental setup (6.78 MHz system).

Parameter	Value	Parameter	Value
L_1	10.53 μH	f_1	6.78 MHz
L_2	3.3 μH	f_2	6.8 MHz
Q_1	361.8	C_1	52.3 pF
Q_2	284.0	C_2	166 pF
V_1	25 V	k	0.142

FIGURE 13. Load resistance of 6.78 MHz experimental setup terminated in a 2 W CPL at stable equilibrium.

efficiency over all frequencies occurs at resonance $X_2 = 0$ [38] and decreases as the operating frequency is adjusted off-resonance.

Consider a synchronously tuned SSIPT/CPL system, in which the primary and secondary resonate at the same frequency ω_o. Due to the stability criterion (19), the optimal solution closest to ω_o is available at frequencies which satisfy the equality: $R_{e,opt} = |\mathbf{Z}_{th}|$. There will in general be two solutions to this equation (one frequency above ω_o, and the other below ω_o). It is common practice to operate above resonance to force the primary current to lag the input voltage, which is necessary for zero voltage switching (ZVS). After the frequency is determined, the corresponding input voltage can be found by solving $\mathbf{V}_1$ using the AC Thevenin equivalent circuit in Fig. 4 and applying (1):

$$V_g = \frac{\pi}{2\sin(\pi D)}\sqrt{\frac{2P_o}{R_{e,L}}}\left|\frac{\mathbf{Z}_{th} + R_{e,L}}{\mathbf{G}_v}\right|. \qquad (26)$$

The operating frequency and input voltage found using the method described above will yield a near-optimal solution for maximizing efficiency that is useful for initiating a parameter sweep. The selection of the off-resonance frequency will be further addressed in the section IV(B).

IV. EXPERIMENTAL VALIDATION

Two different SSIPT systems – one tuned to 6.78 MHz and another tuned to 165 kHz– were constructed to validate results. Each SSIPT system was terminated with an electronic load, and the steady-state system responses were measured over frequency for different load conditions. This section presents the results.

A. 6.78 MHz SYSTEM

A photograph of the 6.78 MHz system is shown in Fig. 12 and its system parameters are presented in Table 2. We are interested in 6.78 MHz because this is the operating frequency used in the A4WP standard. Our system was driven with an Amplifier Research 75A250A RF power amplifier and terminated in a BK Precision 8601 DC electronic load programmed in CW mode to sink 2 W. The full-bridge rectifier was constructed with PDS3100-13 diodes from Diodes
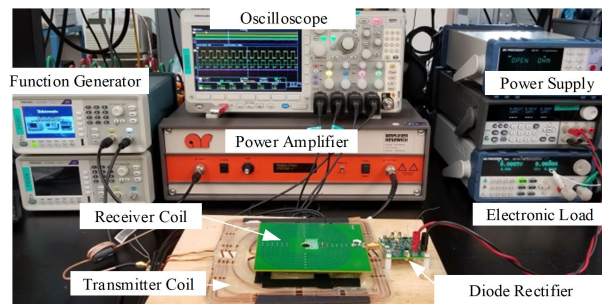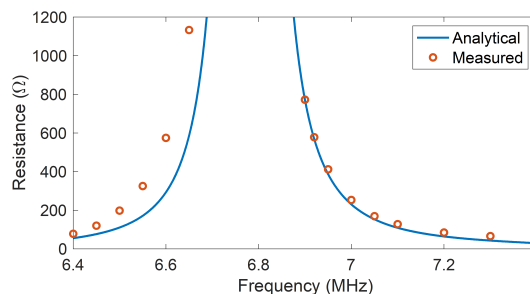
Incorporated. The transmit coil used was a single-layer multiturn inductor (210 mm -by- 210 mm) constructed with AWG 15 wire, and the receive coil was a smaller flat single-layer spiral coil on a PCB. No shielding or ferrites were used, and the coil-to-coil distance was approximately 1 cm.

Figs. 13 and 14 present plots of the DC load resistance and efficiency as functions of frequency. We see that as the operating frequency approaches the resonant frequency (6.78 MHz), the stable equilibrium resistance rises significantly (Fig. 13) and efficiency decreases (Fig. 14). Calculated and measured results in Fig. 13 show fair agreement. The largest disagreement between measured and calculated results are the efficiency curves shown in Fig. 14. This disagreement is likely due to measurement tolerance as well as rectifier diode conduction losses and parasitic capacitances that are not included in the analytical model. As we shall demonstrate, we achieve much better agreement at lower frequencies in which these non-ideal effects are less significant.
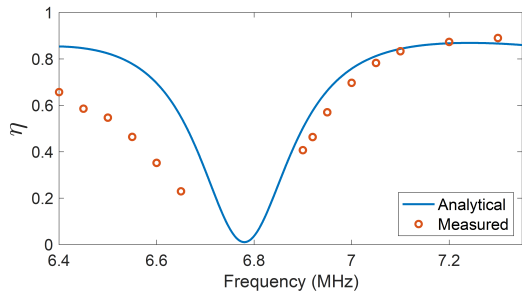
FIGURE 14. Power transfer efficiency of 6.78 MHz experimental setup terminated in a 2 W CPL at stable equilibrium.
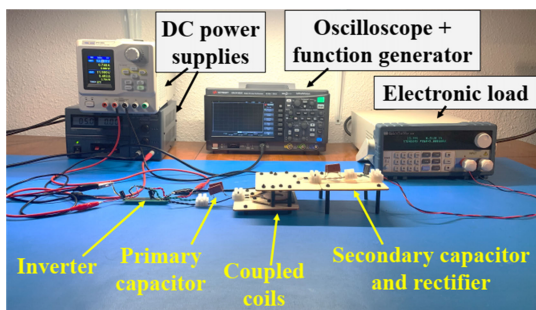

FIGURE 15. Experimental set-up (165 kHz system).

TABLE 3. System parameters of the experimental setup (165 kHz system).

Parameter	Value	Parameter	Value
L_1	25.88 μH	C_1	36.13 nF
L_2	26.07 μH	C_2	35.99 nF
Q_1	193.6	f_1	164.6 kHz
Q_2	187.26	f_2	164.3 kHz
V_F	0.45 V	$R_{ds(on)}$	65 mΩ
D	0.5	k	0.206
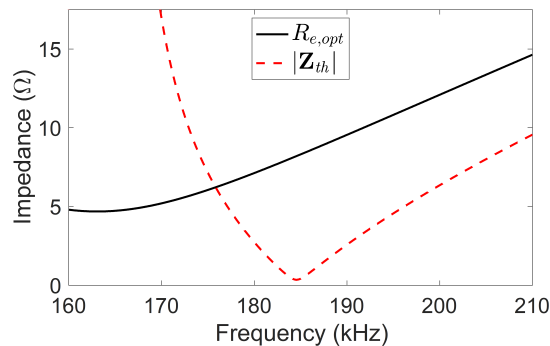
FIGURE 16. $R_{e,opt}$ and $|\mathbf{Z}_{th}|$ and versus frequency (analytical).

B. 165 kHz SYSTEM

Fig. 15 presents a photograph of the experimental 165 kHz wireless charging system. We chose 165 kHz because this frequency is within the typical 87 to 205 kHz operating range used by the popular WPC Qi wireless power standard for inductively charging portable consumer electronics [39]. A possible application involving a CPL at this frequency is inductively charging an off-the-shelf device by connecting the wireless power receiver to the device's charging port. In such a case, the load would constitute the device's integrated battery management system, which typically behaves as a CPL over the majority of the charging cycle. The principal parts of the system are the half-bridge inverter, coupled-inductor resonant circuit, passive half-wave rectifier, and electronic load. For a set of system components and parameters, our goal is to select an inverter switching frequency f and DC input voltage V_g that maximizes efficiency of the SSIPT/CPL system for a given output power. No communication is assumed between the primary and secondary.

System components include an EPC9201 half-bridge inverter, WE-WPCC coils (part number 760308110) with a 2.3 cm air gap, SR340 Schottky rectifier diodes, and a XL4015 buck converter. The inverter's FET on-resistance $R_{ds(on)} = 65$ mΩ and the duty cycle $D = 0.5$. The rectifier diode forward voltage $V_F = 0.45$ V. The primary inductance $L_1 = 25.88$ μH, capacitance $C_1 = 36.13$ nF, resonant frequency $f_1 = 164.6$ kHz, and unloaded quality factor $Q_1 = 193.6$. The corresponding secondary parameters are $L_2 = 26.07$ μH, $C_2 = 35.99$ nF, $f_2 = 164.3$ kHz, and $Q_2 = 187.26$. The coupling coefficient $k = 0.206$. In Table 3, the values of parameters have been summarized.

Fig. 16 is a plot of $|\mathbf{Z}_{th}|$ versus the optimal rectifier input resistance ($R_{e,opt}$). This plot is generated using analytical equations with measured variables (k, L_1, L_2, C_1, C_2, Q_1, Q_2, *etc*.) for a 5 W system with a half bridge rectifier and half bridge inverter. For simplicity, the rectifier loss is not included in this plot. The purpose of generating such a figure is to give the designer a direction for finding an appropriate operating point (i.e,. input voltage and operating frequency). The designer looks for the intersection of $|\mathbf{Z}_{th}|$ with the optimum rectifier input resistance. In Fig. 16, this occurs for a frequency of 175.84 kHz. We also see that at 175.84 kHz the optimal rectifier input resistance is 6.22 Ω. Next we can plug these into (26) to find the optimal input voltage at 175.84 kHz, which we find to be 11.1 V. Assuming the rectifier is not too lossy, this tells us that the optimal solution is near $f = 175.84$ kHz and $V_g = 11.1$ V, which informs the region for the parameter sweep.

Fig. 17 represents the efficiency contour, where the frequency and DC input voltage are swept for the same 5 W system. In addition, this plot (Fig. 17) includes the rectifier loss for completeness. In Fig. 17, the red X marks the absolute maximum possible efficiency point and the red circle marks a good practical operating point. The white region in the contour plot is the invalid region, in which the output power P_o is less than the maximum available power P_{max} from the SSIPT system. The practical operating point is chosen (corresponding to the red circle in Fig. 17) because this operating point yields near optimal efficiency while significantly decreasing the sensitivity to variations in input voltage and frequency. The maximum possible efficiency (red X) efficiency is 0.873, while the efficiency of the point (red
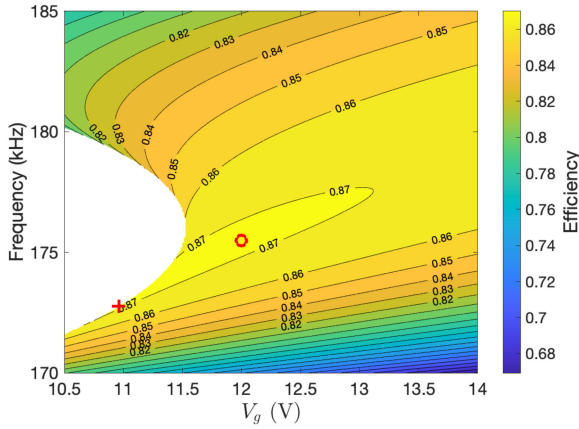
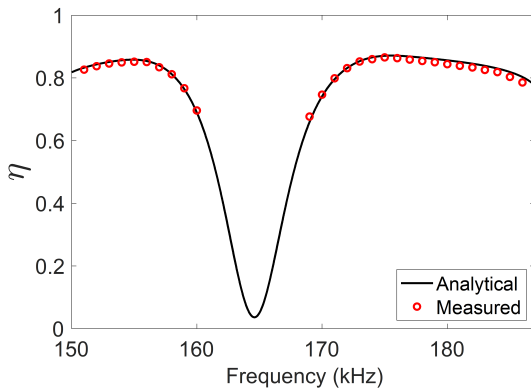**FIGURE 17.** 2D contour plot of efficiency for 5 W system.

FIGURE 18. Efficiency versus operating frequency for a CPL-loaded SSIPT system with V_g = 12 V and P_L = 5 W (analytical and measured).
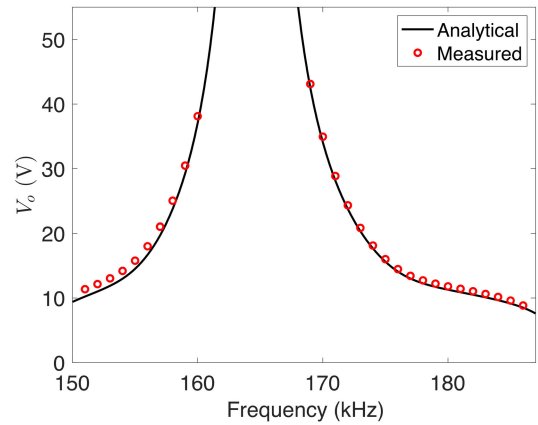

FIGURE 19. DC output voltage versus operating frequency for a CPL-loaded SSIPT system with V_g = 12 V and P_L = 5 W (analytical and measured).

Substituting $V_F = 0.45$ V and $V_o = 15$ V into (27) yields $\eta_{rec} = 0.943$ at 175.5 kHz, which compares well with the measured rectifier efficiency of $\eta_{rec} = 0.940$. With this, the measured wireless link efficiency without the rectifier is 0.871/0.94 = 0.93. This is only slightly less than the theoretical possible maximum efficiency $\eta_{max} = 0.94$, which we calculate using $R_{e,opt}$ given by (25) at resonance ($X_2 = 0$ and $\omega = \omega_2$). The wireless link efficiency can be improved by increasing the coupling coefficient k; however, out of interest we have chosen to consider a system with looser coupling ($k = 0.206$) compared to a typical Qi-compliant system in which k is around 0.65-0.8 [41].

V. CONCLUSION

In this work, we address some fundamental knowledge gaps for SSIPT/CPL systems that we believe have not been fully explored in the literature. In particular, we analyzed the small-signal stability of a SSIPT/CPL system and developed an impedance-based stability criterion that is simple, agrees with intuition, and based on reasonable assumptions. We also showed that the power transfer efficiency is minimum at the resonant frequency of the primary resonator. This behavior is contrary to that of a SSIPT system terminated in a CRL (e.g., a resistor) which can achieve maximum efficiency at the resonant frequency. Finally, we used the stability criterion is to develop a straightforward approach for finding the operating frequency and input voltage that achieves near-maximum power transfer efficiency. This solution is useful as a starting point to speed up a parameter sweep over input voltage and operating frequency for maximizing efficiency. We believe our results are beneficial improving the design process of SSIPTs with loads that behave as CPLs, such as tightly regulated power converters.

We found that the measurements for the 165 kHz system agreed very well with the analytical models. On the other hand, efficiency measurements for the 6.78 MHz system showed more disagreement but did still exhibit the basic

circle) is 0.871. This point (red circle) corresponds to an input voltage and frequency operating point of: $V_g = 12$ V and $f = 175.5$ kHz.

Fig. 18 compares the measured and calculated (analytical) frequency responses, which shows good agreement. At the design frequency $f = 175.5$ kHz the measured and calculated efficiencies (η) are above 0.87. The red circles are measured data and the black line is the analytical. This plot includes the losses due to the rectifier. So the efficiency is the full DC-to-DC efficiency of the system including the inverter, resonant circuit, and rectifier.

The power loss in the rectifier is a significant portion of the overall system loss and is mainly due to the forward voltage drop V_F across each diode. Fig. 19 shows a plot of the measured output DC voltage V_o over frequency. In high-power IPT systems V_F is typically negligible compared to the output DC voltage V_o; however, in our case $V_F = 0.45$ V, which is non-negligible compared to $V_o = 15$ V at 175.5 kHz. The efficiency η_{rec} of the half-wave rectifier alone can be calculated as [40]:

$$\eta_{rec} = \frac{1}{1 + \frac{2V_F}{V_o}}. \tag{27}$$

features predicted at resonance (i.e., high equilibrium load impedance and minimum efficiency). We believe that at the high operating frequencies, the simple diode model we assumed is not adequate and needs improvement for better agreement. Other challenges at MHz frequencies include higher sensitivity to measurement error and parasitic capacitances.

For future work, it would be useful to study how SSIPT/CPL systems perform against disturbances (e.g., changes in coupling coefficient). It would also be useful to compare how various IPT topologies (e.g., series-series, series-parallel, LCC-series, etc.) perform with CPLs in terms of efficiency, bandwidth, sensitivity to coupling coefficient changes, etc. The performance and features of these topologies are better understood for ordinary loads than for CPLs.

APPENDIX

To prove (13) consider the SSIPT system shown in Fig. 20, which is driven by a DC input voltage $v_g(t) = V_g$ and terminated in a DC current sink $i_{out}(t) = I_o$. Note that the quiescent output voltage is $v_{out}(t) = V_o$. If the output current $i_{out}(t)$ is suddenly increased from I_o to $I_o + \delta I_0$ then the system will undergo a transient step response and the output voltage $v_{out}(t)$ will change over time from V_o to its new quiescent value $V_o + \delta V_0$. For a small disturbance, such that $I_o \gg \delta I_0$ and $V_o \gg \delta V_0$, the DC small-signal input impedance can be approximated as $Z_g(0) \approx -(\delta V_0)/(\delta I_0)$. In the differential limit we obtain $Z_g(0) = -(dV_0)/(dI_0)$.

To find $Z_g(0) = -(dV_0)/(dI_0)$, we first solve for the AC output voltage magnitude $|V_2|$ by analyzing the AC Thevenin equivalent circuit in Fig. 4 terminated in a general AC effective load resistance $R_{e,L}$:

$$|V_2| = \frac{|V_1 G_{v,AC}| R_{e,L}}{|Z_{th} + R_{e,L}|}$$
$$= \frac{|V_1 G_{v,AC}| R_{e,L}}{\sqrt{|Z_{th}|^2 + R_{e,L}^2 + 2 R_{e,L} Re[Z_{th}]}}. \quad (28)$$

Next we use (1) – (4) to re-express (28) in terms of the DC terminal variables V_g, V_o, and I_o:

$$V_o = \frac{|G_{v,AC}| \frac{V_o}{I_o} \left(\frac{2}{\pi^2}\right) d_{12} c_{12} V_g \sin(\pi D)}{\sqrt{|Z_{th}|^2 + \left(\frac{V_o}{I_o} \frac{2 d_{12}^2}{\pi^2}\right) + 2\left(\frac{V_o}{I_o} \frac{2 d_{12}^2}{\pi^2}\right) Re[Z_{th}]}}. \quad (29)$$

Squaring both sides of (29), simplifying, and rearranging terms yields the following expression:

$$I_o^2 |Z_{th}|^2 + V_o^2 \left(\frac{2 d_{12}^2}{\pi^2}\right)^2 + 2 I_o V_o \left(\frac{2 d_{12}^2}{\pi^2}\right) Re[Z_{th}]$$
$$= \left(|G_{v,AC}| V_g \frac{\sin(\pi D) 2 c_{12}}{\pi}\right)^2. \quad (30)$$

Taking the derivative of both sides of (30) with respect to I_o, and substituting $Z_g(0) = -(dV_0)/(dI_0)$ and $R_L = V_0/I_0$
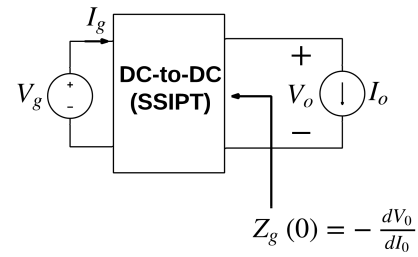

FIGURE 20. Simplified block diagram of SSIPT system driven by a DC input voltage V_g and terminated in a DC current sink I_o.

yields:

$$2|Z_{th}|^2 - 2 Z_g(0) R_L \left(\frac{2 d_{12}^2}{\pi^2}\right)^2$$
$$+ 2\left(R_L - Z_g(0)\right)\left(\frac{2 d_{12}^2}{\pi^2}\right) Re[Z_{th}] = 0. \quad (31)$$

Solving (31) for $Z_g(0)$ gives:

$$Z_g(0) = \left(\frac{\pi^2}{2 d_{12}^2}\right) \frac{|Z_{th}|^2 + R_L \left(\frac{2 d_{12}^2}{\pi^2}\right) Re[Z_{th}]}{R_L \left(\frac{2 d_{12}^2}{\pi^2}\right) + Re[Z_{th}]}. \quad (32)$$

Finally we use (4) to substitute $R_{e,CPL} = R_L(2 d_{12}^2/\pi^2)$ into (32) which equals (13).

REFERENCES

[1] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: Definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Trans. Veh. Technol.*, vol. 55, no. 4, pp. 1112–1125, Jul. 2006.

[2] A. Khaligh, "Realization of parasitics in stability of DC–DC converters loaded by constant power loads in advanced multiconverter automotive systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2295–2305, Jun. 2008.

[3] S. C. Smithson and S. S. Williamson, "Constant power loads in More Electric Vehicles—An overview," in *Proc. 38th IEEE Ind. Electron. Soc.*, Dec. 2012, pp. 2914–2922.

[4] A. Emadi, B. Fahimi, and M. Ehsani, "On the concept of negative impedance instability in the More Electric Aircraft power systems with constant power loads," *SAE Trans.*, vol. 5, pp. 689–699, Dec. 1999.

[5] W. Chayinthu, K. N. Areerak, K. L. Areerak, and A. Srikaew, "The optimized cascade PI controllers of the generator control unit in the aircraft power system," *Int. J. Electr. Comput. Eng.*, vol. 7, no. 5, pp. 488–496, 2013.

[6] G. Sulligoi, D. Bosich, G. Giadrossi, L. Zhu, M. Cupelli, and A. Monti, "Multiconverter medium voltage DC power systems on ships: Constant-power loads instability solution using linearization via state feedback control," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2543–2552, Sep. 2014.

[7] J. R. LeSage, R. G. Longoria, and W. Shutt, "Power system stability analysis of synthesized complex impedance loads on an electric ship," in *Proc. IEEE Electric Ship Technol. Symp.*, Apr. 2011, pp. 34–37.

[8] A. Kwasinski and C. N. Onwuchekwa, "Effects of instantaneous constant-power loads on DC micro-grids for sustainable power systems," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 862–869.

[9] M. K. AL-Nussairi, R. Bayindir, S. Padmanaban, L. Mihet-Popa, and P. Siano, "Constant power loads (CPL) with microgrids: Problem definition, stability analysis and compensation techniques," *Energies*, vol. 10, no. 10, p. 1656, Oct. 2017.

[10] E. Hossain, R. Perez, A. Nasiri, and R. Bayindir, "Stability improvement of microgrids in the presence of constant power loads," *Int. J. Electr. Power Energy Syst.*, vol. 96, pp. 442–456, Mar. 2018.

[11] E. Hossain, R. Perez, and R. Bayindir, "Stability analysis of MIMO microgrid systems in d–q axis platform with constant power loads based on popov absolute stability criterion," *Electr. Power Compon. Syst.*, vol. 45, no. 19, pp. 2200–2215, Nov. 2017.

[12] E. Hossain, R. Perez, S. Padmanaban, L. Mihet-Popa, F. Blaabjerg, and V. Ramachandaramurthy, "Sliding mode controller and Lyapunov redesign controller to improve microgrid stability: A comparative analysis with CPL power variation," *Energies*, vol. 10, no. 12, p. 1959, Nov. 2017.

[13] E. Hossain, R. Perez, S. Padmanaban, and P. Siano, "Investigation on the development of a sliding mode controller for constant power loads in microgrids," *Energies*, vol. 10, no. 8, p. 1086, Jul. 2017.

[14] S. Singh, A. R. Gautam, and D. Fulwani, "Constant power loads and their effects in DC distributed power systems: A review," *Renew. Sustain. Energy Rev.*, vol. 72, pp. 407–421, May 2017.

[15] V. Grigore, J. Hatonen, J. Kyyra, and T. Suntio, "Dynamics of a buck converter with a constant power load," in *Proc. 29th Annu. IEEE Power Electron. Specialists Conf.*, 1998, pp. 72–78.

[16] A. M. Rahimi and A. Emadi, "Active damping in DC/DC power electronic converters: A novel method to overcome the problems of constant power loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1428–1439, May 2009.

[17] M. N. Hussain, R. Mishra, and V. Agarwal, "A frequency-dependent virtual impedance for voltage-regulating converters feeding constant power loads in a DC microgrid," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 5630–5639, Nov. 2018.

[18] S. Arora, P. Balsara, and D. Bhatia, "Input–Output linearization of a boost converter with mixed load (Constant voltage load and constant power Load)," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 815–825, Jan. 2019.

[19] C. T. Rim and C. Mi, *Wireless Power Transfer for Electric Vehicles and Mobile Devices*. Chichester, U.K.: John Wiley & Sons, Ltd, 2017.

[20] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, 1976, pp. 366–382.

[21] C. M. Wildrick, F. C. Lee, B. H. Cho, and B. Choi, "A method of defining the load impedance specification for a stable distributed power system," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 280–285, May 1995.

[22] X. Feng, J. Liu, and F. C. Lee, "Impedance specifications for stable DC distributed power systems," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157–162, Mar. 2002.

[23] S. D. Sudhoff, S. F. Glover, P. T. Lamm, D. H. Schmucker, D. E. Delisle, and S. P. Karatsinides, "Admittance space stability analysis of power electronic systems," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 36, no. 3, pp. 965–973, Jul. 2000.

[24] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for DC power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3525–3535, Sep. 2014.

[25] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3075–3078, Nov. 2011.

[26] Z. Huang, D. of Electronic, and H. K. P. U. Information Engineering, "Revisiting stability criteria for DC power distribution systems based on power balance," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 1, pp. 76–85, Apr. 2017.

[27] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Inverse nyquist stability criterion for grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1548–1556, Feb. 2017.

[28] K. Cavanagh, P. Vorobev, and K. Turitsyn, "Stability of DC networks with generic load models," 2018, *arXiv:1803.01918*. [Online]. Available: http://arxiv.org/abs/1803.01918

[29] X. Zhang, X. Ruan, and C. K. Tse, "Impedance-based local stability criterion for DC distributed power systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 916–925, Mar. 2015.

[30] Y. Narusue, Y. Kawahara, and T. Asami, "Maximizing the efficiency of wireless power transfer with a receiver-side switching voltage regulator," *Wireless Power Transf.*, vol. 4, no. 1, pp. 42–54, Mar. 2017.

[31] Y. Zhang, T. Kan, Z. Yan, and C. C. Mi, "Frequency and voltage tuning of Series–Series compensated wireless power transfer system to sustain rated power under various conditions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1311–1317, Jun. 2019.

[32] R. W. Erickson and D. Maksimoviä, *Fundamentals Power Electronics*, 2nd ed. Boston, MA, USA: Springer, 2001.

[33] S. Aldhaher, *Design and Optimization of Switched-Mode Circuits for Inductive Links*. Cranfield, U.K.: Cranfield Univ., 2014.

[34] Q.-C. Zhong and X. Zhang, "Impedance-sum stability criterion for power electronic systems with two converters/sources," *IEEE Access*, vol. 7, pp. 21254–21265, 2019.

[35] A. bin Jusoh, "The instability effect of constant power loads," in *Proc. Nat. Power Energy Conf.*, 2004, pp. 175–179.

[36] M. Cupelli, L. Zhu, and A. Monti, "Why ideal constant power loads are not the worst case condition from a control standpoint," *IEEE Trans. Smart Grid*, vol. 6, no. 6, pp. 2596–2606, Nov. 2015.

[37] J. Hahn, T. Edison, and T. F. Edgar, "A note on stability analysis using Bode plots," *Chem. Eng. Educ.*, vol. 5, pp. 208–211, Dec. 2001.

[38] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025–4034, Jul. 2015.

[39] WPC. *Qi specifications*. Accessed: Oct. 27, 2020. [Online]. Available: https://www.wirelesspowerconsortium.com/knowledge-base/specifications/download-the-qi-specifications.html

[40] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

[41] Q. Tian and L. Jia, "WPC qi mobile device rx coil design and optimization," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2020, pp. 3140–3146.
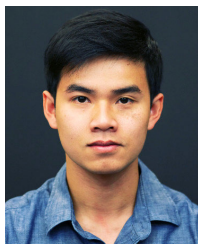
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