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A Compact Short-Channel Analytical Drain Current Model of Asymmetric Dual-Gate TMD FET in Subthreshold Region Including Fringing Field Effects

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ABSTRACT A compact drain current model is developed for an asymmetric, dual gate, monolayer $2-D$ Transition metal dichalcogenide (TMD) field effect transistor (FET) in the subthreshold region. The work includes the effect of source to drain tunneling and gate dielectric fringing effects. The model is systematically derived for an asymmetric, dual gate structure. The model developed is also extended into a dual-gate symmetric structure. The characteristic length expression has only physical and dimensional parameters including the contribution of fringing field effects from both front and back gate dielectric. The model is validated with simulation results obtained using NEGF based nanodevice simulators and experimental data of WSe_2 p-channel FET. Also, transfer characteristics, output characteristics, subthreshold swing and output resistance are compared with reported data in literatures. A close agreement is observed with some disparity arising because of the non-inclusion of back gate fringing effects and source to drain tunneling in their models. The proposed model captures the effects of different high-κ gate dielectric materials and its thicknesses. Impact of temperature is also studied on transfer characteristics. The model is also scalable from ultrashort channel regime to long channel regime. Finally, the model can be applicable not only for TMD materials but other $2-D$ materials also.

INDEX TERMS $2-D$, TMD, FET, fringing effect, NEGF, drift-diffusion.

I. INTRODUCTION

2-D Transition metal dichalcogenides (TMDs) have attracted a lot of attention to the scientific community because of its interesting properties like natural bandgap, impurity charge free surfaces and atomic scale thicknesses [1], [2].Their properties make it suitable channel materials for ultrascaled technology nodes below 10 nm. Transition metal dichalcogenides are compounds formed by transition metals and chalcogen atoms. There are various TMDs garnering attention recently like MoS_2, WSe_2, $MoSe_2$, WTe_2 etc. Monolayer TMDs achieve a bandgap of around 1.6-2.0 eV which is suitable for ultra low power applications, thus could potentially solve a major bottleneck for the current Silicon technology.

For circuit exploration purpose, it is essential to develop compact I-V models for TMD based Field effect transistors. There have been several efforts in this direction ever since the inception of these materials. In [3], authors have developed long channel models for TMD FET utilizing drift-diffusion transport based model. In [4], some non-ideal effects like interface traps, mobility degradation and inefficient doping effect are included in the drift-diffusion model. In [5], authors have proposed compact I-V models for $2D$ material FETs using semiclassical transport based approach including several nonideal effects. However the model is applicable for long channel transistors having channel length around 100 nm. In [6], Taur et. al. have developed short channel

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models for $2-D$ material channel FETs. But the authors did'nt discuss development of compact, closed form expressions for current related to geometric and physical parameters of $2-D$ FET. However, in [10], [11], authors have developed the framework for analyzing short channel effects in $2-D$ material FETs using generalized scale length approach. Subthreshold I-V model for short-channel TMDFETs is proposed in [7]. In their work, authors have verified the results using a drift-diffusion based simulator. However, in TMD FETs for channel length below 10 *nm*, transport mechanism is not drift-diffusion based thus their model fails to model short-channel TMDFETs. Also the model developed does'nt include back gate fringing field effects. In [8], author has proposed a short channel model for symmetric TMD FET in the subthreshold region. The model is developed from the short channel model in [6], [10]. The characteristic length expression contains empirical parameters which lacks physical meaning and author has mentioned the inclusion of those parameters solely to fit the numerical simulation results. The derivation of the characteristic length expression is not clearly described and also it underestimates the impact of back gate thickness which will be described later in this paper. Author has claimed to model down to channel length of 3 *nm*, however they report characteristic length (λ) varying from (4.05-4.85) *nm*. Now as mentioned in [10], lowest order scale length can be termed as characteristic length only for channel length preferably above 2λ. So, characteristic length expression mentioned in the paper should have taken higher order expressions for modelling down to 3 *nm*. Also, such complex expression of characteristic length is highly undesirable as it would limit the development of a compact model. Modeling technique described by [8] does'nt take care of this limitation even though authors report results for channel length down to 3 *nm*. Also the approach is applicable for selected ranges of dielectric constants of dielectric and channel materials and its thicknesses severely limiting our purpose to develop the compact model for any arbitrary $2-D$ TMD FET. Further, at such nanometric dimensions, source to drain tunneling can't be ignored. However this is not taken care of in prior literatures to the best of authors' knowledge.

Principal contributions of our work are as follows:

- This work for the first time derives the compact subthreshold model for an asymmetric TMD FET structure including the source to drain tunneling effect and front and back gate dielectric fringing effects. The approach can be smoothly extended to develop the model for a symmetric structure described in [8]. Further the model can be utilized for any arbitrary $2-D$ material FET structure.
- Back gate fringing field effect is included in the developed model. Work in [8] does'nt include the impact of back gate fringing field effects, and is only applicable for symmetric TMD FET. In [7], although it claims it includes the fringing field effect but it includes the effect using fitting parameter which underestimates the impact and is only validated with drift diffusion based simulator.
- The developed model is validated using NEGF based simulator, NanoTCAD ViDES [13] and Experimental data [14]. It is compared with the results in [7] and [8] in terms of transfer characteristics, output characteristics, output resistance and subthreshold swing. A close conformity is observed with disparity at shorter channel lengths because of non-inclusion of source to drain tunneling and back gate fringing effects in their models.
- The study has been carried out for different front and back gate dielectric materials i.e. SiO_2, Y_2O_3, HfO_2, BaO and TiO_2 and thicknesses (i.e. from 2 *nm* to 6 *nm*).
- The study has been performed for different channel lengths from 120 *nm* to 5 *nm* to verify the applicability of our model in ultra short channel length regime. The work also proves the scalability of our model from long channel to ultrashort channel regime.
- Impact of temperature on transfer characteristics is studied.
- Impact of channel length and dielectric thickness on transfer characteristics and subthreshold swing is also studied.

The paper is organized as follows. In section II, the compact subthreshold current model including source to drain tunneling model and gate dielectric fringing field effects has been methodically derived for both asymmetric and symmetric TMD FET structure. Section III discusses the results in detail. Finally, the conclusions are drawn in Section IV.

II. DERIVATION OF COMPACT SUBTHRESHOLD MODEL

A. ASYMMETRIC DUAL GATE STRUCTURE

Fig. 1(a) shows the schematic of the asymmetric Dual-gate monolayer TMD FET device, where, x is the channel direction and, y is perpendicular to the channel. Parameters considered in the model are shown in Table 1. Nourbakhsh et. al. has reported, that tunneling from source to drain of MoS_2 MOSFET does not significantly contribute to transport in sub 10 nm regime due to its high effective mass and large bandgap [12]. Whereas, materials with low bandgap and effective mass will suffer from source to drain tunneling in subthreshold region. So, source to drain tunneling has been included in the proposed model to utilized it for any arbitrary $2-D$ materials as described in subsection C. Considering an infinitesimal Gaussian enclosure in the $2-D$ material channel as depicted in Fig. 1(b), we arrive at the below mentioned expression,

$$qN_{ch}\Delta x = T_{ch}[k_{ch}\xi_{C,x}(x) - k_{ch}\xi_{C,x}(x+\Delta x)] + \Delta x[k_{ch}\xi_{C,y}(y+\Delta y) + k_{ch}\xi_{C,y}(y)] \quad (1)$$

Here, field moving into the surface is taken to be positive and coming out of the surface is considered to be nagative. Now, the Gaussian enclosure in front gate dielectric results in,

$$0 = T_{fox}[k_{fox}\xi_{fox,x}(x) - k_{fox}\xi_{fox,x}(x+\Delta x)] + \Delta x[k_{fox}\xi_{fox} - k_{ch}\xi_{C,y}(y)] \quad (2)$$

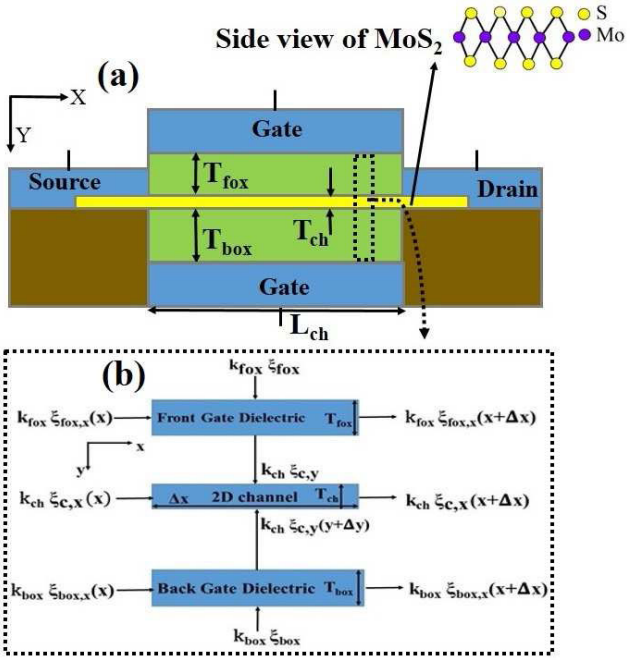

FIGURE 1. (a) Cross section of an Asymmetric, dual-gate monolayer TMD FET (In this case, MoS_2 is shown as the $2-D$ TMD material used in the channel). Here, T_{fox} and T_{box} are the thicknesses of the front and back gate oxide respectively. L_{ch} and T_{ch} are the channel length and thickness of the TMD FET. (b) Expanded view of the infinitesimal Gaussian enclosure in the channel region, front and back gate dielectric region. Here, k_{ch}, k_{fox} and k_{box} are the dielectric constants of the TMD channel, front and back gate oxide respectively.

TABLE 1. Parameters of the TMD FET structure.

Symbols	Definition	Nominal values/range of values/Definition
L_{ch} (in nm)	Channel length	(5-120)
W_{ch} (in μm)	Channel width	1.0
T_{ch} (in nm)	Channel thickness	0.65
N_{ch} (in $/cm^2$)	Channel doping concentration	6.5×10^7
k_{ch}	Dielectric constant of the channel	4.8
k_{SiO2}	Dielectric constant of Silicon Dioxide	3.9
α	Front gate dielectric parameter	$\frac{k_{fox}}{k_{SiO2}}$
β	Back gate dielectric parameter	$\frac{k_{box}}{k_{SiO2}}$
$EOTF$	Effective thickness of the front gate dielectric	$T_{fox}\left(\frac{k_{SiO2}}{k_{fox}}\right)$
$EOTB$	Effective thickness of the back gate dielectric	$T_{box}\left(\frac{k_{SiO2}}{k_{box}}\right)$
N_{src} (in $/cm^2$)	Source doping concentration	1×10^{13}
N_d (in $/cm^2$)	drain doping concentration	1×10^{13}
g_s	Spin degeneracy factor	2
g_v	Valley degeneracy factor	2

Similarly, the Gaussian enclosure in back gate dielectric results in,

$$0 = T_{box}[k_{box}\xi_{box,x}(x) - k_{box}\xi_{box,x}(x+\Delta x)] + \Delta x[k_{box}\xi_{box} - k_{ch}\xi_{C,y}(y+\Delta y)] \quad (3)$$

Here, $\xi_{C,x}$ and $\xi_{C,y}$ are the Electric fields in the channel in lateral and vertical direction respectively. Now, Equation (1) can be simplified to,

$$qN_{ch} = -k_{ch}T_{ch}\frac{d\xi_{C,x}}{dx} + k_{ch}(\xi_{C,y}(y) + \xi_{C,y}(y+\Delta y)) \quad (4)$$

Here, $\xi_{C,y}(y)$ and $\xi_{C,y}(y+\Delta y)$ are the vertical Electric field components on the front and back surface of the $2-D$ TMD channel arising because of the Front and back gate bias, the fringe field due to high k dielectric is included in the model by taking the gaussian enclosure in both the dielectrics [7] as shown in Fig. 1(b).

Equation (2) can be simplified to obtain expression of $\xi_{C,y}(y)$ as,

$$\begin{aligned}\xi_{C,y}(y) &= \left(\frac{k_{fox}}{k_{ch}}\right)\xi_{fox} - T_{fox}\left(\frac{k_{fox}}{k_{ch}}\right)\frac{d\xi_{fox,x}}{dx} \\ &= \left(\frac{k_{fox}}{k_{ch}}\right)\xi_{fox} - \alpha.EOTF\left(\frac{k_{fox}}{k_{ch}}\right)\frac{d\xi_{fox,x}}{dx}\end{aligned} \quad (5)$$

Now, as lateral electric field in the channel and the front gate dielectric can be related as, $\xi_{C,x}(x) = \alpha.\eta_F.\xi_{fox,x}(x)$, so Equation (5) can be represented as,

$$\xi_{C,y}(y) = \left(\frac{k_{fox}}{k_{ch}}\right)\xi_{fox} - \left(\frac{EOTF}{\eta_F}\right)\left(\frac{k_{fox}}{k_{ch}}\right)\frac{d\xi_{C,x}(x)}{dx} \quad (6)$$

Here, η_F is a model parameter for the front gate dielectric. Using the same procedure from Equation (3) can be simplified to obtain expression of $\xi_{C,y}(y+\Delta y)$ as,

$$\begin{aligned}\xi_{C,y}(y+\Delta y) &= \left(\frac{k_{box}}{k_{ch}}\right)\xi_{box} - T_{box}\left(\frac{k_{box}}{k_{ch}}\right)\frac{d\xi_{box,x}}{dx} \\ &= \left(\frac{k_{box}}{k_{ch}}\right)\xi_{box} - \beta.EOTB\left(\frac{k_{box}}{k_{ch}}\right)\frac{d\xi_{box,x}}{dx}\end{aligned} \quad (7)$$

As, lateral electric field in the channel and the back gate dielectric can be related as, $\xi_{C,x}(x) = \beta.\eta_B.\xi_{box,x}(x)$, so Equation (7) can be represented as,

$$\xi_{C,y}(y+\Delta y) = \left(\frac{k_{box}}{k_{ch}}\right)\xi_{box} - \left(\frac{EOTB}{\eta_B}\right)\left(\frac{k_{box}}{k_{ch}}\right)\frac{d\xi_{C,x}(x)}{dx} \quad (8)$$

Here, η_B denotes the model parameter for the back gate dielectric. Now, ξ_{fox} and ξ_{box} are the electric fields on the top of front and back gate dielectric respectively. They can be expressed as,

$$\xi_{fox} = \left(\frac{V_{gs} - V_{fb} - \psi_c(x)}{T_{fox}}\right) \quad (9)$$

and,

$$\xi_{box} = \left(\frac{V_{bs} - V_{fbb} - \psi_c(x)}{T_{box}}\right) \quad (10)$$

Here, $\psi_c(x)$ denotes the surface potential of the TMD channel and V_{gs}, V_{bs}, V_{fb} and V_{fbb} are the front gate bias, back gate bias, flat band voltage of front gate oxide and flat band voltage of back gate oxide respectively. Firstly, expression in Equation (9) and Equation (10) are substituted in

Equations (6) and (8) respectively. Finally these expressions in Equation (6) and (8) are substituted in Equation (4) to obtain a simplified expression represented as,

$$\lambda^2 \frac{d^2\psi_c(x)}{dx^2} - \psi_c(x) + \psi_{c,long} = 0 \tag{11}$$

where, λ is called the characteristic length expressed as,

$$\lambda = \left[\frac{T_{fox}T_{box}T_{ch}k_{ch}}{k_{fox}T_{box} + k_{box}T_{fox}} + \frac{T_{fox}T_{box}}{k_{fox}T_{box} + k_{box}T_{fox}} \left(\frac{k_{fox}.EOTF}{\eta_F} + \frac{k_{box}.EOTB}{\eta_B} \right) \right]^{\frac{1}{2}} \tag{12}$$

The expression of λ in Equation (12) includes fringing field from both front and back gate unlike the expression obtained in [7] where, fringing field arising out of back gate is neglected. However for a high-κ dielectric in the back side of TMDFET necessitates the inclusion of back gate fringing effect. Parameters η_F and η_B essentially models the impact of front and back gate on the TMD channel respectively. Also, $\psi_{c,long}$ is the long channel surface potential expressed as,

$$\psi_{c,long} = \frac{k_{fox}T_{box}(V_{gs}-V_{fb}) + k_{box}T_{fox}(V_{bs}-V_{fbb}) - qN_{ch}T_{fox}T_{box}}{k_{fox}T_{box} + k_{box}T_{fox}} \tag{13}$$

Equation (11) can be solved with the boundary conditions at source and drain side as, $\psi_c(0) = V_{bi}$ and $\psi_c(L_{ch}) = V_{bi} + V_{ds}$ as,

$$\psi_c(x) = \psi_{c,long} + (V_{bi} - \psi_{c,long})\frac{\sinh[(L_{ch}-x)/\lambda]}{\sinh(L_{ch}/\lambda)} + (V_{bi} + V_{ds} - \psi_{c,long})\frac{\sinh(x/\lambda)}{\sinh(L_{ch}/\lambda)} \tag{14}$$

In this case, surface potential along the channel, ψ_c varies only along x-direction because a monolayer TMD channel is considered having channel thickness $\sim 0.65\ nm$. So it is assumed that potential variation along the perpendicular to channel direction (y-direction) is insignificant compared to the variation along the channel. Here, V_{bi} is the built in potential the source-channel junction and V_{ds} is the applied drain to source bias. V_{bi} can be expressed as,

$$V_{bi} = \left(kT/q\right)\ln\left(N_{src}N_{ch}/N_{int}^2\right)$$

Here, N_{src} is the doping concentration in the source side and N_{int} is the intrinsic carrier concentration in the channel. Both are generally expressed in the unit of cm^{-2}. Thus the model developed can be utilized for any arbitrary TMD FET having asymmetric gate oxide material and thickness.

B. SYMMETRIC DUAL GATE STRUCTURE

The model developed in the previous subsection can be extended to a symmetric structure having identical front and back gate dielectric material and thickness. The expression of characteristic length, λ can be derived from Equation (12) as,

$$\lambda = \left[\frac{T_{fox}T_{ch}k_{ch}}{2k_{fox}} + \frac{k_{fox}EOTF^2}{\eta_F.k_{SiO2}} \right]^{\frac{1}{2}} \tag{15}$$

Also, long channel surface potential simplifies to,

$$\psi_{c,long} = \left(V_{gs} - V_{fb} - \frac{qN_{ch}T_{fox}}{2k_{fox}} \right) \tag{16}$$

Here, for symmetrical structure, $T_{fox} = T_{box}$, $k_{fox} = k_{box}$, $EOTF = EOTB$ and $\eta_F = \eta_B$.

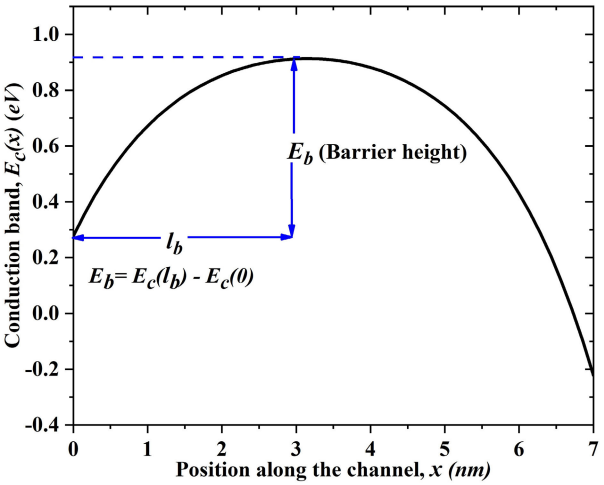

FIGURE 2. Conduction band, $E_c(x)$ Vs. position along the channel, x for V_{gs}=0 V and V_{ds}=0.5 V with equivalent oxide thickness, EOT=0.41 nm for both front and back gate oxides.

C. SOURCE TO DRAIN TUNNELING MODEL

Source to drain tunneling is inevitable for ultra short channel 2-D FETs. The model can be developed from the energy band profile. The conduction band profile of MoS_2 FET has been plotted in Fig. 2. From the figure, following expression can be written as,

$$E_c(x) = -q * \psi_c(x) + \frac{E_g}{2} \tag{17}$$

Now, E_b (barrier height) can be written as,

$$E_b = E_c(l_b) - E_c(0) \tag{18}$$

The surface potential minima or the conduction band maxima occurs where electric field is zero. So, by using $-\frac{d\psi_c(x)}{dx} = 0$, at $x = l_b$ it is found that,

$$l_b = \lambda.tanh^{-1}\left(\frac{(V_{bi} - \psi_{c,long})cosh(L_{ch}/\lambda)}{(V_{bi} - \psi_{c,long})cosh(L_{ch}/\lambda)} + \frac{(V_{bi} + V_{ds} - \psi_{c,long})}{(V_{bi} - \psi_{c,long})cosh(L_{ch}/\lambda)}\right) \tag{19}$$

For any arbitrary energy, E, the expressions for intersection points, x_s (near source-channel junction) and x_d (near

drain-channel junction) have been derived as [15],

$$x_s = L_{ch} - \lambda sinh^{-1}\left(\frac{(E - E_g/2 + q\psi_{c,long})sinh(L_{ch}/\lambda)}{q(\psi_{c,long} - V_{bi})}\right) \quad (20)$$

$$x_d = \lambda.sinh^{-1}\left(\frac{(E - E_g/2 + q\psi_{c,long})sinh(L_{ch}/\lambda)}{q(\psi_{c,long} - V_{ds} - V_{bi})}\right) \quad (21)$$

Now, the source to drain tunneling probability (T_{WKB}) can be evaluated using WKB approximation [16] as in Equation (22),

$$T_{WKB}(E) = e^{-\frac{2\sqrt{2m^*}\int_{x_s}^{x_d}\sqrt{E_c(x)-E}dx}{\hbar}} \quad (22)$$

Here, m^*, $E_c(x)$, E are effective mass of the carrier, conduction band energy and the carrier energy respectively.

The drain to source current due to tunneling is evaluated using Landauer's formula as given in Equation (23),

$$I_{d,tun} = \frac{2 * q}{h} \times \int_{Ec(0)}^{Ec(l_b)} M(E)T_{WKB}(E)(fs - fd)dE \quad (23)$$

Here, $M(E)$ is the number of the conduction modes for $2-D$ materials and can be written as [17],

$$M(E) = W_{ch}g_s g_v \frac{\sqrt{2m^*(E - Eg)}}{\pi\hbar} \quad (24)$$

Here, W_{ch}, g_s, g_v and $\hbar$ are width of the channel, spin degeneracy factor, valley degeneracy factor and reduced planck's constant respectively.

D. DRAIN CURRENT CALCULATION

The subthreshold drain current can be evaluated according to the expression obtained from [9], [10] as,

$$I_{d,sub} = \frac{W_{ch}kT\mu(N_{int}^2/N_{ch})\left[1 - e^{-qV_{ds}/kT}\right]}{\int_0^{L_{ch}} e^{-q\psi_c(x)/kT}dx} \quad (25)$$

Total drain to source current, I_{ds} can be obtained by using Equations (25) and (23).

$$I_{ds} = I_{d,sub} + I_{d,tun} \quad (26)$$

Here, W_{ch} is the channel width, k is Boltzmann's constant, T is temperature and μ is the carrier mobility and $I_{d,tun}$ is tunneling current due to the carriers tunneling from source to drain.

III. RESULTS AND DISCUSSION

Our developed model is verified with numerical simulation data obtained using NEGF based nanodevice simulator, NanoTCAD ViDES [13] as well as with experimental data of WSe_2 p-channel FET [14]. The parameters considered in this work are mentioned in Table 2. The flatband voltage (V_{FB}) in this work is taken to be 0.19 V. For the asymmetric structure, we have varied the dielectric constant of the front gate dielectric by selecting various oxides. However, the back gate oxide is considered to be Silicon dioxide (SiO_2) and back gate bias is 0 V. For the symmetric structure, both front and back gate oxides are of the same material and tied to a common bias voltage. The validation of our model against NEGF based simulator is shown in Fig. 3. The model is also validated with the experimental result is shown in Fig. 4. The proposed model exhibits a close agreement with NEGF simulation and experimental data in subthreshold region. The proposed model is deviating after $V_{gs} = 0.17$ V for NEGF simulation data and after $V_{gs} = -0.35$ V for Experimental

TABLE 2. Relevant parameters of monolayer MoS_2 considered in this work.

Parameters	Asymmetric FET [7]	Symmetric FET [8]
Band gap, E_g (in eV)	1.67	1.80
Electron affinity, χ (in eV)	4.28	4.28
Dielectric constant	4.8	4.8
Effective Mass of electron (m_e)	0.467	0.45
Effective Mass of hole (m_h)	0.544	—
Mobility ($cm^2/V.s$)	320	200

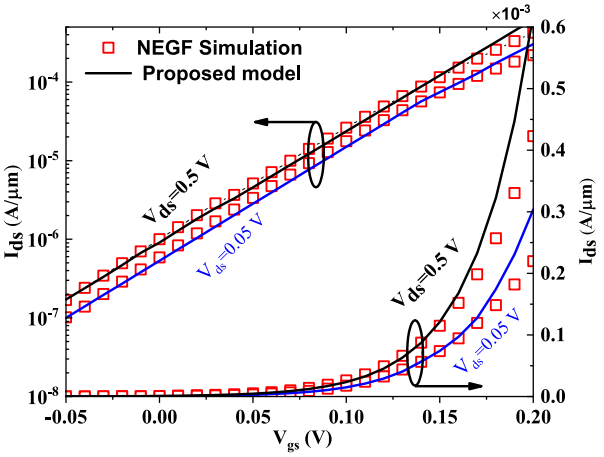

FIGURE 3. Drain current (I_{ds}) versus Gate to source bias (V_{gs}) for different drain to source bias, V_{ds} with front and back gate oxide as HfO_2 with an equivalent oxide thickness of 0.41 nm.

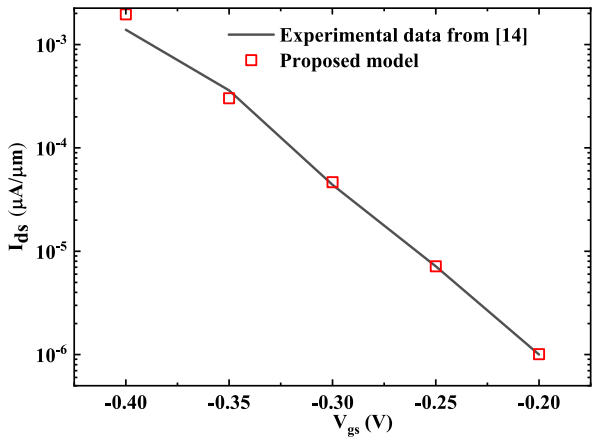

FIGURE 4. Drain current, (I_{ds}) versus Gate to source bias, (V_{gs}) for back gate, (V_{gb}) = -40 V and drain to source bias, V_{ds} = -0.05 V with channel length, L_{ch} = 9.4 μm, front and back gate oxides are ZrO_2 (T_{fox} =17.5 nm, k_{fox} = 12.5) and SiO_2 (T_{box} = 270 nm, k_{box}= 3.9) respectively.

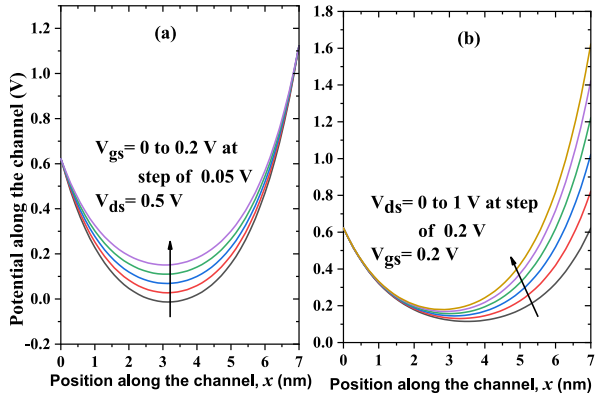

FIGURE 5. (a) Channel potential, $\psi_c(x)$ versus position along the channel, (x) for different (V_{gs}) with $V_{ds} = 0.5\ V$, (b) Channel potential, $\psi_c(x)$ versus position along the channel, (x) for different (V_{ds}) with $V_{gs} = 0.2\ V$.

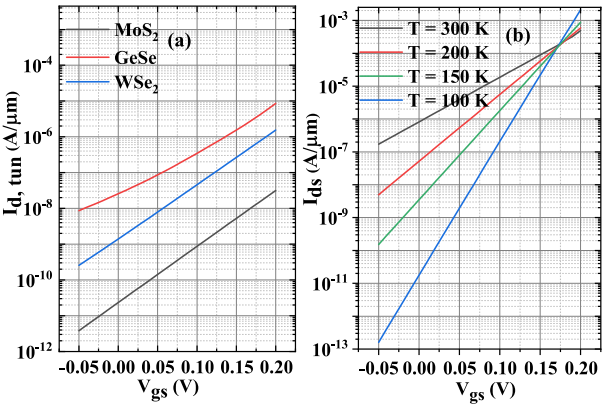

FIGURE 6. (a) Drain to source tunneling current ($I_{d,tun}$) versus Gate to source bias (V_{gs}) for different materials (MoS_2, $GeSe$, WSe_2),(b) Drain to source current, I_{ds} versus Gate to source bias (V_{gs}) for different temperatures, with $V_{ds} = 0.5\ V$. Front and back gate oxide is HfO_2 with an equivalent oxide thickness of 0.41 nm.

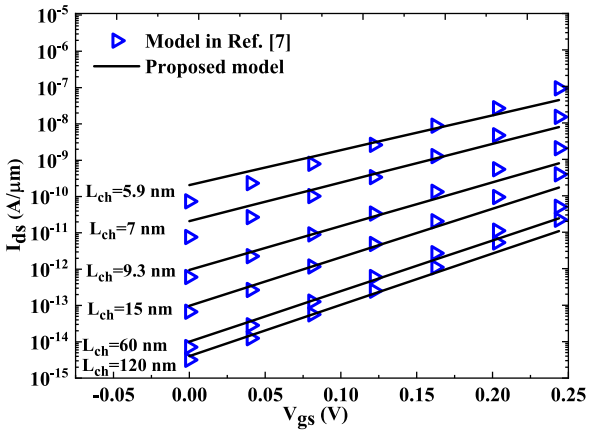

FIGURE 7. Drain current (I_{ds}) versus Gate to source bias (V_{gs}) for different channel lengths with V_{ds}=0.64 V, front gate oxide is HfO_2 with an equivalent oxide thickness of 0.41 nm.

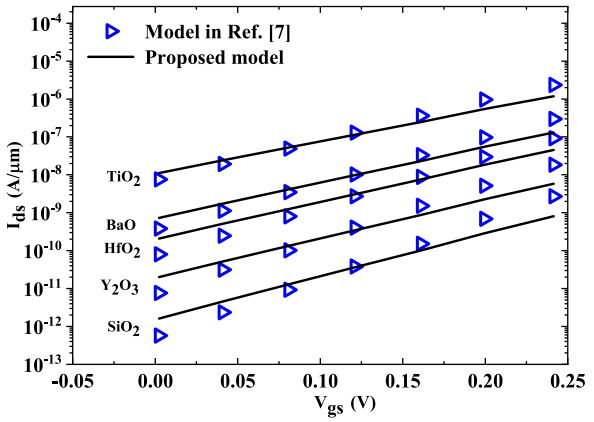

FIGURE 8. Drain current versus gate to source bias for different gate dielectric materials, SiO_2 (k=3.9ε_0),Y_2O_3 (k=15ε_0), HfO_2 (k=25ε_0), BaO (k=33ε_0) and TiO_2 (k=50ε_0) with an EOT of 0.41 nm and V_{ds}=0.64 V.

data (as WSe_2 p-FET is chosen), this is because of $I_{ds} - V_{gs}$ characteristics obtained from NEGF simulation and Experimental data enter to region other than subthreshold after $V_{gs} = 0.17\ V$ for NEGF simulation and $V_{gs} = -0.35\ V$ for experimental data respectively. Fig. 5 (a) and (b) depict the channel potential variation with V_{gs} at $V_{ds} = 0.5\ V$ and with V_{ds} at $V_{gs} = 0.2\ V$ respectively. The tunneling current, $I_{d,tun}$ with respect to V_{gs} for different materials MoS_2 ($E_g = 1.8\ eV$, $me = 0.45$) [8], $GeSe$ ($E_g = 1.3\ eV$, $me = 0.2$) [18] and WSe_2 ($E_g = 1.6\ eV$, $me = 0.33$) [19] is shown in Fig. 6 (a). Fig. 6 (b) depicts the transfer characteristics of MoS_2 FET at different temperatures. By observing Fig. 6 (b), it can be inferred that Zero temperature coefficient (ZTC) occurs at $V_{gs} = 0.14\ V$. Fig. 7 depicts the comparison of our model against the model available in [7]. It can be observed that our model shows a close proximity with the model of [7] for different channel lengths from 5.9 nm (short channel) to 120 nm (long channel) in the subthreshold region. As the model is developed for the subthreshold region, so V_{gs} is kept below 0.25 V. An insignificant difference in OFF current is noted for channel length of 5.9 nm. This is observed because back gate fringe field effect has been considered in our model. Fig. 8 confirms that our model can accommodate different dielectric materials. Here, the dielectric materials considered are, $SiO_2(k_{fox} = 3.9\varepsilon_0)$, Y_2O_3 ($k_{fox} = 15\varepsilon_0$), HfO_2 ($k_{fox} = 25\varepsilon_0$), BaO ($k_{fox} = 33\varepsilon_0$) and TiO_2 ($k_{fox} = 50\varepsilon_0$).

The output resistance (R_{out}) is a significant parameter for analog applications. Fig. 9 shows the variation of R_{out} with drain to source bias (V_{ds}). It can be observed that our model and model in [7] are matched till $V_{ds} = 0.2\ V$. This is because our model is valid in subthreshold region with $V_{gs} < 0.2\ V$. Model in [7] overestimates the value of R_{out} for $V_{ds} \geq 0.2\ V$.

From Fig. 10 it is evident that Model in [7] does not track the variation in back gate dielectric thickness whereas the effect of back gate is included in our model. This is the limitation of the model in [7]. In our proposed model, the characteristics length is increasing with back gate oxide thickness and that will further impact the electrostatics of the device under consideration. The comparison of Characteristic length with [7], [8] is shown in Fig. 11. It is observed that

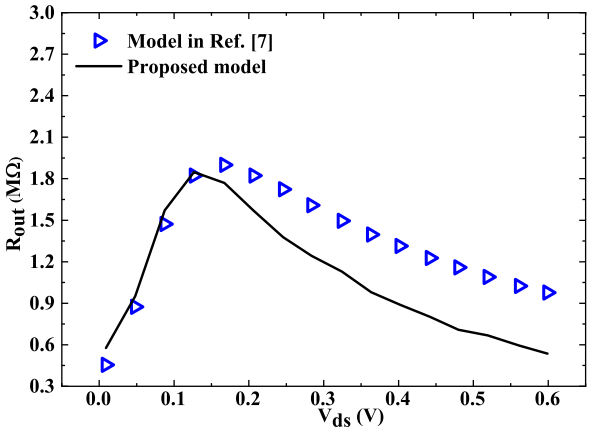

FIGURE 9. Comparison of output resistance for proposed model with model data of [7] under V_{gs}=0.3 V, front gate oxide is HfO_2 with an equivalent oxide thickness of 0.41 nm.

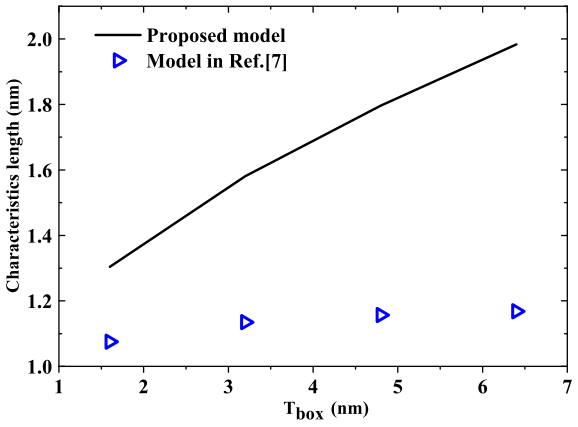

FIGURE 10. Plot of Characteristic length versus back gate oxide thickness (T_{box}) with HfO_2 as front gate oxide having thickness of 2.63 nm.

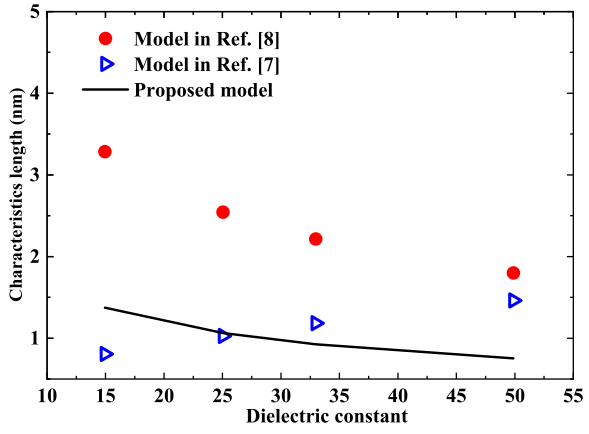

FIGURE 11. Plot of characteristic length versus different front gate dielectric materials with T_{fox} of 2.63 nm (i.e., For symmetric structure, both front and back gate dielectric materials are the same and simultaneously varied).

characteristic length obtained in our model, model of [7] are all below 1.5 nm for different high-κ front gate dielectric cases. Model in [8] clearly is less scalable than others because

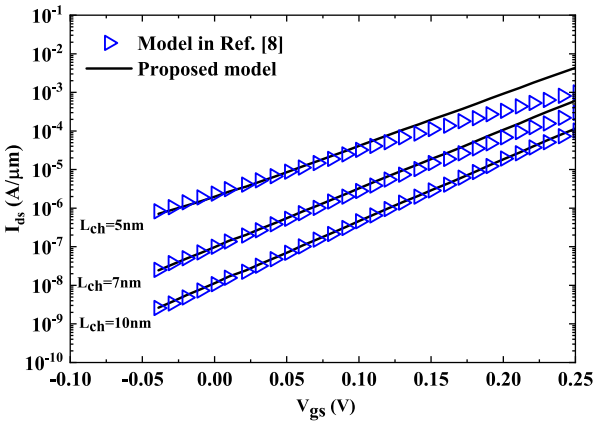

FIGURE 12. Drain current (I_{ds}) versus gate to source bias (V_{gs}) for different channel lengths and comparison with model data in [8] with HfO_2 as gate oxide having an EOT of 0.31 nm and V_{ds}=0.4 V.

the characteristic length reported is higher than other cases. Higher-k dielectric reduces the characteristics length for our model and in [8]. This points out the requirement of high-κ dielectric for oxides in ultra short channel regime. Further, an inverse trend is observed for the data reported in [7] pointing the usage of low-k dielectric materials which is not supported by existing literatures.

Fig. 12 shows the comparison of transfer characteristics with model reported in [8]. Some deviation is observed for the proposed model in comparison to the data obtained by model in [8] for channel length of 5 nm above a V_{gs} of 0.15 V. However, nice agreement is observed for channel length greater than 5 nm. This deviation happens for short channel length because of the characteristic length expression in our model includes both front and back gate fringing effects which is inaccurately modeled in [8]. Fig. 13 shows a good matching of transfer characteristics for lower V_{gs} ($\leq$ 0.2 V) and starts deviating for higher V_{gs} and gate oxide thicknesses. As thickness is increasing, our model and model in [8] starts deviating

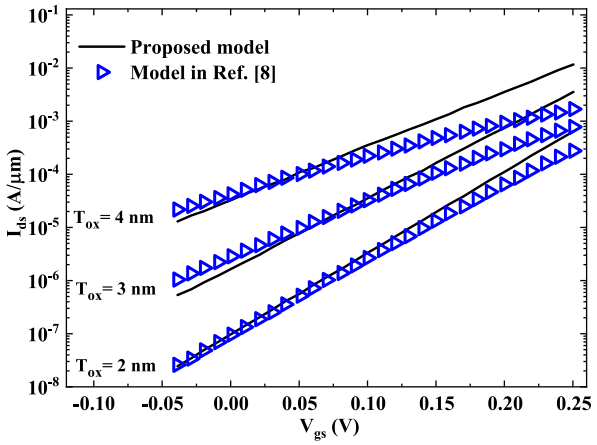

FIGURE 13. I_{ds} versus V_{gs} plot for different front and back gate oxide thicknesses and comparison with model in [8] with HfO_2 as gate oxide having an EOT of 0.31 nm, V_{ds}= 0.4 V and L_{ch}=7 nm.

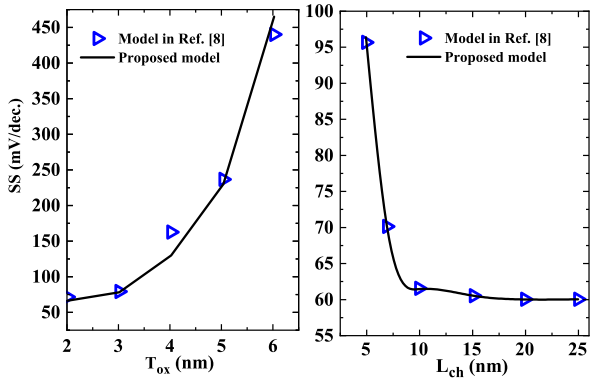

FIGURE 14. Comparison of Subthreshold swing (*SS*) versus (a) oxide thickness (T_{fox}).

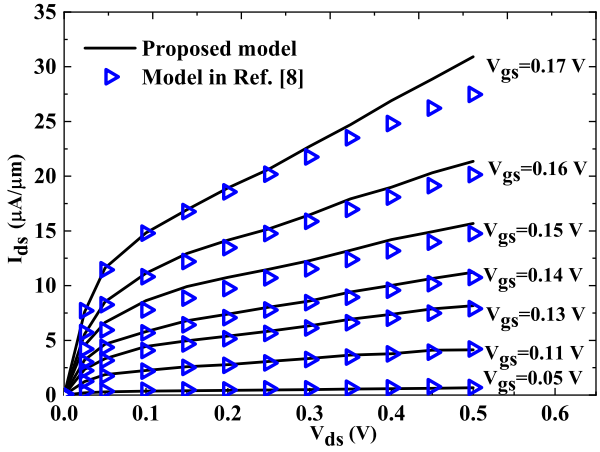

FIGURE 15. Output characteristics of monolayer TMD FET with HfO_2 as gate oxide having an EOT of 0.31 *nm* and with a channel length of 7 *nm*.

after certain V_{gs}. It is also observed that the trend in [8] leaves subthreshold region (saturation behaviour is observed) at $V_{gs} \geq 0.15\ V$ and $V_{gs} \geq 0.10\ V$ for $T_{ox} = 3\ nm$ and $4\ nm$ respectively.This behaviour is not expected at such a low V_{gs}. In our case, the trend does not show any saturation behaviour, which depicts that TMD FET remains in subthreshold region below $V_{gs} = 0.2\ V$.

A comparison of subthreshold swing (SS) for different channel lengths and oxide thicknesses with Model in [8] is shown in Fig. 14((a),(b)). It shows a good conformity with the model in [8]. The comparison of output characteristics is shown in Fig. 15. A critical observation depicts that our model shows lower output resistance at higher V_{gs} which is because of proper consideration of fringing effect in the model. So the developed model is scalable and we have shown good matching from ultrashort channel length of 5 nm to long channel of 120 nm channel length. However theoretically our model is applicable till $2\lambda = 3\ nm$. The model developed is universal as it can be applied for both asymmetric and symmetric gate structure. The model is not only confined to TMD materials like MoS_2, WSe_2, $MoSe_2$, WTe_2 etc., but also applicable for other $2-D$ materials like Graphene, Silicene etc.

IV. CONCLUSIONS

A compact analytical I-V model is presented for an asymmetric, dual gate, monolayer $2-D$ Transition metal dichalcogenide field effect transistor in the subthreshold region. The model includes the effect of source to drain tunneling and gate dielectric fringing effects. The model is methodically derived for an asymmetric, dual gate structure. The model developed is well extended into a symmetric dual gate structure also. The characteristic length expression has dependence only on physical and dimensional parameters and includes the contribution of fringing effects from both front and back gate dielectric materials. The model is validated with simulation results obtained using NEGF based nanodevice simulator [13] and experimental data in [14]. Also, transfer characteristics, output characteristics, subthreshold swing and output resistance are compared with reported literatures of both asymmetric [7] and symmetric structures [8]. A close conformity is observed with some disparity arising because of the non-inclusion of back gate dielectric fringing field effects and source to drain tunneling [7], [8]. The model can well adapt to the effects of different high-κ dielectric materials and its thicknesses. The model is shown to be scalable from ultrashort channel regime to long channel regime. Finally, the model is not confined to only $2-D$ TMD materials but applicable for any arbitrary $2-D$ materials also.

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