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60-V Non-Inverting Four-Mode Buck–Boost Converter With Bootstrap Sharing for Non-Switching Power Transistors

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ABSTRACT This paper presents a non-inverting buck–boost converter for high-voltage automotive applications. The converter includes a newly proposed controller chip and four off-chip NMOS power transistors with two bootstrap capacitors. Conventional non-inverting buck–boost converters have two operation modes: the buck and boost modes. This study implements four operation modes for smooth transition between these modes. In converters with four operation modes, non-switching high-side power transistors require continuous high gate-driving voltages without the bootstrapping operation. The designed non-inverting buck–boost converter drives non-switching high-side NMOS transistors through the proposed bootstrap-sharing technique. A new current sensing technique is also proposed that works reliably under high-voltage operating conditions. This current sensing enables the converter's modulation scheme of the current programmed control. The proposed converter was fabricated using a 0.18 μm BCD 1P4M process. The total chip area is $2.50 \times 2.50\ mm^2$, including the bonding pads. The output voltage range is from 1.05 to 60 V, with a typical input automotive battery voltage of 14 V. Because the automotive battery exhibit a wide voltage fluctuation, the input voltage range is designed from 7 to 60 V. Its switching frequency range is from 600 to 1000 kHz and the maximum power efficiency is 96.1% at a load current of 1.5 A.

INDEX TERMS Buck–boost converter, current mode, bootstrap sharing, current sensing.

I. INTRODUCTION

Power converters are an important aspect of electronic systems owing to their high power conversion efficiency, especially for battery-operated systems. Among the various power converter architectures, non-inverting buck–boost converters are becoming vital for wide input voltage ranges [1]–[7]. For low-voltage portable devices, non-inverting buck–boost converters are important for maximizing the use of discharged battery voltage [8]–[12].

The demand, and therefore the market for high-voltage power converters is rapidly increasing. The automotive electronics market is among the fastest growing markets, and efficient power conversion is important for supplying power to automotive batteries [13]–[15]. Automotive batteries experience an extremely wide voltage variation due to their use in car starters and load dump conditions. Their voltage can rise to more than 100 V in less than a second. A clamped load-dump limits the peak voltage below 40 – 60 V [16]. Therefore, to be effective, power converters for automotive applications should be designed for an input voltage range of at least 40 – 60 V [17], [18]. This paper proposes a non-inverting buck–boost converter that uses automotive battery as a power source. The designed converter is applicable to a wide range of unidirectional power conversion applications such as light emitting diode (LED) headlamps, navigation, and displays [19]–[21].

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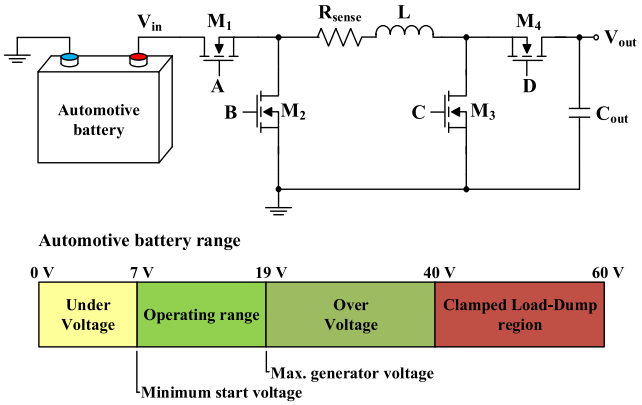

FIGURE 1. Non-inverting buck–boost converter with high-side NMOS switches.

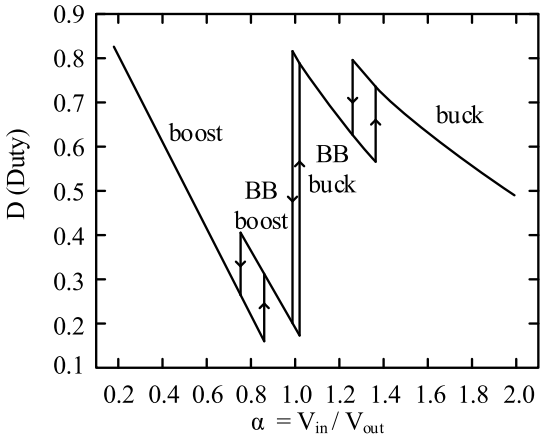

FIGURE 2. Operation ratio.

Non-inverting buck–boost converters are essential in generating a stable output voltage. However, the design of the converters becomes challenging for high-voltage applications, and the bipolar-CMOS-DMOS (BCD) process should be used to handle the high-voltage range. Most of the current non-inverting buck–boost converters are designed for low-voltage mobile products, and they use the standard CMOS process. Recently, the first published results for a high-voltage buck–boost controller circuit were introduced in [18], but a thorough discussion of this circuit has not been published yet. This paper demonstrates the operation of a non-inverting buck–boost converter operating up to 60 V and provides details of the proposed control schemes for the four switches. Most of the earlier publications on positive buck–boost converters were designed for low-voltage operation below 5 V, and they have only two or three operation modes. This paper discusses the bootstrap sharing for high-voltage, four-mode circuits, which require high-side NMOS transistors.

Fig. 1 shows the basic components of the converter without the details of the duty controller. It also shows the input voltage range of the converter, which can be up to 60 V under load dump conditions [16]. The designed converter can operate for this wide range of input voltages, and changes the operation mode accordingly.

All four switches are implemented using off-chip NMOS power transistors. Because NMOS high-side switches are used, bootstrapping circuits are also implemented for high-side gate drivers. A small series resistor is connected to the inductor for current sensing. Conventional buck–boost converters have two operation modes: buck and boost mode [10], [22]. However, when the input and output voltage levels are close, duty control becomes very sensitive to small noise. Thus, the controller for the three operation modes is designed for intermediate input and output voltage boundaries [23], [24]. The four operation modes are designed to solve the problem of ambiguous control boundaries [9], [25]. This control method provides stable duty control even when the input voltage approaches the output voltage.

A standard CMOS implementation using PMOS power transistors for high-side switches is straightforward because the PMOS switch can be turned on by driving 0 V to the gate. When the supply voltage is 5 V or less, the complete converter, including the controller, can operate at the single supply voltage [8]–[10]. However, if the system operates from higher power supply voltages, the implementation of the controller circuit becomes more complicated. Level shifters are usually required, and the high-side switches are commonly implemented using the NMOS transistors instead of the PMOS transistors [26]. Because the high-side NMOS transistor must be controlled at a higher voltage than the supply voltage, the capacitive bootstrap driving is implemented through the switching operation of the power stages [26], [27]. When the positive buck–boost converter operates in two modes, this issue does not pose a significant design challenge; since all four power transistors turn on and off in one switching period, conventional bootstrapping can be used. However, the four-mode operation requires certain high-side transistors to be turned on at all times in some operation modes, which is explained later in Fig. 3.

This condition requires a technique to maintain the voltage level of the non-switching high-side power transistors in four-mode buck–boost converters. This paper proposes a new bootstrap-sharing scheme to solve this issue. The remainder of this paper is organized as follows. Section II describes the operation of the four-mode non-inverting buck–boost converter and its implementation issues. Section III discusses the details of the circuit implementation, including the proposed bootstrap-sharing technique. The measurement results are provided in Section IV, and conclusions are drawn in Section V.

II. BUCK–BOOST CONVERTER OPERATION

The designed non-inverting buck–boost converter has four operation modes to control the four switches shown in Fig. 1. The conventional buck mode or boost mode is used when there are large differences between the input and output voltages. Fig. 2 shows the operation modes and theoretical

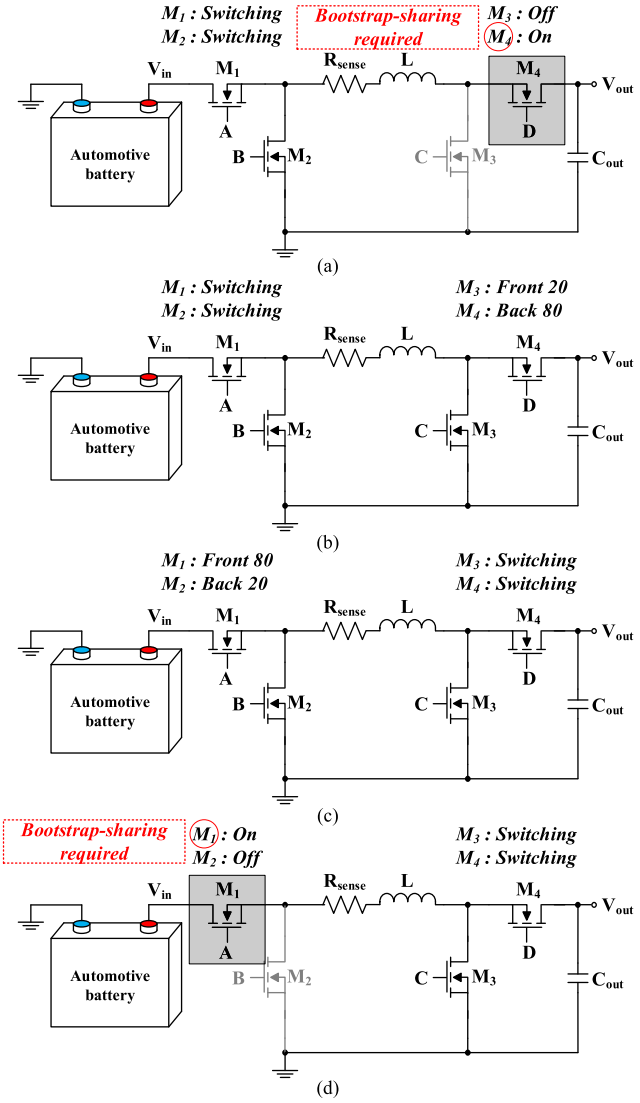

FIGURE 3. Operation switches of the (a) buck mode, (b) BB-buck mode, (c) BB-boost mode, and (d) boost mode.

duty ratio. When the input and output voltages are close and the ratio is approximately one, the third or fourth operation modes are activated, which are the buck–boost buck (BB-buck) mode and the buck–boost boost (BB-boost) mode, respectively. The ratio of V_{in} and V_{out} is defined as α.

$$\alpha = \frac{V_{in}}{V_{out}} \tag{1}$$

The mode is determined by the input and output voltage ratio, with hysteresis to prevent chattering. As shown in Fig. 2, the mode change from buck to BB-buck requires a ratio α of 1.25, while the mode change from BB-buck to buck requires α of 1.35.

$$Hysteresis \begin{cases} \alpha > 1.35 & (\text{BB-buck} \rightarrow \text{buck}) \\ \alpha < 1.25 & (\text{buck} \rightarrow \text{BB-buck}) \end{cases} \tag{2}$$

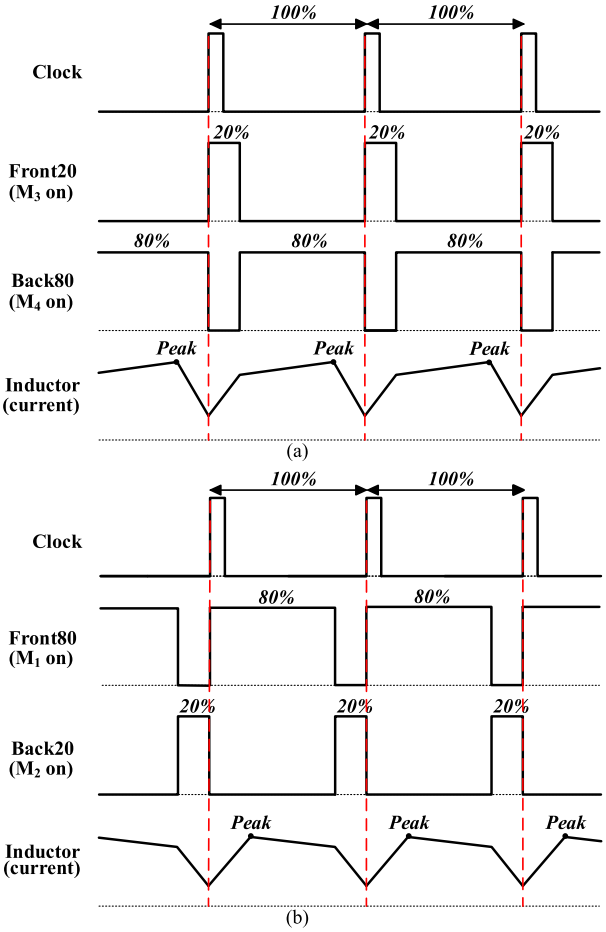

FIGURE 4. Duty cycle of the (a) BB-buck mode, and (b) BB-boost mode.

When the converter is in BB-buck mode, α should be lower than 0.98 to change the mode to BB-boost. Similarly, the mode change from BB-boost to BB-buck requires a larger α than 1.02, owing to hysteresis.

$$Hysteresis \begin{cases} \alpha > 1.02 & (\text{BB-boost} \rightarrow \text{BB-buck}) \\ \alpha < 0.98 & (\text{BB-buck} \rightarrow \text{BB-boost}) \end{cases} \tag{3}$$

A mode change between the BB-boost and boost modes is also activated via hysteresis, as shown below.

$$Hysteresis \begin{cases} \alpha > 0.85 & (\text{boost} \rightarrow \text{BB-boost}) \\ \alpha < 0.75 & (\text{BB-boost} \rightarrow \text{boost}) \end{cases} \tag{4}$$

Fig. 3 shows the four operation modes with their switch configurations [9], [25]. For high power conversion efficiency, NMOS power transistors are used as high-side switches. Fig. 3(a) and (d) show the buck and boost configurations, respectively. The buck configuration is identical to the conventional buck with the M_4 switch set to the *on* state, while M_3 is set to the *off* state. Since the M_4 switch should always be on without switching for buck operation, the conventional bootstrapping scheme cannot be used for this switch. Therefore, a novel scheme should be developed

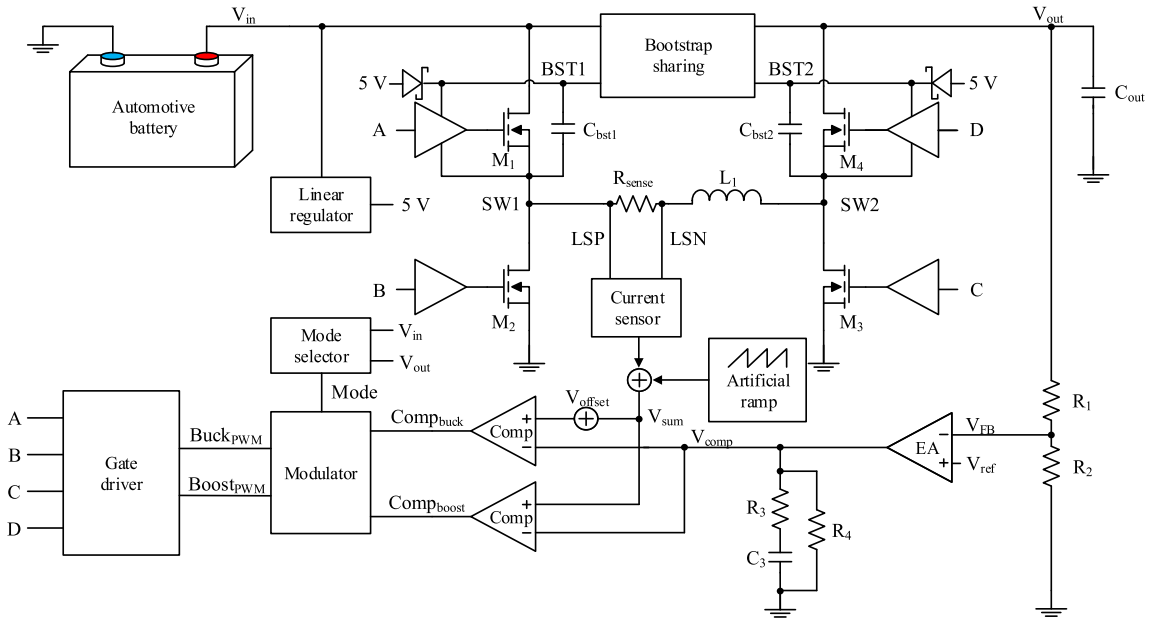

FIGURE 5. Non-inverting buck–boost converter architecture.

to maintain a high gate driving voltage for this switch. The same issue arises for the M_1 switch in boost mode. To effectively drive these switches, a bootstrap-sharing technique is developed. The bootstrap-sharing technique ensures that the switch remains *on* at all times in buck and boost modes.

For the intermediate boundary region, where the input voltage is slightly higher than the output voltage, all switches turn on and off with appropriate duty controls. Fig. 4(a) shows the control signals for the M_3 and M_4 switches. M_3 is set to *on* with a fixed 20% duty cycle at the beginning of each cycle, which is controlled by the Front20 signal. Similarly, the Back80 signal represents the last 80% of each cycle and turns on the M_4 switch for that time period. Slightly different values of the duty ratio for these control signals can be used to implement the four-mode buck–boost converter. The decisions pertaining to the duty ratio of these control signals are analyzed in [25]. M_1 turns on at the beginning of each cycle via the clock signal, as in conventional buck converters. Toggling of the M_1 and M_2 switches occurs during the Back80 time period via the buck controller's feedback loop. Fig. 3(c) shows the configuration of the BB-boost mode. Switches M_1 and M_2 operate with the duty cycles, as shown in Fig. 4(b). Switches M_3 and M_4 are toggled during the Front80 time period via the boost control loop.

This four-mode buck–boost operation was demonstrated in [9] for low-voltage applications using CMOS (two NMOS and two PMOS) switches. The high-voltage buck–boost circuit was recently demonstrated in [18], but the details of the circuit description are limited. Our paper provides solutions for four-mode operation using the BCD process.

III. BUCK–BOOST CONVERTER IMPLEMENTATION

Fig. 5 shows the architecture of the designed buck–boost converter. The four NMOS switches, an inductor, a sensing resistor, and an output capacitor are used as off-chip components, as shown in Fig. 1. The two Schottky diodes and C_{bst1} and C_{bst2} capacitors are also off-chip components for the bootstrapping operation, which are used to power the high-side NMOS switches. The other components constitute the controller part. The on-chip linear regulator generates a 5 V supply voltage for the controller part and the bootstrapping circuits.

The controller generates a pulse-width modulation (PWM) signal to control the duty ratio of the power converter. Two control schemes are widely used for generating the PWM signal: the voltage mode control and current mode control [28]. In this design, the current mode control is used for a fast feedback response [29]. Based on the input and output voltage levels, one of the four operation modes of the buck–boost converter is selected by the mode selector circuit. The feedback voltage (V_{FB}) is connected to the error amplifier (EA), and the reference voltage (V_{ref}) is connected to another input. The error amplifier and compensation R-C network generate the (V_{comp}) signal, which determines the duty ratio of the converter by the comparator. The positive input of the comparator results from the summing circuit of the sensed current signal and the artificial ramp as in the common current-mode controllers. The current flowing through the inductor is sensed by the voltage drop of the sense resistor (R_{sense}). The controller consists of two control loops. The buck and BB-buck modes are controlled via the $Comp_{buck}$

path, while the boost and BB-boost modes are controlled via the $Comp_{boost}$ path.

The basic operation principle of the converter is similar to that of common low-voltage buck–boost architectures. In addition, the importance of an artificial ramp is well documented in the literature [28]. The designed buck–boost converter is used for high-voltage applications; thus, it differs considerably from low-voltage converters. The circuit design examples of the level shifters and bootstrapping can be found in [26]; therefore, the details are not described in this paper.

Three key issues are addressed in this study. The first is the duty control scheme when the operation mode changes. The second is the bootstrap-sharing scheme to drive a high-side NMOS switch that is always turned on during certain operation modes. The third is the high-voltage current sensing scheme for buck–boost operation. The circuits for the three key issues are explained below. Other important blocks that constitute the converter are also explained.

A. MODE SELECTION AND DUTY CONTROL

As shown in Fig. 2, the operation mode is determined by the ratio of the input and output voltages. The mode selector in Fig. 5 compares the boundaries of the input and output ratios with those of the comparators. The built-in hysteresis removes the possibility of chattering, which is the frequent toggling of modes when the ratio is at the mode boundaries. This block generates a mode signal that selects either the buck or boost loop as the feedback loop. Furthermore, the switch operations are controlled depending on the mode as shown in Fig. 3.

A DC offset voltage V_{offset} is added, depending on the mode selected. The EA has an off-chip compensation capacitor, and the capacitor voltage V_{comp} is compared with the current sensing signal. As shown in Fig. 2, when the operation mode changes, the duty cycle experiences a steep jump. The V_{comp} level should change instantly when the smooth mode changes, but it is impossible to charge the compensation capacitor instantly because of the limited bandwidth of the feedback loop. Therefore, instead of changing the capacitor voltage, the DC offset voltage is added to the V_{sum} signal, as shown in Fig. 5.

B. PROPOSED BOOTSTRAP SHARING

Fig. 6 shows two possible choices for power switch implementation. It is assumed that the gate drivers operate at 5 V, as in common LDMOS power transistors [26]. Fig. 6(a) shows a case in which a high-side PMOS transistor is used. In low-voltage applications under 5 V, the gate of a high-side PMOS transistor can be pulled down to 0 V to turn on the switch. This makes it simple to design the gate driver in this case using standard CMOS circuits.

Fig. 6(b) shows the case with a high-side NMOS transistor. To turn on the high-side NMOS, the gate driver should operate at a higher supply voltage than V_{in}. High-side NMOS power transistors are commonly used in high-voltage power converters. The high-side NMOS transistor requires a bootstrapping circuit that includes an off-chip diode and a capacitor [26], [27]. As shown in Fig. 5, the bootstrap capacitors (C_{bst1} and C_{bst2}) are charged to 5 V when the switching nodes (SW1 and SW2) are pulled down to 0 V. When the switching nodes are pulled up, the capacitor voltages are boosted to high-voltages and power the high-side transistors. The common high-voltage buck or boost converters operate with this conventional bootstrapping scheme.

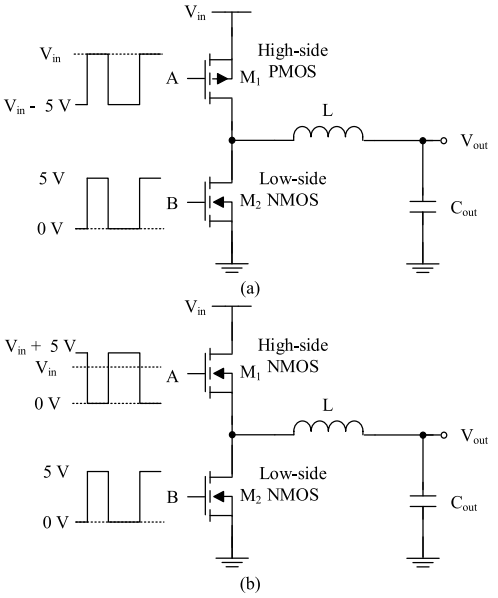

FIGURE 6. Buck mode switches: (a) High-side PMOS, (b) High-side NMOS.

However, in high-voltage four-mode buck–boost converters, high-side switches are always required to be *on* in certain operation modes. Figs. 3(a) and (d) show such cases. The M_4 transistor in Fig. 3(a) and M_1 transistor in Fig. 3(d) should always be turned on in their respective operation modes. The conventional bootstrapping scheme requires switching of the power transistors, and a special technique needs to be used for non-switching high-side power transistors. The proposed bootstrap-sharing technique allows the current to flow from the active bootstrapping capacitor to the inactive bootstrapping capacitor. For example, when the converter is in buck mode, as shown in Fig. 3(a), the C_{bst2} capacitor shown in Fig. 5 is charged by sharing the bootstrap operation of C_{bst1}. The voltage level of the inactive bootstrap capacitor is sensed; if the level drops below the low boundary, the bootstrap-sharing circuit is enabled, thus allowing the current to flow.

Fig. 7 shows the proposed bootstrap-sharing circuit, which has two voltage sensing circuits and two current control circuits. A separate pair is used for each set of bootstrapping circuits. Two diodes are used to supply voltage to each high-voltage node (HV1 and HV2). A higher voltage is supplied to the HV node through the forward-biased diode, and another diode blocks the voltage in reverse mode. As there are two HV nodes in Fig. 7, a total of four diodes are used for the two HV

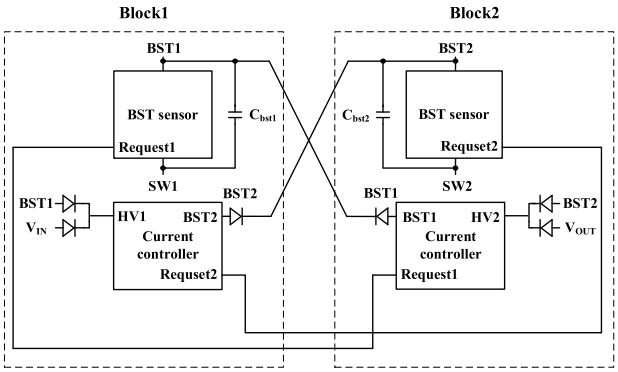

FIGURE 7. Proposed bootstrap-sharing circuit.

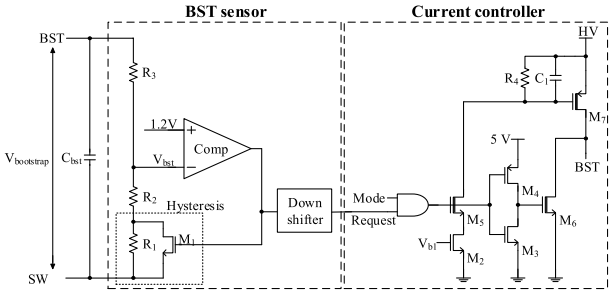

FIGURE 8. BST sensor and current controller.

nodes. The BST1 and BST2 nodes are the bootstrap capacitor (C_{bst1} and C_{bst2}) voltages, which are shown in Fig. 5. The BST sensor senses the voltage level of the capacitor. If the voltage of the non-switching BST block drops below the low boundary, the charge is supplied from the switching BST block by the current controller. A diode is located in each bootstrap-sharing path to supply power in one direction and to protect the reverse current.

The schematics of the BST sensor and the current controller are shown in Fig. 8. In buck mode, when the high-side switch is always on (see Fig. 3(a)), the voltage level of BST2 shown in Fig. 5 decreases with time. The voltage of the bootstrap capacitor should be maintained using the proposed bootstrap-sharing technique to prevent unwanted turning-off of the switch. Because the high-side driver operates via the power supply rails of the BST and SW, the BST sensor and the current controller operate at the same supply rails. The bootstrap capacitor is located between the BST and SW, so the capacitor voltage can be represented by Equation 5:

$$V_{bootstrap} = BST - SW \tag{5}$$

Normally, the bootstrap voltage is regulated to 5 V using switching operations. The resistor-divided voltage V_{bst} is compared with the reference voltage of 1.2 V by the comparator, as shown in Fig. 8. The hysteresis is implemented by the M_1 transistor. If the bootstrap capacitor is discharged below the reference voltage, the Request signal changes to high logic via the comparator. The Request signal turns on the

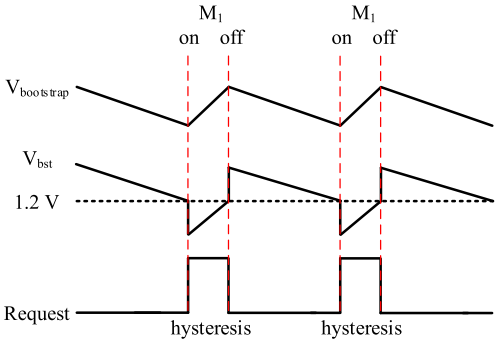

FIGURE 9. BST sense with hysteresis.

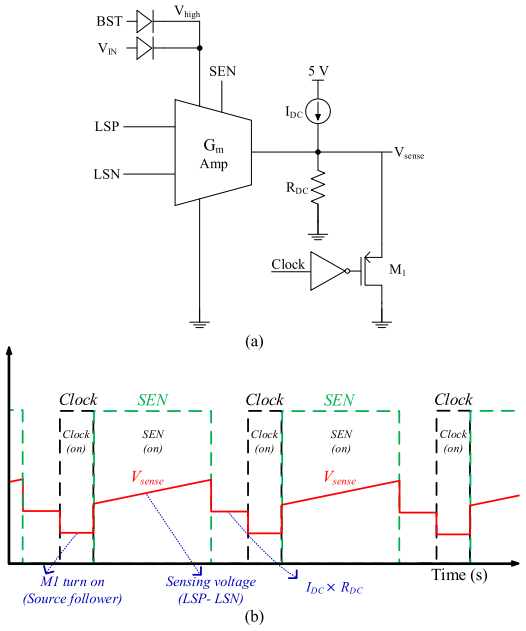

FIGURE 10. Proposed current sensor (a) circuit, and (b) waveform.

M_5 transistor, and the current flows through the R_4 resistor. The voltage drop of R_4 activates the M_7 transistor to enable the current flow from the higher voltage bootstrap capacitor to the lower voltage one.

Fig. 9 shows the waveforms of this process. As $V_{bootstrap}$ decreases, the voltage-divided V_{bst} also decreases. When V_{bst} drops below the reference voltage of 1.2 V, the comparator in Fig. 8 generates a high output. To prevent unwanted chattering of the comparator output due to noise, the hysteresis is implemented by M_1 and R_1. When the comparator's output toggles to a high level, it turns on the M_1 to short the R_1 resistor. Owing to this hysteresis circuit, V_{bst} experiences a sudden voltage drop, as shown in Fig. 9. The comparator output then goes through the down shifter to generate the Request signal.

C. PROPOSED CURRENT SENSOR

The sensing resistor is connected in series with the inductor, and generates a voltage drop proportional to the amount of current. Because the resistor decreases the power conversion efficiency, a small resistance should be used. Therefore,

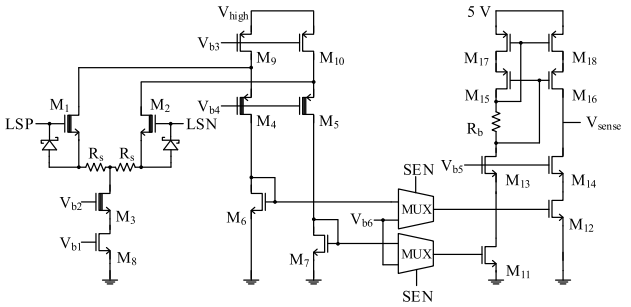

FIGURE 11. Current sensing G_m amp circuit.

the voltage drop across the sensing resistor also becomes small, while significant switching noise surrounds the sensing circuit. There are two difficulties in designing a current sensor for such a hostile environment. The first is the high-voltage. The high-voltage nature of the converter makes it difficult to use compact and high-speed CMOS transistors. To address this issue, high-voltage transistors should be used; and the parasitic capacitors of these transistors degrade the speed of the sensing circuit. Conventional sensing circuits use a feedback technique for accurate and fast operation. The high-voltage interface does not allow for a simple connection between the feedback components, and a sufficient bandwidth of the feedback loop is not easy to achieve because of its the parasitic nature. The second difficulty is the rejection requirement of the common-mode fluctuation during the switching operation. Since the terminal voltages of the inductor and the series-connected sense resistor fluctuate from 0 V up to 60 V, the input signals (LSP and LSN in Fig. 5) to the current sensor have the same voltage fluctuation.

The supply voltage to the current sensor is generated through two diodes, as shown in Fig. 10(a). When the M_1 switch in Fig. 5 is turned on, the left side of the inductor is connected to the V_{in} level, and the inductor current increases.

To ensure that the sensor transistors stay in the saturation region, a bootstrapped voltage (BST), which is higher than V_{in}, is supplied to the current sensor through the diode. When the voltage level of BST is pulled down to 5 V, V_{in} is supplied to the current sensor through another diode. The sense timing signal (SEN) controls the sensing timing and blocks signal transfer when a large voltage fluctuation occurs owing to the on/off operations of the power transistor.

The DC voltage level of V_{sense} is set by the DC current source (I_{DC}) and resistor (R_{DC}). When the clock initiates the PWM operation, the SW node experiences a large fluctuation, and the sensing circuit receives a sudden variation in input voltage. The V_{sense} output also experiences a large fluctuation before it ultimately settles down. The PMOS transistor M_1 operates as a source follower during this fluctuation period, maintaining the output voltage at a constant level. If the clock signal reaches a high level, the gate of the PMOS transistor M_1 becomes 0 V. V_{sense} becomes the DC voltage level, which is the gate-source voltage of the M_1 transistor. After the clock signal toggles to a low level, M_1 turns off and the normal sensing operation begins. The signal waveforms and timing are shown in Fig. 10(b).

The design of the sensing G_m amplifier is shown in Fig. 11. The G_m amplifier has two stages, and the power supply domains are different for each stage. The first stage operates in the high-voltage domain, while the second stage operates in the controller's low-voltage domain. The first stage of the amplifier is based on the folded-cascode architecture. Two source degeneration resistors (R_s) are included to increase the linearity [30].

M_1, M_2, M_4, and M_5 transistors are implemented via high-voltage LDMOS transistors. Because the common-mode voltage levels of the LSP and LSN nodes follow the switching voltage of SW1 in Fig. 5, the input of the sensing circuit experiences fast and large fluctuations. Zener diodes are connected between the gate and source of the M_1 and M_2 transistors to maintain the gate-source voltage below a safe operating range. The sensed current information is transferred to the low-voltage domain through the current mirroring scheme. The SEN signal controls the transfer timing by controlling the multiplexer. Since the output of the G_m amplifier is the current, the current-to-voltage conversion is performed using the resistor R_{DC} in Fig. 10(a).

The overall gain of the current sensor is

$$V_{sense} \approx I_L R_{sense} G_m R_{DC} \tag{6}$$

where I_L is the inductor current and R_{sense} is the sensing resistance in Fig. 5. The output impedance of the G_m amplifier is significantly larger than that of the R_{DC}, so the gain equation only considers R_{DC} for the sake of simplicity.

IV. MEASUREMENT RESULTS

The non-inverting buck–boost converter is implemented using the 1P4M 0.18 μm BCD process. The inductor is 4.7 μH, and the output capacitor is 10 μF. The input voltage ranges from 7 to 60 V, and the output voltage ranges from 1.05 to 60 V. The switching frequency and efficiency are closely related [31]. Consideration this point, the switching frequency is set between 600 kHz and 1 MHz. This allows a non-inverting buck–boost converter to achieve high efficiency.

Fig. 12 shows the load regulation performance with fixed input and output voltages. The load current changes from 0 to 1.5 A, and the AC-coupled output voltage is monitored. The output voltage settles down quickly after the initial sudden variation.

Fig. 13 shows the voltage regulation performance with respect to the input voltage change in a wide range of 7 to 60 V. For this wide input voltage range, the converter experiences all four operation modes. The output voltage is regulated well for all mode changes.

The waveforms for the four operating modes are shown in Fig. 14. The measurement waveforms are for the switching frequency of 1 MHz at 1.5 A load current. With the output voltage set to 17.5 V, the input voltage of 25 V

TABLE 1. Performance Summary and Comparison with Other Buck–Boost Converters.

	[32]	[8]	[33]	[34]	[18]	This Work
Year	2013	2014	2015	2017	2019	2020
Process	0.5 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm BCD	0.18 μm BCD
V_{in} $[V]$	3.3	2.7 – 5.5	2.9 – 4.5	2.5–5.0	4.0 – 60.0	7.0 – 60.0
V_{out} $[V]$	1.8 – 5.0	2.0 – 5.0	3.8 – 5.9	3.3	0.8 – 60.0	1.05 – 60.0
I_{load}(max) $[A]$	0.5	2.0	0.3	0.4	1.5	1.5
f_{sw} $[MHz]$	5	2.5	1	1.66	2	1
L $[H]$	0.2μ	1μ	10μ	1μ	1μ	4.7μ
C_{out} $[F]$	3μ	33μ	4.7μ	10μ	22μ	10μ
Peak Efficiency [%]	90	91	91	98	95	96

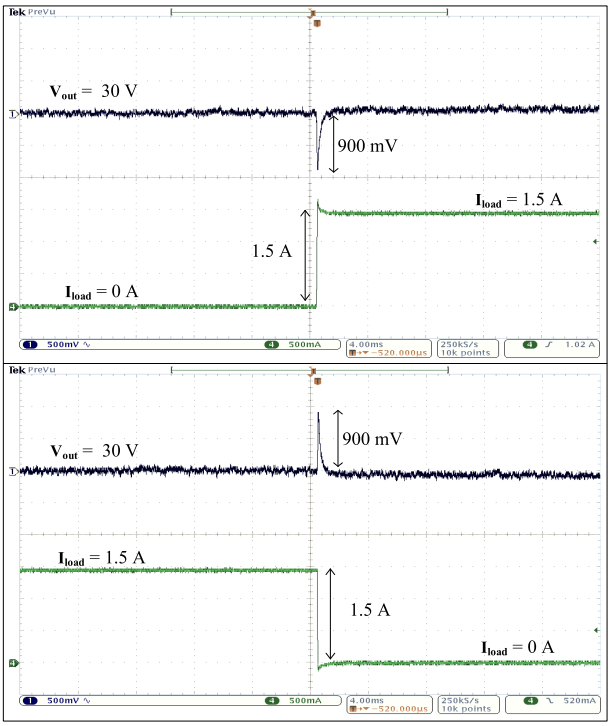

FIGURE 12. Load transition.

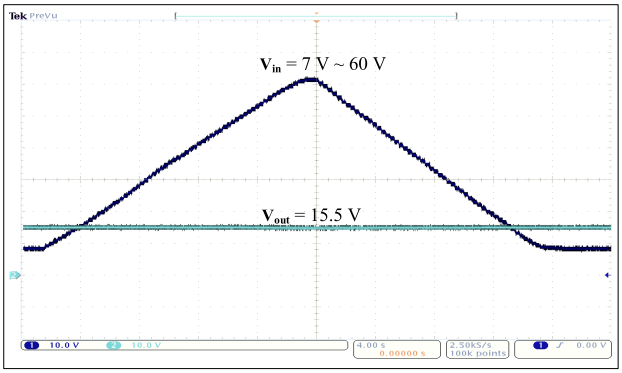

FIGURE 13. Line regulation.

transitions the converter into buck mode. When the input voltage is decreased to 19 V, the input and output voltage difference becomes small, and the converter operates in the BB-buck mode. The measured inductor current exhibits the expected operation mode, as explained in Section II. The other two operation modes are shown in Fig. 14 with different input voltages. When the input voltage decreases to 16 V, the converter enters the BB-boost mode. If the input voltage decreases to 10 V, the converter operates in boost mode. Because the input voltage is significantly lower than the output voltage, the converter operates in the conventional boost mode, requiring only two switches for operation. For the all four operation modes, the test results show that the converter operates up to 1.8 A load current. When the load current is increased to 2.0 A, an unstable inductor current waveform begins to appear in boost mode.

Fig. 15 shows the measured efficiency graph of the designed converter at an output of 17.5 V. The maximum efficiency is 96.1% when the load current is 1.5 A, and the supply voltage is 22 V at a switching frequency of 600 kHz.

A performance comparison is shown in Table 1. Most of the earlier works on non-inverting buck–boost converters were for low-voltage applications. A high-voltage application requires a BCD process, and additional issues arise that have been described in this paper. A BCD circuit was recently introduced in [18], but the authors did not provide a full

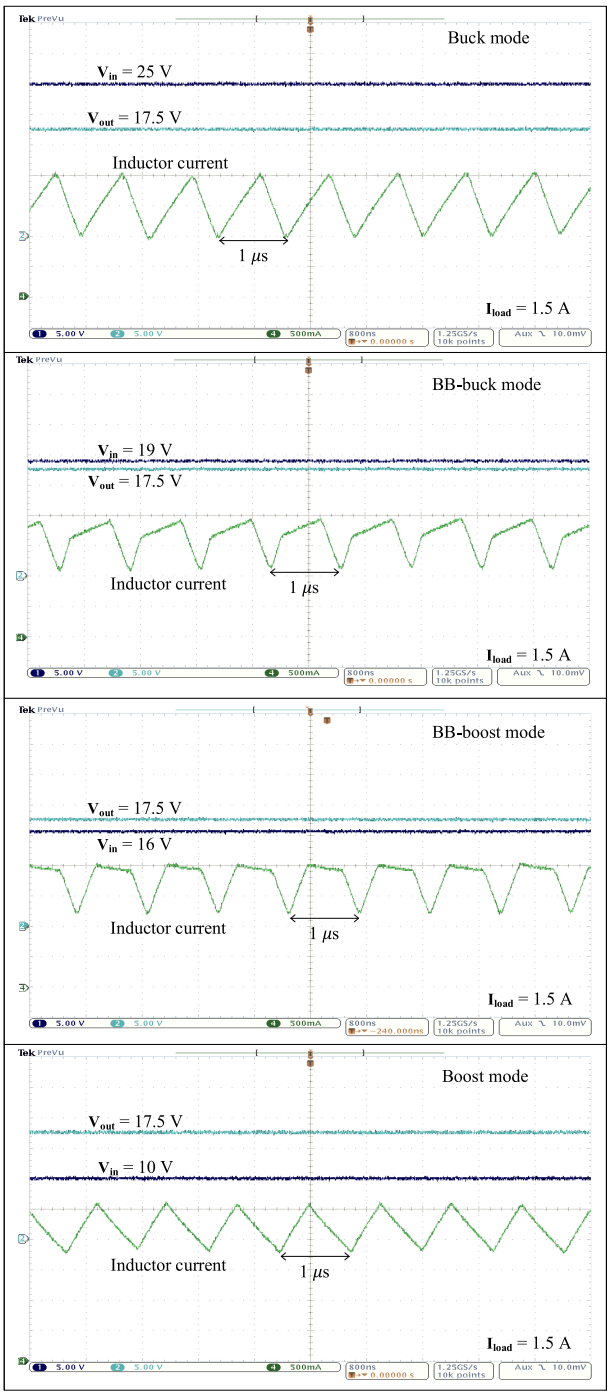

FIGURE 14. Operating mode waveforms.

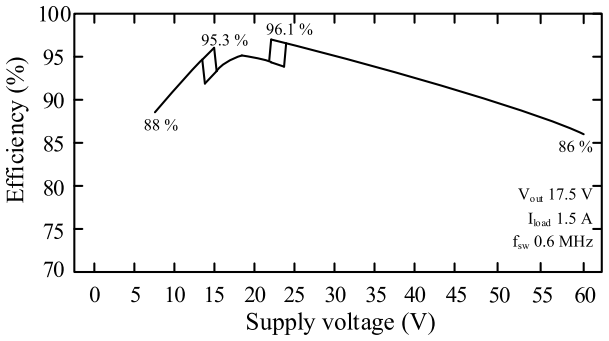

FIGURE 15. Efficiency.

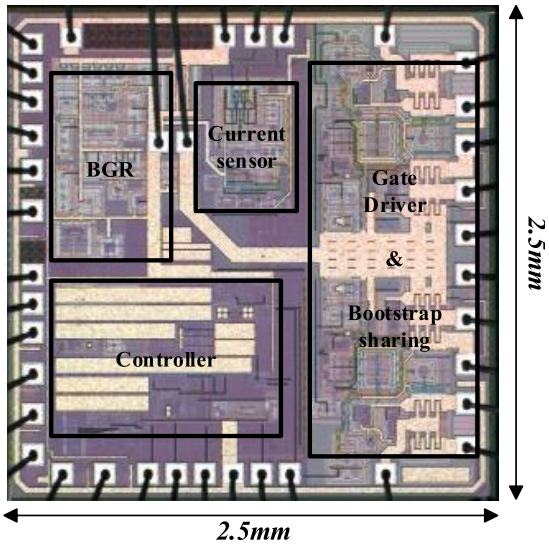

FIGURE 16. Chip micrograph.

description of the circuit. Fig. 16 shows the chip micrograph of the BCD circuit with a die area of 2.50 × 2.50 mm^2.

V. CONCLUSION

In this paper, bootstrap sharing by sensing the voltage level of the bootstrap capacitor has been proposed as a solution to non-switching high-side NMOS transistors. If the level drops below the lower threshold, the switch opens a current path from the switching bootstrap capacitor to the non-switching capacitor to charge the latter. In addition, a new current sensing scheme is proposed to sense the inductor current for the current programmed feedback control. Because the common-mode voltage of the current sensing nodes fluctuates with the wide input voltage range, the proposed scheme operates at the open-loop transconductance amp architecture. The measured peak power conversion efficiency is 96.1% when the load current is 1.5 A and the supply voltage is 22 V at a switching frequency of 600 kHz. The proposed high-voltage buck–boost converter can operate over the entire input range of 7 to 60 V for various high-voltage applications.

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