IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 18, 2020, accepted November 6, 2020, date of publication November 17, 2020, date of current version December 2, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3038583

A Framework for Optimum Determination of LCL-Filter Parameters for N-Level Voltage Source Inverters Using Heuristic Approach

BASEM ALAMRI AND YASSER MOHAMMED ALHARBI
Department of Electrical Engineering, College of Engineering, Taif University, Taif 21944, Saudi Arabia
Corresponding author: Basem Alamri (b.alamri@tu.edu.sa)

This work was supported by the Scientific Research Deanship, Taif University, Saudi Arabia, under Project Number 1-440-6163.

ABSTRACT The use of voltage source multilevel inverters (VS-MLIs) has grown enormously over the last decade, and it is expected that these inverters will be deployed in future power grids (smart grids), especially for medium voltage–high power applications. This paper investigates the application of passive power filters (PPFs) for harmonic mitigation at the output of VS-MLIs for more efficient grid integration of renewable energy sources. It proposes a generic model, using a heuristic approach, for the optimum design of an LCL power filter at the output of VS-MLIs. The proposed model transforms the LCL filter design problem into an optimization problem and applies a genetic algorithm (GA) to solve it. The objective function to be optimized is a multi-objective function based on inverters' total harmonic distortion and energy losses. The optimization problem is subject to applied design constraints. As a main optimization objective, a precise evaluation methodology for the inverter power losses is presented, which was built according to a practical switching device datasheet. The method is applicable to any VS-MLI topology and any number of levels (N). As a case study, the proposed design optimization approach was implemented to optimally design the LCL filter at the output of a grid connected 11 KV, 5 MVA 7-level cascaded H-bridge multilevel invert (CHB-MLI). The IGBT module Device IGBT of type FZ400R65KE3 by Infineon was used for simulation. MATLAB-SIMULINK is used for the modelling and simulation. We found that the proposed design approach is more generic, efficient, and simple to apply than conventional design approaches which requires more system detail, relies more on the designer's experience, and normally does not results in optimum design. The proposed approach is generic and can be applied for different VS-MLIs topologies and for any number of levels (N).

INDEX TERMS DC/AC inverters, LCL filter, power quality, genetic algorithm, multilevel inverter, renewable energy, power conversion, grid integration.

I. INTRODUCTION

The world is facing a real threat from the effect of global warming which is mainly arises because of releasing more greenhouse gases to the atmosphere. As per the Paris climate agreement, signed on December 2015, the world is committed to keep the global temperature rise well below 2 °C. Electricity generation from fossil fuels contributes significantly to the problem of global warming, as it burns carbon fuels producing large amount of carbon dioxide. For this reason, the world is reforming its energy mix with more clean and sustainable power generation from alternative and renewable energy sources. As per the IRENA-2020 report, the newly installed capacity of renewable energy was 176 GW in 2019 [1]. Solar PV accounts for 98 GW of the newly installed capacity, followed by wind power with 59 GW, followed by hydropower and bioenergy, which have increased by 12 GW and 6 GW, respectively. The growth in geothermal energy was just under 700 MW. Figure 1 depicts the renewable share in the annual power capacity growth. This high growth in newly installed generating capacity from renewable energy sources is expected to continue. In addition to growth in global electricity demands, electrification of the transportation sector is considered a key factor in efforts to reduce the levels of greenhouse gas emissions. Hence, much more penetration of PV solar power plants and wind power farms into future power grids is expected.

Power utility grid integration of medium- and large-scale PV and wind power plants is accomplished via power electronics inverters and converters, which are considered a major

The associate editor coordinating the review of this manuscript and approving it for publication was Tariq Masood.

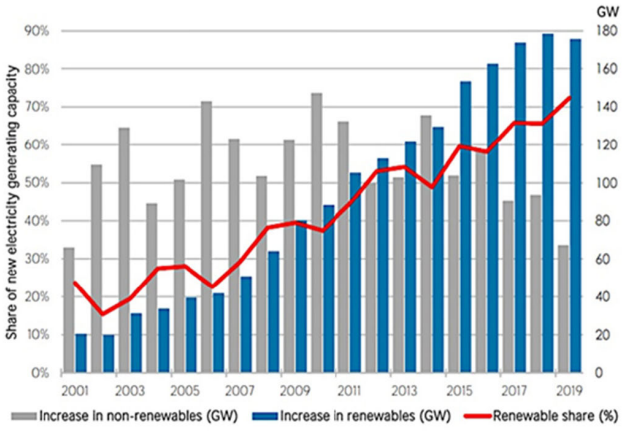

FIGURE 1. Renewable share of annual power capacity growth [1].

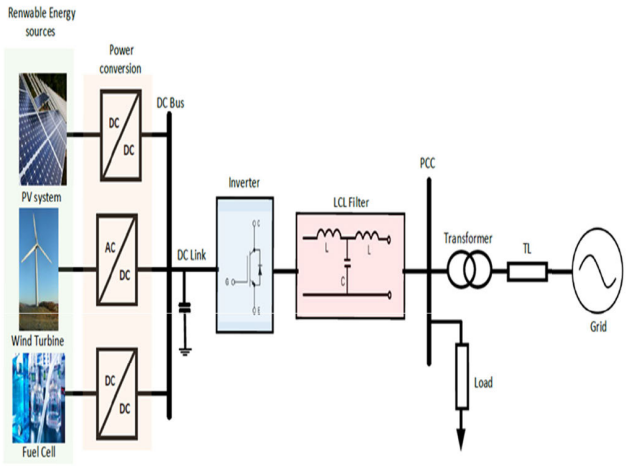

FIGURE 2. Basic grid integration of different renewable energy sources implementing LCL filter.

source of power harmonics and cause power quality issues in the system. Therefore, in order to meet the harmonic limits recommended in international standards for acceptable harmonic levels in power grids, such as IEEE-519, it is crucial to efficiently design the inverter and the size of the output filter required for optimal grid integration of renewable sources [2]. The conventional voltage source inverters generate the output voltage waveform in two levels only. On the other hand, the new multilevel inverters generate the output voltage waveform in a multilevel staircase waveform that makes the generated output much closer to a pure sinusoidal waveform than a two-step inversion in the conventional or classic topologies. The key merits and features of multilevel inverters, compared with conventional two-level inverters, include: 1) At low switching frequency, higher output voltage can be generated, 2) the output voltage can be synthesized with multiple smaller steps, resulting in lowering the voltage stress (dv/dt), 3) the inverted output signal features low total harmonic distortion (THD), 4) electro-magnetic interference (EMI) is minimized, 5) the size of the required output filter is reduced, and 6) output is generated with a higher fundamental component [3]. Nowadays, voltage source multilevel inverters (VS-MLIs) are applied widely in medium voltage-high power applications, especially for the grid integration of intermittent renewable energy sources such as solar PV and wind power plants.

The wide deployment of power electronics inverters in future power grids will induce more power harmonics to the grids. Power system harmonics have adverse effects on power systems and equipment, such as overloading, heating, reduction of life, aging of insulators, and many other effects. Power harmonics is considered a major issue of power quality as it affects both the utility and the customer. In practice, there are many sources that generate harmonics in power systems. Non-linear loads with the huge developments in power electronics technology, there has been a rapid growth of non-linear loads in electrical power systems, which are known to be a major source of harmonics in power systems. Power electronics converters and the use of power semiconductor switching in their operation are other major sources of harmonics in modern electrical power systems. With the need for more penetration of renewable and sustainable energy sources such as solar PVs, wind turbines, and fuel cells, the future sustainable power systems will rely more on power conversion technologies that result in more generation of harmonics within the system.

There are several practical techniques that can mitigate harmonics in power systems. Among these, harmonic filtering is very widely applied. Power harmonic filters can be classified mainly into 1) passive power filters (PPF), and 2) active power filters (APF) [4]. PPFs are very commonly applied in power systems due to their many advantages over APFs such as low cost, almost free of maintenance, simple structure, and simple operation. This paper investigates the application and design of PPFs for harmonic mitigation at the output of multilevel VSIs for grid integration of efficient renewable energy sources. The research focuses on the application of LCL filters at the output of VS-MLIs for efficient integration of renewable energy sources as illustrated in Figure 2.

The problem of PPF design is a combinatorial optimization problem. The conventional design relies on detailed system information, including system impedance, loads and harmonics profile. Engineering experience is needed for them, but it might not result in optimum filter design. The main objective of this paper is to develop a generic optimization model based on a genetic algorithm to optimally design the LCL filter at the output of multilevel inverters for efficient grid integration of renewable energy source. The optimization model is based on an evaluation of precise energy losses to ensure the optimum design according to system constraints..

II. SERIES POWER FILTER TOPOLOGIES

To suppress harmonics caused by the switching devices of voltage source inverters, a passive power filter is usually placed at the output of the inverter [5]. A survey of published papers on power electronic filtering using PPFs shows a great deal of interest over the past view years, and many topologies have been proposed by researchers. However, there are three basic topologies that are widely applied and considered

1. L-Filter
2. LC-Filter
3. LCL-Filter

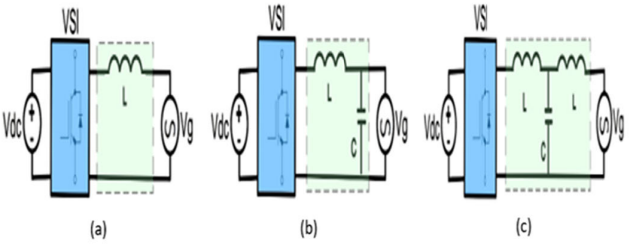

FIGURE 3. Basic series power filter topologies: (a) L-Filter; (b) LC-Filter; (c) LCL-Filter.

mature technologies in industry [6]. These topologies are listed below and the circuit configurations for each topology is illustrated in Figure 3

1. L-Filter
2. LC-Filter
3. LCL-Filter

To choose the best topology to be applied at the output of the multilevel inverter, several factors and features should be analyzed such as efficiency, weight, and volume [7]. The L-Filter is a first order filter and is typically applied for converters switched at high frequency [8]. The main problem with using a large input L-filter that it has low attenuation of harmonics and is bulky [9]. The LC-Filter is a second order filter that has better damping than the L-Filter and has excellent performance and voltage quality. However, a high inductance value is required to achieve the filter's cut-off frequency, which will cause a problem when connecting this topology to the grid, as the resonance frequency of the filter will be dependent on the grid impedance [8]. In addition to that, the capacitor in both the L-filter and LC-filter may be exposed to line voltage harmonics, which results in high currents. Hence, the L-filter and the LC-filter topologies are not preferred.

The LCL-filter shown in Fig. 1-c is a third-order filter. This topology has excellent current ripple attenuation and can use small inductance values [8]. It is capable of damping high frequency (HF) noise because of its extra inductance [9]. In contrast with the L-filter and the LC-filter, the capacitor in the LCL-filter is not exposed to line voltage harmonics. The LCL-filter topology is superior to other topologies [10], [11]. The key attractions are: high current ripple rejection [12], fast dynamic response [13], low voltage drop [14], high power factor [15], low volume and weight, and low dependence on the grid impedance [13]. For this reason, it is preferred for medium voltage-high power utility applications. In this study, the design of the LCL filter is considered due its superiority over the other topologies.

III. APPLIED LCL FILTER DESIGN METHODS

Many design methods for the LCL filter have been proposed in the literature. In any design method, several factors should be considered, including current ripple, filter size, ripple attenuation, and to avoid resonance with the grid, a damping solution must be added in series with the capacitor. Table 1 summarizes the main applied LCL design methodologies by researchers over the last 10 years, with a focus on the last three years.

The main steps involved in the conventional procedure of LCL power filter design are:

- Design of the inverter-side inductance (L_i). This should be chosen to limit the inverter side ripple current to 10-30% of the fundamental current [26]. This is can be calculated by the following equation [28]:

$$L_i = \frac{U_{DC}}{16 \times f_s \times \Delta I_{L-max}} \tag{1}$$

  where ΔI_{L-max} represents the 10-30% current ripple
- Selection of the grid-side inductance (L_g) and the filter capacitor (C_f) based on the required harmonic suppression is needed as per IEEE-519. It is important when selecting the values of (L_g, C_f) to ensure that the maximum allowable change in the power factor value is within 5%. This means that the reactive power absorbed by the filter capacitor (C_f) is always less than 5% of the kVA rating of the inverter [26].
- It is necessary to control the resonant frequency of the filter and ensure it is far from the grid frequency and at the same time greater than half of the switching frequency [8]. In this step, a passive or active damping is commonly added to the filter circuit.

The transfer function for the LCL filter is

$$G(s) = \frac{i_g(s)}{v_i(s)} = \frac{1 + R_{SD}C_f S}{L_i L_g C_f S^3 + (L_i + L_g) R_{SD} C_f S^2 + (L_i + L_g) S} \tag{2}$$

The transfer function basic block diagram for the LCL filter is depicted in Figure 4. The next section explains the proposed optimization model for LCL filter design. It highlights the main drawbacks of the conventional design approach and the need for more efficient algorithms. Hence, a detailed proposed model is illustrated for the optimum design of LCLs at the output of VS-MLIs.

IV. PROPOSED OPTIMIZATION MODEL FOR LCL POWER FILTER DESIGN

The conventional approach requires additional details about the electrical power systems under investigation, and essentially relies on engineering experience. Finally, the conventionally designed circuit might not achieve optimum LCL filter design [31]. In this paper, we have tried to overcome these drawbacks and have investigated and applied more efficient methods to solve the problem. The proposed method investigates the design problem of LCL filters at the output of multilevel VSIs for efficient grid integration of renewable energy source. The study aims to develop a generic step by step methodology to effectively design the LCL filters at the output of multilevel VSIs. The design problem was converted into an optimization problem to be solved using a heuristic

TABLE 1. Summary of literature review of LCL design.

Authors	Year	Design Methodology
C. Gurrola, et al. [16]	2020	Harmonic modelling based, 3-phase, grid connected, 2-level inverter, passive series Rs damping, Renewable energy sources
Tang Weiyu et al. [17]	2020	Critical damping ratio method, single-phase, grid connected, 3-level inverter, passive series Rs damping, DC grid connected applications
K.B. Park et al. [18]	2020	Comprehensive analytical optimization, 3-phase, grid connected, 2-level inverter, parallel connected VSC applications
Y. Kim and H. Kim [19]	2019	Analytical mathematical, 3-phase, grid connected, 3-level inverter, passive Rs damping, grid connected inverter
H. Oruganti et al. [20]	2018	Conventional with PRD Controller, 1-phase, grid connected, 7-level inverter, passive series Rs damping.
Kouchaki and Nymand [21]	2018	Comprehensive analytical approach, 3-phase, grid connected, 2-level rectifier, power factor correction
A. Lachichi et al. [22]	2018	Optimum design, grid connected, 3-phase, multilevel MMC, hybrid AC/DC micro grid applications
S. Davood et al. [23]	2018	Mathematical approach, 1-phase, grid connected, 2-level inverter, passive series and parallel damping, general DC input source
D. Mustafa et al. [24]	2018	Conventional, 3-phase, grid connected, 2-level inverter, passive series Rs damping
L. Yong et al. [25]	2017	Comprehensive design flow considering filter size and space constraints, 3-phase, 2-level inverter, passive series Rs damping, aerospace applications
Ravicant et al. [26]	2017	Conventional, 3-phase, grid connected, 5-level inverter, passive series Rs damping, DSTATCOM
C. Mahamat et al.[27]	2017	FFT analysis based, 3-phase, grid connected, 2-level inverter, passive series Rs damping, solar PV
Noah K. Serem [9]	2015	Conventional, single-phase, stand-alone, 3-level inverter, passive series Rs damping, renewable energy source
A.E.W.H Kahlane et al. [8]	2014	Conventional, single-phase, grid connected, 3-level inverter, passive series Rs damping, solar PV
Xu Renzhong et al. [28]	2013	Conventional, 3-phase, grid connected, 2-level inverter, passive parallel Rs damping, solar PV
A. Reznik et al. [29]	2012	Conventional practical, single-phase, grid connected, 2-level inverter, passive series Rs damping, wind turbine
A. A. Rockhill et al. [30]	2011	frequency-domain-model based, 3-phase, grid connected, 3-level inverter, new passive damping filter, wind turbine

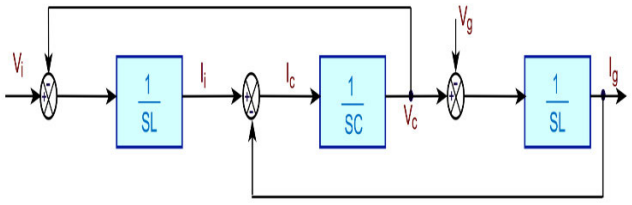

FIGURE 4. Transfer function basic block diagram for the LCL-filter.

TABLE 2. Key design principles and considerations for efficient LCL power filter design.

Key Efficient LCL filter design principles
➢ Filter-design parameters L_i, C_f and L_g should satisfy the filtering objective
➢ Limits harmonic distortion of voltage and current at PCC as per IEEE standards
➢ Minimize filter size, energy losses and THD.
➢ Limit power factor variations at PCC
➢ Avoid frequency resonance with the grid and ensure better harmonics attenuation

approach. A genetic algorithm (GA) was adopted to minimize the objective function with respect to design constraints. As a case study, seven-level cascaded H-bridge multilevel inverter (CHB-MLI) was considered. The optimization model satisfies the key design principles and considerations listed in Table 2.

A. PROBLEM FORMULATION AND OBJECTIVE FUNCTION

The design parameters of the LCL power filter are the inductor at the inverter side Li, the inductor at the grid side L_g, the capacitance of the filter C_f, and damping series resistance R_{sd}. In the proposed model, the design problem is transformed into an optimization problem in which a design objective function is minimized subject to applied design constraints. The optimization model should minimize a multi-objective function with respect to applied constraints. The filter design parameters are the output of the applied algorithm. In the proposed method, a multi-objective function is set to be minimized for the filter design and formulated as follows:

- Objective 1: minimize the total harmonic distortion for the output voltage waveform THD_v

$$f_1 = Min.THD_v \tag{3}$$

$$THD_v = \sqrt{\sum_{n=2}^{\infty}\left(\frac{U_n}{U_1}\right)^2} \tag{4}$$

where:
THD_v: the total harmonic distortion of output voltage.
U_n: the n^{th} harmonic magnitude of output voltage.
U_1: the fundamental component of output voltage.

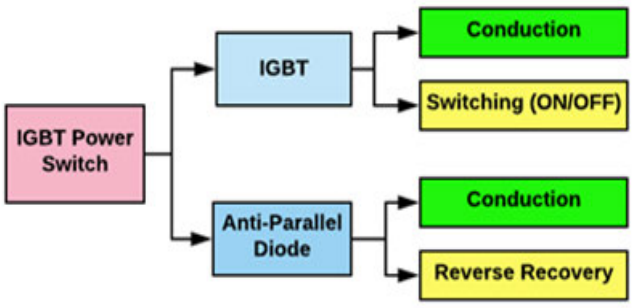

FIGURE 5. Main power losses associated with the IGBT power switch.

- Objective 2: minimize the energy loss cost.

$$f_2 = Min.\left(f_{Energy\_Cost}\right) \tag{5}$$

The main energy losses in multilevel inverters are those associated with the power switching devices. There are mainly four types of these losses which are [32]: conduction losses, switching losses, off-state losses, and gate losses. In practice, the off-state and gate losses are negligibly small. Hence, only the conduction and switching losses are considered in this analysis. Figure 5 illustrates the classification of power losses considered for each IGBT power switch in this objective. For the LCL filter design, the energy losses are calculated precisely for each switch [32], [33].

In semiconductor devices, the power loss that occurs while the device is at the on-state and conducting current is defined to be the device conduction losses. At the conduction stage, the dissipated power can be calculated for the IGBT and the antiparallel diode by multiplying the on-state saturation voltage by the on-state current [32], [33].

$$P_{conduction} = |i_c| \times v_{on} \tag{6}$$

The on-state voltage is modeled by a quadratic equation in terms of the on-state current based on the actual semiconductor device datasheet. Hence, there will be two separate equations for the on-state voltage, one for the IGBT and one for the antiparallel diode. On the other hand, the switching losses are defined as the power loss dissipated during the process of turning on and off the semiconductor device. It is closely proportional to the switching frequency and contributes substantially to the inverter total losses, especially when a high switching frequency is applied. The switching energy losses for the power switch are: the IGBT turn-on loss (E_{on}), the IGBT turn-off loss (E_{off}), and the antiparallel diode turn-off (E_{rec}) loss. Because of the fast conducting of the diode during forward biasing, the antiparallel diode turn-on loss is normally neglected. These switching losses are calculated for the IGBT and the antiparallel diode according to the modelled quadratic equations of K_{on}, K_{off}, and K_{rec}. Here, the energy factor K is modeled by dividing the energy by the switching current as per the curves provided in the device datasheet.

$$E_{on} = |i_c| \times K_{on} \tag{7}$$

$$E_{off} = |i_c| \times K_{off} \tag{8}$$

$$E_{rec} = |i_c| \times K_{rec} \tag{9}$$

Figure 6 depicts the flow chart for calculating the precise applied power losses for each switch. The cost of energy losses is modeled using an equivalent annualized capital cost with respect to the present value factor [34]:

$$f_{Operating\_Cost}(\$) = H \times U_{Energy} \times \frac{(1+i)^y - 1}{i\,(1+i)^y} \times P_{loss} \tag{10}$$

where:

H: is total operating hours annually (h/year)

U_{Energy}:is the energy cost in (US \$/kWh),

i: is the annual interest rate for capital cost, which is assumed to be 5%,

y: is the levelaization period or system lifetime (years), which is assumed to be 15 years

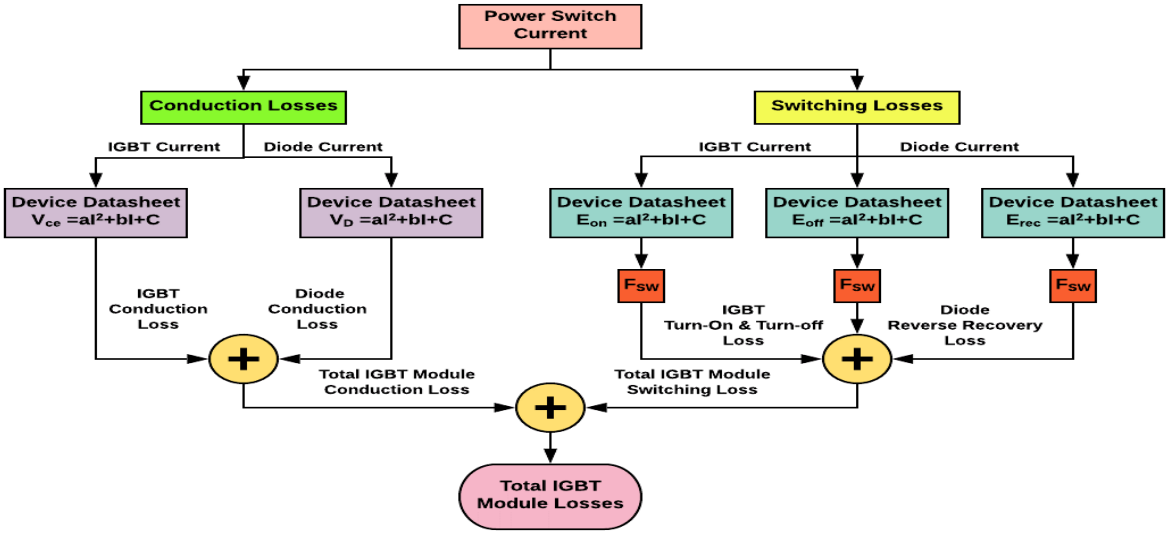

FIGURE 6. General block diagram for switching module power loss calculations.

TABLE 3. IEEE-519 standard recommended voltage-distortion limits at PCC [35].

Bus Voltage at PCC	Voltage Distortion	THD_v
$1\ kV < V \leq 69\ kV$	3.0 %	5.0 %
$69\ kV < V \leq 161\ kV$	1.5 %	2.5 %
$V > 161\ kV$	1.0 %	1.5 %

TABLE 4. IEEE-1547 recommended current-distortion limits at PCC (120 V – 69 kV) and SCR of 20 [36].

Harmonic Order (h)	Percent of rated current (%)
h < 11	4
11 ≤ h < 17	2
17 ≤ h < 23	1.5
23 ≤ h < 35	0.6
35 ≤ h	0.3
$\%THD_i$	5

B. OPTIMIZATION APPLIED CONSTRAINTS

When designing an LCL power filter, the borders of constraints should be maintained to ensure proper operation of the electrical power system under investigation. The developed multi-objective design function is to be optimized subject to several technical constraints: voltage and current distortion at PCC, inductance ripple current, total filter inductance size, filter capacitance size, and resonant frequency of the filter. These are explained in the following.

1) HARMONICS PROFILE OF GRID CURRENT AND OUTPUT VOLTAGE

As per the IEEE-519 [35] and IEEE-1547 [36] standards, the voltage and current distortion limits should not be exceeded. In the case of voltage levels up to 69 kV, the THD_v should be maintained under 5%, with non-individual voltage harmonics exceeding 3%. On the other hand, the THD_i follows the standards limits according to the system short-circuit ratio. Tables 3 and 4 show the limits of voltage and current distortions as per IEEE-519 and IEEE-1547, respectively.

2) INDUCTANCE RIPPLE CURRENT AND TOTAL INDUCTANCE

At the inverter side, the inductance ripple current should be limited to between 10% to 30% of the rated current. To limit the inductance ripple current, the LCL should be designed with higher impedance. However, the higher the filter impedance, the greater the drop in the voltage across the filter. Hence, the total inductance of the filter is limited to 0.15 pu. [26], [29]

$$\frac{V_{Source-Phase}}{\sqrt{6}\,(n-1)\,f_{sw}\,i_{ripp-max}} \leq L_i \leq \frac{V_{Source-phase}}{\sqrt{6}\,(n-1)\,f_{sw}\,i_{ripp-min}} \tag{11}$$

TABLE 5. LCL optimization model.

Mathematical Model for LCL Filter Design Optimization
$Min.\,[\,w_1 f_1 + w_2 f_2]$
Subject to:
THD_v & THD_i $<$ *standards limits*
$0.1\ i_{rated} \leq i_{ripp} \leq 0.3\ i_{rated}$
$\frac{V_{Source-Phase}}{\sqrt{6}\,(n-1)\,f_{sw}\,i_{ripp-max}} \leq L_{i,g} \leq \frac{V_{Source-phase}}{\sqrt{6}(n-1)\,f_{sw}\,i_{ripp-min}}$
$L_i + L_g \leq 0.15\ L_B$
$C_f \leq 0.05\ C_B$
$10\ f_g \leq f_{res} \leq 0.5\ f_{sw}$

where $V_{Source-Phase}$ is the rms value of source voltage, n is the inverter number of levels, $i_{ripp-max}$ and $i_{ripp-min}$ are the maximum and minimum limits of inductance ripple current respectively.

3) FILTER CAPACITANCE

Because the LCL filter capacity should not exceed the maximum power factor variations of 5%, the capacitance of the filter should be kept to less than 5% of the system base capacitance:

$$C_f \leq 0.05 C_B \tag{12}$$

where C_f is the filter capacitance and C_{Base} is the base value of the system capacitance.

$$C_B = \frac{1}{w_g Z_B} \tag{13}$$

$$Z_{Base} = \frac{V^2_{Source-LL}}{P_i} \tag{14}$$

Here $V_{Source-LL}$ is the source line to line voltage and P_i is the inverter rated active power.

4) RESONANT FREQUENCY OF THE FILTER

To avoid resonance with the grid, the LCL filter frequency should be much greater than the grid frequency. It is also recommended to keep the filter resonant frequency at least 50% less than the switching frequency of the inverter. This is to ensure better attenuation of inverter generated harmonics and to avoid harmonics amplification and system destabilizing [14].

$$10 f_g \leq f_{res} \leq 0.5 f_{sw} \tag{15}$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_g + L_i}{L_g L_i C_f}} \tag{16}$$

Table 5 summarizes the applied mathematical model for LCL design optimization.

C. GA OPTIMIZATION FOR LCL FILTER DESIGN

A GA is basically a heuristic global evolutionary optimization algorithm (EA). Its working principle is based on mechanics

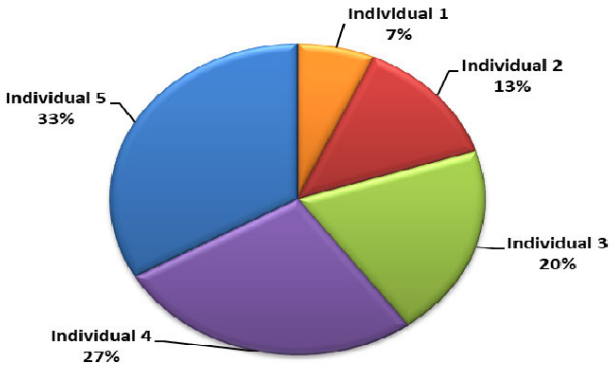

FIGURE 7. Sample of roulette wheel selection and the assigned areas for population individuals.

of natural selection and genetics. In comparison to other EA optimizations, the key attraction is that GA searches by population rather than individual points. GA is very widely and commonly applied for both constrained and unconstrained optimization problems. In this study, GA was applied to solve for the optimum design of shunt passive power filters (PPF) at the output of different levels CHB-MLI. GA optimization consists of five main steps: 1) initialization of the population, 2) evaluation of fitness function, 3) selection, 4) apply genetic operators, and 5) stopping criterion. [37]

In the initialization step, the algorithm is initialized and he parameters of the optimization problem are coded. Based on the parameter coding approach, either in a binary or floating-point string, a set of solutions is randomly generated. The next step is the evaluation of fitness function to test the goodness of a generated solution, a fitness function is applied as an evaluation tool. In this paper, an objective function was defined as a fitness value (FV). This function is critically important and should be well-defined as it has a great impact on the quality of the solution. At selection stage, parents are chosen according to selection rules to produce off-spring chromosomes. The selected parents are the main contributors to generate to the next generation. Accordingly, the fittest individual is most likely to survive and the less fit are to be annihilated. Figure 7 depicts an example of a roulette wheel selection approach.

Crossover swaps over several bits between parents. The purpose of this is to exchange some genes to form a new improved combination. Figure 8 demonstrates an example of GA one-point individual crossover. Mutation is considered a very important operator to further improve the quality of the next generation by altering some genes. Figure 9 gives an illustration for a bit-by-bit flipping mutation example at a random position for any optimization algorithm, it is critically required to tell the algorithm when to stop and terminate. This step is defined as the stopping criterion of the applied algorithm. The flow chart of the applied LCL design optimization model is depicted in Figure 10.

V. SIMULATION RESULTS AND DISCUSSION

The proposed model has been applied according to the system parameters presented in Table 6. The multilevel inverter is

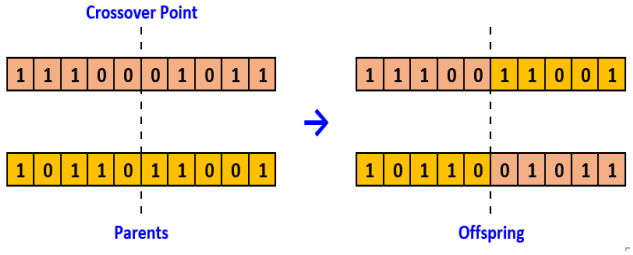

FIGURE 8. Example of GA individual crossover.

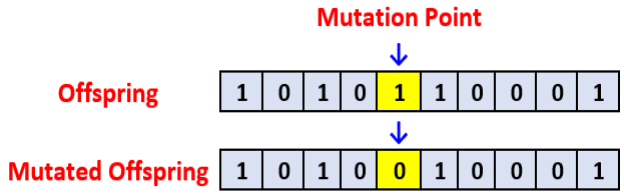

FIGURE 9. Example of bit-by-bit flipping single mutation.

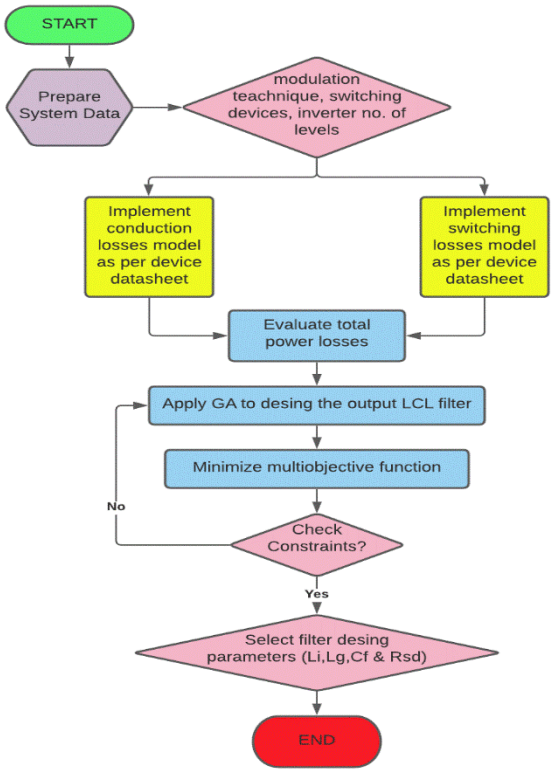

FIGURE 10. General model architecture for the applied LCL-filter design optimization approach.

chosen to be a CHB-MLI with 7 levels as a case study. The employed circuit layout for the three-phase 7-level CHB-MLI is shown in Figure 11. Each phase is composed of three bridge circuits. The output of the inverter is 11 kV, 5 MW and operated at 0.8 lagging power factor. The simulated model for the inverter was built as a three-phase to reflect

TABLE 6. System parameters for the grid connected inverter under investigation.

Parameter	Symbol	Value
Grid line voltage	Vg	11 kV
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	5 KHz
DC link voltage per cell	V_{DC}	2.72 kV
Inverter output power	P_i	5 MW
Base Current	I_B	262.43 A
Base Impedance	Z_B	24.2 Ω
Base Inductance	L_B	77.03 mH
Base Capacitance	C_B	131.5 µF

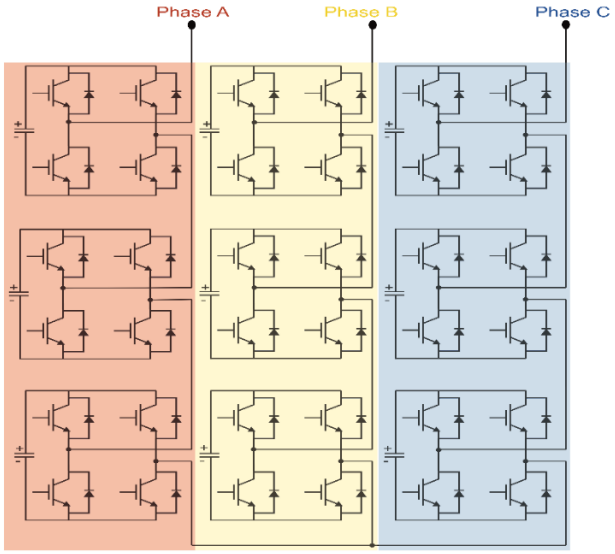

FIGURE 11. Three-phase circuit configuration of 7-level CHB-MLI.

more practical results. MATLAB-SIMULINK was used for the modeling and simulation.

Sinusoidal Pulse Width Modulation (SPWM) was applied to control the inverter. The main idea of SPWM modulation is to generate a control pulse by comparing a sinusoidal reference waveform with a triangular carrier waveform. When applied to multilevel inverter control, there should be one reference waveform signal and multi-carrier triangular waveforms. In the case of an n-level inverter, (n–1) triangular carriers are needed [38]. During the control process, each carrier waveform is compared with the reference waveform. This comparison results in generating a string of control pulses, which are used to control the power switch. Whenever the reference waveform is greater than the carrier signal, the active power switch is ON. For the developed optimization model, Phase-Disposition (PD-SPWM) was adopted to control the inverter. This modulation was chosen as it generates a better harmonic profile than other SPWM techniques do [39].

FIGURE 12. Typical appearance of FZ400R65KE3 IGBT module [40].

The selection of the IGBT module considered for the inverter design was based on its blocking voltage and market availability. In practice, the HV-IGBTs are operated at only 50–60% of their blocking voltage capability to ensure a reliable operation. For the considered CHB-MLI with output voltage of 11 kV, each bridge was connected to 2.722 kV DC voltage. Accordingly, the IGBT switching module of type FZ400R65KE3 by Infineon was selected. This switch has a blocking voltage capability of 6.5 kV, and a maximum forward current of 400 A. Figure 12 depicts the typical appearance of this module. Datasheet for this switching device is given in [40].

Based on the module data sheet, the characteristics of the switching device was studied for the IGBT switch and the antiparallel diode. Figure 13 presents the output characteristics of the IGBT switch and the forward characteristics of the antiparallel diode. These curves are used to evaluate the conduction losses. On the other hand, Figure 14 shows the module switching energy losses: the IGBT turn-on losses (E_{on}), the IGBT turn-off losses (E_{off}) and the antiparallel diode turn-off (E_{rec}) loss. These curves are applied when calculating the switching losses. For precise power loss evaluation and modeling, a curve-fitting tool was implemented for these curves, each curve being represented by a polynomial equation, as follows.

$$v_{ce} = -1 \times 10^{-5} I_c^2 + 0.0128 I_c + 1.2882 \quad (17)$$

$$K_{on} = -4 \times 10^{-7} I_c^3 + 0.0004 I_c^2 - 0.1097 I_c + 16.984 \quad (18)$$

$$K_{off} = 7 \times 10^{-6} I_c^2 - 0.0048 I_c + 6.511 \quad (19)$$

$$K_{rec} = -3 \times 10^{-7} I_D^3 + 0.0003 I_D^2 - 0.0944 I_D + 13.37 \quad (20)$$

The simulated three-phase output phase-to-ground and phase-to-phase voltage waveforms are demonstrated in Figures 15 and 16, respectively, for 7-level CHB-MLI. Before implementing the LCL filter, the THD of the phase-to-ground voltage was almost 6.5%. This value is higher than the recommended standard of less than 5% for THD. Furthermore, all individual harmonics are required to be less than 3%. This was found to be violated by the 31st harmonic, which is recorded to be close to 4%. Figure 17 shows the harmonic profile for the phase-to-ground voltage before adding the LCL filter.

For efficient renewable energy grid integration and to improve the harmonic profile at the inverter output, the developed GA based optimization model has been applied to solve

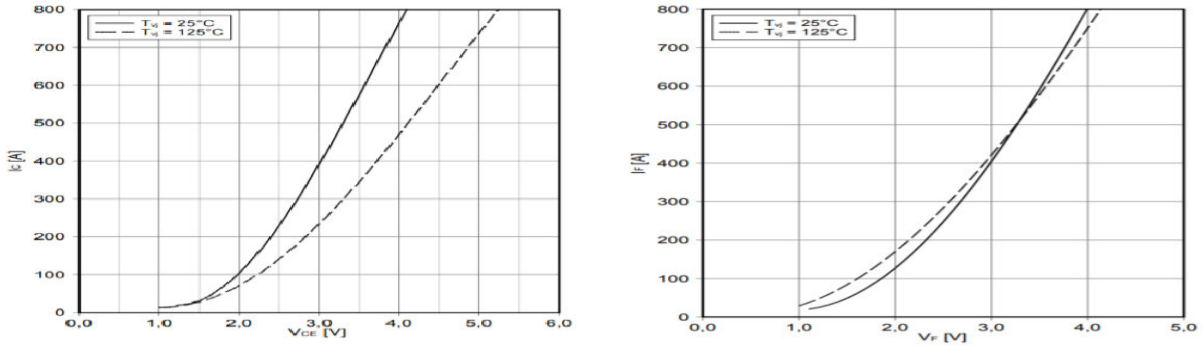

FIGURE 13. FZ400R65KE3 module characteristic: (a) output characteristic for IGBT switch; (b) forward characteristic for the antiparallel diode. [40].

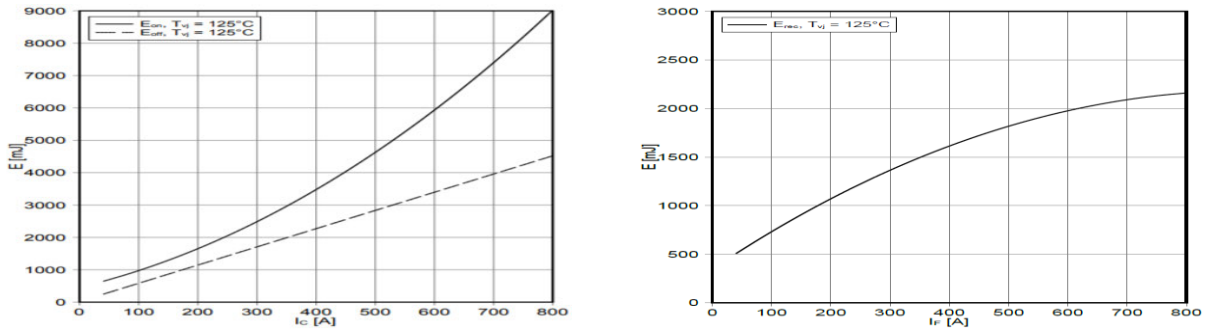

FIGURE 14. Typical switching losses for FZ400R65KE3 module: (a) IGBT switching losses; (b) antiparallel switching losses [40].

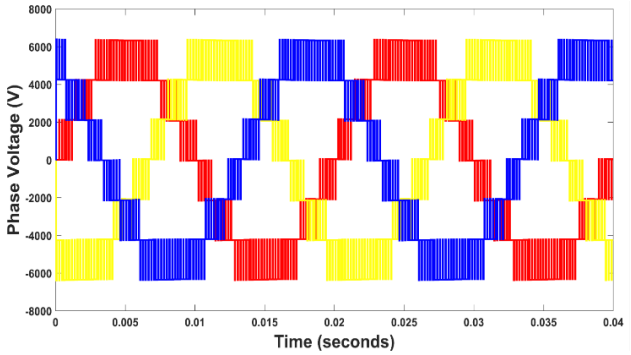

FIGURE 15. Three-phase (L-G) output voltage for 7-level CHB-MLI before filter implementation.

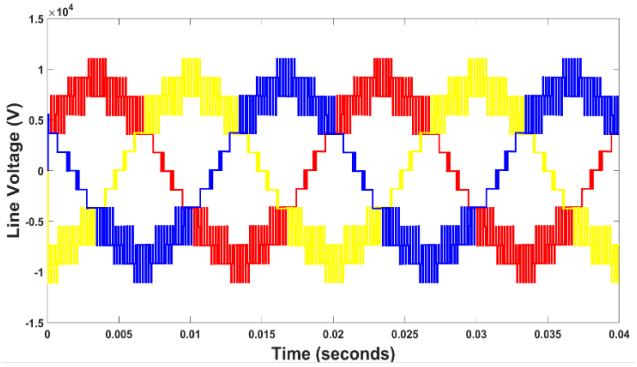

FIGURE 16. Three-phase (L-L) output voltage for 7-level CHB-MLI before filter implementation.

for the optimum design of the LCL passive power filter. The optimization should ensure the minimization of a multi-objective function compromising of THD and power losses. The optimization is restricted with the applied system constraints given previously in Table 5. Figure 18 demonstrates how the selection of the filter design parameters L_i, L_g and C_f affects the value of the resonance frequency of the designed filter. Based on the LCL filter design constraints, the minimum acceptable limit for the resonance frequency is 10 times the fundamental frequency. On the other hands, the maximum allowable resonance frequency for the designed filter is half of the inverter switching frequency. Accordingly, the value of resonance frequency should be between 500 and 2500 Hz. The obtained LCL design result and the applied GA parameters are summarized in Tables 8 and 9, respectively. The performance of GA for the optimum design of LCL at the output of 7-level CHB-MLI is shown in Figure 19.

After implementing the designed LCL filter at the output of the 7-level CHB-MLI under investigation, the quality of the output waveform was significantly improved. Figures 20 and 21 depict the output phase-to-ground and line-to-line voltage waveforms, respectively. The THD of the phase voltage was reduced from 6.5% to almost 2%. After adding the LCL filter, all the individual harmonics were lowered to much less than 1% except for the 3rd harmonic, which was also lowered but to less than 2%. It is worth mentioning here

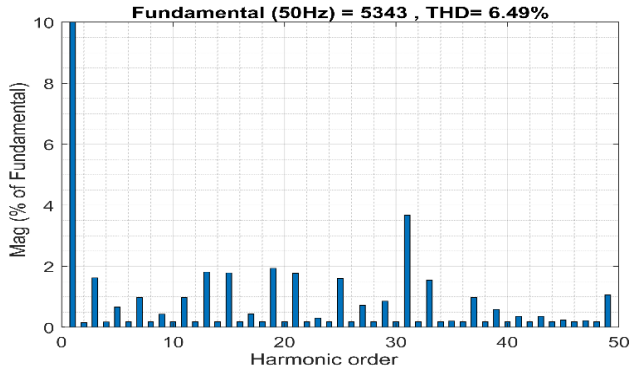

FIGURE 17. Harmonic profile for the output phase voltage before adding the LCL filter.

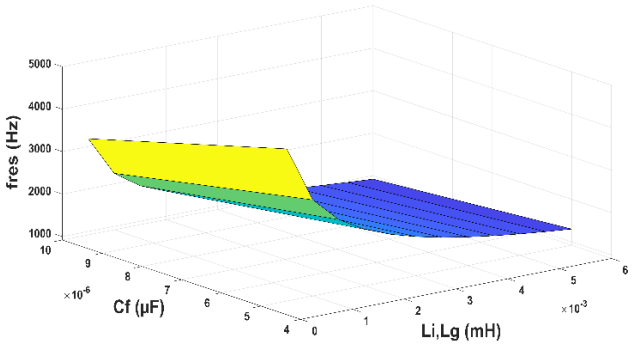

FIGURE 18. Resonant frequency at different LCL filter design parameters.

TABLE 7. Applied GA parameters and settings.

GA Applied Parameters	
Population Size	*50*
Selection function	*Stochastic Uniform*
Crossover rate	*0.8*
Mutation rate	*0.5*
Stopping criteria	*50 stall generation*

TABLE 8. GA design for the LCL filter.

LCL Filter Designed Parameters	
L_i (mH)	1.6
L_g (mH)	2.3
C_f (μF)	6.6
R_{SD} (Ω)	3.98
f_{res} (kHz)	2.018

that the THD figures are much lower due to the cancellation of triplen harmonics. Figure 22 shows the harmonic profile for the output phase-to-ground voltage after adding the LCL filter.

The transfer function for the optimum design LCL filter is given by Equations 22 and 23 for the filter with series resistive damping and without damping, respectively. Figure 23 depicts the Bode diagram of both functions. It is clear from the figure that the impact of adding the series

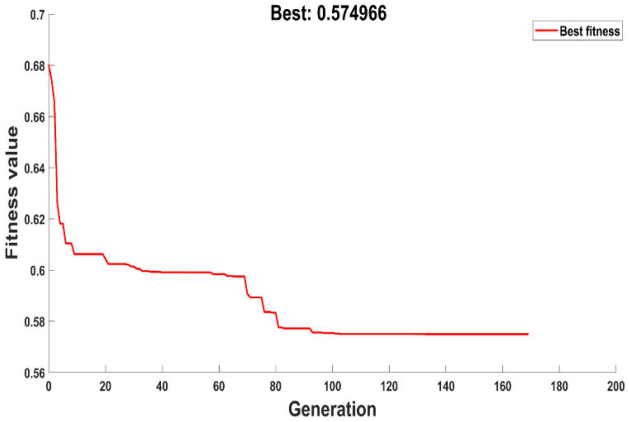

FIGURE 19. GA performance for LCL filter design optimization.

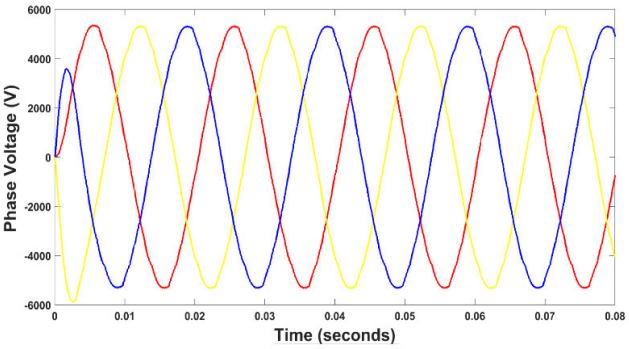

FIGURE 20. Three-phase (L-G) output voltage for 7-level CHB-MLI after filter implementation.

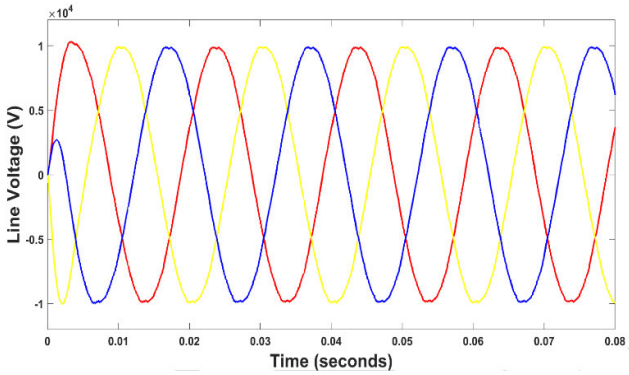

FIGURE 21. Three-phase (L-L) output voltage for 7-level CHB-MLI after filter implementation.

damping suppresses the peak at the resonance frequency. At higher frequencies, the designed LCL filter with series damping performs better than the LCL-filter without damping. However, at low frequencies the performance of both filters are identical. The increase in the value of series damping resistance results in better peak suppression at that resonance frequency. The impact of different values of series resistance R_{SD} for damping is illustrated in Figure 24.

$$G(s) = \frac{i_g(s)}{v_i(s)} = \frac{1}{(2.429x10^{-11})S^3 + (3.9x10^{-3})S} \quad (21)$$

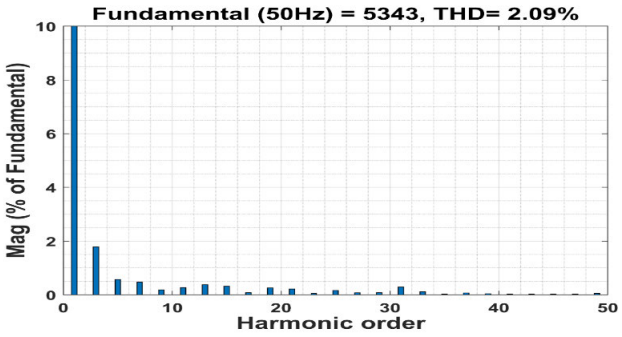

FIGURE 22. Harmonic profile for the output phase voltage after adding the LCL filter.

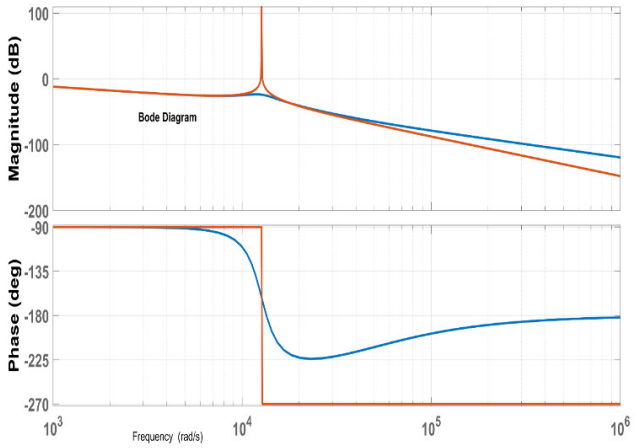

FIGURE 23. Bode diagram of designed LCL filter.

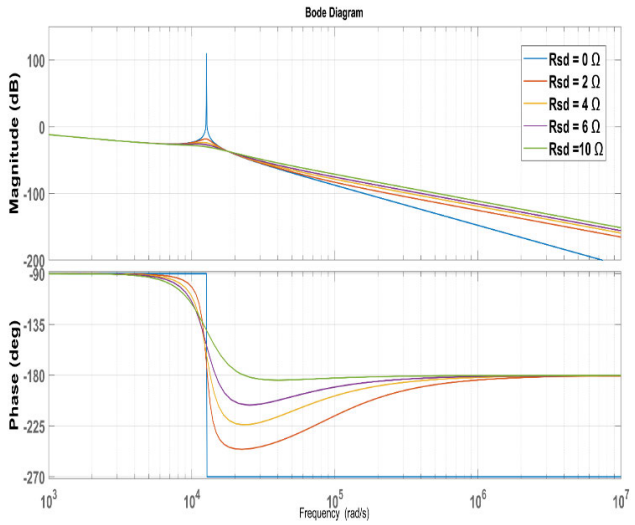

FIGURE 24. Bode diagram of designed LCL filter at different values of series damping R_{SD}.

VI. CONCLUSION

Renewable energy penetration into power grids is growing rapidly to meet the fast-growing global electricity demand. Technologies such as solar PVs power plants, wind turbine farms, battery energy storage, and fuel cells are expected to dominate future smart grids. As these technologies are integrated with power grids through power electronics, mainly converters and inverters, harmonics levels in power systems is expected to greatly increase. Power harmonics results in severe effects for both utility and customers. Among the applied solutions for mitigating these harmonics, passive power filters (PPF) are economic and widely applied for industrial and utility applications. LCL passive power filters are applied for efficient integration of different renewable energy generating sources. Their main function is to maintain power harmonic levels well below those recommended by technical power quality standards.

This study investigated the problem of designing thane LCL power filter at the output of VS-MLIs for better integration of renewable energy sources. The paper aims to provide a generic model to optimize the design for the LCL filter at the output CHB-MLI in high-power–medium-voltage applications. This was accomplished by developing a new optimization model based on a heuristic approach to overcome the design challenges of conventional approaches. In this mode, a multi-objective function of key measures such as THD and power losses is to be minimized subject to design and system constraints. GA was implemented for the optimization. The evaluation of power losses was carried out according to a precise method of estimation. The model is generic, and the objective function can be modified to meet the designer's different requirements and prospects. However, defining the objective function should be done with more caution, as it critically affects the optimization. Implementation of the proposed model to a case study was found to be simple and efficient. The designed LCL filter improved the power quality significantly at the output of the inverter under investigation. The developed model can be also applied to different levels of VS-MLIs and other topologies such as Neutral-Point Clamped (NPC-MLI) and Flying Capacitor (FC-MLI).

ACKNOWLEDGMENT

The authors would like to acknowledge the financial support received from the Scientific Research Deanship, Taif University, KSA, through Grant No. 1-440-6163.

REFERENCES

[1] A. Irena, "Renewable capacity highlights," in *Proc. Int. Renew. Energy Agency (IRENA)*, Abu Dhabi, United Arab Emirates, 2020, pp. 1–8. [Online]. Available: https://www.irena.org//media/Files/IRENA/Agency/Publication/2020/Mar/IRENA_RE_Capacity_Highlights_2020.pdf?la=en&hash=B6BDF8C3306D271327729B9F9C9AF5F1274FE30B

[2] R. Langella, A. Testa, and E. Alii, *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*. Hoboken, NJ, USA: Wiley, 2014.

[3] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[4] J. Arrillaga and N. R. Watson, *Power System Harmonics*. Hoboken, NJ, USA: Wiley, 2004.

[5] S. Eren, M. Pahlevaninezhad, A. Bakhshai, and P. K. Jain, "Composite nonlinear feedback control and stability analysis of a grid-connected voltage source inverter with *LCL* filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5059–5074, Nov. 2013.

[6] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, May 2003.

[7] S. V. Araujo, A. Engler, B. Sahan, and F. L. M. Antunes, "LCL filter design for grid-connected NPC inverters in offshore wind turbines," in *Proc. 7th Internatonal Conf. Power Electron.*, Oct. 2007, pp. 1133–1138, doi: 10.1109/ICPE.2007.4692556.

[8] A. Kahlane, L. Hassaine, and M. Kherchi, "LCL filter design for photovoltaic grid connected systems," *J. Renew. Energies*, vol. 5, pp. 227–232, Dec. 2014.

[9] N. K. Serem, "Electrical power quality improvement for renewable energy systems using LCL filter," *Int. J. Sci. Eng. Res.*, vol. 6, no. 10, p. 954, 2015.

[10] Y. Han, M. Yang, H. Li, P. Yang, L. Xu, E. A. A. Coelho, and J. M. Guerrero, "Modeling and stability analysis of *LCL* -Type grid-connected inverters: A comprehensive overview," *IEEE Access*, vol. 7, pp. 114975–115001, 2019.

[11] S. Jayalath and M. Hanif, "Generalized LCL-filter design algorithm for grid-connected voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 1905–1915, Mar. 2017.

[12] X. Ruan, X. Wang, D. Pan, D. Yang, W. Li, and C. Bao, *Control Techniques for LCL-Type Grid-Connected Inverters*. Cham, Switzerland: Springer, 2018.

[13] S. Jayalath and M. Hanif, "AnLCL-filter design with optimum total inductance and capacitance," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6687–6698, Dec. 2017.

[14] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-Filter-Based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep. 2005.

[15] R. Pena-Alzola, M. Liserre, F. Blaabjerg, M. Ordonez, and Y. Yang, "LCL-filter design for robust active damping in grid-connected converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 4, pp. 2192–2203, Nov. 2014.

[16] C. Gurrola-Corral, J. Segundo, M. Esparza, and R. Cruz, "Optimal LCL-filter design method for grid-connected renewable energy sources," *Int. J. Electr. Power Energy Syst.*, vol. 120, Sep. 2020, Art. no. 105998.

[17] W. Tang, K. Ma, and Y. Song, "Critical damping ratio to ensure design efficiency and stability of LCL filters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 315–325, Jan. 2021, doi: 10.1109/TPEL.2020.3000897.

[18] K.-B. Park, F. D. Kieferndorf, U. Drofenik, S. Pettersson, and F. Canales, "Optimization of LCL filter with integrated intercell transformer for two-interleaved high-power grid-tied converters," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2317–2333, Mar. 2020.

[19] Y.-J. Kim and H. Kim, "Optimal design of LCL filter in grid-connected inverters," *IET Power Electron.*, vol. 12, no. 7, pp. 1774–1782, Jun. 2019.

[20] H. Oruganti, S. Dash, C. Nallaperumal, and S. Ramasamy, "A proportional resonant controller for suppressing resonance in grid tied multilevel inverter," *Energies*, vol. 11, no. 5, p. 1024, Apr. 2018.

[21] A. Kouchaki and M. Nymand, "Analytical design of passive LCL filter for three-phase two-level power factor correction rectifiers," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3012–3022, Apr. 2018.

[22] A. Lachichi, A. Junyent-Ferre, and T. Green, "Optimal design of a LCL filter for LV modular multilevel converters in hybrid AC/DC microgrids application," in *Proc. IECON - 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 3973–3978, doi: 10.1109/IECON.2018.8592846.

[23] D. Solatialkaran, F. Zare, T. K. Saha, and R. Sharma, "A novel approach in filter design for grid-connected inverters used in renewable energy systems," *IEEE Trans. Sustain. Energy*, vol. 11, no. 1, pp. 154–164, Jan. 2020.

[24] M. Dursun and M. K. Dosoglu, "LCL filter design for grid connected three-phase inverter," in *Proc. 2nd Int. Symp. Multidisciplinary Stud. Innov. Technol. (ISMSIT)*, Oct. 2018, pp. 1–4, doi: 10.1109/ISMSIT.2018.8567054.

[25] Y. Liu, "LCL filter design of a 50-kW 60-kHz SiC inverter with size and thermal considerations for aerospace applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8321–8333, Oct. 2017.

[26] R. Pandey, R. Tripathi, and T. Hanamoto, "Comprehensive analysis of LCL filter interfaced cascaded H-Bridge multilevel inverter-based DSTATCOM," *Energies*, vol. 10, no. 3, p. 346, Mar. 2017.

[27] C. Mahamat, M. Petit, F. Costa, R. Marouani, and A. Mami, "Optimized design of an LCL filter for grid connected photovoltaic system and analysis of the impact of neighbors' consumption on the system," *J. Elect. Syst.*, 2017, vol. 13, no. 4, pp. 618–632.

[28] X. Renzhong, X. Lie, Z. Junjun, and D. Jie, "Design and research on the LCL filter in three-phase PV grid-connected inverters," *Int. J. Comput. Electr. Eng.*, vol. 5, no. 3, p. 322, 2013.

[29] A. Reznik, M. G. Simoes, A. Al-Durra, and S. M. Muyeen, "LCL filter design and performance analysis for small wind turbine systems," in *Proc. IEEE Power Electron. Mach. Wind Appl.*, Jul. 2012, pp. 1–7.

[30] A. A. Rockhill, M. Liserre, R. Teodorescu, and P. Rodriguez, "Grid-filter design for a multimegawatt medium-voltage voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1205–1217, Apr. 2011.

[31] A. Dastfan, H. Yassami, and M. R. Rafiei, "Optimum design of passive harmonic filter by using game theory concepts," *Intell. Syst. Elect. Eng. J.*, vol. 4, pp. 13–22, Dec. 2014.

[32] B. Alamri and M. Darwish, "Precise modelling of switching and conduction losses in cascaded h-bridge multilevel inverters," in *Proc. 49th Int. Univ. Power Eng. Conf. (UPEC)*, Cluj-Napoca, Romania, 2014, pp. 1–6, doi: 10.1109/UPEC.2014.6934613.

[33] B. Alamri and M. Darwish, "Power loss investigation for 13-level cascaded H-bridge multilevel inverter," *J. Energy Power Sour.*, vol. 2, no. 6, pp. 230–238, 2015.

[34] M. T. Elmathana, A. F. Zobaa, and S. H. E. Abdel Aleem, "Economical design of multiple-arm passive harmonic filters for an industrial firm–Case study," in *Proc. IEEE 15th Int. Conf. Harmon. Qual. Power*, Jun. 2012, pp. 438–444, doi: 10.1109/ICHQP.2012.6381242.

[35] *IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems*, Standards 519-2014, 2014

[36] *Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces*, Standards 1547-2018, 2018.

[37] B. Alamri and M. Darwish, "Power loss investigation in HVDC for cascaded H-bridge multilevel inverters (CHB-MLI)," in *Proc. IEEE Eindhoven PowerTech*, Jun. 2015, pp. 1–7, doi: 10.1109/PTC.2015.7232810.

[38] S. P. Sunddararaj, S. Srinivasarangan Rangarajan, and S. N, "An extensive review of multilevel inverters based on their multifaceted structural configuration, triggering methods and applications," *Electronics*, vol. 9, no. 3, p. 433, Mar. 2020.

[39] M. Arman and M. Darwish, "Critical review of cascaded H-bridge multilevel inverter topologies," *Int. Rev. Electr. Eng.*, vol. 4, no. 5, pp. 730–743, 2009.

[40] Infineon. (2020). *FZ400R65KE3 Datasheet*. [Online]. Available: https://www.infineon.com/dgdl/Infineon-FZ400R65KE3-DataSheet-v03_02-EN.pdf?fileId=db3a30433784a040013798ff06d02788

BASEM ALAMRI received the B.Sc. degree (Hons.) in electrical engineering from the King Fahd University of Petroleum and Minerals (KFUPM), the M.Sc. degree (Hons.) in electrical power systems from King Abdulaziz University, Jeddah, Saudi Arabia, the M.Sc. degree in sustainable electrical power from Brunel University, London, U.K., in 2007 and 2008, respectively, and the Ph.D. degree in electrical power engineering from Brunel University, in 2017. He is currently an Assistant Professor of Electrical Engineering with the College of Engineering, Taif University. His research interests include power systems, power quality, power filter design, and smart grids, with a particular emphasis on the integration of renewable energy sources with power grids. He is a member of many international and local professional organizations. He is also a Certified Energy Auditor (CEA®), Certified Energy Manager (CEM®), and a Certified Measurement & Verification Professional (CMVP®) of the Association of Energy Engineers (AEE), USA. He has received many awards and prizes, including a certificate from the Advance Electronics Company (AEC) in recognition of the Outstanding Academic Achievement during the B.Sc. degree with KFUPM. He also received the National Grid (NG) Prize, the Power Grid Operator in the U.K., for being the top distinction student of the M.Sc. degree of the SEP Program with Brunel.

YASSER MOHAMMED ALHARBI received the Ph.D. degree in electrical engineering from Curtin University, Australia. He is currently an Assistant Professor with the Department of Electrical Engineering, Taif University, Saudi Arabia. His research interests include renewable energy systems, power system stability, power electronics, power quality, and system simulation.