IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received October 21, 2020, accepted November 4, 2020, date of publication November 16, 2020,
date of current version December 2, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3038153

A Graphene Field-Effect Transistor Based Analogue Phase Shifter for High-Frequency Applications

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This work was supported in part by the Ministerio de Ciencia, Innovación y Universidades, Agencia Estatal de Investigación (AEI), European Regional Developments Fund (ERDF/FEDER), under Project TEC2017-89955-P and Project EQC2018-004963-P (MINECO/AEI/FEDER), in part by the FEDER/Junta de Andalucía-Consejería de Economía y Conocimiento under Project B-RNM-375-UGR18; and in part by the European Commission through the Horizon 2020 Project Wearable Applications Enabled by Electronic Systems on Paper (WASP) under Contract 825213. The work of Enrique G. Marin was supported by the Juan de la Cierva Incorporación under Grant IJCI-2017-32297 (MINECO/AEI). This work was supported by the European Union's Horizon 2020 Research and Innovation Programme under Grant GrapheneCore2 785219 and Grant GrapheneCore3 881603, in part by the Ministerio de Ciencia, Innovación y Universidades under Grant RTI2018-097876-B-C21(MCIU/AEI/FEDER, UE), in part by the European Regional Development Funds (ERDF) through the Programa Operatiu FEDER de Catalunya 2014-2020, with the support of the Secretaria d'Universitats i Recerca of the Departament d'Empresa i Coneixement of the Generalitat de Catalunya for emerging technology clusters to carry out valorization and transfer of research results, and in part by GraphCAT under Project 001-P-001702.

ABSTRACT We present a graphene-based phase shifter for radio-frequency (RF) phase-array applications. The core of the designed phase-shifting system consists of a graphene field-effect transistor (GFET) used in a common source amplifier configuration. The phase of the RF signal is controlled by exploiting the quantum capacitance of graphene and its dependence on the terminal transistor biases. In particular, by independently tuning the applied gate-to-source and drain-to-source biases, we observe that the phase of the signal, in the super-high frequency band, can be varied nearly 200° with a constant gain of 2.5 dB. Additionally, if only the gate bias is used as control signal, and the drain is biased linearly dependent on the former (i.e., in a completely analogue operation), a phase shift of 85° can be achieved making use of just one transistor and keeping a gain of 0 dB with a maximum variation of 1.3 dB. The latter design can be improved by applying a balanced branch-line configuration showing to be competitive against other state-of-the-art phase shifters. This work paves the way towards the exploitation of graphene technology to become the core of active analogue phase shifters for high-frequency operation.

INDEX TERMS Field-effect transistor (FET), graphene, phase shifters, quantum capacitance, radio-frequency (RF) devices.

I. INTRODUCTION

In the last few years the number of applications where graphene is involved has increased drastically in almost every field of electronics. Its use in flexible electronics [1], [2] along with its intrinsic material properties [3]–[10], have postulated it as one of the main candidates to play a leading role in the future of the industry. However, due to the absence of band gap in graphene and its consequent inability (at the device level) to be effectively turned off, this progress has been especially notorious in the field of RF electronics. Some examples of the main advancements can be found among radio-frequency (RF) power detection applications [11], high-frequency (HF) transmission lines [12], RF low power applications [13], fifth-generation (5G) antenna arrays [14], or printed sensing applications for the Internet of Things (IoT) [15]. However, in the RF field, there are still some electronics components that indeed play an essential role in multiple communication systems embedded in radars or satellites [16]–[18], that remain unexplored. One notorious case corresponds to phase shifters, elements of paramount importance in order to control and direct the main radiation lobe of

The associate editor coordinating the review of this manuscript and approving it for publication was Wenjie Feng.

antenna arrays. In particular, this ability of the arrays allows for a reduction in power consumption and an overall improvement of the signal-to-noise ratio (SNR) of the antenna [19], both crucial features in communication systems.

Although phase shifters are well-known RF systems, the design of purely analogue architectures, advantageous due to their higher precision and reduced complexity, has been technologically limited to two main approaches. First, the use of varactors as periodical loads of transmission lines, so to modify the equivalent circuit capacitance with a control voltage [20]–[23]. However, due to its passive nature, these topologies will always present some insertion losses (IL). Second, the implementation of transistor-based architectures either in all-pass filter configuration with a flat amplitude passing band and a voltage-dependent phase [24], or emulating the varactor structure by employing high electron mobility transistors [25].

An alternative strategy is getting the phase variation through a quadrature amplitude modulation (QAM) technique, where the so-called in-phase/quadrature (I/Q) signals (with a 90° phase difference between each other) feed two voltage gain amplifiers (VGAs), and are later added up. The resulting phase shift is controlled by changing the relative amplitudes of the I/O signals [26]–[31]. This strategy results in quite complex circuits (including the I/Q generator, VGAs, and signal adders) as well as a digital control system.

However, in spite of the increasing number of effective prototypes of graphene RF devices such as graphene field-effect transistors (GFETs) [32], as well as one-dimensional (1D) flexible RF diodes [33], none of them have already been explored for the aforementioned purpose. In this context, we propose a bias-controlled analogue phase shifter based on a GFET by taking advantage of the possibility of tuning the graphene quantum capacitance with the FET terminal biases thanks to its low density of states around the Dirac point [34]. Not only is the use of graphene-based technology for this application novel and relevant, but also the fact that the phase shift can be controlled solely by an analogue signal without impacting on its gain. In this regard, the proposed phase shifter architecture consists of only one device and the role of the control signal is played by the gate bias with the drain bias linearly depending on the former. The proposed design achieves a 85° phase shift, keeping a gain of 0 dB with a maximum variation of 1.3 dB. In order to reduce the source mismatch, the design is improved by applying a balanced branch-line amplifier configuration providing return losses higher than 30 dB. The performance and main figures of merit (FoMs) of the proposed graphene-based phase shifters are compared against the state-of-the-art with promising results.

II. GRAPHENE FET AS PHASE SHIFTER

The design and analysis of an RF phase shifter founded in graphene require a physics-based description of the electrical behavior of a GFET at a compact and analytical level suitable for standard circuit simulators. To this purpose, we employ the large-signal model implemented in Verilog-A by some of the authors [35], embedding it into Keysight Advanced Design System. This GFET compact model has been thoroughly validated in [36] by the assessment of the DC characteristics, transient dynamics, and frequency response of a variety of graphene-based circuits such as a HF voltage amplifier [37], a high-performance frequency doubler [38], a subharmonic mixer [39], and a multiplier phase detector [40] showing a very good agreement between measurements and simulations.

TABLE 1. Graphene technology parameters used in the design of the analogue phase shifter.

Variable	Value	Variable	Value
T	300 K	L	1 μm
μ	2000 cm^2/Vs	W	1 μm
V_{G0}	0 V	C_{ox}	0.11 pF/μm^2
Δ	0.1 eV		

In order to proceed with the device-level analysis, it is important to first introduce the graphene technology parameters considered within the design. Table 1 summarizes them, where T is the temperature; μ represents the effective carrier mobility; V_{G0} is the gate offset voltage; Δ is the inhomogeneity of the electrostatic potential due to electron-hole puddles; W and L are the channel width and length, respectively; and C_{ox} is the oxide capacitance per unit area.

The inspirational property of a GFET that postulates it as a candidate to be the core of an active analogue phase shifter is the bias-tunable quantum capacitance originated by the reduced density of states of graphene around the Dirac point [34]. To take advantage of this inherent property, the graphene quantum capacitance, C_q, has to be dominant over the gate geometrical oxide capacitance, $C_{ox} = \epsilon_0\epsilon_{ox}/t_{ox}$. In a metal-insulator-graphene structure C_{ox} and C_q are working in series [41], and therefore, achieving a design with $C_{ox} \gg C_q$ allows to leverage the C_q tunability. This effect can be observed by analyzing the intrinsic device capacitances (C_{ij}) of the GFET which relate the incremental charge (ΔQ_i) at a terminal i with a varying voltage (ΔV_j) applied to a terminal j assuming that the voltage at all the other terminals remains constant [35],

$$C_{ij} = \begin{cases} -\frac{\partial Q_i}{\partial V_j}, & i \neq j \\ \frac{\partial Q_i}{\partial V_j}, & i = j \end{cases} \tag{1}$$

where i and j stand for g (gate), d (drain), and s (source) respectively. The dynamic regime of a three-terminal GFET can be described by just four out of nine intrinsic capacitances [42], [43], C_{ij} in Eq. (1). In order to illustrate the device capacitive tunability with terminal biases, Fig. 1 shows the gate (V_{GS}) and drain (V_{DS}) bias dependences of the selected set of capacitances, namely C_{gs}, C_{gd}, C_{sd} and C_{dg}, considering the device technology described in Table 1. As can be observed, all intrinsic capacitances show large variations in the selected range of bias proving that, due to the C_q tunability, using a control signal based on V_{GS} and/or V_{DS} can be eventually

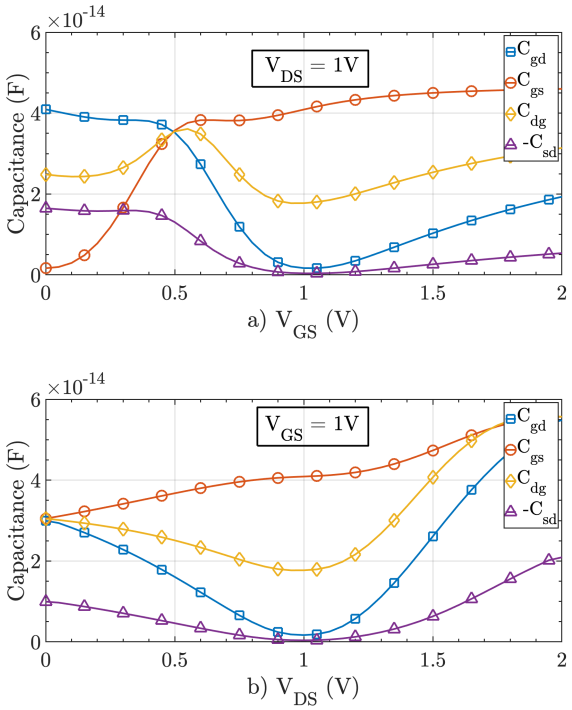

FIGURE 1. Intrinsic capacitances C_{gs} (red circles), C_{gd} (blue squares), C_{sd} (purple triangles) and C_{dg} (yellow diamonds) of the GFET employing the technology summarized in Table 1 versus (a) gate bias and (b) drain bias.

exploited for phase shifting operation through the variation of the capacitive response of the device.

To the purpose of selecting the RF band of operation, a bare and quick estimation of the RF performance limits of the GFET technology can be achieved by calculating the cut-off frequency, f_T, and maximum oscillation frequency, f_{max} [44], [45]. In particular, the expected RF FoMs for the technology described in Table 1 are $f_T = 18.9$ GHz and $f_{max} = 25.1$ GHz at $V_{GS} = V_{DS} = 1$ V. These values have been estimated considering that the source and drain metal-graphene contact resistances are limited to $R_s \cdot W = R_d \cdot W = 100\,\Omega\mu$m [46]–[48], respectively; and the gate resistance is $R_g \cdot L = 5\,\Omega\mu$m. As a rule of thumb, the operating frequency should be lower than 20% of f_{max} so as to guarantee sufficient power gain. In order to fulfill this requirement, we have opted for a design within the S-band of the spectrum. Specifically, the chosen operating frequency of the phase shifter is 3 GHz. Nevertheless, future improvements of the GFET technology would allow our design procedure to be extended beyond this frequency range.

III. PHASE SHIFTER GRAPHENE CIRCUIT

As it is known, an analogue phase shifter is expected to produce a phase shift in the output with respect to the input, as dictated by a control signal, while the amplitude of the output is minimally attenuated by a constant factor. In order to implement this concept using graphene, we propose a GFET operating in common-source (CS) configuration, thus forming a two-port network. As shown in Fig. 2, the RF

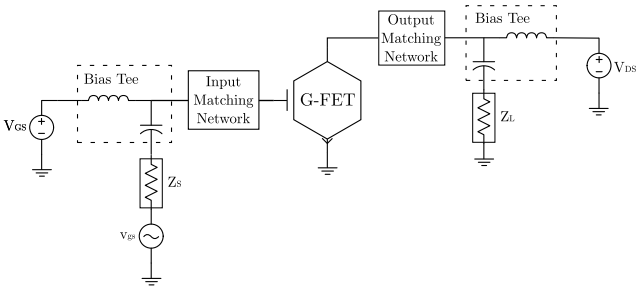

FIGURE 2. Schematic of the phase shifter. The GFET is used as the active element. IMN and OMN allow to maximize the power transfer from the source to the load and, at the same time, minimize signal reflection from the load. Bias tees at both input and output ports are considered, each one consisting of an ideal capacitor to allow the AC through but uncoupling the DC, and an ideal inductor to allow the DC through but uncoupling the AC signal.

signal and DC biases are combined by using bias tees consisting of L/C networks which properly block the AC/DC components, respectively. Source and load impedances, Z_S and Z_L respectively, are assumed equal to the characteristic impedance, set to $Z_0 = 50\,\Omega$. In order to achieve a good power transfer, two matching networks are employed; while to the purpose of gaining stability, a shunt resistor of 1.65 kΩ is added to the gate of the GFET even though this will entail some gain losses. Unconditional stability is achieved for V_{GS} and $V_{DS} = 1$ V, which allows us to calculate the reflection coefficients Γ_S and Γ_L for the maximum available gain (MAG). Input and output matching networks (IMN and OMN, respectively) are designed to simultaneously satisfy $\Gamma_{in} = \Gamma_S^*$ and $\Gamma_{out} = \Gamma_L^*$ so as to yield conjugate matching in both ports. Both matching networks are composed by a shunt capacitor ($C_{IMN} = 465.26$ fF, $C_{OMN} = 55.13$ fF) and a series inductor ($L_{IMN} = 35.07$ nH, $L_{OMN} = 37.32$ nH). The IMN is configured in a C-L topology while the OMN is configured in a L-C topology. It is important to note that the lumped components here used are assumed to be ideal. Tolerance and quality factor (Q) issues associated with them could affect the design and, therefore, they should be analyzed in detail for the integrated circuit technology employed in an eventual realization of the circuit.

In a phase controlled antenna array, the phase shifter feeds each element of the array in a way that the amplitude and phase difference of the input current at each element determine the shape and direction of the main lobe of radiation, respectively. Thus, for a proper array design, it is of utmost relevance to be able to select the direction of the main lobe (changing the relative phases between the input signals of the antennas), while keeping the shape of the radiation pattern unaltered (maintaining the signal amplitudes of all elements balanced). Therefore, in terms of the scattering (S) parameters, a two-port phase shifter feeding each antenna must be able to keep the magnitude of S_{21} ($|S_{21}|$) constant while tuning its phase in a controlled way (ϕ_{21}), where ports 1 and 2 of the system refer here to the gate-source and drain-source terminals, respectively. The rest of the S parameters (S_{11}, S_{12} and S_{22}) are also important to guarantee an acceptable power

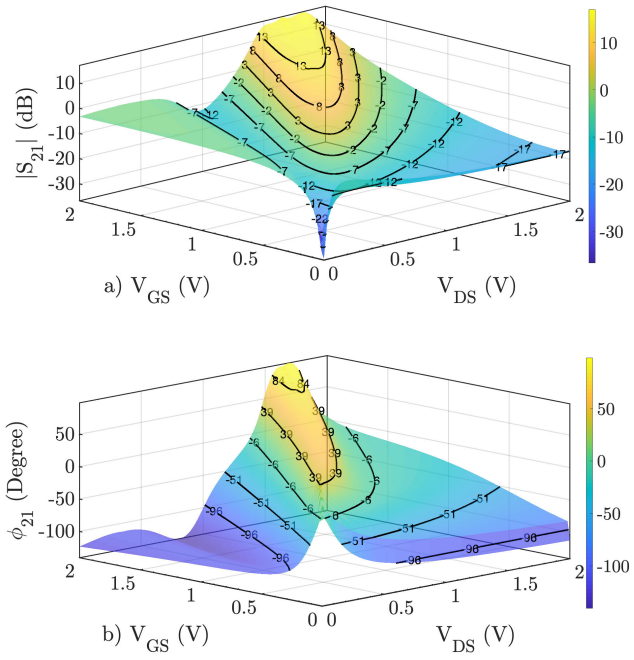

FIGURE 3. Isocurve plots of a) $|S_{21}|$ (dB) and b) ϕ_{21} (Degree) versus both V_{GS} and V_{DS}.

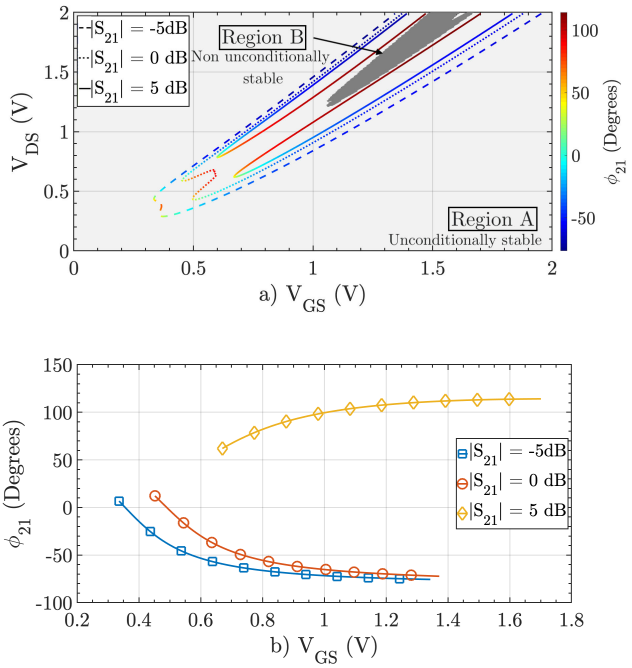

FIGURE 4. a) Bias dependence of the phase shift ϕ_{21} for three gain values $|S_{21}| = -5$ dB (dashed line), 0 dB (dotted line) and 5 dB (solid line). Bias combinations that do not guarantee unconditional stability for the device are coloured in dark grey, and are represented by region B. b) Gate bias dependence of the phase shift for the same three constant gain values by considering that the drain bias is simultaneously modified to mantain the selected $|S_{21}|$ value (analogue control).

transfer from the input to the output and are addressed by the proper design of the IMN and OMN.

In particular, IMN and OMN in Fig. 2 are optimized in order to achieve a value of the matching coefficient (M) as high as possible. Generally, matching networks are designed for a single bias point, but in this case, both V_{GS} and V_{DS} of the GFET have to be changed so to enable the phase shifting while keeping a constant amplitude, so it is crucial to have a high M value for a large window of V_{GS} or V_{DS} combinations. In this regard, we have assessed that M is over 0.7 for the bias window under test.

In the design of Fig. 2, we expect that, by changing V_{GS} or V_{DS}, the intrinsic capacitances of the GFET will vary, as shown in Fig. 1a, and so will do ϕ_{21}. The interest of the design is to keep at the same time a constant $|S_{21}|$. In order to better understand the ϕ_{21} and $|S_{21}|$ dependencies on the bias, Figs. 3a and 3b depict their corresponding isocurves as a function of V_{DS} and V_{GS}. As can be observed, both $|S_{21}|$ and ϕ_{21} show a strong dependence on V_{DS} and V_{GS} what can be exploited for the design of the phase shifter. It should be highlighted that each isocurve of Figs. 3a and 3b provides a $V_{GS} - V_{DS}$ combination ensuring a constant $|S_{21}|$ and ϕ_{21}. Moreover, the phase isocurves depict a different dependence on $V_{GS} - V_{DS}$ compared to amplitude isocurves, unveiling the possibility of applying a bias combination (i.e., a simultaneous variation of both V_{GS} and V_{DS}) such that, harnessing the quantum capacitance tunability of graphene, would yield a constant amplitude while the phase is appropriately modified.

It is also interesting to note here that it would be possible to change the design technique and playing with the amplitude of the output signal ($|S_{21}|$) while maintaining a constant phase shift ϕ_{21}, and this result would also be of notable interest as it would allow the radiation pattern to change while keeping the direction of the main lobe.

Following on with the phase shifter design, Fig. 4a shows the ϕ_{21} variation (color scale) as a function of the bias combinations that keep a constant value of $|S_{21}|$: -5 dB (dashed line), 0 dB (dotted line) and 5 dB (solid line). In order to ensure the unconditional stability of the circuit, the so-called K-Δ test [49] is carried out. In that regard, Fig. 4a shows two different regions denoted as A (light grey) and B (dark grey). Region A represents the bias combinations where unconditional stability is achieved. As for Region B, it contains the bias points where the stability of the circuit cannot be assured, i.e., there are bias combinations inside Region B where either the stability is conditioned or the circuit is directly unstable. For this reason, we have chosen to restrict the design to Region A, ensuring that the circuit is unconditionally stable.

Using a purely digital control, i.e., allowing any possible $V_{GS} - V_{DS}$ combinations that provide a constant specific gain, would result in large phase shift ranges, e.g. $\Delta\phi_{21} \simeq 180°$ keeping $|S_{21}| = 0$ dB. If an analogue control is considered, i.e., a linear relation is forced between V_{DS} and V_{GS}, the range of $\Delta\phi_{21}$ diminishes. Nevertheless, the analogue control would rely only on one signal, e.g., V_{GS}, and an extraordinary simple control circuit would be required (that may be implemented by a DC-DC converter, or in case efficiency is not a constraint, a simple voltage divider). This outstanding linear relation between both biases can be estimated for each

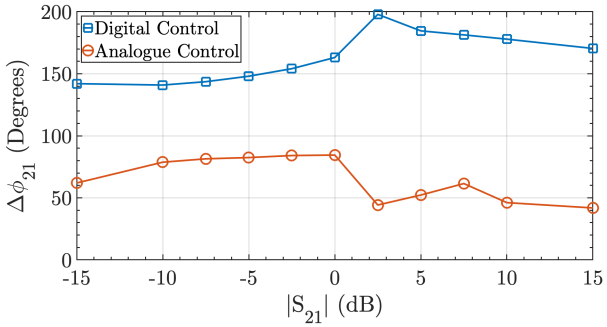

FIGURE 5. Maximum feasible phase shift range with digital (blue squares) and analogue (red circles) control versus $|S_{21}|$.

$|S_{21}|$ isocurve by applying a standard linear regression and ensuring that the determination coefficient (R^2) is higher than 0.9999. In this regard, Fig. 4b) shows the performance of the analogue controlled phase shifter, demonstrating $\Delta\phi_{21}$ values higher than 50° for the three gain values considered and with a remarkable value of $\Delta\phi_{21}$ higher than 80° for $|S_{21}| = 0$ dB.

As the maximum phase shift range $\Delta\phi_{21}$ depends on the gain value, we have evaluated it under two scenarios: (i) when the digital control is selected, and (ii) when the linear relation between V_{GS} and V_{DS} is assumed. The results are depicted in Fig. 5, where $\Delta\phi_{21}$ is plotted for gains ranging from -15 dB up to 15 dB, considering either a digital or an analogue control. According to Fig. 5, $|S_{21}| = 0$ dB happens to be in good trade-off between power gain and phase shift when designing an analogue phase shifter. It should be highlighted that it is possible to obtain a higher gain at the expense of losing some phase shift. This trade-off, however, can be balanced with the inclusion of an additional amplifier in the design of the phase shifter.

In order to evaluate the variations in $|S_{21}|$ that the purely analogue control of the phase shifter induces (due to the small depart from linearity of the actual $V_{GS} - V_{DS}$ combinations), Fig 6a depicts the outcome of the analogue controlled phase shifter for $|S_{21}| = 0$ dB. As can be seen, when forcing the linear relation for $V_{GS} - V_{DS}$, still a 85° phase shift range is achieved while satisfying a gain of 0 dB and a maximum variation of 1.3 dB of $|S_{21}|$.

Fig. 6b completes the analysis of the analogue controlled phase shifter showing the compression point at 1 dB (CP 1 dB) and the third order interception point (IP3) as main FoMs to assess the linearity of the amplifier. The CP 1 dB is considerably low (lower than -30 dBm for the worst case), which limits the input power of the phase shifter to -30 dBm. When using this device in reception applications, the signal may be free from any distortion as the power of the received signals in most of the wireless transmission protocols is typically lower than that value. However, the current design for the graphene phase shifter would be quite limited for transmission applications, and power stages should be added after it to provide enough power to the transmitted signal. In any case, due to the likely interest of using the proposed phase shifter as both, transmitter and receiver, a bidirectional configuration of the device is proposed in Appendix A. In spite of this, it is worth to mention that improvements in the performance of GFET technology are expected in the future [50], so that this non-linear behavior should be improved.

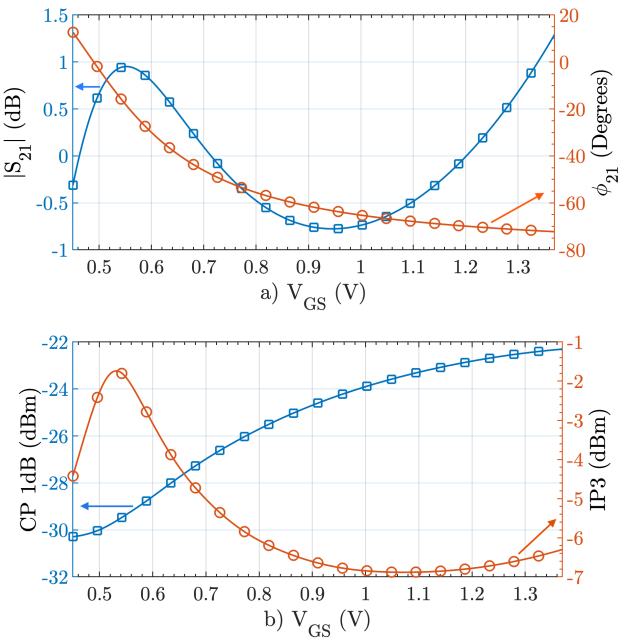

FIGURE 6. a) $|S_{21}|$ (blue squares) and ϕ_{21} (red circles) variation; and b) compression point at 1 dB (blue squares) and third order interception point (red circles) versus the analogue control provided by the gate bias.

It is also important to mention that a frequency analysis of the proposed phase shifter has been carried out. The results show that the phase shifter in its current form is only suitable to work in narrowband applications. Further developments should be implemented in order to increase the bandwidth of the circuit, and in particular input and output wideband matching networks should be used.

We have carried out in Table 2 a comparison among different state-of-the-art topologies currently employed to implement phase shifters and the one proposed in this work. In terms of the IL, our proposal is the only one that is able to supply some gain to the signal, thanks to the use of an amplifier configuration based on the GFET. On the other hand, the main limitations of our design are: (i) return losses (RL) are still limited to poor values, and (ii) the range of phase shift is not the widest, although this is to a certain point balanced by the particular simplicity of the analogue control hardware.

With the aim of attaining a better performance in terms of return losses, we explore the feasibility of using a balanced configuration with a branch-line coupler. The attention paid to the achievement of flat insertion losses and a wide range of phase shift, may lead to a degradation of the standing-wave-ratio (SWR) at input and output ports, thus endangering the power generator as the reflected power could be too high. In our particular situation, we are continuously changing the bias of the device, and therefore operating the device in different bias points to those for which the matching networks

TABLE 2. Comparison among state-of-the-art phase shifter topologies.

Shift Method	Control Type	Frequency (GHz)	IL (dB)	RL (dB)	$\Delta\phi$ (Degrees)	Reference
Switched Line	Digital	13-18	2.7	22	349.3	[51]
Reflection type	Analogue	2	1	13.4	385	[52]
Network type	Digital	0.5-1	2.5	13	360	[53]
Loaded Transmission Line	Analogue	1	2	15	183	[54]
GFET CS Amplifier	Digital	3	-2.5	0.9	197.9	This work
GFET CS Amplifier	Analogue	3	0	0.4	84.5	This work
Balanced Amplifier	Analogue	3	0	30.4	85.5	This work

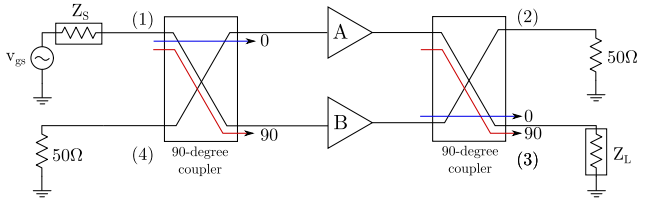

FIGURE 7. Schematic of the balanced amplifier. Two amplifiers, A and B, are used along with two 90° hybrid couplers. The schematic of the amplifiers is shown in Fig. 2.

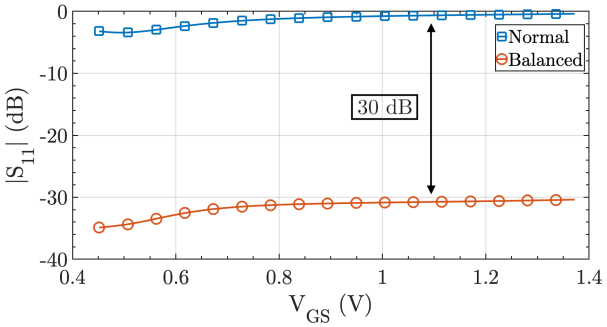

FIGURE 8. Comparison of the $|S_{11}|$ parameter (blue squares) of the former configuration presented in Fig. 2 and of the balanced amplifier (red circles) presented in Fig. 7.

were originally designed. This is the reason why the analysis of the return losses shown in Table 2 gives poor results in the worst case. The adoption of a balanced configuration solves this issue by using two hybrid couplers at input and output ports, along with two amplifiers [55]. The schematic of the circuit designed to this purpose is depicted in Fig. 7. The hybrid coupler is characterized by its scattering parameters, which can be ideally described as:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{2}$$

So that, if all ports of the coupler are matched, the power entering into port 1 is evenly divided between ports 2 and 3, with a 90° phase shift one with respect to the other. Port number 4 is isolated, so no power would be coupled to it [49]. With the proper analysis, the global parameters of the network S_{11} and S_{21} can be calculated by following Eqs. (3) and (4), respectively, where a and b subscripts denote the S-parameters of A and B amplifiers respectively. It is of special interest the case where both amplifiers are alike, as in this case $S_{11} = S_{22} = 0$ and S_{21} is equal to the gain of one of the parallel branches of the coupler (with a phase shift of 90°). This means that it is possible to get rid of any reflected power at the input port, with no gain losses, at the cost of a higher complexity of the circuit.

$$S_{11} = \frac{e^{-j\pi}}{2}(S_{11a} - S_{11b}) \tag{3}$$

$$S_{21} = \frac{e^{-j\frac{\pi}{2}}}{2}(S_{21a} + S_{21b}) \tag{4}$$

Finally, Fig. 8 compares S_{11} as a function of the device bias for the single branch configuration (Fig. 2) and the alternative balanced configuration (Fig. 7). As expected, the results show that as both branches of the design are identical, the reflection coefficient is strongly diminished, providing a reduction of more than 30 dB in S_{11}. Adopting this new configuration, the return losses are RL = 30.4 dB for the worst case, which makes the balanced amplifier phase shifter topology comparable to the rest of the technologies considered in Table 2. Again, the use of this balanced configuration is possible thanks to the use of an amplifier configuration based on the GFET.

As for the phase shift range shown in Table 2, even though our solution yields a range which is one-fourth of other state-of-the-art devices, it does not preclude its use for numerous applications: many antenna arrays would need no more than 10° shift in their pointing, for which a controllable phase shift of 80° is enough.

A broader phase shift range would be easily achieved by cascading several balanced amplifiers. As the reflection parameter of the balanced amplifier configuration of the phase shifter is extremely low, the cascading would be successfully obtained and, therefore, a multi-stage phase shifter can be readily attained. Eventually, if we cascaded four of these balanced structures, a phase shift range of around 360° would be obtained, making our device fully competitive with other ones in terms of phase shift range.

IV. CONCLUSION

This work presents a graphene-based phase shifter operating in the S-band, able to produce a phase shift on an input RF signal while maintaining a constant gain. Quantum capacitance tunability of graphene is leveraged in order to achieve this phase modulation, combined with an original design procedure. Phase shifts higher than 180° are possible, as well as gains above 15 dB, due to the amplifier configuration adopted with the GFET as the core element. Moreover,

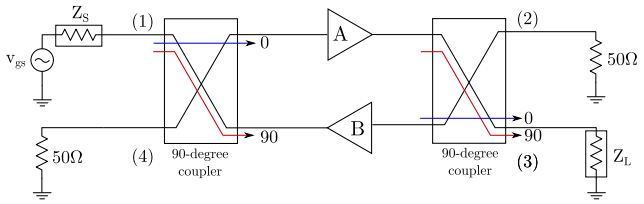

FIGURE 9. Schematic of the balanced amplifier in a bidirectional operation. In this case, amplifier B is mirrored vertically, so that its input is fed in port 3, and the output is extracted from port 1. The schematic of the amplifiers employed in this design is depicted in Fig. 2.

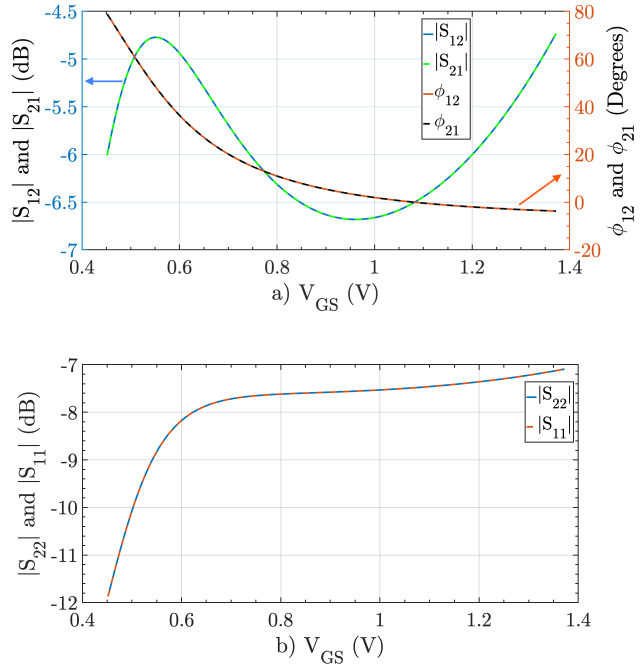

FIGURE 10. a) $|S_{12}|$ and ϕ_{12} variation and b) $|S_{22}|$ and $|S_{11}|$ variation versus V_{GS}.

a completely analogue operation has been demonstrated achieving a phase shift of up to 84.5° and keeping a maximum variation of 1.3 dB. The RL have been considerably increased by using a balanced configuration based on the amplifier topology employed. These results demonstrate the potential of graphene technology for the future development of improved high-frequency applications and in particular for analogue phase shifters.

APPENDIX A
BIDIRECTIONAL OPERATION

This Appendix shows the results of employing the balanced amplifier phase shifter simultaneously as a transmitter and as a receiver. These calculations are of great importance, as they may be required for its application in phased-array techniques in reception and transmission, thus improving the global efficiency of the system not just in one direction but in both. This device is made by vertically mirroring amplifier B from the topology shown in Fig. 9 so that its input is fed in port 3 and the output is extracted from port 1. The final schematic is shown in Fig. 9.

In the bidirectional system, $S_{22} = S_{11}$ and $S_{12} = S_{21}$. As can be seen in Fig. 10a, the shape of the amplitude and phase of the bidirectional amplifier is the same shown in Fig. 6a, but instead of 0 dB now we have a −6 dB gain, which is still acceptable even though it means we are lossing some power. The phase is also shifted but the range of variation remains identical. The reflection parameter $|S_{22}| = |S_{11}|$ shows in Fig. 10b values lower than −7 dB for the worst case. Although this value is not optimal, it is still acceptable. In conclusion, we have demonstrated a system able to work as a phase shifter in both directions symetrically with a −6 dB gain and RL = 7 dB for the worst case.

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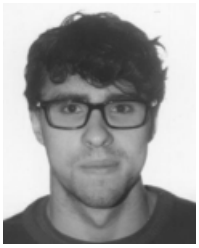

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