An Asymmetric Short-Circuit Fault Ride-Through Strategy Providing Current Limiting and Continuous Voltage Supply for Three-Phase Three-Wire Stand-Alone Inverters

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ABSTRACT The three-phase three-wire stand-alone inverter is required to have short-circuit fault ride-through ability to achieve continuity of power supply. Generally the inverter works in current-controlled mode in symmetric short-circuit conditions, but voltage limiting and harmonic distortion will appear under this method when asymmetric short-circuit fault occurs. Several existing methods for asymmetric fault ride-through can achieve current limiting without voltage limiting, however, none of them can guarantee that the healthy phase voltage keeps constant before and after fault. This article proposes a fault ride-through strategy for asymmetric short-circuit conditions, which not only keeps the healthy phase voltage constant with different loads, but also makes the fault phase current limited and controllable. This goal is achieved by a simple control structure combining α-axis voltage control and β-axis current control at the same time. Furthermore, the voltage and current characteristics of this method under different load conditions have been analyzed, the analysis results indicate that the impact of different loads on fault ride-through performance is almost negligible. The correctness of theoretical analysis and the effectiveness of proposed strategy is verified by experimental results.

INDEX TERMS Asymmetric short-circuit, fault ride-through, current limiting, three-phase three-wire stand-alone inverter.

I. INTRODUCTION

With the development of industrial technology, the three-phase stand-alone inverter is playing a more and more important role in various applications, such as Uninterruptible Power Supply (UPS), distributed power system, microgrid and so on, which requires high commands on power quantities, power supply continuity and reliability [1]–[5]. The inverter should supply the load continuously and steadily. It is required to cope with abnormal conditions and have fault ride-through ability. In numerous abnormal conditions, short-circuit fault is the most severe one, the fault current must be limited to avoid damaging the power semiconductor

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devices [6]–[9]. Normally one inverter would supply multiple loads, which may include some critical loads. For these critical loads, there are high reliability requirements, and the loss of output voltage is unacceptable. Thus, selective protection is necessary, and the inverter needs to have the ability to achieve fault ride-through without shutdown [10], [11]. When one of the loads suffered a short-circuit fault, appropriate control strategy should be adopted to cooperate with the protection devices to clear the fault branch quickly, and then resume normal power supply after the fault is cleared, thereby the selective protection has been realized [10]–[12]. Moreover, the three-phase inverter including three-phase three-wire inverter usually feeds some single-phase loads, and their power supply should not be affected by other phases, even if other phases fail.

Several references have investigated the short-circuit fault ride-through method [11]–[14]. Usually the dual loop controller (outer voltage loop and inner inductor current loop) in synchronous reference frame (*dq* frame) is adopted in three-phase stand-alone inverter. The inverter works in voltage-controlled mode (VCM) in normal condition, while working in current-controlled mode (CCM) during the short-circuit fault [13]. The inverter will return to the VCM from CCM after the fault is cleared. Current limiting can be guaranteed by the saturation block of voltage loop [15]. This control method could work well in three-phase symmetric short-circuit fault. However, voltage limiting and harmonic distortion would appear under asymmetric faults [16]. As a result, the output current cannot be controlled as expected, and the power semiconductor devices may be damaged.

Focusing on the fault ride-through issue under asymmetric short-circuit situation, firstly this article makes the goals of fault ride-through process clear, which are:

1) the healthy phase voltage should keep constant before and after fault and under different loads;

2) the fault phase current should be limited and controllable to trigger the action of protection devices like breakers to clear the fault branch.

These goals are easy to achieve in three-phase four-wire system since the fault phases could work in CCM while the healthy phases continue to work in VCM during the fault [17]–[19]. But in the three-phase three-wire system, there are physical constraints on the voltage and current between the three phases, so the three phases cannot be controlled separately, which makes the asymmetric fault ride-through problem more difficult.

In order to accomplish the current limiting control of three-phase three-leg stand-alone inverter during asymmetrical fault without output voltage limiting, the mechanism of the voltage limiting under asymmetrical fault was investigated in [20] and a current limiting strategy with the current limiting references regulated by an introduced phase angle was proposed. However, all phases worked in CCM with different references, which means the voltage of healthy phase could not keep constant in different load conditions, also there is no guarantee of immutability before and after the fault. So that the power supply of healthy phase load will be affected. In [21], a current limiting strategy with parallel virtual impedance was proposed. The drawback of this method is that the design procedure of virtual impedance is complicated and the system stability issue should be concerned carefully due to the introduction of virtual impedance.

These controllers proposed in [20] and [21] are both implemented in *abc* frame. Another way is to control in *dq* frame. A sequence-based control strategy with current limiter was proposed in [22]. There are separate controllers in *dq* frame in positive- and negative-sequence to deal with the unbalanced voltage and current signals while the current limiter is accomplished in *abc* frame. However, this control structure is too complicated since the controllers are established

in both positive- and negative-sequence, and a total of ten coordinate transformation operations are needed. Besides, all the methods proposed in [20]–[22] have a common problem, the RMS value of healthy phase voltage cannot keep constant before and after fault, and it also cannot keep constant if the load changed during the fault ride-through process. Thus, the power supply continuity and reliability of healthy phases cannot be guaranteed even though the fault occurs in other phases.

In order to achieve these goals of asymmetric fault ride-through process, this article proposes a fault ride-through strategy, whose control structure is established in $\alpha\beta$ frame. The main idea is to assign different tasks of α-axis and β-axis controller, the β-axis controller worked in CCM to limit current during the fault, while the α-axis controller still worked in VCM to supply the load of healthy phase continuously and steadily. Another advantage of this proposed method is that its control algorithm is very simple. The theoretical analysis and experimental verification prove that the proposed fault ride-through strategy could work well and is a pretty good solution in asymmetric short-circuit fault ride-through occasions.

The rest of this article is organized as follows. Section II presents the proposed asymmetric short-circuit fault ride-through strategy and explains its principle. The voltage and current characteristics under this method and its influence on selective protection and fault ride-through are studied in Section III. Experimental verifications are shown in Section IV. Finally, conclusions are drawn in Section V.

II. PROPOSED FAULT RIDE-THROUGH STRATEGY

There are three types of asymmetric faults in the three-phase power supply system: single line-to-ground fault, double line-to-ground fault and line-to-line fault. For a three-phase three-wire system, there is no ground terminal connected to the loads [23]. The insulation fault to ground is another type of fault, the control system of the inverter cannot help to clear the fault and cannot play a role in fault handling in this case, and the leakage protection devices are needed to work. Thus, only the line-to-line fault is addressed in this article.

As mentioned above, the goals of the fault ride-through process should be defined clearly first. When the asymmetric short-circuit fault occurs, the fault phase current should be limited to protect the power semiconductor devices, then the protection devices like breakers will be triggered to clear the fault branch, so that the selective protection can be realized. In the meanwhile, the healthy phase needs to be supplied continuously and steadily. Thus, these goals require that the healthy phase should be controlled as voltage source while the fault phase should be controlled as current source.

This section first derives the circuit model of the three-phase three-wire stand-alone inverter under asymmetric short-circuit fault, then a fault ride-through method is proposed, whose control structure is established in $\alpha\beta$ frame. The β-axis controller works in CCM while the α-axis controller still works in VCM during the fault.

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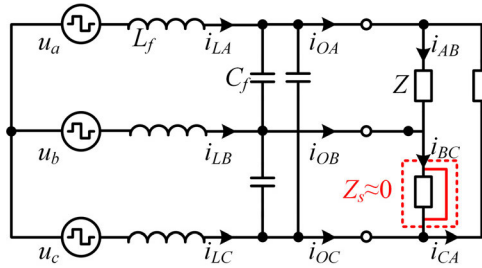
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FIGURE 1. The equivalent circuit under phase BC short-circuit fault.

A. CIRCUIT MODEL

If the short-circuit fault occurs between phase B and phase C, the equivalent circuit is shown in Fig.1, and the other cases can be analyzed in a similar way. In Fig.1, u_a, u_b, u_c represent the arm voltage of each phase, and i_{LA}, i_{LB}, i_{LC} represent the inductor current of each phase. The output voltage and current can be expressed as (1)-(3), where v_{AB}, v_{BC}, v_{CA}, i_{AB}, i_{BC} and i_{CA} are the output line-to-line variables, while v_A, v_B, v_C, i_{OA}, i_{OB} and i_{OC} are the output phase-to-neutral variables.

$$\begin{cases} v_{AB} = i_{AB} \cdot Z \\ v_{BC} \approx 0 \\ v_{CA} \approx -v_{AB} \end{cases} \tag{1}$$

$$\begin{cases} v_A = \dfrac{v_{AB} - v_{CA}}{3} = \dfrac{2}{3}v_{AB} = \dfrac{2}{3}i_{AB} \cdot Z \\ v_B = \dfrac{v_{BC} - v_{AB}}{3} = -\dfrac{v_{AB}}{3} \\ v_C = v_B = -\dfrac{v_{AB}}{3} \end{cases} \tag{2}$$

$$\begin{cases} i_{OA} = i_{AB} - i_{CA} = \dfrac{2v_{AB}}{Z} \\ i_{OB} = i_{BC} - i_{AB} = i_{BC} - \dfrac{v_{AB}}{Z} \\ i_{OC} = i_{CA} - i_{BC} = -i_{BC} - \dfrac{v_{AB}}{Z} \end{cases} \tag{3}$$

Suppose that the impedance of each phase is Z before the fault occurs. Then BC phase short-circuit fault occurs and Z_s represents the impedance of BC phase during the fault. This article only discusses the metallic short-circuit fault, which is the severest situation, and Z_s is almost equal to 0 in this case.

Note that the healthy phase should be controlled as voltage source while the fault phase should be controlled as current source to achieve the aims of the asymmetric short-circuit fault ride-through. However, there are physical constraints on the voltage and current between the three phases. Actually there are only two control degrees of freedom due to the coupling between the three phases. The control goals of healthy phase and fault phase are different and independent. It is difficult to achieve the control target that the healthy phase works in VCM and the fault phase works in CCM if the controller is implemented in *abc* frame. Moreover, it should be noted that the output currents of phase B and phase C are not only related to the short-circuit current (i_{BC}), but also to the load, which means that they contain the information of both the fault phase and the healthy phase. This makes their physical meaning unclear, and it is difficult to determine the

voltage and current references in *abc* frame to achieve the purpose of current limiting. Consequently, the controllers can be implemented in $\alpha\beta$ frame. The voltage and current of α and β axis can be controlled separately.

Transforming the mathematical model to $\alpha\beta$ frame, the expressions of output voltage and current in $\alpha\beta$ frame are given in (4) and (5).

$$\begin{bmatrix} v_{O\alpha} \\ v_{O\beta} \end{bmatrix} = \begin{bmatrix} \dfrac{2}{3} & -\dfrac{1}{3} & -\dfrac{1}{3} \\ 0 & \dfrac{1}{\sqrt{3}} & -\dfrac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}$$

$$= \begin{bmatrix} v_A \\ 0 \end{bmatrix} = \begin{bmatrix} \dfrac{2}{3}v_{AB} \\ 0 \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} i_{O\alpha} \\ i_{O\beta} \end{bmatrix} = \begin{bmatrix} \dfrac{2}{3} & -\dfrac{1}{3} & -\dfrac{1}{3} \\ 0 & \dfrac{1}{\sqrt{3}} & -\dfrac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} i_{OA} \\ i_{OB} \\ i_{OC} \end{bmatrix}$$

$$= \begin{bmatrix} \dfrac{2v_{AB}}{Z} \\ \dfrac{2\sqrt{3}}{3}i_{BC} \end{bmatrix} = \begin{bmatrix} i_{OA} \\ \dfrac{2\sqrt{3}}{3}i_{BC} \end{bmatrix} \tag{5}$$

From (4) and (5), it can be known that the voltage and current of α axis reflect the information of healthy phase. The current of α axis depends on the load of healthy phase. While the voltage and current of β axis reflect the information of fault phase. Its voltage is almost equal to 0 due to the short-circuit fault, and its current is related to the current of phase BC, which should be limited.

B. PROPOSED CURRENT LIMITING AND FAULT RIDE-THROUGH STRATEGY

Based on the above analysis, a current limiting and fault ride-through strategy is proposed in this article. The control diagram in the normal condition is shown in Fig.2(a), outer output voltage loop and inner inductor current loop in $\alpha\beta$ frame is adopted, and the control structures of α and β axis are the same. When a short-circuit fault occurred in phase BC, the dual loop is still adopted in α axis to supply the load of healthy phase, while current limiting control is adopted in β axis to protect the power semiconductor devices from damage and trigger the action of protection devices like breakers to clear the fault branch, as shown in Fig.2(b), where the PR controller is adopted to eliminate steady-state error. The design method of PR controller has been widely studied [24], [25], this article will not repeat it.

The references of control system in the normal condition are given in (6), where V_N is the RMS value of rated line-to-line voltage, and φ_α is the initial angle.

$$\begin{cases} v^*_{\alpha\_pre} = \dfrac{\sqrt{2}V_N}{\sqrt{3}}\cos(\omega t + \varphi_\alpha) \\ v^*_{\beta\_pre} = \dfrac{\sqrt{2}V_N}{\sqrt{3}}\cos(\omega t + \varphi_\alpha - \dfrac{\pi}{2}) \end{cases} \tag{6}$$

In order to supply the load of healthy phase continuously and steadily during the fault, the line-to-line voltage
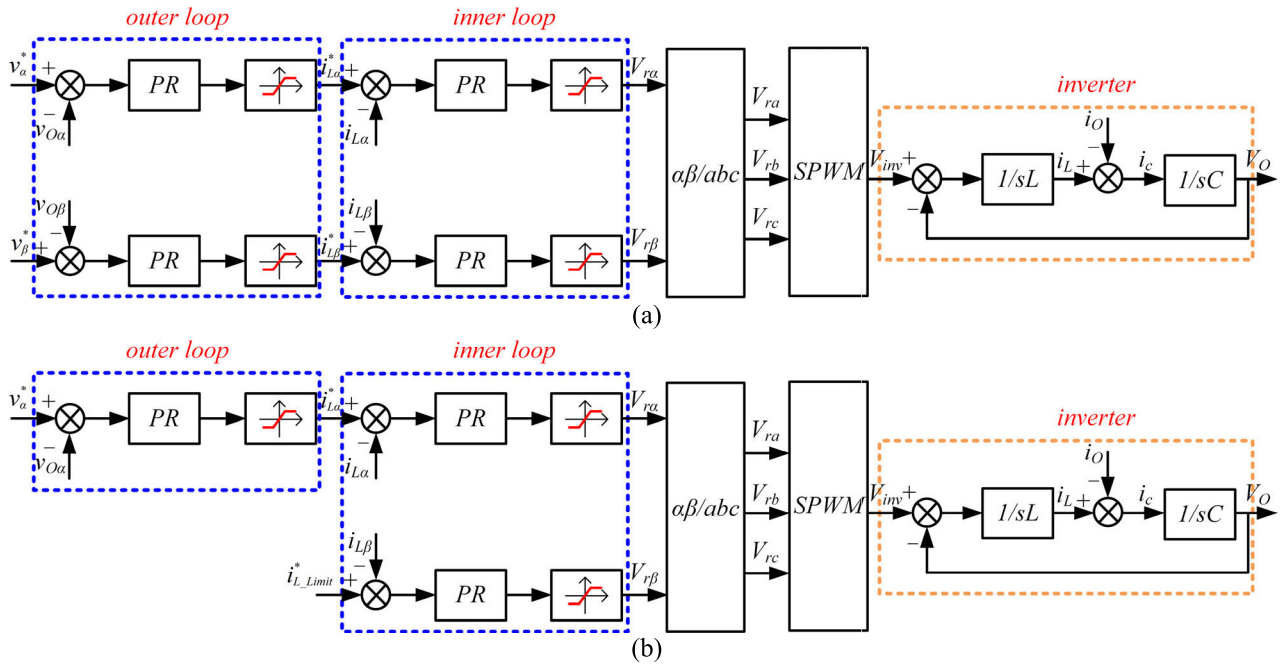
FIGURE 2. Control diagrams. (a) in the normal condition; (b) during the asymmetric short-circuit fault.

(RMS value) of healthy phase, namely the value of V_{AB}, should keep constant. Thus, the amplitude of v_α^* should be $2/\sqrt{3}$ times before the fault according to (4). The phase angle of v_α^* can keep constant before and after fault, which means v_{AB} will have a phase change. To simplify the control algorithm, the phase angle of i_β^* keeps consistent with $v_{\beta\_pre}^*$, and the output current behaviors in *abc* frame will be analyzed in Section III. Thus, the references of control system during the fault are given in (7), where $I_{L\_Limit}^*$ is the current limit value.

$$\begin{cases} v_\alpha^* = \dfrac{2\sqrt{2}V_N}{3}\cos(\omega t + \varphi_\alpha) = \dfrac{2}{\sqrt{3}}v_{\alpha\_pre}^* \\ i_\beta^* = \sqrt{2}I_{L\_Limit}^* \cos(\omega t + \varphi_\alpha - \dfrac{\pi}{2}) \end{cases} \quad (7)$$

If the short-circuit fault occurs in phase AB or phase CA, this strategy still works, only needs to change the reference angles of $\alpha\beta$ coordinate system, as shown in Fig.3. In these two cases, the new coordinate system is named $\alpha'\beta'$ and $\alpha''\beta''$ coordinate system, respectively. Equation (7) needs to be rewritten as (8) and (9) in phase CA and phase AB short-circuit conditions, respectively.

$$\begin{cases} v_\alpha^{*\prime} = \dfrac{2\sqrt{2}V_N}{3}\cos(\omega t + \varphi_\alpha - \dfrac{2\pi}{3}) \\ i_\beta^{*\prime} = \sqrt{2}I_{L\_Limit}^* \cos(\omega t + \varphi_\alpha - \dfrac{\pi}{2} - \dfrac{2\pi}{3}) \end{cases} \quad (8)$$

$$\begin{cases} v_\alpha^{*\prime\prime} = \dfrac{2\sqrt{2}V_N}{3}\cos(\omega t + \varphi_\alpha - \dfrac{4\pi}{3}) \\ i_\beta^{*\prime\prime} = \sqrt{2}I_{L\_Limit}^* \cos(\omega t + \varphi_\alpha - \dfrac{\pi}{2} - \dfrac{4\pi}{3}) \end{cases} \quad (9)$$
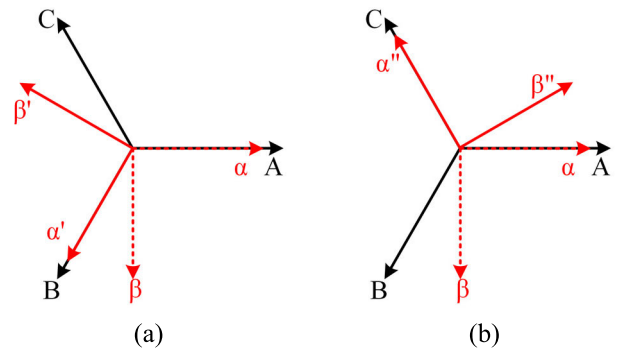

FIGURE 3. Reference coordinate system. (a) in phase CA short-circuit condition; (b) in phase AB short-circuit condition.

The whole control process of the proposed fault ride-through method is shown in Fig.4. Firstly the fault phase should be identified. When an asymmetric short-circuit fault occurs, the output voltages and currents of healthy phase and fault phase will be different, and the output currents of fault phase will increase significantly. Therefore, the fault type can be identified quickly, and the selection of the coordinate system ($\alpha\beta$, $\alpha'\beta'$, or $\alpha''\beta''$ coordinate system) can be determined accordingly. Also the voltage and current references can be determined based on (7)-(9). After the close-loop calculation and the inverse Clark transformation, the modulation signals in *abc* coordinate system can be obtained.

From (6) and (7), it can be seen that only the references of controllers have been changed though the control structure of β axis has been changed before and after fault. If the reference coordinate system needs to be changed from $\alpha\beta$ to $\alpha'\beta'$ or $\alpha''\beta''$, the historical error data and output data of the
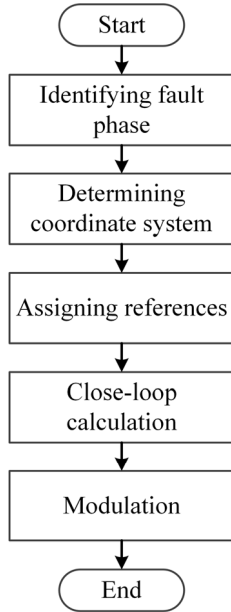
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FIGURE 4. The flow chart of the proposed fault ride-through method.

controllers need to be cleared. Then, the smooth switching between the normal operation and the fault operation can be guaranteed.

III. FAULT CURRENT CHARACTERISTICS ANALYSIS

Since the control system is established in $\alpha\beta$ frame, the voltage and current characteristics in *abc* frame, especially the fault phase current characteristics, should be analyzed to get a comprehensive understanding. Morever, the influence on fault ride-through and selective protection under this proposed method will be assessed in this section.

A. FAULT CURRENT CHARACTERISTICS UNDER THE PROPOSED METHOD

The rated current is expressed as (10), where Z_N is the rated load (Δ-connected). The current references in *abc* frame are shown in (11).

$$I_N = \frac{\sqrt{3}\,V_N}{Z_N} \tag{10}$$

$$
\begin{bmatrix} i_{LA}^* \\ i_{LB}^* \\ i_{LC}^* \end{bmatrix}
=
\begin{bmatrix}
1 & 0 \\
-\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} \\
-\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2}
\end{bmatrix}
\cdot
\begin{bmatrix} i_{L\alpha}^* \\ i_{L\beta}^* \end{bmatrix}
$$
$$
=
\begin{bmatrix}
i_{L\alpha}^* \\
-\dfrac{1}{2} i_{L\alpha}^* + \dfrac{\sqrt{3}}{2} i_{L\beta}^* \\
-\dfrac{1}{2} i_{L\alpha}^* - \dfrac{\sqrt{3}}{2} i_{L\beta}^*
\end{bmatrix}
\tag{11}
$$

Usually the current limit value is set as 2-3 times the rated value [21]. In this article, it is set as two times the rated value,

as shown in (12).

$$I_{L\_Limit}^* = 2I_N \tag{12}$$

It can be assumed that the actual values can track the reference values ideally if the controllers could achieve zero steady error. Generally the capacitance value of filter capacitor of the inverter is small, thus the capacitor current in the steady state is very small compared with the inductor current and can be ignored [20]. Therefore, the inductor current is equal to the output current if the capacitor current is ignored.

Within the scope of this research, the power factor (PF) of load is from 0.8 (lag) to 1. According to the analysis in section II, $I_{O\alpha}$ is determined by the load. The instantaneous current reference $i_{L\alpha}^*$ is equal to $i_{O\alpha}$ according to the above assumption. Thus, the range of $I_{L\alpha}^*$ is expressed as (13).

$$I_{L\alpha}^* = I_{O\alpha} \in \left[0, \frac{2V_N}{Z_n}\right] = \left[0, \frac{2}{\sqrt{3}}I_N\right] \tag{13}$$

Firstly, the pure resistive load case is considered, the load of healthy phase changed from no load to full load. The phasor diagrams before and during the fault are given in Fig.5, where V_{AB}, V_{BC} and V_{CA} are the output line-to-line voltage vectors, while V_A, V_B, V_C, I_{OA}, I_{OB} and I_{OC} are the output phase-to-neutral vectors. The length of the vector V_{AB} and V_{CA} remain unchanged before and after fault, which means that the RMS values of V_{AB} and V_{CA} keep constant and the load of healthy phase could be supplied continuously and steadily. $I_{L\alpha}^*$ and $I_{L\beta}^*$ are the current references, in addition, $I_{L\alpha\_half}^*$ and $I_{L\alpha\_full}^*$ are the α-axis current references at half load and full load condition, respectively. $I_{L\beta}^*$ is the current limit reference. The vector I_{OB} and I_{OC} can be synthesized from $I_{L\alpha}^*$ and $I_{L\beta}^*$ according to (11) since I_{OB} (or I_{OC}) is equal to I_{LB}^* (or I_{LC}^*). Also I_{OB_half} (or I_{OC_half}) and I_{OB_full} (or I_{OC_full}) are the output currents at half load and full load condition, respectively.

Combining (11)-(13), the output currents of phase B and phase C can be expressed as (14) in this case.

$$
I_{OB1} = I_{OC1} = I_{LC1}^* = \frac{\sqrt{\left(I_{L\alpha}^*\right)^2 + \left(\sqrt{3}I_{L\_Limit}^*\right)^2}}{2}
$$
$$
\in \left[\sqrt{3}I_N, \sqrt{\frac{10}{3}}I_N\right] \approx [1.7321 I_N, 1.8257 I_N] \tag{14}
$$

The output current of phase A is only related to load, and it is equal to $I_{o\alpha}$ according to (5), the expression of I_{OA} is shown in (15).

$$I_{OA} = I_{o\alpha} \in \left[0, \frac{2V_N}{Z_n}\right] = \left[0, \frac{2}{\sqrt{3}}I_N\right] \tag{15}$$

In this case, the maximum and minimum values of output currents will be achieved in full load and no load condition, respectively. Equation (16) will be satisfied.

$$
\begin{cases}
I_{OB1\_max} = I_{OC1\_max} = \sqrt{\dfrac{10}{3}}I_N \\[2mm]
I_{OB1\_min} = I_{OC1\_min} = \dfrac{\sqrt{3}}{2}I_{L\_Limit}^* = \sqrt{3}I_N
\end{cases}
\tag{16}
$$

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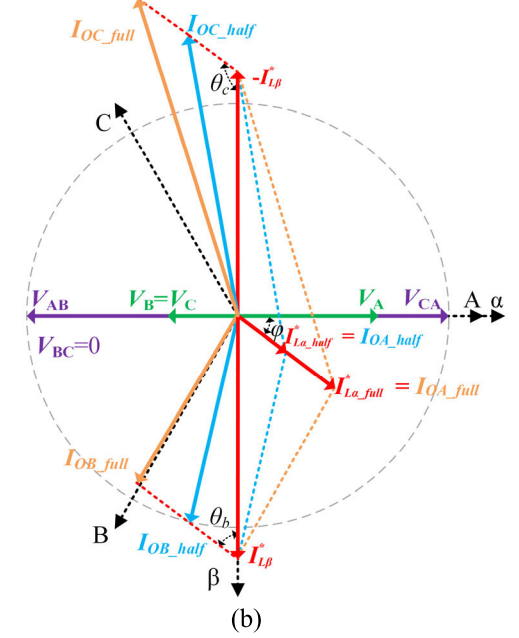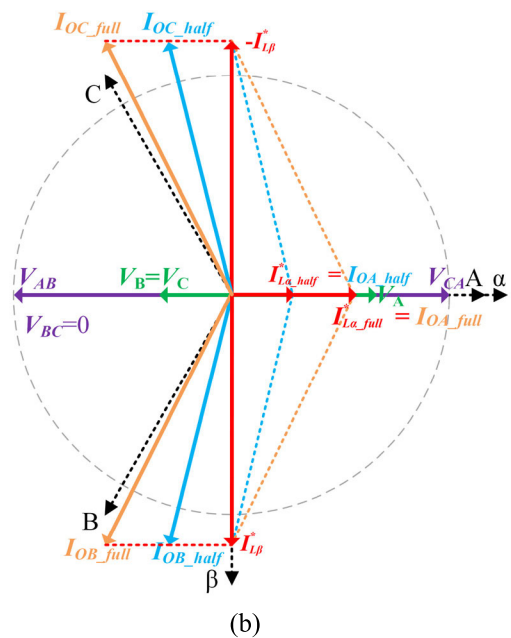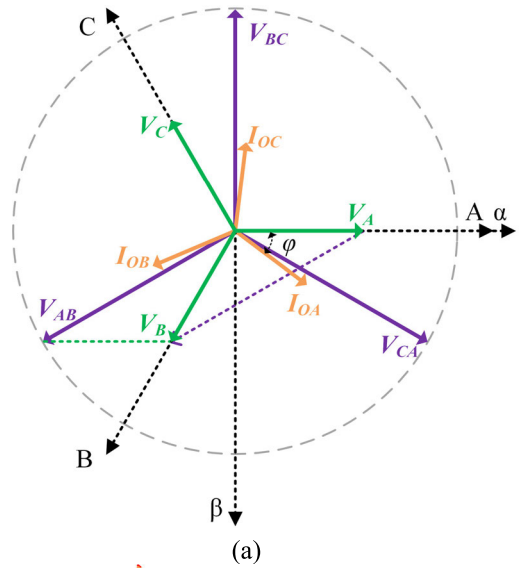
FIGURE 5. Phasor diagrams in the pure resistive load case. (a) before fault; (b) during the asymmetric short-circuit fault.
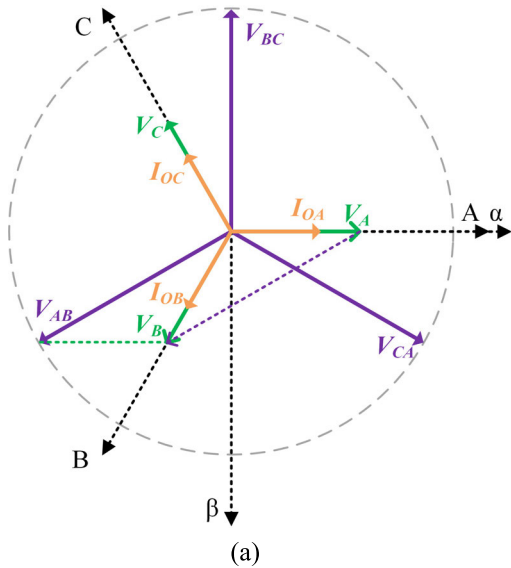

FIGURE 6. Phasor diagrams in the resistive-inductive load case. (a) before fault; (b) during the asymmetric short-circuit fault.

Next, the resistive-inductive load case (the power factor is 0.8) is considered. When the load of healthy phase changed from no load to full load, equation (13) is still effective.

The phasor diagrams before and during the fault are given in Fig.6. Also the RMS values of V_{AB} and V_{CA} can keep constant in different load conditions during the fault. Similarly, the vector $I_{L\alpha}^*$ can be drawn and φ is the power factor angle of load. Then, the vector I_{OB} and I_{OC} can be synthesized from $I_{L\alpha}^*$ and $I_{L\beta}^*$.

Based on Fig.6, (17) and (18), as shown at the bottom of the next page, can be obtained, and the output current ranges of phase B and phase C can be calculated, as shown in (19), as shown at the bottom of the next page.

It is easily known that the upper border of I_{OB} and the lower border of I_{OC} are achieved in no load condition, while the

lower border of I_{OB} and the upper border of I_{OC} are achieved in full load condition.

Actually (17) and (18) are generalized expressions, which means they were effective in any linear load case including the pure inductive load case and the pure capacitive load case ($\varphi \in [-\pi/2, \pi/2]$). Similarly, the output current ranges can be expressed as (20) in the pure inductive load case.

$$\begin{cases} I_{OB3} \in \left[\sqrt{\dfrac{4}{3}}I_N, \sqrt{3}I_N\right] \approx [1.1547I_N, 1.7321I_N] \\ I_{OC3} \in \left[\sqrt{3}I_N, \sqrt{\dfrac{16}{3}}I_N\right] \approx [1.7321I_N, 2.3094I_N] \end{cases} \quad (20)$$

Fig.7(a) shows the output current values of phase B and phase C in different load conditions, and the maximum and

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TABLE 1. The Output Current Ranges of Phase B and Phase C in Different Load Cases.

	From no load to full load			
	I_{OB}	I_{OC}	$\max\{\max[I_{OB},I_{OC}]\}$	$\min\{\max[I_{OB},I_{OC}]\}$
Case1: pure resistive load	$\left[\sqrt{3}I_N, \sqrt{\dfrac{10}{3}}I_N\right]$	$\left[\sqrt{3}I_N, \sqrt{\dfrac{10}{3}}I_N\right]$	$\sqrt{\dfrac{10}{3}}I_N \approx 1.8257I_N$ (at full load)	$\sqrt{3}I_N \approx 1.7321I_N$ (at no load)
Case 2: resistive-inductive load case (PF= 0.8)	$\left[\sqrt{\dfrac{32}{15}}I_N, \sqrt{3}I_N\right]$	$\left[\sqrt{3}I_N, \sqrt{\dfrac{68}{15}}I_N\right]$	$\sqrt{\dfrac{68}{15}}I_N \approx 2.1292I_N$ (at full load)	$\sqrt{3}I_N$ (at no load)
Case 3: pure inductive load	$\left[\sqrt{\dfrac{4}{3}}I_N, \sqrt{3}I_N\right]$	$\left[\sqrt{3}I_N, \sqrt{\dfrac{16}{3}}I_N\right]$	$\sqrt{\dfrac{16}{3}}I_N \approx 2.3094I_N$ (at full load)	$\sqrt{3}I_N$ (at no load)

minimum curves of output current (the phase with higher current) in different power factor angles are shown in Fig.7(b). The ranges of I_{OB} and I_{OC} as well as $\max\{\max[I_{OB}, I_{OC}]\}$ and $\min\{\max[I_{OB}, I_{OC}]\}$ in three typical cases mentioned above (pure resistive load case, resistive-inductive load case with a power factor of 0.8, pure inductive load case) are summarized in TABLE 1, where $\max\{\max[I_{OB}, I_{OC}]\}$ and $\min\{\max[I_{OB}, I_{OC}]\}$ represent the maximum and minimum values of $\max[I_{OB}, I_{OC}]$ from no load to full load, respectively.

B. INFLUENCE ON FAULT RIDE-THROUGH
Note that the purpose of current limiting in fault ride-through process are:

1) to prevent the power semiconductor devices from damage due to excessive current;

2) to trigger the action of protection devices like breakers and clear the fault branch to realize selective protection.

The first item requires the maximum value of output current in the whole load range should be limited within the safe range of the power semiconductor devices. The second one requires the minimum value of output current (the phase with higher current) in the whole load range should be larger than the action threshold of protection devices like breakers,

so that the fault branch can be cleared by breakers under any load condition. These requirements can be expressed as (21), where I_{con} is the maximum allowable value of power semiconductor devices and $I_{trigger}$ is the action threshold of the breakers.

$$\begin{cases} \max\{\max[I_{OB}, I_{OC}]\}|_{no\,load \to full\,load} < I_{con} \\ \min\{\max[I_{OB}, I_{OC}]\}|_{no\,load \to full\,load} > I_{trigger} \end{cases} \quad (21)$$

This article focuses on the pure resistive load and the resistive-inductive load conditions (PF is 0.8-1).

According to the above analysis, it is easily known that output currents of phase B and phase C were related to the load and the current limit value.

Note that $\min\{\max[I_{OB}, I_{OC}]\}|_{no\,load \to full load}$ is always obtained in no load condition according to TABLE 1 and Fig.7. What's more, it only depends on the set current limit value and is not related to the power factor of load according to (14)-(20), as shown in (22).

$$\min\{\max[I_{OB}, I_{OC}]\}|_{different\,load} \equiv \frac{\sqrt{3}}{2}I^*_{L\_Limit} = \sqrt{3}I_N \quad (22)$$

The action threshold of the breakers needs to be designed cooperating with the current limit value and the inverter capacity. According to (21) and (22), it can be known that

$$\begin{cases} I_{OB2} = \sqrt{\left(\dfrac{I^*_{L\alpha}}{2}\right)^2 + \left(\dfrac{\sqrt{3}I^*_{L\_Limit}}{2}\right)^2 - 2\cdot\dfrac{I^*_{L\alpha}}{2}\cdot\dfrac{\sqrt{3}I^*_{L\_Limit}}{2}\cdot\cos(\theta_b)} \\ I_{OC2} = \sqrt{\left(\dfrac{I^*_{L\alpha}}{2}\right)^2 + \left(\dfrac{\sqrt{3}I^*_{L\_Limit}}{2}\right)^2 - 2\cdot\dfrac{I^*_{L\alpha}}{2}\cdot\dfrac{\sqrt{3}I^*_{L\_Limit}}{2}\cdot\cos(\theta_c)} \end{cases} \quad (17)$$

$$\begin{cases} \cos(\theta_b) = \cos(\pi/2 - \varphi) \\ \cos(\theta_c) = \cos(\pi - \theta_b) = \cos(\pi/2 + \varphi) \end{cases} \quad (18)$$

$$\begin{cases} I_{OB2} \in \left[\sqrt{\dfrac{32}{15}}I_N, \sqrt{3}I_N\right] \approx [1.4606I_N, 1.7321I_N] \\ I_{OC2} \in \left[\sqrt{3}I_N, \sqrt{\dfrac{68}{15}}I_N\right] \approx [1.7321I_N, 2.1292I_N] \end{cases} \quad (19)$$
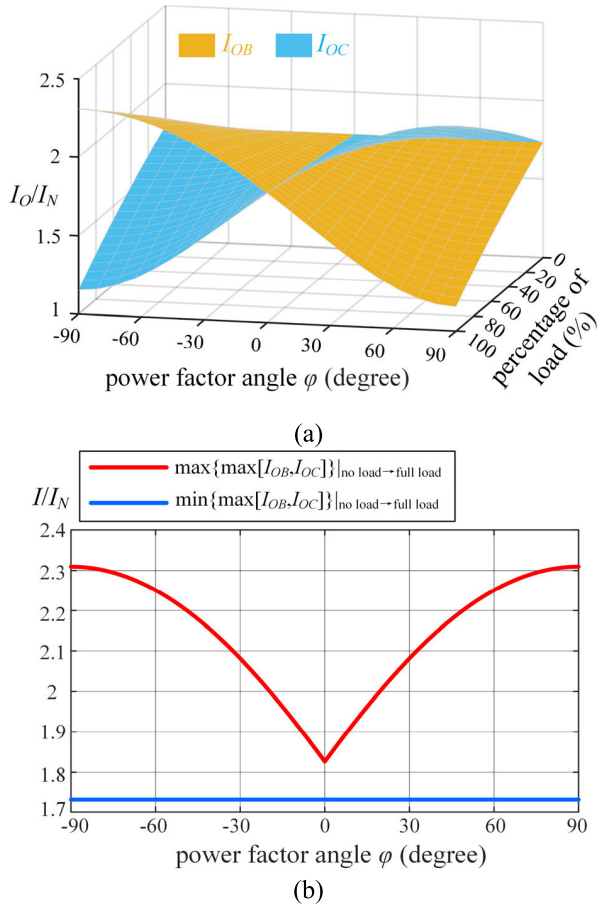
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FIGURE 7. The output current values of phase B and phase C in different load conditions. (a) I_{OB} and I_{OC} in different loads. (b) the maximum and minimum curves of output current (the phase with higher current) in different power factor angles.

as long as the set current limit value, $I^*_{L\_Limit}$, was larger than $2/\sqrt{3}$ times the action threshold of the breakers, the breakers can be activated and the fault branch can be cleared, then the selective protection will be achieved.
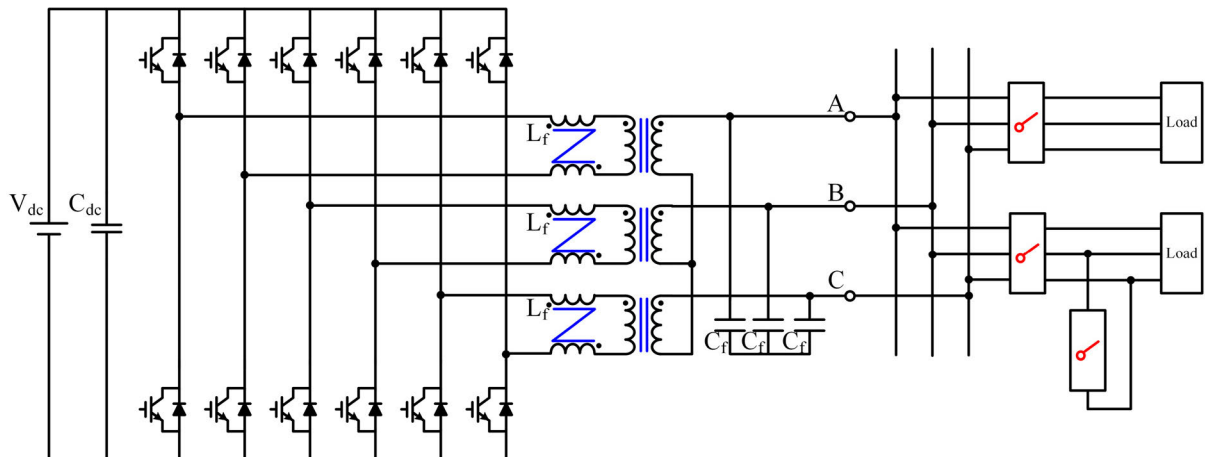
In addition, $\max\{\max[I_{OB}, I_{OC}]\}|_{\text{no load}\rightarrow\text{full load}}$ is always obtained in full load condition. Its value is related to the power factor of load. It is about $1.8257I_N$ when PF=1, while it is about $2.1292I_N$ when PF=0.8, which is the maximum value within all load ranges. Though the maximum value of output current can not be limited to the set limit value strictly, its variation range is small since this current is mainly determined by I^*_β, namely, the set current limit value. The maximum value is within acceptable range and it has little effect on device selection. Even in more extreme load cases like the pure inductive load or the pure capacitive load, the maximum value is only about $2.3094I_N$. The power semiconductor devices will not be damaged due to excessive current. The fault branch can be cleared by the protection devices like breakers, then selective protection can be achieved. Thus, the influence caused by load variation can be ignored. This proposed strategy has a very simple control structure and can perfectly meet the expected goals mentioned in Section II. It can work well in asymmetric short-circuit fault ride-through occasions.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed asymmetric short-circuit fault ride-through strategy, the experimental results will be presented in this section. This article focuses on the pure resistive load and the resistive-inductive load conditions (PF is 0.8-1) since it is the most typical condition. Thus, only the pure resistive load case and the resistive-inductive load case with a power factor of 0.8 are tested in this section.

A three-phase combined inverter prototype has been developed, whose structure is shown in Fig.8. It can be modeled as Fig.1, and its parameters are listed in TABLE 2.

The experimental results with different load conditions are shown in Fig.9. Fig.9(a) shows the experimental waveforms under no load condition. The inverter worked under no load condition at the initial time, then phase BC short-circuit fault occurred. It can be seen that the fault phase output voltage, V_{BC}, changed to almost 0, while the RMS value of healthy

FIGURE 8. Three-phase combined inverter topology.

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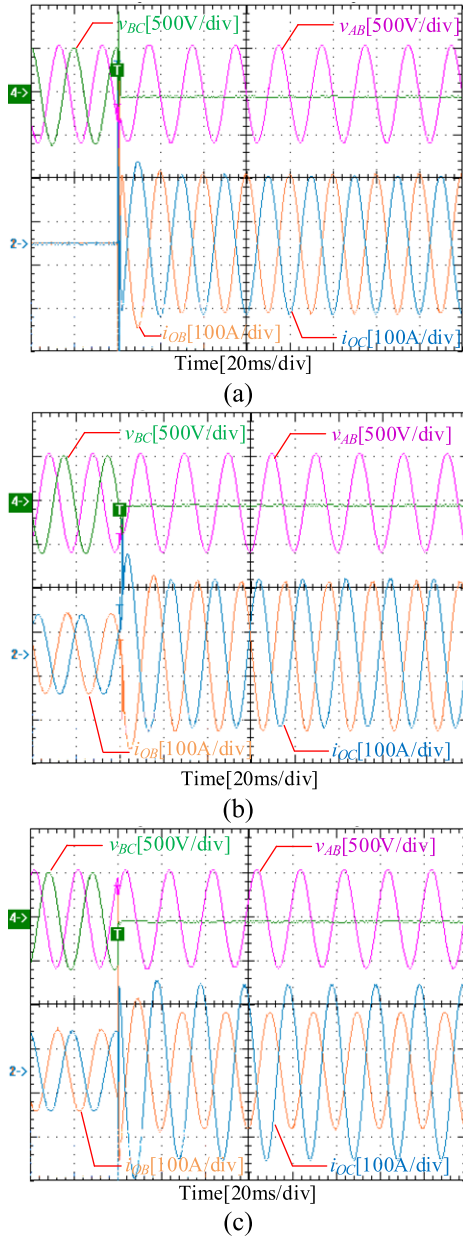| Designed parameters	Values
DC Input Voltage (V_{dc})	350~640V
Rated Output Voltage (V_o)	390V RMS (line-to-line)
Rated Output Current (I_o)	65A RMS
Equivalent Filter Inductor (L_{eq})	420uH
Filter Capacitor (C_f)	70uF
Switching Frequency (f_s)	7.8kHz
Set Current Limit Value in β axis ($I^*_{L\_Limit}$)	130A RMS

(a)

(b)

(c)

FIGURE 9. Experimental waveforms in different load conditions in phase BC short-circuit condition. (a) in no load condition. (b) in full load condition (pure resistive load). (c) in full load condition (resistive-inductive load, PF=0.8 lag).

phase output voltage, V_{AB}, kept consistent with that before fault. Besides, the fault phase currents, I_{OB} and I_{OC} were
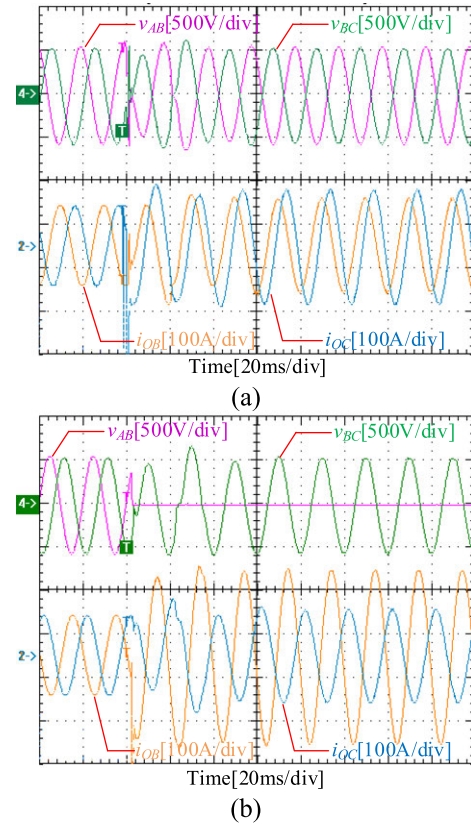

(a)

(b)

FIGURE 10. Experimental results in full load condition (resistive-inductive load case, PF=0.8 lag). (a) in phase CA short-circuit condition. (b) in phase AB short-circuit condition.

limited. The control targets of fault ride-through process mentioned above have been achieved. The fault phase worked in CCM while the healthy phase worked in VCM, and the power supply of healthy phase load did not been affected.

Then experimental results under full load condition are given. Experimental waveforms with pure resistive load case and resistive-inductive load (PF=0.8 lag) case are shown in Fig.9(b) and (c), respectively. According to Fig.9, V_{AB} can also keep constant before and after fault in no load and full load condition, which means power supply reliability of healthy phase can be guaranteed. I_{OB} and I_{OC} are equal in pure resistive load case, and they are different when PF≠1, which is consistent with theoretical analysis. The fault phase current values in different load cases are presented in TABLE 3. It can be seen that the experimental results are in good agreement with the theoretical values. The output currents are limited as expected, thus, the power semiconductor devices will not be damaged by overcurrent. The fault branch can be cleared with the cooperation of the protection devices like breakers, then selective protection can be achieved. The correctness of theoretical analysis has been verified.

The experimental results in full load condition (resistive-inductive load case, PF=0.8 lag) when the short-circuit fault occurred in phase CA and phase AB are shown in Fig.10(a) and (b), respectively. Comparing Fig.10 with Fig.9(c), it can be found that the healthy phase still worked

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TABLE 3. Fault Phase Current in Different Load Conditions.

		Theoretical value	Experimental result
In no load condition	I_{OB}	112.6A	113.1A
	I_{OC}	112.6A	113.0A
In full load condition (pure resistive load)	I_{OB}	118.7A	118.8A
	I_{OC}	118.7A	120.2A
In full load condition (resistive-inductive load, PF=0.8 lag)	I_{OB}	94.9A	96.2A
	I_{OC}	138.4A	138.6A

in VCM and the fault phase worked in CCM, which means the control targets could be met perfectly. Changing the reference angles of the $\alpha\beta$ coordinate system, the proposed strategy is still applicable in phase CA or phase AB short-circuit conditions. The experimental results have validated the effectiveness of this method.

V. CONCLUSION

In order to accomplish fault ride-through in asymmetric short-circuit situation, the fault phase current should be limited and controllable, while the output voltage of healthy phase should keep constant to supply the load continuously and steadily. To achieve this goal, a current limiting and fault ride-through strategy has been proposed in this article. It has the following features:

1) The controller was built in $\alpha\beta$ frame. The current limiting was realized in β axis, while the α-axis controller still worked in VCM. Its control structure is very simple.

2) The output current characteristics in *abc* frame with different loads under this proposed method were analyzed and the influence on fault ride-through caused by different loads was assessed. Though the output current of fault phase cannot be limited to the set value strictly, it only varies in a small range within safe operation area, the power semiconductor devices still can be protected effectively. The analysis results proved that this method could work well under different load conditions.

3) This method not only limits the output current of the fault phase, but also ensures that the healthy phase worked in VCM, and the healthy phase voltage can always keep constant in the whole fault ride-through process. Thus, the power supply of healthy phase load will not be affected.

All the goals of asymmetric fault ride-through process mentioned in Section I and Section II can be achieved perfectly. Thus, this proposed method is a good solution in asymmetric short-circuit fault ride-through occasions. The correctness of theoretical analysis and the effectiveness of proposed fault ride-through strategy have been verified by experimental results.

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