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Influence of Fringing-Field on DC/AC Characteristics of $Si_{1-x}Ge_x$ Based Multi-Channel Tunnel FETs

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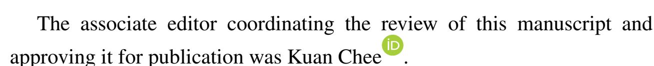
ABSTRACT Tunnel field-effect transistors (TFETs) are the decent performance estimators in the prospective of short-channel effects. In such structures, a small inter-gate separation (IGS) is a key factor that appraises for high packed-density with more number of channels (N) to deliver superior performance. Hence, the investigation is majorly focused on scaling IGS and its fringing-field impact on device behavior for the first time. The outcomes reveal that the high fringing-field initiates for IGS < 10 nm and influences the tunneling probability and scattering strongly at 1-nm IGS, which affect the DC and RF characteristics; hence, optimized values of IGS are investigated and determined as IGS > 10 nm. The results state that the optimized IGS can provide source to deliver high ratio of on- and off-current (I_{on}/I_{off}). Even though, a small IGS is beneficial for reduction in the total capacitance, the RF performance improvement depends on a large IGS. The investigation is further extended and quantified for the finest IGS in multi-channel TFETs when N varies from 1 to 10. These analyses are assessed for the emerging technological nodes.

INDEX TERMS Band-to-band tunneling model, channel number (N), fringing-field, inter-gate separation, multi-channel tunnel-field effect transistor, $Si_{1-x}Ge_x$.

I. INTRODUCTION

The significant foremost factors as per the device requirements based on current technology nodes are scaling and abrupt switching mechanisms. At this point, the supply voltage scaling is predominant in the digital applications due to their quadratic dependence on the dynamic power supply. In addition, the reduction of fundamental limit factor of the subthreshold swing (SS) as 60 mV/dec to improve switching mechanism is also significant. One of the promising devices that can effectively gratify these two requirements is the tunnel field-effect transistors (TFETs). Currently, the TFETs are suffered with low tunneling probability and high ambipolar current. However, many experimental and simulation works have been showing the anticipated results to solve these concerns [1]–[5]. The major improvements are carried out based on the reduction of energy bandgap (E_g) through low bandgap materials (such as Ge, IV-V group materials, and strained-Si) [6], reducing screening tunneling length (λ) by scaling dielectric material (high-κ) [7], excess field generations through alternative geometrical structures such as the line tunneling (or so-called the vertical tunneling) for the enhancement of tunneling area [8], [9].

The hetero-structured TFETs are needed to demonstrate high-performance and high ratio of the on- and off-currents [10]. In this perspective, silicon-germanium (SiGe) has been proven as quite effective choice, because of its quality in crystalline structure like silicon (Si). Furthermore, it comprises of strain which results in low electron-hole masses to enhance the tunneling probability of the device with low interval scattering and improved hetero-interfaces (while accumulating dielectric materials) [11]. Furthermore, use of SiGe results in high-speed performance even at similar biasing circumstances like Si material. Owing to this, many works were reported for the improvement of tunneling probability in TFETs by varying different mole fractions (x) of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Ge [12]–[15]. Above all, SiGe has shown the ability to replace silicon with simple CMOS processing steps rather going for aggressive processing steps like major compound semiconductors and 2D materials [16].

It has been known that TFETs are most considerable choices in computing applications such as non-volatile memory's due to their superior DC characteristics [17]. The recent demonstrations on TFETs have been stated that these structures can be reliable at scaling below 10-nm dimensions [18]. These figures estimate the ability of TFETs and their further scope in the digital-era with low power, and fast-switching speed. However, the requirement of high-packing density in improving computations, performance and many more applications is crucial. This can be achieved through stacking of multiple channels via multi-fin architectures. Few works are majorly concerned about the channel/fin width and height variations and their effects on the performance rather the high-packing density determination factor such as pitch/inter-gate separation (IGS) [19], [20]. This factor of investigation can be greatly helpful for an increased packing density and to govern suitable choices and alternative solutions in the fabrication [21]–[23]. In general, fringing-field in the geometrical structures of TFETs has shown as predominant and beneficial factor as compared with MOSFETs [24]. However, these fields also influence the off-state current during low pitch/IGS through strong mutual coupling (never been demonstrated), while multiple channels are stacked together. Hence, we for the first time investigate the effects of fringing-field on multi-channel structures in TFETs to govern the effect of DC and RF performance by scaling the IGS.

In this work, the explored multi-channel TFETs (mChTFETs) comprised with the advantages of SiGe and including spacer at relevant positions of the structure is investigated by scaling IGS to estimate the fringing-field effect. Foremost, we estimate the effect of fringing-field on tunneling probability for varied effective-oxide-thickness (EOT). Further examines the effect of fringing-field on the DC and RF characteristics with varied values of IGS and increased channel number (N). Note that the value of $N = 2$ is considered for mChTFETs throughout the article unless stated. This article is organized as follows. The configuration of device simulation is stated in Section II along with fabrication steps. Section III reports the results and discussion. The conclusions are given in Section IV.

II. THE CONFIGURATION OF DEVICE SIMULATION

The design and characterization of mChTFETs is carried out by our device simulation setup with experimentally quantified models [25]–[28]. The major physics related to tunneling resembling nonlocal trap-assisted tunneling (TAT) model by Hurkx and dynamic nonlocal tunneling model for band-to-band tunneling (BTBT) are included [29]. Furthermore, the doping dependence and high-field saturation mobility, the Shockley-Read-Hall generation-recombination, the bandgap narrowing effect, and the Fermi Dirac statistics are also included as the device physics. Especially, the effect of ballistic transport calculated using non-equilibrium Green's function is also included to make the results as more accurate and robust [30].

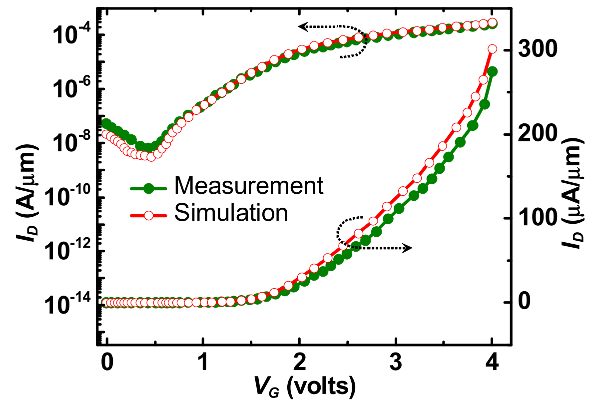

FIGURE 1. Plot of the authenticated simulation data with that of measurement [2].

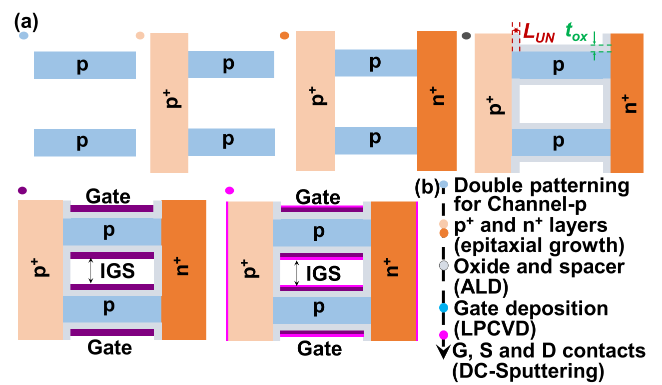

FIGURE 2. (a) The systematic simplified fabrication process flow for the design of mChTFETs. (b) The predictable fabrication processing mechanisms (top to bottom).

Primarily, the device simulation is verified with the models quantified before with that of experimental data, as illustrated in Fig. 1 [2]. The material parameters and tunneling factors related to BTBT model are considered based on calibrated data. Subsequently, the calibrated direct and indirect path parameters as A_{dir}, B_{dir}, A_{indir}, and B_{indir} for $Si_{0.6}Ge_{0.4}$ are 1.34×10^{20} cm^{-3} S^{-1}, 54.05 MVcm^{-1}, 2.44×10^{15} cm^{-3} S^{-1}, and 16.8 MVcm^{-1} by having the tunneling mass of electron and hole as 0.328 and 0.421 m_0 [31].

A. DESIGN OF mChTFETs

Although we focus on the numerical study, the fabrication steps of the explored mChTFETs are briefed, as shown in Fig. 2, based on the standard guidelines [32]. Fig. 2a expresses the step down approaches for the proposed device and the relevant fabrication methodologies are specified in Fig. 2b. The structure of mChTFETs ($N = 2$) stating definite regions is depicted in Fig. 3a and the corresponding device dimensions are listed in Table 1. The device dimensions are scaled based on the constant-field scaling and the available experimental data [33], [34]. Note that the IGS is dependent on the difference in pitch and thicknesses of channel, oxide, and metal regions (t_{ch}, t_{ox}, and t_m)

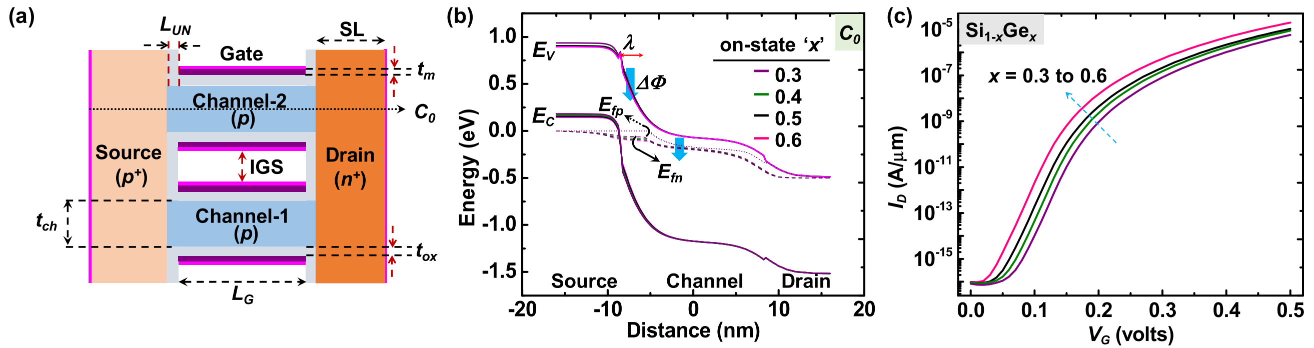

FIGURE 3. (a) Design overview of the proposed mChTFETs structure of $N = 2$. (b) Effect of energy bandgap for the varied Ge fraction '*x*' along the cut-line C_0 during on-state ($V_G = V_D = 0.5$ V). (c) I_D-V_G characteristics for the varied *x* of mChTFETs at the bias levels of $V_G = V_D = 0.5$ V. Reduction in λ, $\Delta\Phi$, and fermi level corresponds for an increased I_{on} and I_{off}, eventually reduced threshold voltage.

TABLE 1. Device specifications and materials used.

Parameter	Material	Value
Channel thickness (t_{Ch})	Silicon	5 nm
Source/Drain length (SL)	$Si_{1-x}Ge_x$/Si	7.5 nm
Effective oxide thickness (t_{ox})	SiO_2/HfO_2	0.78 – 1 nm
Gate length (L_G)	TiN	15 nm
Spacer-underlap (L_{UN})	HfO_2	3 nm
Inter-gate separation (IGS)	Air medium	1 – 10 nm
Source doping concentration (p^+)	Boron	1×10^{20}
Channel doping concentration (p)	Boron	1×10^{16}
Drain doping concentration (n^+)	Arsenic	1×10^{19}
Gate-metal thickness (t_m)	TiN	3 nm
Gate-electrode work-function	TiN	4.3 eV

as expressed in

$$IGS = pitch - t_{Ch} - 2(t_{ox} + t_m). \tag{1}$$

Therefore, the critical thickness IGS = 1 nm corresponds to the channel/fin pitch of > 15 nm. Notably, the possible fin-pitch of 10 - 20 nm is demonstrated through the self-aligned quadruple patterning techniques [35]–[38]. In addition, the scaled EOT is considered based on the technology nodes specified for sub-7-nm and reduced the HfO_2 thickness up to 1 nm as per the experimental limitations by keeping a fixed SiO_2 thickness of 0.6 nm [39]. It is evident that the lattice distance between the atoms exists in Hf to O atoms is 0.21-0.24 nm, hence there exists at least 4 layers of oxide for thickness of 1 nm.

B. IMPORTANCE OF $Si_{0.6}Ge_{0.4}$

The materials employed as $Si_{1-x}Ge_x$ (with 'x' as mole fraction of Ge) being the source and rest with that of Si. Retaining $Si_{1-x}Ge_x$ over channel and drain regions establishes for an increased ambipolarity due to deeper band banding at channel-drain junction [10], hence $Si_{1-x}Ge_x$ at source alone is an effective choice. Further, the effect of Ge content on proposed structure is investigated as specified in Figs. 3b and c for the device shown in Fig 3a. The observations are made with respect to energy band diagram and drain current (I_D). Fig. 3b specifies that, an increased 'x' origins for reduced energy bandgap (E_g), the tunneling width (λ) and the reduction in tunneling-barrier height ($\Delta\Phi$). The observed reduction in $\Delta\Phi$ for the mole fraction 'x' from 0.3 to 0.6 is identified as an average of 20 to 30 meV. There by reduction in λ and the reduction in fermi levels (E_{fn} and E_{fp}) are attained as major contributors for the BTBT. This accomplish for high on-state current (I_{on}) at higher values of Ge fraction. Whereas, the higher 'x' supplies enlarged off-state current (I_{off}) as well (Fig. 3c) and hence optimum value of 'x' is needed. In addition, it could be able to view in Fig. 3c that the increased I_{off} for $x > 0.4$ is higher in compared to $x < 0.4$. This is because of switching $Si_{1-x}Ge_x$ into Ge alone ($x = 1$) provide provision to have large TAT during off-state because of very low bandgap. Hence, the optimized value of 'x' is considered as 0.4 to maintain higher I_{on}/I_{off} ratios [25].

Spacer with HfO_2 is adopted as gate-source underlap for maintaining low I_{off} and decent control over multi-gate and multi-channel structures. The absence of the spacer leads to direct impact on gate-over-source, which resembles for shift in potential barrier and there by expansion in λ. Furthermore, the absence of spacer in point-tunneling devices lead to increased field at channel-drain junction, implies high off-state current [40]. It is to be noted that the gate-source overlap on to the source is a contradictory case in vertical/line tunneling devices as followed with the concept of tunneling perpendicular to the gate [41], [42].

III. RESULTS AND DISCUSSION

Foremost, the influence of fringing-field and its origin is delivered by scaling down the critical gate-dielectric thickness (t_{ox}) in mChTFETs. The physical factors such as electron-BTBT and electric-field distribution are investigated with the varied IGS values through the scaled EOT. Here, the influence of fringing-field on DC parameters such as the I_D, the ratio of I_{on}/I_{off}, the transconductance (g_m), the drain- induced barrier thinning (DIBT), and subthreshold swing (SS) are evaluated. In addition, the AC/RF factors of unit-gain cut-off frequency (f_t), maximum oscillation frequency (f_{max}), gate-to-drain capacitance (C_{gd}), and the total gate-capacitance (C_{gg}) are discussed. Furthermore, extending the determination of an effective IGS value for an increased channel number that is influenced with low fringing-field is also evaluated.

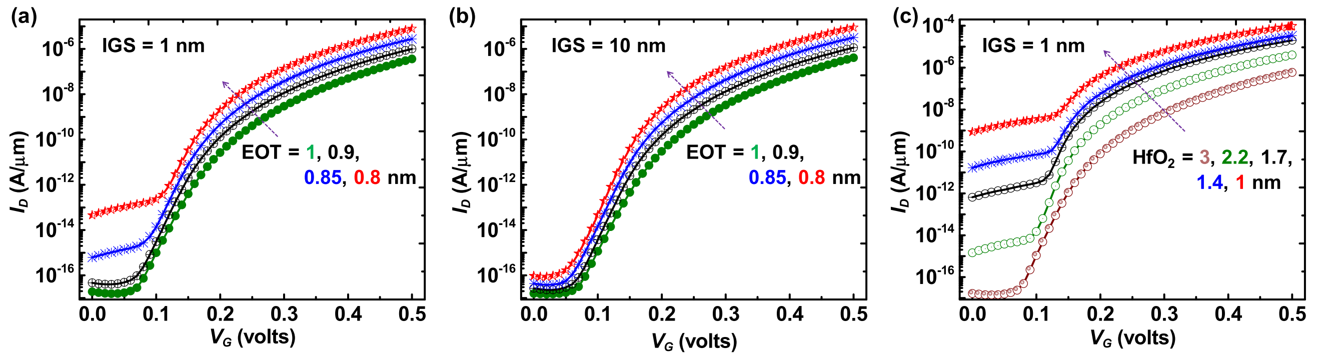

FIGURE 4. Effect of I_D-V_G for the scaled EOTs of the mChTFETs with (a) IGS = 1 nm and (b) IGS = 10 nm, respectively. (c) I_D-V_G curves with scaled HfO_2 thicknesses at IGS = 1 nm. Here, $V_G = V_D = 0.5$ V is biased for all cases. The off-state performance is worsened at IGS = 1 nm than that of IGS = 10 nm for both the gate-dielectric options of EOT and HfO_2 alone (including Fig. 5).

A. ORIGIN OF FRINGING-FIELD AND ITS EFFECT

The origin of field is mainly influenced by the gate, oxide region and the effect caused through mutual coupling as the two semiconductor plates (channel/fins) approaching closer (IGS). Hence, the investigation of fringing-field influenced through the scaled EOT for a fixed t_m is made in prior.

The I_D-V_G characteristics of the mChTFETs with respect to the IGS of 10 and 1 nm for the scaled EOT are depicted in Figs. 4a and b. It is clearly observed that the influence of the fringing-field for the case of IGS = 10 nm is marginal, compared to the case of 1 nm. The reason behind the large I_{off} is either through oxide leakage or the strong coupling (IGS). To understand this scenario, the further analyses are needed. Therefore, here we considered HfO_2 alone as gate-dielectric because of its strong fringing-field generation due to high-κ. On the other hand, it is also to be pointed that the HfO_2 alone is beneficial than the EOT of same thickness values [24]. Nevertheless, influence of critical thickness of HfO_2 on the I_D-V_G characteristics of the proposed structure with the scaled IGS of 10 and 1 nm are depicted in Fig. 4c and Fig. 5, respectively. The I_{on} is greatly improved (because of low t_{ox}) but the off-state leakage is relatively poor at small IGS compared to low EOT values. It directs that the HfO_2 alone as gate-dielectric with a reasonable IGS is an effective choice for achieving high I_{on}/I_{off}. However, the scaled EOT and HfO_2 alone discloses that the major influence in fringing-field is initiated through IGS rather than gate-dielectric in mChTFETs. In addition, the electron BTBT profile depicted in Fig. 6 clears that the existence of electron BTBT rate even at off-state condition is identified at IGS = 1 nm. This tunneling is occurred in the $Si_{1-x}Ge_x$ as inter-valley scattering of electrons at high fringing-field. Because, the variation in energy at different valleys (Γ, L, and X) in $Si_{0.6}Ge_{0.4}$ as of 1.24 and 0.93 eV, respectively from the expressions [43]

$$\nabla E_g(\Gamma - L) = 759.6 + 1086.0x + 330.6x^2 \qquad (2)$$

and

$$\nabla E_g(\Gamma - X) = 894.1 + 42.1x + 169.1x^2, \qquad (3)$$

where the notation ∇ denotes the energy variation in meV. Thus, the transmission of electrons called internal-valley

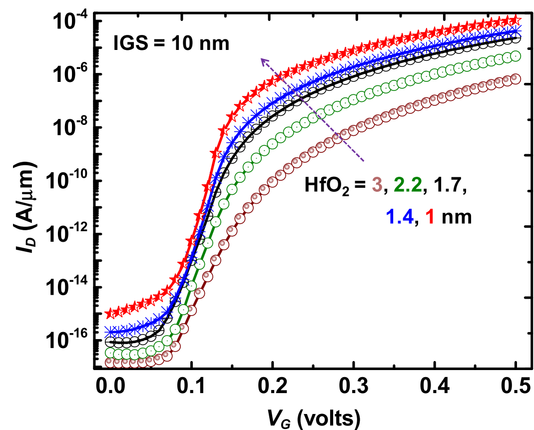

FIGURE 5. The I_D-V_G characteristics depending on the scaled HfO_2 thickness of the mChTFETs at IGS = 10 nm with $V_G = V_D = 0.5$ V.

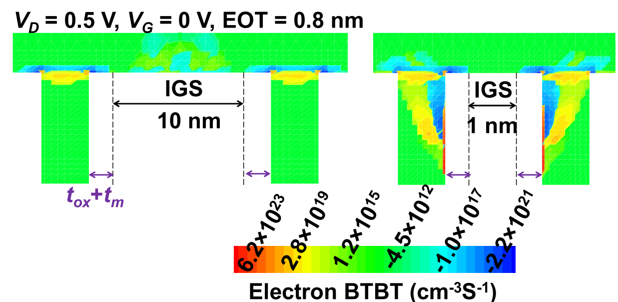

FIGURE 6. Observed electron BTBT during off-state is shown for an EOT of 0.8 nm. It is observed that the higher tunneling rate is viewed for IGS = 1 nm (right-figure) due to dominated fringing-field.

scattering at source-channel junction can only be possible at high-field generations caused at the small IGS. Hence, the major source of the off-state current is through generation in high fringing-field at the small IGS. This field is because of strong mutual-coupling as the IGS approaches closer.

B. ELECTRIC-FIELD FOR SCALED IGS

The electric-field distribution is extracted for the proposed device along the vertical (C_0) and horizontal (C_1) directions, as stated in Fig. 7. Fig. 7a shows the variation in the electric-field with respect to the varied IGS values with the observation of increased fringing-field as the IGS approaches

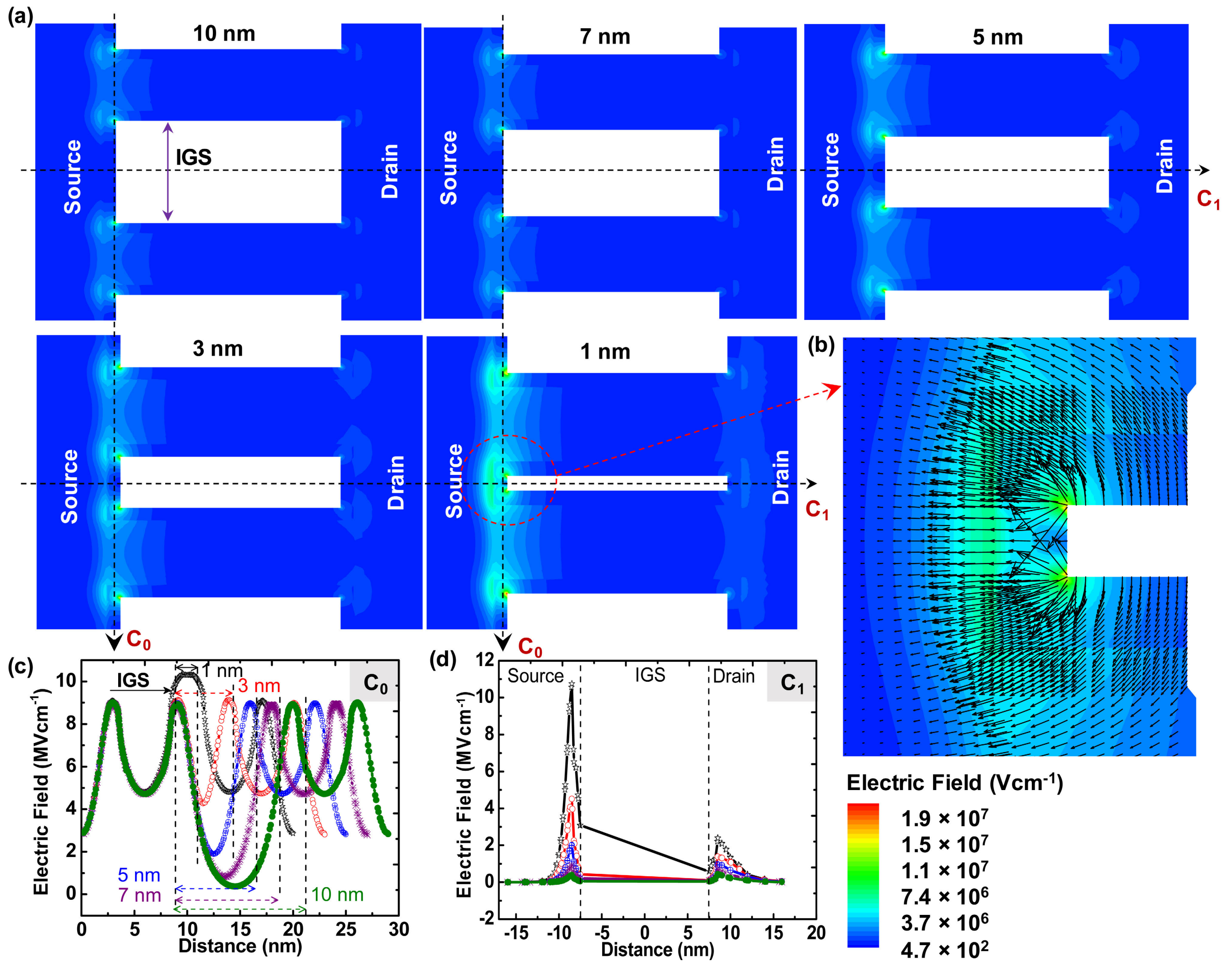

FIGURE 7. (a) Plots of the electric-field distribution of the device with EOT = 0.8 nm for the scaled IGS at $V_G = V_D = 0.5$ V. (b) Plot of the fringing-field direction for the case of IGS = 1 nm (outset). (c) Electric-field distributions along C_0 covering source and IGS regions. (d) Electric-field distribution along C_1 covering source-IGS-drain regions (same labelling as (c)). Among all, high-fields can be identified for IGS = 1 nm either along C_0 or C_1.

closer. The strong effect of fringing-field along with field-directions for the case of IGS = 1 nm can be viewed in Fig. 7b. Here, the high-field distributions are noticed for the small IGS (= 1 nm) and low-field distributions for the large IGS (= 10 nm) near the source-IGS spacing regions along horizontal and vertical directions, can be seen from Figs. 7c and d. The increased electric-field majorly existed at the edges of gate-contact (source-channel and channel-drain junctions). This would provide excess energy for the electrons in valence band of source. The gained energy and momentum through excess energy in the valance band would make the electrons to tunnel from internal valleys that prominent for large off-state currents and reasonable on-state currents, respectively.

In general, it is to be noted that the field distributions at the channel-drain junction are weaker in TFETs because of less band bending or low depletion region. This is due to moderately doped channel (Si) and drain (Si) junctions (large bandgap), thus it exists with insignificant band bending. Therefore, in the account of multi-channel structure, though the fringing-field contribution can be considered as significant one for low IGS (as viewed in Fig. 7d); however, it is marginally less compared to fringing-field at the source-channel junction. No matter how, the distribution of fringing-field keeps increasing upon reduced IGS from 10 to 1 nm, as seen from Fig. 7d. Thus, the effect of fringing-field will become stronger while the hetero or low bandgap materials are used.

C. ELECTRON BTBT FOR SCALED IGS

The electron BTBT profiles for the scaled IGS from 1 to 10 nm are depicted in Fig. 8. Fig. 8a exposes that the overall cross-sectional area of tunneling is diminished (blue) at the surmounted gate-interface for small IGS values (from 1 to 7 nm). Whereas, the IGS of 10 nm could be able to produce total area of tunneling. It means that the fringing-field that arises due to electrostatic coupling is dominated while the channels (along with gate) approaching closer. For detailed analyses, the electron BTBT profiles are extracted along C_0 and C_1 directions and are depicted in Figs. 8b and c. The negative spikes shown in Fig. 8b for the IGS reducing from

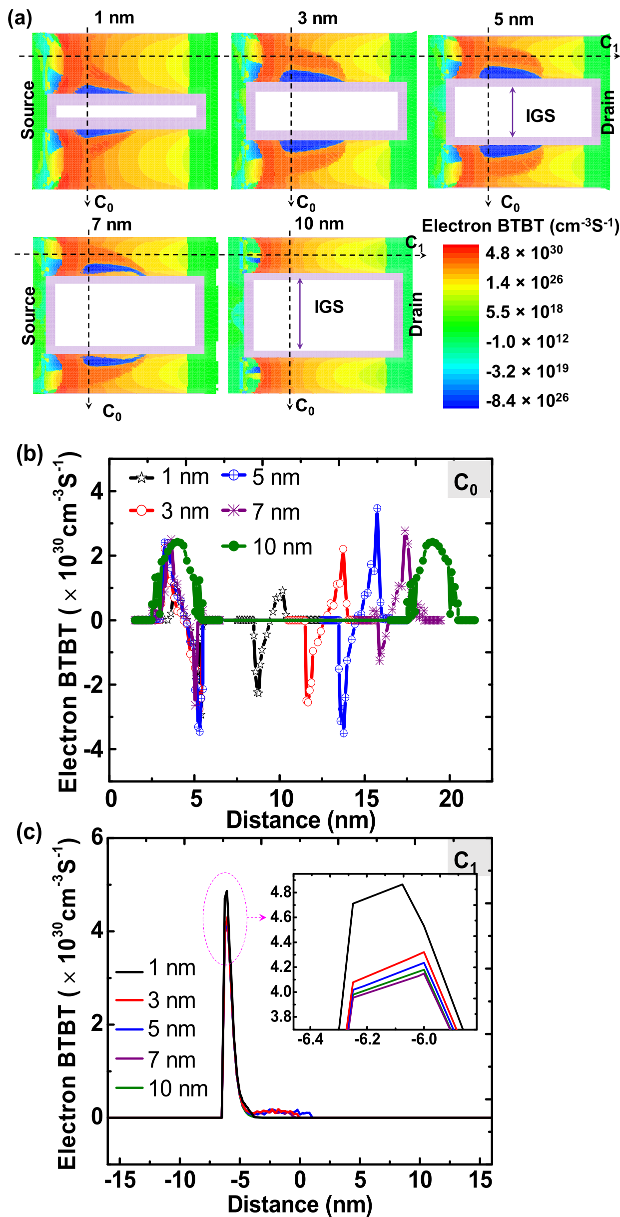

FIGURE 8. (a) Electron BTBT profiles inside the mChTFETs with the varied IGS, where the EOT = 0.8 nm ($V_D = V_G = 0.5$ V). (b) Electron BTBT along the C_0 covering source and IGS regions. (c) Electron BTBT along C_1 covering source-channel-drain regions. The reduction in overall tunneling area is viewed for IGS < 10 nm (Fig. 8b), and strong tunneling is identified (Fig. 8c) at the source-channel junction because of strong fringing-field at the interface as stated before.

8 to 1 nm indicate the reduced BTBT rate. Even though the smallest IGS (= 1 nm) is achieved with less overall-tunneling rate, but the maximum tunneling is achieved within the shortest tunneling path length due to strong electrostatic coupling at the interfaces (Fig. 8c). In addition, the strong electrostatic coupling deflects the tunneling path (radial direction) as the IGS approaches closer, there by variation in BTBT is observed. The deflection in tunneling path and effect of electrostatic coupling are seen to be nullified at the largest IGS (= 10 nm) and provide scope for large cross-sectional area of tunneling.

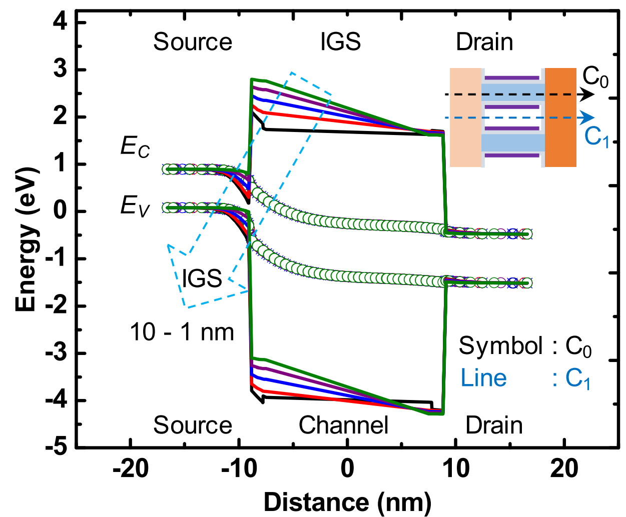

FIGURE 9. Energy band diagram of mChTFETs for the scaled IGS from 10 to 1 nm (top to bottom). The plot is drawn along source-channel-drain junctions (along C_0) and source-IGS-drain junctions (along C_1) at $V_D = V_G = 0.5$ V. Since, the effect of fringing-field is significant at source-IGS region (Figs. 7a and b) therefore the strong depletion for low IGS (= 1 nm) can be seen along C_1.

D. EFFECT OF E_G ON SCALED IGS

The effect of energy band diagram on scaled IGS is depicted in Fig. 9. For clear understanding, the band diagram is depicted along source-channel-drain junctions (along the cut-line C_0 depicted in inset of Fig. 9) addition to source-IGS-drain junctions (along the cut-line C_1). This dictates that the strong influence of fringing-field at low IGS makes strong depletion at source-IGS region, implies bend in bands is observed. Upon using optimum IGS this depletion can be eventually reduced so that the fields are well controlled. On the other hand, the band influence along C_0 and across the channel-drain junctions is insignificant.

E. DC CHARACTERISTICS

Fig. 10a depicts the I_D-V_G characteristics of the $Si_{0.6}Ge_{0.4}$ mChTFETs for the varied IGS. The maximum tunneling current by the TFET at the specified bias of V_G (= 0.5 V) is calibrated as I_D or I_{on}. Similarly, the off-state (or leakage) current at the bias of V_G (= 0 V) and the applied potential (V_{Dsat} = 0.5 V) is termed as I_{off}. It is observed in Fig. 10a that the I_D is proportionally increased for an enlarged IGS. This is due to accommodation of high density of states through enlarged source and drain regions. Whereas, the strong influence of fringing-field that is observed for the case of IGS = 1 nm can be able to re-boost the I_{on} than the next of IGS = 3 nm. Nevertheless, the influence of fringing-field is stronger for the off-state than that for the on-state. Therefore, the I_{off} is observed as worsen for the 1- and 3-nm IGS, respectively, pre the discussion above. Thus, the I_{on}/I_{off} ratio is (Fig. 10b) low, compared with the case of IGS $\geq$ 5 nm. Means, a suitable IGS is beneficial to control the device performance during the on- and off-state conditions. In addition, the extracted g_m shows as proportionate to that of I_{on}, i.e. dominated field at very small IGS = 1 nm and proper control at IGS = 10 nm constituted for an increased

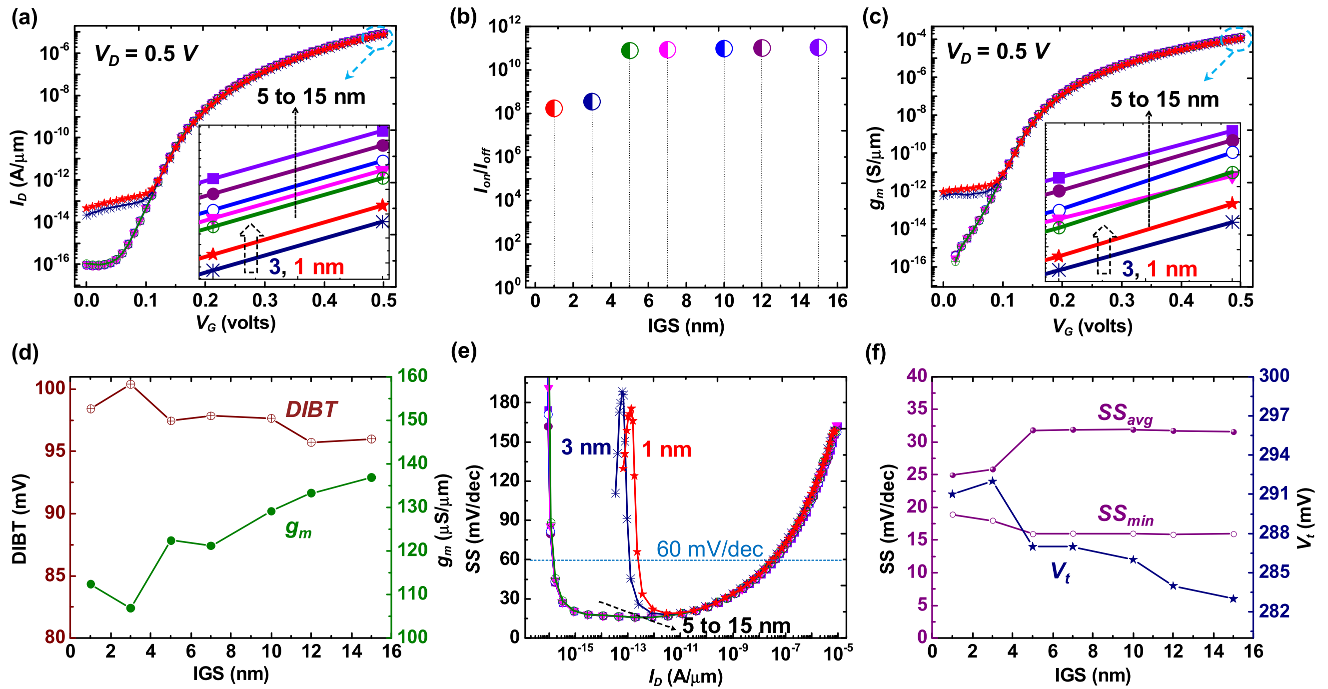

FIGURE 10. DC characteristics of the mChTFETs with respect to the varied IGS for the EOT of 0.8 nm. (a) I_D-V_G. (b) I_{on}/I_{off}. (c) g_m-V_G. (d) g_m and DIBT. (e) SS calculations with respect to I_D at V_G = 0.5 V. (f) SS and V_t. Increase in IGS accommodate for enlarged I_D due to proportionate increase in source and drain regions, implies high density of states for tunneling. Similarly, low IGS influences for large I_{off} and re-boost in I_{on} at very low IGS (= 1nm) are observed. In similar other factors of g_m, SS and V_t perceives better characteristics at IGS≥10 nm than low IGS.

TABLE 2. DC characteristic comparison among the explored and reported Si/SiGe TFETs under the same threshold voltage (= 0.28 V) and $V_G = V_D$ = 0.5 V, where $N = 1$ is fixed.

Structure	I_{on} (μA/μm)	I_{off} (A/μm)	SS_{avg} (mV/dec)
This Work	4.4	5.4×10^{-17}	32.0
[32]	5.5	1.0×10^{-09}	52.8
[19]	0.5	0.5×10^{-12}	46.0
[44]	0.1	1.0×10^{-12}	52.0
[45]	0.8	3.0×10^{-14}	41.0

conductance as depicted in Figs. 10c and d. The DIBT is extracted from the threshold voltages (V_t) for the bias levels of linear drain-bias voltage (V_{Dlin} = 0.05 V) and saturation bias voltage (V_{Dsat} = 0.5 V) for a gate bias (V_G) of 0.5 V respectively. As depicted in Fig. 10d discloses that the DIBT can be slightly improved at large IGS values by making prominent control at the channel-drain junction. In addition, the excess fringing-field generations at very small IGS (= 1 nm) can make improved transport and thus provides slight reduction in DIBT. However, the reduction is not significant compared to large IGS values. Hence, it is understood that the field also influence over channel-drain junction (not shown) at small IGS and thus it is observed to be higher DIBT at the IGS of 3 nm.

Other DC characteristics such as SS of minimum (SS_{min}) and average (SS_{avg}) along with V_t variation with respect to IGS scaling are examined here. It is well known that the TFETs have significantly less slope compared to MOSFETs and thus it's specified with two slopes as SS_{min} and SS_{avg}. The least specified slope points of SS_{min} can be defined as the minimum slope at any point of its current transition during the linear region and SS_{avg} termed as the slope existed between the points of threshold voltage to the intial voltage at which the current transition begins [7]. The extracted SS values with respect to variation in I_D is depicted in Fig. 10e. The extracted data reveals that the fluctuations as seen at small IGS (1 and 3 nm) affects greatly on SS. Thus, high SS is seen even at low I_{on} (during off-state) compared to other IGS values. Further more, Fig. 10f depicts the extracted values of SS for the varied IGS. The variation of the SS_{min} is high at the small IGS (1 and 3 nm) and can be minimized or unaffected at large IGS values. Similarly, the SS_{avg} is less at a small IGS because of its condensed transition region (Fig. 10a). Thus, the sweep slightly reduces and then will be constant at large IGS values. Further, the observed V_t based on constant current method (in delivering 0.1 μA/μm orders of current [7]) is more sensitive at the small IGS. Since, the transport below the subthreshold regime is affected with fringing-field and hence the threshold value needed to be higher to achieve the desired current criteria. The V_t can be reduced at large IGS values through enhancement of transport mechanism.

Table 2 tabulates the DC characteristic comparison among the explored and reported Si/SiGe TFETs [19], [32], [44], [45] under the similar threshold voltage and the same biases. Our device with the best geometry exhibits controllable I_{off} which is the minimal among all devices. Notably, the SS_{avg} = 32 mV/dec is superior to others.

F. EFFECT OF IGS ON DC CHARACTERISTIC WITH RESPECT TO DIFFERENT SOURCE MATERIALS

Here the material options as Si and Ge are considered in place of SiGe to asses the performance effect on scaled IGS. The DC characteristics for Si and Ge based mChTFETs by

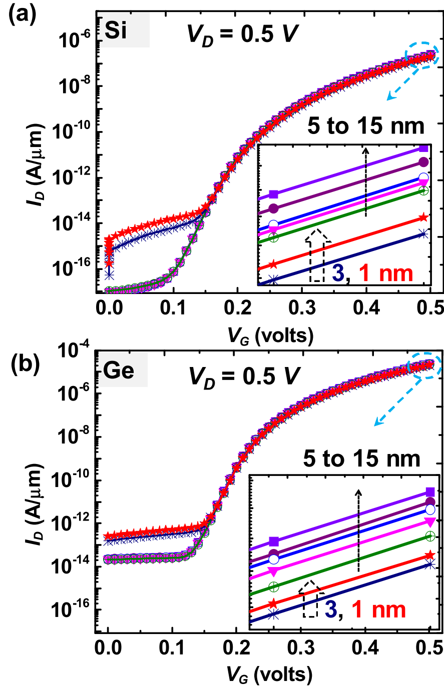

FIGURE 11. I_D-V_G **characteristics of (a) Si and (b) Ge based mChTFETs by scaling IGS from 1 to 15 nm. It is observed that IGS of 1 and 3 nm are affected with high fringing-field and therefore the** I_{off} **increases for both the Si and Ge based mChTFETs (as like seen for SiGe based mChTFETs). In addition, the Ge bandgap is sensitive to tunneling, thus the** I_{on} **and** I_{off} **are increased proportionally compared with that of Si.**

scaling the IGS from 1 to 15 nm are depicted in Fig. 11. From Figs. 11a and b, it is understood that the fringing-field effect is seen as higher for reduced IGS as like SiGe; in addition, it will be even stronger for low-bandgap materials like Ge compared to Si or SiGe (similar to Figs. 7 and 8, not shown here). Therefore, the high I_{off} can be seen in Fig. 11b for Ge based mChTFETs compared to Si (Fig. 11a). Notably, the on-state performance is boosted with Ge based source in mChTFETs due to its low energy bandgap and high density of states for tunneling. To compensate the on- and off-state performance, the $Si_{0.6}Ge_{0.4}$ is the most suitable option, as viewed in Fig. 10a and section-B. Neverthless, the optimum IGS of 10 nm is still beneficial irrespective of material considerations to reduce the fringing-field effect that can overcome with poor off- and on-state performances.

G. AC AND RF CHARACTERISTICS

The major AC and RF characteristics of f_t, f_{max} and parasitic capacitances such as C_{gg} and C_{gd} are discussed and depicted in Fig. 12. It is eminent that the C_{gs} has the minor impact on total capacitance due to higher conduction for an increased gate-voltage over source-channel junction, hence which is not adopted in this discussion [46]. The C_{gd} is the major contributor to switching time in TFETs, hence the study is extended to analyze the belongings [47].

The effect of C_{gd} and C_{gg} with the variation in gate-bias at $V_{Dsat}/2$ is considered for the varied IGS, as depicted in Figs. 12a and b. This consideration of $V_{Dsat}/2$ is understood that the analog circuits are modelled through *p*- and *n*-type transistors through the shared supply bias voltage [48]. The variation in capacitance is entirely based on the concept of electrostatic coupling arisen while the IGS is approaching closer (like in Multi-fin FETs) [49]. This coupling would make reduction in capacitance (C_{gd} and C_{gg}) as the IGS approaches closer. In general, the total capacitance C_{gg} is the sum of C_{gs} and C_{gd}. However, the C_{gs} is least contributor over C_{gd} in TFETs; therefore the maximum contribution for C_{gg} is achieved from C_{gd} as depicted in Fig. 12b [50].

Fig. 12c shows the impact of IGS on f_t and f_{max} for the scaled IGS at drain-bias of $V_{Dsat}/2$. The expressions used for the extraction of f_t and f_{max} as [51]

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{4}$$

and

$$f_{\max} = \frac{f_t}{\sqrt{4R_g(g_{ds} + 2\pi f_t C_{gd})}}. \tag{5}$$

The results specified in Fig. 12c disclose that both maximum value (at $V_G = 0.5$) of f_t and f_{max} are dependent similar with respect to the scaled IGS. As seen before, the small IGS is equipped with a strong fringing-field that has the probability to enhance the conductance, and low capacitance through mutual coupling are able to produce high

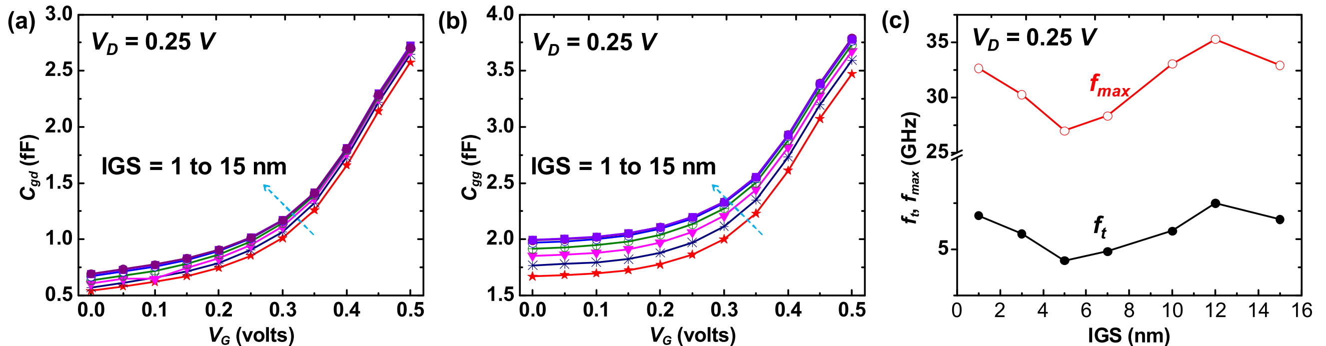

FIGURE 12. **Extracted (a)** C_{gd} **and (b)** C_{gg} **(c)** f_t **and** f_{max} **for the scaled IGS (1 to 15 nm) of the mChTFETs at the EOT of 0.8 nm (**$V_G = 0.5$ **V). Increase in mutual coupling at low IGS corresponds for reduction in** C_{gd} **and** C_{gg}**. The dominated** g_m **enhancement than increased** C_{gg} **responsible for high** f_t **and** f_{max} **at large IGS.**

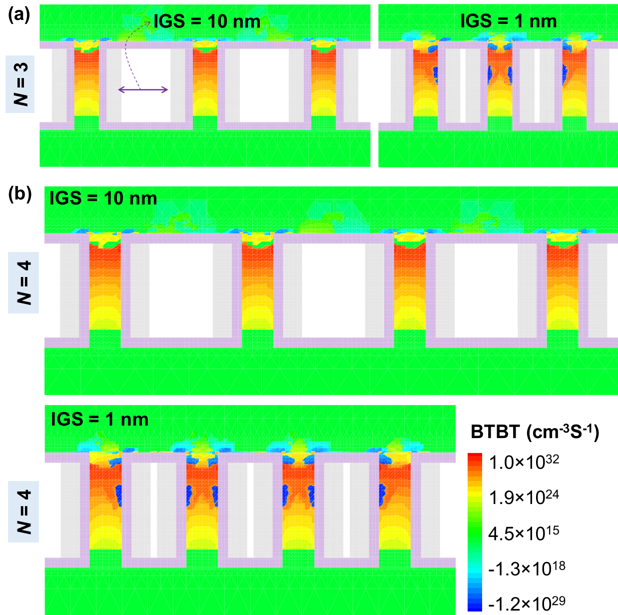

FIGURE 13. Effect of electron BTBT at scaled IGS of 1 and 10 nm, for (a) $N = 3$, and (b) $N = 4$ with $V_D = V_G = 0.5$ V. The controlled IGS of 10 nm is maintained with complete tunneling cross-sectional area even for varied $N \geq 2$.

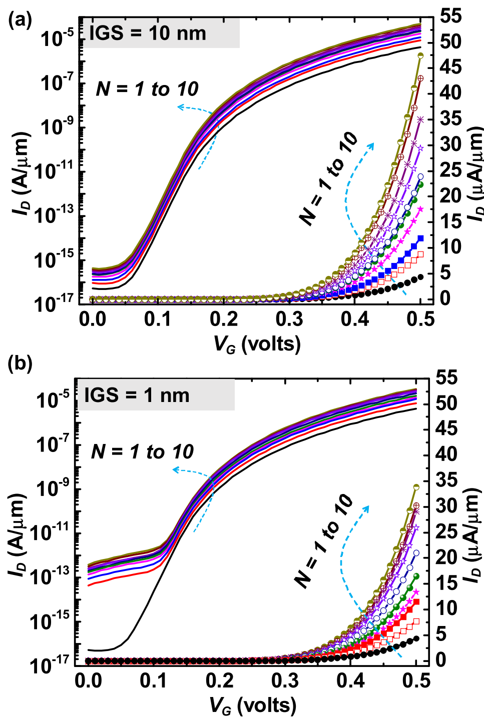

FIGURE 14. I_D-V_G characteristics of the mChTFETs for the varied $N = 1$ to 10 at the IGS of (a) 10 nm and (b) 1 nm having $V_D = V_G = 0.5$ V. High I_{off} and low I_{on} due to high fringing-field and reduction in overall tunneling are at IGS of 1 nm is observed for $N = 1$ to 10. In addition, good agreement with I_{on} multiplication as $N \times I_{on1}$ is attained for N number of channels because of its improved tunneling area.

frequency levels. In addition, the large IGS value corresponds to high-conductance than the conductance achieved through fringing-field. However, slightly enlarged capacitance can still remain at large IGS values but insignificant compared to high conductance. Therefore, the large IGS value could

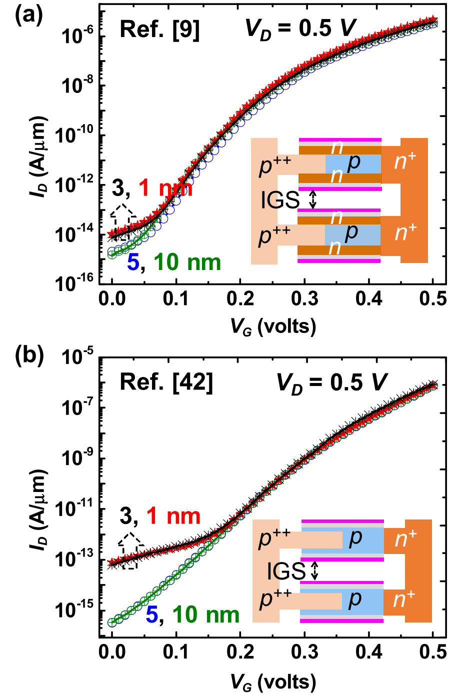

FIGURE 15. Plots of the I_D-V_G curves of the multi-channel vertical TFETs from the references (a) [9] and (b) [42]. Both the cases of IGS = 1 and 3 nm impact high fringing-field, so the I_{off} increases. Notably, the high work function (compared with our structure) has been used to control the off-state current of the vertical TFETs because of their sensitivity.

be a reasonable option to achieve improved RF performance. In overall, an IGS of 10 nm or even higher might be an effective choice to compensate both of the DC and RF variations for emerging technology nodes.

H. EFFECT OF IGS FOR AN INCREASED N

Further investigation is considered to validate the IGS of 10 nm as an effective choice even for increased number of channels ($N > 2$). Hence, the physical insight of IGS with respect to N varying from 1 to 10 is further examined by using high-end computational setup. Here, the electron BTBT for $N = 3$ and 4 with IGS of 1 and 10 nm is shown in Fig. 13. It is observed that the advantage of IGS = 10 nm still withstand without any limitation in tunneling area, compared to 1 nm, as like $N = 2$. However, the parasitic resistive and capacitance values in addition to the stated C_{gd} and C_{gg} for $N > 3$ are varied, which may affect RF performance seriously (needs further investigation). Furthermore, the observed I_D-V_G characteristics for $N = 1$ to 10 with IGS of 10 nm and 1 nm is also depicted in Fig. 14. Ideally, the required value of maximum I_{on} for a N-channel device could be of $N \times I_{on1}$. The explored structure is able to achieve the expected results in the orders of N for IGS $\geq$ 10 nm.

I. EFFECT OF IGS IN ALTERNATIVE STRUCTURES

The influence of friging-field is also estimated for alternative structures of vertical TFETs [9], [42]. Due to lack of full study on these structures, we do further design and examine them by extending to multi-channel scheme. These devices with $N = 2$ and varied IGS are simulated; the effect of

the scaled IGS from 1 to 10 nm on the I_D-V_G curves is dipicted in Fig. 15. The strong influence of the IGS at 1 and 3 nm is similar irrespective of the device options, as shown in Figs. 10a and 11. No matter how, electrical characteristics of vertical TFETs are more sensitive in the vertically stacked region which should be subject to further investigations.

IV. CONCLUSION

The investigation towards the effect of fringing-field on the scaled IGS of the mChTFETs has been reported. Physical constrains including the effect of EOT, electron BTBT and electric-field for various devices (IGS from 15 to 1 nm) and an optimized IGS for an increased N have been examined. It has been noticed that the mutual coupling among channels at small IGS influences the increased I_{off}, impacts the tunneling probability, and fluctuates RF performance as well. The influence at the small IGS can be nullified through an optimum separation of IGS $\geq$ 10 nm. Therefore, key findings of this study can be applied to increase the packing density for emerging technology nodes.

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