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Study on Chip Reliability Modeling Based on Mutually Dependent Competing Failure of Solder Joints in Different Failure Modes

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ABSTRACT The chip is a core functional component. Its reliability plays a vital role in electronic equipment normal operation. As the typical cause for chip malfunction, the solder joint degradation is selected to study chip reliability. The degradation models of solder joint in different failure modes are established through data-driven and failure physical model, and chip reliability model is constructed based on mutually competing failures of multiple solder joints. First, the chip reliability degradation test and finite element modeling(FEM) are carried out under coupled environment stress. The solder joint failure modes and degradation processes are studied through the analysis of test data, microstructure and mechanical simulation. Then, solder joint degradation models are established based on Coffin-Manson and Paris functions that have been modified by a data-driven method. Taking the solder joint failure time of degradation model as the characteristic parameter of Weibull distribution, the solder joint reliability function is obtained. Finally, mutually dependent competing failure theory is cited to describe the correlation about solder joint reliability of different failure modes, then the chip reliability model is established. The parameter estimation is realized by the inference function for margins (IFM) method. From verification tests, results show models are highly consistent with the actual reliability, indicting our reliability modeling method achieves the transition from underlying solder joint level to integrated component level. The joint application of different models can make up for the deficiencies of the single model and obtain more accurate results. In addition, we determined that intermetallic compounds (IMC) are main source of model error.

INDEX TERMS Reliability, chip solder joint, degradation, competing failure.

I. INTRODUCTION

With the development of prognostic and health management technology, electronic equipment support is being transformed from traditional time-based maintenance to condition-based maintenance. As the premise of condition-based maintenance, accurate assessment of electronic equipment health status becomes very important [1], [2].

In the modern electronic industry, chips are widely applied for their logic judgment and calculation functions [3], [4]. Therefore, to establish an effective chip reliability model is significant for studying chip stability and electronic equipment status. Researchers have found that solder joints are the main concentrated area of chip stress-strain response, indicating that chip reliability is related to solder joint fatigue failure closely [5]. Especially as the function expanding, equipment work circumstances are becoming harsher such as vibration, high or low temperature. This makes solder joints susceptible to be damaged [6]. A single solder joint breakdown may result in chip failure completely. Therefore, chip reliability modeling based on solder joint failure is necessary.

There are two universal approaches to study the solder joint degradation and failure: degradation test and virtual simulation. For degradation test, researchers apply a certain environmental load on solder joints through test bench, and collect parameters that can characterize degradation for later degradation process analysis. In [7]–[9], researchers monitored the current, voltage and radio frequency impedance of solder joints. They found solder joint electrical parameters would change significantly when they were about to fail.

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After the degradation test, failure samples of solder joints can be analyzed. Some scholars studied the microstructure of solder joints [10], [11] by scanning electron microscope (SEM). However, it is not sufficient, just relying on microscopic cracks, to consider the mechanism of solder joint degradation. Hu [12] and Huang [13] performed FEM simulation of quad flat package (QFP) and compared strain location and actual crack location. Majid *et al.* [14] performed FEM simulation of ball grid array (BGA) solder joint to study occurrence location of maximum peeling stress. Che *et al.* [15] used quarter FEM to research QFP fatigue life and they found QFP fatigue life is much longer than BGA solder joints. Also, some scholars quoted the classic failure physical models, such as strain and energy fatigue models, to assess solder mechanics performance. In [16], [17], Coffin-Manson model and Morrow model were used to identify the relationships between the mechanical data and fatigue life. In [18], Darveaux model was used to predict solder joint remaining life. Chen et al [19] modified a failure physical model considering coupling environment stress. Osarumen et al [20]employed the Garofalo creep model by FEM simulate to discuss the creep effect of material solder joint.

The traditional methods of studying solder joint degradation are data-driven and failure physics methods. The drawbacks of data-driven method are that the modeling accuracy of is closely related to data acquisition, data size and intelligent algorithms, and test data is easy to be notably affected by multiple outside factors. In practice, the convergence of the results is difficult to guarantee. In terms of failure physics method, the deficiency is that there is still much controversy about the solder joint failure mechanism under coupled stress, such as random vibration loads, thermal loads, etc.. Since most of failure physical models are only suitable for single stress when they are established, some model parameters are not applicable under coupled environment stress. Therefore, the model needs to be improved to achieve more accurate results.

In studying chip reliability, Tang *et al.* [21] attached sheet strain gauges near-critical chip solder joints to measure strain for predicting chip fatigue life. Zhang et al [22]investigated chip package interaction to estimate chip stresses in module level, so that to perform a robust design of chip reliability. However, the strain tested accuracy is related to measurement position and sensor performance closely. And it is difficult to detect strain value or strain distribution of different solder joints through physical experiment. In [23], chip solder joints were connected in series to form a daisy chain, and chain voltage across is used to characterize the chip degradation process. In addition, some scholars [24], [25] used field programmable gata array (FPGA) chip internal logic to characterize the status. For example, they monitored single solder joint resistance of FPGA chips. When the solder joint impedance change significantly, this shows the chip is completely invalid immediately. Some researchers studied chip life from failure physical methods. In [26], the Anand model was revised to study solder joint degradation from physical mechanism to predict the chip life. It is evident that the methods adopted in these studies to characterize chip reliability are to monitor the mechanical or electrical parameters of solder joint. Also, in most studies,the researcher only uses the degradation data of the most vulnerable solder joint. However, according to chip reliability degradation test, the failure mode of first failed solder joint may be any one of the failure modes, and its location is not unique either. It is therefore difficult to establish the chip reliability model.by traditional methods. Moreover, if each solder joint can lead to chip functional failure, chip life is equal to the minimum failure time of all solder joints. In this case, there is a competitive failure relationship between chip solder joints. But traditional methods do not consider the joint influence of multiple solder joints competitive degradation.

At present, reliability modeling based on competitive failure theory has been widely studied and applied. Bagdonavicius [27] uses Gaussian, Gamma and other random processes to establish the reliability model of competitive degradation. Huang and Asking [28] gave the reliability function of competing failures under the assumption that sudden and degraded failures are independent of each other. Wang and Pham [29] considered the external shock and internal degradation comprehensively, and use the time-varying Copula function to describe the correlation of competing failures under the coexistence of multiple degradation failures and sudden failures. Che HY *et al.* [30] developed a reliability model with the mutual dependent competing of degradation and shock processes. They found the reliability was weakened significantly as considering mutual dependence. Hao SH *et al.* [31] took advantage of Stress-Strength models and Cumulative damage model to study above similar problem. Cao YS *et al.* [32] explored the two dependent and competing failure processes in the context of multi-state systems with multiple components, and obtained reliability functions. Peng *et al.* [33] gave the general form of the dependent competitive failure model and analyzed the reliability evaluation about the competitive failure of a Microelectromechanical Systems (MEMS) system. Huang *et al.* [28] put forward an extension of electronic device reliability analysis considering multiple competing failure modes. Bai *et al.* [34] estimated the multicomponent stress-strength model reliability according to dependent Weibull stress variables and exponential strength variables based on Gumbel Copula. Qiu *et al.* [35] evaluated system reliability performance with competing failures from a dependent two-stage failure process. Zeng, ZG *et al.* [36] studied the dependent failure behavior from failure mechanisms based on physics-of-failure (PoF) models to get a deterministic model. Although the competitive failure theory has been widely applied in other areas, limited studies are using it to study the failure relationship between multiple solder joints to establish a component reliability model. It is one of the innovations of this study to combine the competitive failure theory with our research object.

This article takes chip solder joint degradation and failure as the research basis for chip reliability. The degradation data,

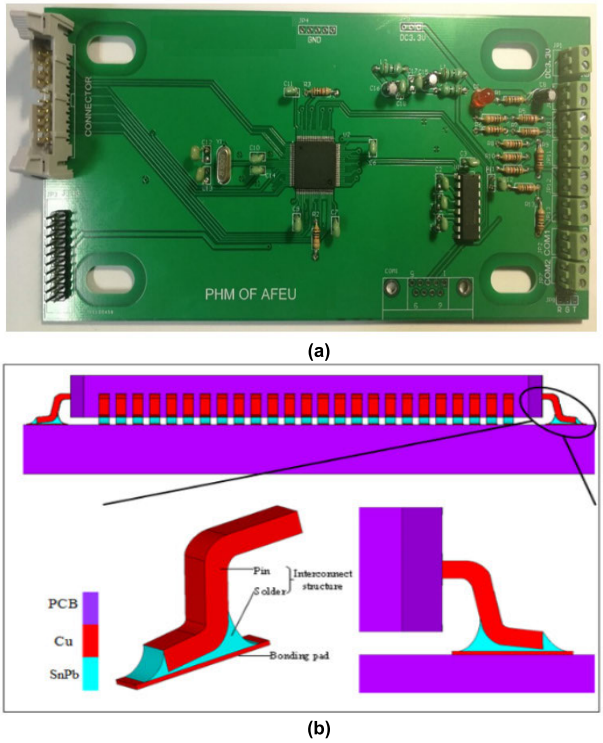

FIGURE 1. (a) Test piece. (b) QFP solder joint.

microscopic failure and mechanical simulation are studied for the solder joint failure mode and degradation stages through environmental test, SEM analysis, and finite element simulation, respectively. Failure physical models are modified by solder joint status data and finite element simulation results so that two-stage degradation models of solder joints are established to predict solder joint theoretical failure time. We use this data as the characteristic parameter of Weibull distribution model, linking solder joint degradation model with reliability model. The Copula function is used to establish a chip reliability model that takes into account the mutually dependent competitive failure of solder joints. The model parameters are estimated by IFM estimation method, Finally, verification tests are set up to verify the model accuracy and analyze the source of error.

II. CHIP RELIABILITY DEGRADATION TEST AND FINITE ELEMENT MODELING

The test object is the STM32 chip using QFP package. Chip pins are fixed on the PCB board through SnPb solder. Test piece is shown in Figure 1(a). The structure simulation of solder joint is shown in Figure 1(b).

In order to monitor solder joint state, a capacitor is connected with solder joint to form a resistor-capacitance circuit before applying the environmental load. When fatigue damage occurs to the solder joint structure, the solder joint resistance will change, which can affect the charging time of the capacitor. According to GJB150.16/16A [37], three test groups under random vibration tests at different temperatures are carried out, and the test load spectrum is shown in Table 1.

TABLE 1. Degradation Test Scheme Under Random Vibration at Different Temperatures.

Test	Temperature (^oC)	Random vibration (g^2 / Hz)
a	-25	
b	25	0.8
c	75	

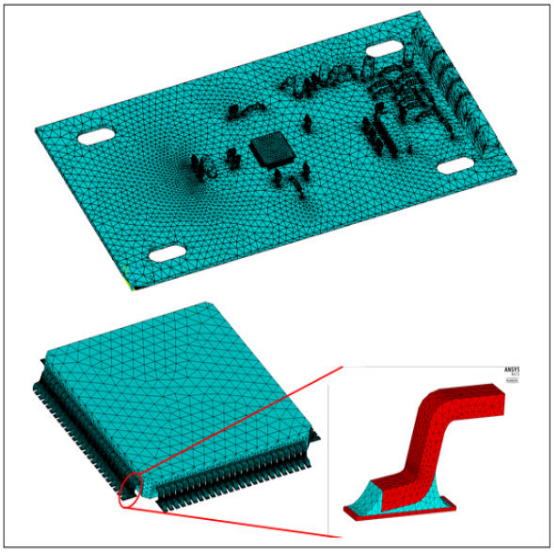

FIGURE 2. Finite element model of test piece, chip and QFP solder joint.

Because it has been determined firstly natural frequency of our test pieces is about 243.5 Hz, the frequency range of the test random vibration is 220 Hz to 260 Hz [13].

Three-dimension model is established by finite element software ANSYS. According to GB / T25712-2010 [38]., defective test piece has been eliminated. So we believe that chips tested are ideal [12], [13], [39], [40]. The established model are shown in Figure 2.

Vibration fatigue is a typical high-cycle fatigue under low stress and high frequency loads. Generally, the fatigue crack propagates in elastic region without obvious plastic deformation, so purely elastic analysis in finite element simulation can meet requirements. Material properties of Test b are listed in Table 2. We select Anand constitutive model to describe solder joint mechanical properties. Test piece is fixed on vibration table through four bolt holes located at PCB corners, so full displacement constraints are imposed on the inner wall of holes, as boundary condition.

III. CHIP SOLER JOINTS FAILURE ANALYSIS

After extracting the degradation data, the microstructure of corresponding solder joints is analyzed by SEM. Comparing the degradation data and SEM results, it is found that degradation data trends have three correspondences with micro crack

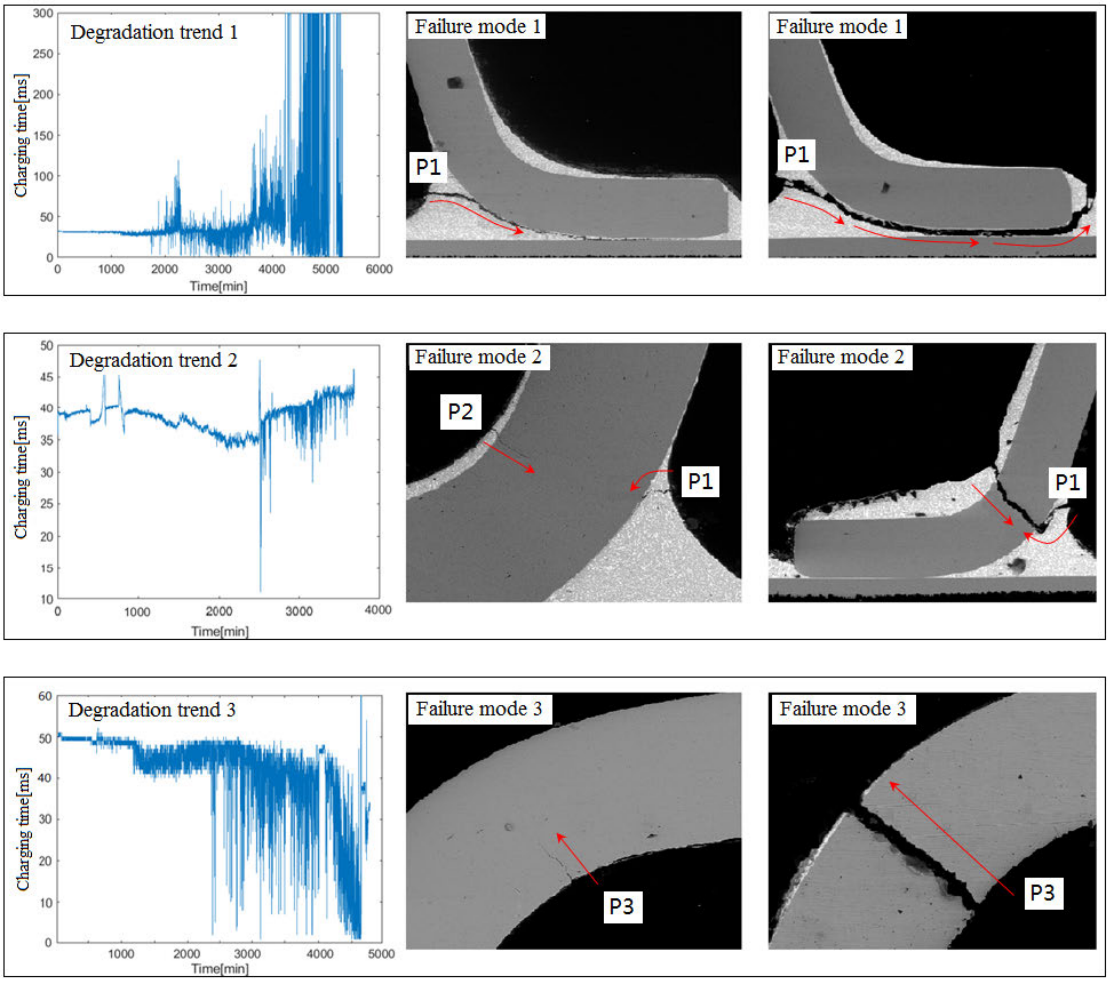

FIGURE 3. The degradation data and micro-crack of three solder joint failure modes.

TABLE 2. Material Properties.

Material	Young's modulus (GPa)	Poisson's ratio	Density (kg/m3)	CET (1/K)
PCB(Fr4)	22	0.40	1900	21x10-6
Pin (Copper)	141	0.35	8700	16.6x10-6
Chip (Silicon)	17	0.28	2329	2.6x10-6
Solder (60Sn-40Pb)	30	0.40	9000	21x10-6

modes, as shown in Figure 3. We can identify the failure mode based on the degradation path. Degradation trend 1 corresponds to failure mode 1. Degradation trend 2 corresponds to failure mode 2. Degradation trend 3 corresponds to failure mode 3. In FM1, the degradation data has a gradual increasing trend. The crack appears at the position 1(P1), and then spreads along the contact area between the solder and Cu pin, solder and PCB board. Finally, the pin is completely separated from SnPb solder and PCB board. In FM2, degradation data tends to first decrease and then increase. Cracks initiate at P1, P2 and propagate to the inside of Cu pin. Eventually, the cracks penetrate and pin break. In FM3, degradation data tends to gradually decrease, and crack initiates at P3 of Cu pin and expands laterally causing the pin break.

Figure 4(a) is the strain simulation result of the QFP chip, and Figure 4(b) is the top view of the strain simulation of all QFP chip solder joints. It can be seen intuitively that the strain of the chip is concentrated in the solder joint, indicating that the solder joint is the weak position of the chip and is most prone to fatigue damage. The mechanical response of solder joints at different chip positions is different in terms of value and distribution position. For solder joints, there is different strain distribution at different chip positions. From Figure 5, we find the strain is mainly concentrated in P1,P2,P3 where crack initiation occurs in SEM. From the analysis of strain responses in other test environment, results show that strain concentration area is also found at the P1,P2,P3 in most cases.

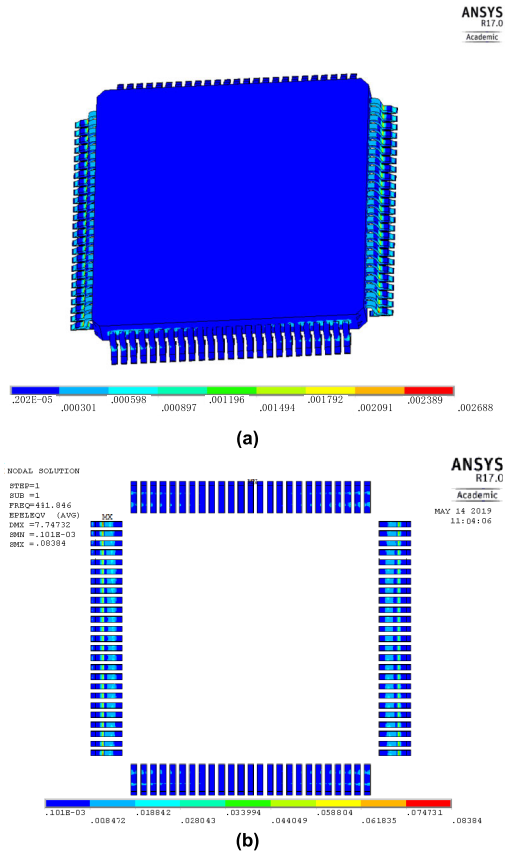

FIGURE 4. (a)Strain distribution of chip. (b)The top view of strain distribution of all chip solder joints.

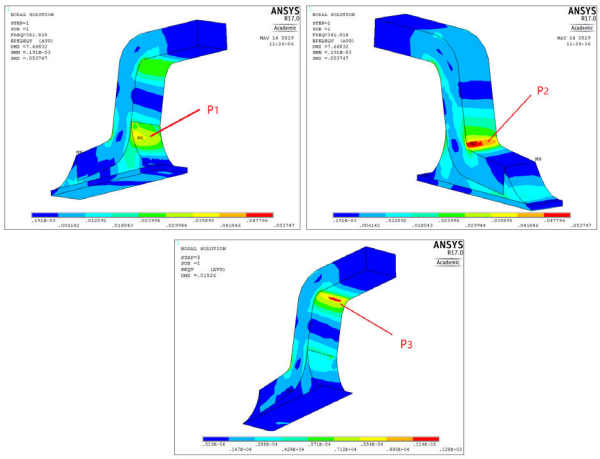

FIGURE 5. Strain simulation of single solder joint.

The degradation data over the entire solder joint life are huge and complicated. This article uses the Principal component of Mahalanobis distance(PCMD) health index method to evaluate the status of solder joints. For a detailed introduction of PCMD health index, please refer to another article [41] of our research team. PCMD health index is obtained by formula (1).

The obtained PCMD health index curve of FM1 is shown in Figure 6.

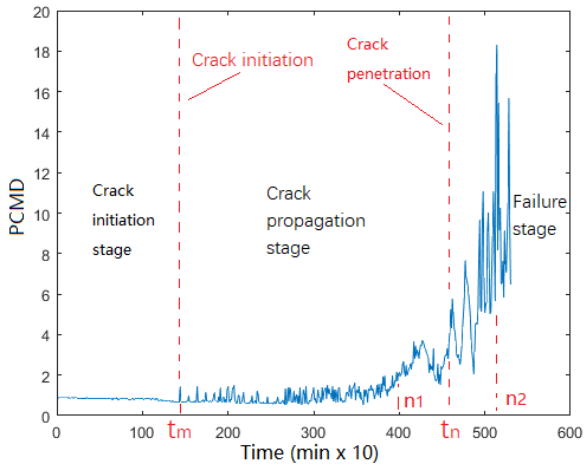

FIGURE 6. PCMD health index curve of FM1.

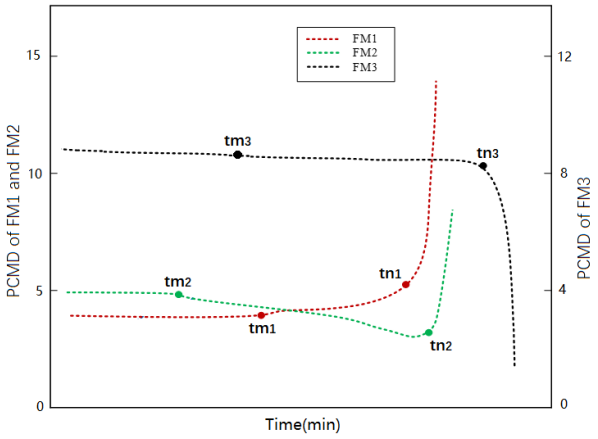

FIGURE 7. PCMD trend of each failure mode.

The degradation process is divided into 3 states: crack initiation stage, crack propagation stage and failure stage.

PCMD fluctuate at t_m first which means solder joint structure begin to have irrecoverable damage (cracks initiation). t_m is the time when the PCMD health index first fluctuates. We define t_n the moment of crack penetration. Due to vibration environment, even if solder broken, it still has weaker electrical conductivity due to repetitive crack opening and closing. Therefore, t_n lies between the moment n_1 and the moment n_2. n_1 is the time when the fluctuation range of the PCMD health index begins to increase; n_2 is the time when the PCMD health index appears its maximum value. Since it is difficult to measure the exact crack penetration time, the average value of n_1 and n_2 is defined as t_n which represents solder joint failure time.

After calculating the PCMD of FM2 and FM3 degradation data, it can be seen that the entire degradation process is able to be divided into three stages by t_m and t_n too, but the degradation trend is obviously different, as shown in Figure 7.

To estimate the solder joint lifetime (failure time), we have used the PCMD health index method to extract the solder joint

full-life degradation process, and the crack initiation time and failure time are determined. In this process, we applied the data-driven method to determine the lifetime. However, the data-driven method requires a large number of experiments to obtain data, which may not be feasible to engineering in practice. Comparatively speaking, it is more convenient and viable to predict the solder joint failure time though establishing the accurate physical model. According to the SEM analysis and finite element simulation analysis of the solder joint, we know that solder joint failure under coupled environmental stress has a clear failure mode and failure mechanism, and it is an important and necessary part in solder joint degradation modeling. Therefore, we hope to study the solder joint degradation and failure from the microscopic physical mechanism. This part aims to establish a clear functional relationship between the fatigue mechanical parameters and solder joint lifetime. The next section introduces the failure physical model, and considering the model applicability, physical models are revised by results of data-driven calculations under coupled environmental stress to obtain degradation models of QFP solder joints of different failure mode.

IV. DEGREDATION MODELING OF CHIP SOLDER JOINT BASED ON FAILURE PHYSICS

To improve the traditional failure physical methods, the Coffin-Manson and Paris model equation parameters are modified through t_m, t_n of PCMD and strain simulation data under coupled stress to model crack initiation stage and crack propagation stage.

Coffin-Manson model can describe the relationship between strain and fatigue life [42]. Because the stress level in high-cycle fatigue is within elastic deformation range, the cracks propagate in the elastic region, the strain belongs to elastic strain. Thus, the plastic strain term in Coffin-Manson equation can be discarded. We can get a modified form of Coffin-Manson equation:

$$\varepsilon = C\frac{\sigma_u}{E}N_f^b \tag{1}$$

E is elastic modulus; ε is the equivalent strain value;C is a constant coefficient. σ_u is the final tensile strength; N_f is number of fatigue life cycle. b is the fatigue strength index. Coffin-Manson has obtained $b = -0.12$ based on a large number of material fatigue life tests [43]–[45]. There will be slight differences in the fatigue strength indexes of different materials, but they are all close to -0.12, so the fatigue strength index is generally set to -0.12 when applying this model.

By fitting equation parameters through PCMD and simulation data, the Coffin-Manson equation can be revised to model crack initiation stage and predict t_m. n_f is defined as fatigue cycle number of per unit time. So:

$$\varepsilon = \frac{C\sigma_u}{E}(t_m n_f)^{-0.12} = \frac{C\sigma_u}{E(n_f)^{0.12}}\frac{1}{t^{0.12}} = A\frac{1}{t_m^{0.12}} \tag{2}$$

A is the strain strength factor, only relevant to the material and n_f. The formula(2) can be converted to the following:

$$t_m = \sqrt[0.12]{A\frac{1}{\varepsilon}} \tag{3}$$

The power spectral density (PSD) of random vibration and test temperature is constant in each test group, σ_u, E, n_f are regarded as constants, so the value of A in each test group is constant too. From the SEM results, we know the cracks of FM1,FM3 appear at single material. So using $1/t_m^{0.12}$ and ε of FM1 and FM3 to fit a straight line, A_{SnPb} and A_{Cu} can be obtained by line slope. FM2 has two cracks, so its t_m is defined as the first crack initiation time:

$$\begin{cases} t_m = \min\left\{t_m^{P1}, t_m^{P2}\right\} \\ t_m^{P1} = \sqrt[0.12]{A_{SnPb}\dfrac{1}{\varepsilon_{P1}}} \\ t_m^{P2} = \sqrt[0.12]{A_{Cu}\dfrac{1}{\varepsilon_{P2}}} \end{cases} \tag{4}$$

where t_m^{P1}, t_m^{P2} is the crack initiation time at P_1 and P_2; $\varepsilon_{P1}, \varepsilon_{P2}$ is strain at P_1 and P_2. Equations (3) (4) establish a relationship between the crack initiation time t_m and the microscopic strain.

The crack propagation time needs to be determined to obtain solder joint failure time. According to SEM results, cracks mainly manifest as penetrating cracks. Since the Paris model has better accuracy in describing such cracks, we select an amended form of Paris model that can describe the relationship of crack growth rate da/dN and strain amplitude $\Delta\varepsilon$, which is expressed as [46]:

$$\frac{da}{dN} = C_\varepsilon\,(\Delta\varepsilon)^{m_\varepsilon} \tag{5}$$

C_ε and m_ε are constants related by material. Take the logarithm on both sides:

$$\ln(da/dN) = \ln C_\varepsilon + m_\varepsilon \cdot \ln(\Delta\varepsilon) \tag{6}$$

The crack propagation time is defined as:

$$t_k = t_n - t_m \tag{7}$$

Since the PCMD fluctuation amplitude changes slowly in crack propagation stage, we assume that the crack grows at a uniform speed, then:

$$\frac{da}{dN} = \frac{L}{t_k} = \frac{L}{t_n - t_m} \tag{8}$$

L is the crack length. And formula (8) is converted as:

$$\ln(t_k) = \ln(t_n - t_m) = \ln\left(C'_\varepsilon\right) + m'_\varepsilon \cdot \ln(\Delta\varepsilon) \tag{9}$$

$C'_\varepsilon = L/C_\varepsilon$, $m'_\varepsilon = -m_\varepsilon$. From Equation(9), we find when the crack length is constant, the crack propagation time is linearly related to strain amplitude in the same material, in the logarithmic coordinate.

According to the crack propagation path of FM1, we can see the crack only propagates inside SnPb and we assume the

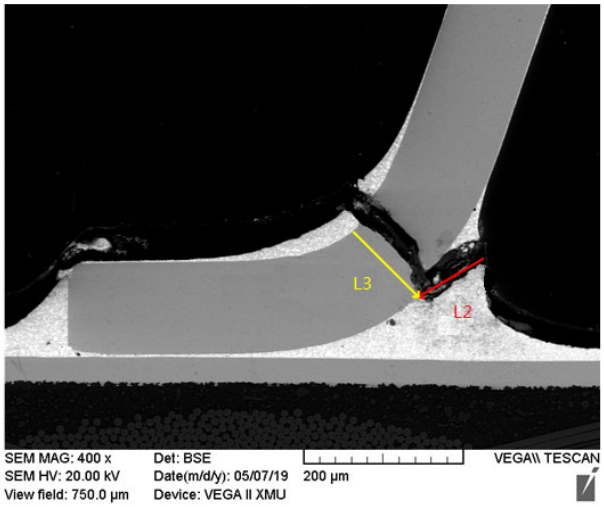

FIGURE 8. Crack propagation of FM2.

crack propagation constant length is L_1 in FM1. By extracting the strain amplitude $\Delta\varepsilon_1$ of crack propagation from simulation results and extracting the crack propagation time t_{k1} from PCMD data, the fitting curve of $\ln(t_{k1})$ and $\ln(\Delta\varepsilon_1)$ can be obtained:

$$\ln(t_{k1}) = a_1 + b_1 \ln(\Delta\varepsilon_1) \tag{10}$$

a_1, b_1 are fitting parameters. The failure time t_{n1} of FM1 is:

$$t_{n1} = t_{m1} + t_{k1} = \sqrt[0.12]{\frac{A_{SnPb}}{\varepsilon_1}} + \frac{e^{a_1}}{\Delta\varepsilon_1^{b_1}} \tag{11}$$

Then the relationship between $\ln(da/dN)$ and $\ln(\Delta\varepsilon)$ in SnPb is:

$$\begin{aligned} \ln(da/dN)_{SnPb} &= \ln(L_1/t_{k1}) \\ &= \ln(L_1) - a_1 - b_1 \ln(\Delta\varepsilon_1) \end{aligned} \tag{12}$$

Similarly, the crack penetrates the entire metal pin in FM3. The constant crack length is set to L_3, then the failure time of FM3 is:

$$t_{n3} = t_{m3} + t_{k3} = \sqrt[0.12]{\frac{A_{Cu}}{\varepsilon_3}} + \frac{e^{a_3}}{\Delta\varepsilon_3^{b_3}} \tag{13}$$

a_3, b_3 are fitting parameters.

For FM2 shown in Figure 8, we define an intersection of two cracks to simplify the analysis, and both cracks terminate at this position. Crack length in SnPb is L_2 and the crack length through the Cu pin is still L_3. Then, the crack propagation time of FM2 is a longer propagation time of two cracks:

$$\begin{cases} t_{k2} = \max\left\{t_{k2}^{Cu}, t_{k2}^{SnPb}\right\} \\ \ln(t_{k2}^{Cu}) = a_3 + b_3 \ln\left(\Delta\varepsilon_2^{Cu}\right) \\ \ln(t_{k2}^{SnPb}) = \ln(L_2) - \ln(da/dN)_{SnPb} \\ \qquad\qquad = a_2 + b_1 \ln\left(\Delta\varepsilon_2^{SnPb}\right) \end{cases} \tag{14}$$

$t_{k2}^{Cu}, t_{k2}^{SnPb}$ are the propagation times of two cracks; $\Delta\varepsilon_2^{Cu}, \Delta\varepsilon_2^{SnPb}$ are the strain amplitudes of two cracks; And $a_2 = \ln(L_2) - \ln(L_1) + a_1$.

The failure time t_{n2} of FM2 is calculated as follows:

$$\begin{aligned} t_{n2} = t_{m2} + t_{k2} &= \min\left\{\sqrt[0.12]{A_{SnPb} \cdot \frac{1}{\varepsilon_{P1}}}, \sqrt[0.12]{A_{Cu} \cdot \frac{1}{\varepsilon_{P2}}}\right\} \\ &+ \max\left\{\frac{e^{a_3}}{(\Delta\varepsilon_2^{Cu})^{b_3}}, \frac{e^{a_2}}{(\Delta\varepsilon_2^{SnPb})^{b_1}}\right\} \end{aligned} \tag{15}$$

Equations (11), (13), and (15) establish the relationship of failure time and strain, strain amplitude of three chip solder joints failure modes, respectively.

In this way, after the model parameters being modified by test and simulation data from coupled loads, traditional failure physical models can be applied in a wider range of complex environment instead of simple single stress. This makes the degradation model established in this study is more in line with the actual situation. On the other hand, from the solder joint degeneration model, we can see that the model input is solder joint strain and strain amplitude, so obtaining accurate solder joint lifetime only needs a finite element simulation. This creates a huge advantage in engineering.

V. CHIP RELIABILITY MODELING BASED ON SOLDER JOINT COMPETITIVE FAILURE

Chip solder joints have many potential failure modes. The failure mode of first failed solder joint may be any one of FM1, FM2, FM3 etc. So the relationship between chip reliability and each solder joint failure mode reliability needs to be described by a competitive failure model. All solder joints of one chip are fixed on the chip package body and PCB. When cracks occur in one solder joint, it will inevitably change the stress-strain distribution of the entire chip. Thus, failure of multiple solder joints has a mutually dependent competitive relationship.

A. CHIP SOLDER JOINT RELIABILITY MODEL BASED ON WEIBULL DISTRIBUTION

Through the chip reliability degradation test, we find that the failure mode of the first failed solder joint is indeed any one of FM1, FM2, and FM3 of Section III. And the failure rate is not a constant value during the lifetime. Weibull distribution can simulate the increasing or decreasing failure rate, so it is widely used in the description of product life distribution [47]. Therefore, this article selects Weibull distribution to study the distribution of failure time. Its distribution function is:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \quad t > 0 \tag{16}$$

The parameters include the shape parameter β and the scale parameter η called the characteristic life, too. The probability

density function of Weibull distribution is:

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)\exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \quad t > 0 \tag{17}$$

According to formula (16), the reliability function of solder joint is:

$$R(t) = 1 - F(t) = \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \quad t > 0 \tag{18}$$

The shape parameter is often regarded as a constant value that does not change with the environmental stress load [47], [48]. Yet according to the SEM analysis and finite element simulation analysis, the microscopic cracks and mechanical responses of each failure mode are different., so it is not accurate to set the shape parameters of different failure modes as a constant value under the same environment. Therefore, this article defines the shape parameter as fixed values under different test environments and sets them to different values as $\beta_1, \beta_2, \cdots, \beta_p$ based on failure modes, while p represents the number of failure modes. Meanwhile, we use theoretical solder joint failure time t_n as the characteristic parameter η of Weibull distribution model.

B. MUTUALLY DEPENDENT COMPETING FAILURE MODEL OF CHIP SOLDER JOINT IN DIFFERENT FAILURE MODES

1) MUTUALLY DEPENDENT COMPETING FAILURE MODEL BASED ON COPULA FUNCTION

The Copula function method is easier to relate to the actual problem, so it has become an important method to solve the mutually dependent competing failure problem [49]. According to Sklar's theorem [50], an p-dimensional joint distribution function can be represented by a Copula function about its p marginal distribution functions:

$$F\left(x_1, x_2, \cdots, x_p\right) = C\left(F_1\left(x_1\right), F_2\left(x_2\right), \cdots, F_p\left(x_p\right); \theta\right) \tag{19}$$

We have assumed that any one of solder joint failure occurrence can lead to chip malfunction, so chip only maintains normal operation when all potential solder joint failures have not occurred. The chip reliability function can also be described by Copula function of each solder failure mode reliability function:

$$\begin{aligned} R(t) &= P\left[T_1 > t, T_2 > t, \cdots, T_p > t\right] \\ &= \hat{C}\left(R_1(t), R_2(t), \cdots, R_p(t); \theta\right) \end{aligned} \tag{20}$$

The chip failure probability due to failure mode k can be obtained, as shown in the formula (21). $f_k(t)$ is the marginal failure probability density function of failure mode k.

$$f^{(k)}(t) = \frac{\partial \hat{C}\left(R_1(t), R_2(t), \cdots, R_p(t); \theta\right)}{\partial R_k(t)} f_k(t) \tag{21}$$

We assume that there are P failure modes in chip solder joints. In i-th test group, a total of $n_i^{(k)}$ failure test samples have the k-th failure mode, and the failure times are $t_{i1}, t_{i2}, \cdots, t_{in_i^{(k)}}$, respectively. j is the sample serial number and $j \in \left[t_{i1}, t_{i2}, \cdots, t_{in_i^{(k)}}\right]$. Then, the likelihood function of all test samples in the i-th test is:

$$\begin{aligned} L_i &= \left[\hat{C}\left(R_1\left(t_{i0}\right), R_2\left(t_{i0}\right), \cdots, R_p\left(t_{i0}\right); \theta\right)^{n_{i0}}\right] \\ &\times \prod_{k=1}^{P}\left[\prod_{j=1}^{n_i^{(k)}} \frac{\partial \hat{C}\left(R_1\left(t_{ij}\right), R_2\left(t_{ij}\right), \cdots, R_p\left(t_{ij}\right); \theta\right)}{\partial R_k\left(t_{ij}\right)} f^{(k)}\left(t_{ij}\right)\right] \end{aligned} \tag{22}$$

In the formula, $\hat{C}\left(R_1\left(t_{i0}\right), R_2\left(t_{i0}\right), \cdots, R_p\left(t_{i0}\right); \theta\right)^{n_{i0}}$ is the probability that a total of n^{i0} samples have not failed at the censoring time $t_{i0}t_{i0} \geq \max\left(t_{i1}, t_{i2}, \cdots, t_{in_i^{(k)}}\right)$. The log-likelihood function of all samples in i tests is:

Considering the calculation difficulty, calculation efficiency and result accuracy, we select the parameter estimation method based on IFM [51], which can effectively simplify calculation as well as ensuring the estimation accuracy.

Step 1: According to failure time data of each failure mode and marginal failure probability density function, the formula (24) is maximized to obtain the estimated values of reliability model parameter β of each failure

$$\begin{aligned} \ln L &= \sum_{i=1}^{m}\left[\begin{array}{l} n_{i0}\ln\left[\hat{C}\left(R_1\left(t_{i0}\right), R_2\left(t_{i0}\right), \cdots, R_p\left(t_{i0}\right); \theta\right)\right] \\ + \sum_{k=1}^{P}\left[\sum_{j=1}^{n_i^{(k)}}\left[\ln\frac{\partial \hat{C}\left(R_1\left(t_{ij}\right), R_2\left(t_{ij}\right), \cdots, R_p\left(t_{ij}\right); \theta\right)}{\partial R_k\left(t_{ij}\right)} + \ln f^{(k)}\left(t_{ij}\right)\right]\right] \end{array}\right] \\ &= \sum_{i=1}^{m}\left[\begin{array}{l} n_{i0}\ln\left[\hat{C}\left(R_1\left(t_{i0}\right), R_2\left(t_{i0}\right), \cdots, R_p\left(t_{i0}\right); \theta\right)\right] \\ + \sum_{k=1}^{P}\left[\sum_{j=1}^{n_i^{(k)}}\left[\begin{array}{l} 2\ln\frac{\partial \hat{C}\left(R_1\left(t_{ij}\right), R_2\left(t_{ij}\right), \cdots, R_p\left(t_{ij}\right); \theta\right)}{\partial R_k\left(t_{ij}\right)} \\ + \ln\frac{\beta_k}{\eta_k}\left(\frac{t_{ij}}{\eta_k}\right)\exp\left[-\left(\frac{t_{ij}}{\eta_k}\right)^{\beta_k}\right] \end{array}\right]\right] \end{array}\right] \end{aligned} \tag{23}$$

TABLE 3. Examples of Solder Joint Failure Data.

Test number	Solder joint FM	Characteristic life η_{ik}	Censoring time t_{i0}	Failure time $t_{ij}^{(k)}$
Test 1	1	η_{11}	t_{10}	$t_{11}^{(1)}, t_{12}^{(1)}, \cdots, t_{1n}^{(1)}$
	2	η_{12}		$t_{11}^{(2)}, t_{12}^{(2)}, \cdots, t_{1n}^{(2)}$
	3	η_{13}		$t_{11}^{(3)}, t_{12}^{(3)}, \cdots, t_{1n}^{(3)}$
Test 2	1	η_{21}	t_{20}	$t_{21}^{(1)}, t_{22}^{(1)}, \cdots, t_{2n}^{(1)}$
	2	η_{22}		$t_{21}^{(2)}, t_{22}^{(2)}, \cdots, t_{2n}^{(2)}$
	3	η_{23}		$t_{21}^{(3)}, t_{22}^{(3)}, \cdots, t_{2n}^{(3)}$

mode.

$$\sum_{i=1}^{m}\sum_{j=1}^{n_i^k} \ln f^{(k)}\left(t_{ij}\right) = \sum_{i=1}^{m}\sum_{j=1}^{n_i^k}\left[\begin{array}{l} \ln \dfrac{\partial \hat{C}\left(R_1\left(t_{ij}\right), R_2\left(t_{ij}\right), \cdots, R_p\left(t_{ij}\right); \theta\right)}{\partial R_k\left(t_{ij}\right)} \\ + \ln \dfrac{\beta_k}{\eta_k}\left(\dfrac{t_{ij}}{\eta_k}\right) \exp\left[-\left(\dfrac{t_{ij}}{\eta_k}\right)^{\beta_k}\right] \end{array}\right] \quad t > 0, k = 1, 2, \cdots, p \tag{24}$$

Step 2: The reliability model parameter β of each failure mode is substituted into log-likelihood function (23), as shown at the bottom of the previous page, and then the log-likelihood function of all subject samples is maximized to obtain the estimated value of Copula function parameter θ.

2) PARAMETER SOLUTION OF CHIP RELIABILITY MODEL BASED ON TEST AND SIMULATION DATA

We exemplify the reliability of solder joints and chips under 25^oC and $0.8g^2/Hz$ random vibration as an example. From the reliability degradation test in Section II and the PCMD health index analysis in Section III, a large amount of solder joint failure time $t_{ij}^{(k)}$ can be obtained. According to solder joint degradation model established in Section IV, the strain, strain amplitude results of the finite element simulation are substituted into formula (11)(13)(15) to calculate the characteristic life η_{ik} of each failure mode. Where i is the test serial number, j is the sample serial number, and k is the failure mode serial number. We take two sets of degradation test data as an example. Its specific form is shown in Table 3.

Copula function has many different forms. They describe the different correlations between variables, which make a model owning different correlation structure. In this article, the optimal Copula function is identified by Akaike Information Criterion (AIC) method, which weighs complexity and the superiority of chip reliability models based on different

TABLE 4. Model AIC Values of Different Copula Functions.

AIC	$2K - 2\ln L_{(\max)}$
Gumbel copula	823.7
Clayton copula	855.2
Frank copula	841.9

Copula functions. We choose widely used Gumbel copula, Clayton copula and Frank copula as alternative functions. The AIC values of reliability models are calculated respectively, as shown in Table 4. K is the number of unknown model parameters, and L is the maximum likelihood function value.

It was found that the model based on Gumbel Copula function has the smallest AIC value, so we chose the Gumbel Copula function. its expression is:

$$C\left(u_1, u_2, \cdots, u_n; \theta\right) = \exp\left(-\left[\begin{array}{l}(-\ln u_1)^\theta + (-\ln u_2)^\theta + \\ \cdots + (-\ln u_n)^\theta\end{array}\right]^{1/\theta}\right) \tag{25}$$

Bring the solder joint failure mode reliability functions (18) into the function (25) to obtain the overall chip reliability function associated with multiple solder joint failure modes:

$$\begin{aligned} R(t) &= \hat{C}\left(R_1(t), R_2(t), \cdots, R_n(t); \theta\right) \\ &= \exp\left(-\left[(-\ln R_1(t))^\theta + (-\ln R_2(t))^\theta \right.\right. \\ &\quad \left.\left. + \cdots + (-\ln R_n(t))^\theta\right]^{1/\theta}\right) \\ &= \exp\left(-\left[\left(\frac{t}{\eta_1}\right)^{\beta_1\theta} + \left(\frac{t}{\eta_2}\right)^{\beta_2\theta} + \cdots + \left(\frac{t}{\eta_n}\right)^{\beta_n\theta}\right]^{\frac{1}{\theta}}\right) \end{aligned} \tag{26}$$

In this research, the most vulnerable solder joints are selected from each failure mode respectively to establish the chip reliability model, and the chip reliability function can be obtained as:

$$\begin{aligned} R(t) &= \hat{C}\left(R_1(t), R_2(t), R_3(t); \theta\right) \\ &= \exp\left(-\left[\left(\frac{t}{\eta_1}\right)^{\beta_1\theta} + \left(\frac{t}{\eta_2}\right)^{\beta_2\theta} + \left(\frac{t}{\eta_3}\right)^{\beta_3\theta}\right]^{\frac{1}{\theta}}\right) \end{aligned} \tag{27}$$

The parameters of the reliability model are estimated using IFM method. In the first stage, the log-likelihood function of the edge probability density of each failure mode is solved, as shown in Equation (28), as shown at the bottom of the next page. $\beta_1, \beta_2, \beta_3$ is calculated on computer using the maximum likelihood method. At the same time, 95% is taken as

TABLE 5. Estimated Values and Confidence Interval of Model Parameters.

	Estimated values	Confidence interval
β_1	2.532	(2.141, 2.765)
β_2	2.369	(1.876, 2.683)
β_3	2.481	(2.353, 3.512)
θ	4.936	(4.334, 6.079)

the estimated confidence level $1-\alpha$ in parameters estimation to obtain the confidence interval of parameters. In the second stage, the log-likelihood function of all samples in i tests is calculated, as shown in equation (29), as shown at the bottom of the page. Also, θ is calculated through maximum likelihood estimation,. Similarly, we take 95% as the estimated confidence level to obtain the confidence interval of the parameter.

The parameters of the reliability model and the confidence interval of the parameters which were directly calculated on computer are displayed in Table 5. The results show that the estimated parameters are within the confidence interval, proving that the parameter estimation result is credible.

The reliability of solder joint during fatigue failure can be calculated by substituting estimated shape parameter β and calculated characteristic life η (theoretical failure time according to solder joint degradation model). Under 25^oC and $0.8g^2/Hz$ random vibration, the characteristic life η_1, η_2, η_3 of three failure modes is calculated, as shown in Table 6.

The chip reliability can be obtained by substituting each failure mode reliability function and estimated Copula function parameter θ into chip reliability equation (27). Therefore, the reliability models of FM1,FM2, FM3 and their chip are $R_1(t), R_2(t), R_3(t), R(t)$ in equation (30),

TABLE 6. Characteristic Life of Three Failure Modes Solder Joints.

Characteristic life /min	η_1	η_2	η_3
	9406	9954	14876

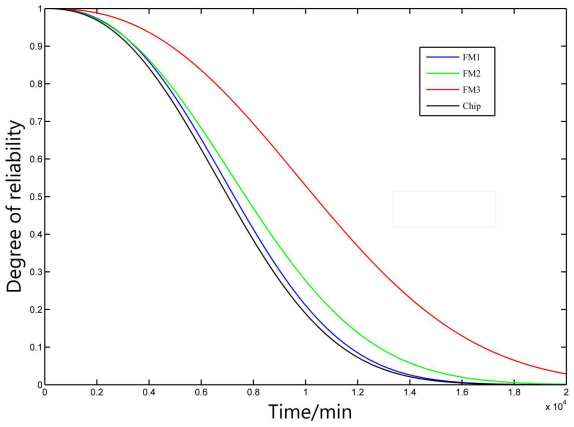

FIGURE 9. The reliability of chip and three solder joint failure modes.

as shown in Figure 9.

$$R_1(t) = \exp\left[-\left(\frac{t}{9406}\right)^{2.532}\right]$$
$$R_2(t) = \exp\left[-\left(\frac{t}{9954}\right)^{2.369}\right]$$
$$R_3(t) = \exp\left[-\left(\frac{t}{14876}\right)^{2.481}\right]$$
$$R(t) = \exp\left(-\left[\left(\frac{t}{9406}\right)^{12.498} + \left(\frac{t}{9954}\right)^{11.693}\right]^{0.203} + \left(\frac{t}{14876}\right)^{12.246}\right) \tag{30}$$

We find FM3 has the highest reliability among the three solder joint failure modes indicating that solder joints are

$$\sum_{i=1}^{m}\sum_{j=1}^{n_i^k} \ln f^{(k)}(t_{ij}) = \sum_{i=1}^{m}\sum_{j=1}^{n_i^k}\left[\ln\frac{\partial \hat{C}\left(R_1(t_{ij}), R_2(t_{ij}), R_3(t_{ij}); \theta\right)}{\partial R_k(t_{ij})} + \ln\frac{\beta_k}{\eta_k}\left(\frac{t_{ij}}{\eta_k}\right)\exp\left[-\left(\frac{t_{ij}}{\eta_k}\right)^{\beta_k}\right]\right], \quad k = 1, 2, 3 \tag{28}$$

$$\ln L = \sum_{i=1}^{m}\left[n_{i0}\ln\left[\hat{C}(R_1(t_{i0}), R_2(t_{i0}), R_3(t_{i0}); \theta)\right] + \sum_{k=1}^{3}\left[\sum_{j=1}^{n_i^{(k)}}\left[2\ln\frac{\partial \hat{C}\left(R_1(t_{ij}), R_2(t_{ij}), R_3(t_{ij}); \theta\right)}{\partial R_k(t_{ij})} + \ln\frac{\beta_k}{\eta_k}\left(\frac{t_{ij}}{\eta_k}\right)\exp\left[-\left(\frac{t_{ij}}{\eta_k}\right)^{\beta_k}\right]\right]\right]\right] \tag{29}$$

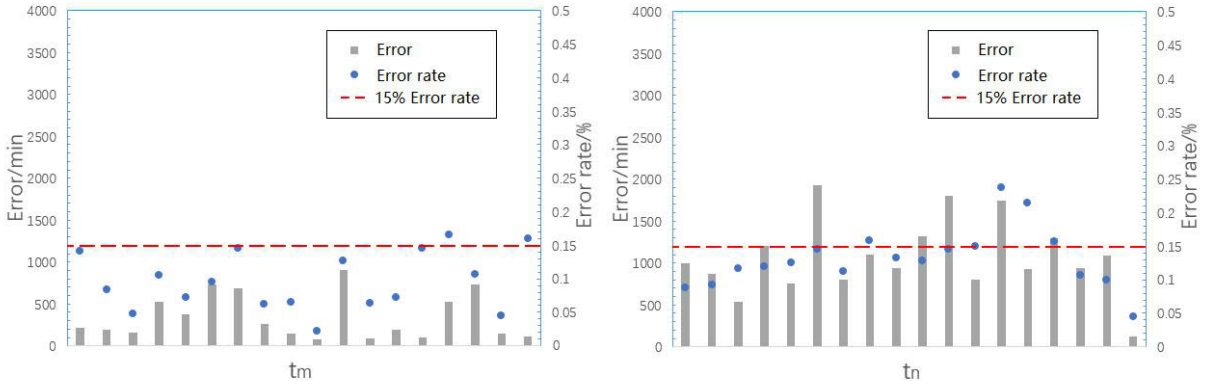

FIGURE 10. Model prediction error distribution of t_m and t_n.

most difficult to fail when strain concentration only appears at P3. FM1's solder joints have the lowest reliability indicating that cracks are more likely to fail when they appear at solder and propagate along with contact areas of different material. The chip reliability is close to the reliability of FM1 solder joint, but lower than the reliability of each solder joint failure mode. This also shows that it is inaccurate to directly characterize the chip reliability according to the most vulnerable solder joint.

C. MODEL VERIFICATION AND ERROR DISCUSSION

We set up verification tests under $25\,^oC$ and $0.8g^2/Hz$ random vibration to verify the accuracy of solder joint degradation models and chip reliability model.

For solder joint degradation model, the actual t_m and t_n are compared with t_m and t_n calculated by degradation model. According to the distribution of model errors shown in Figure 10, we found that model errors are less than 15%, which can meet the accuracy requirement.

At the same time, we find the accuracy of t_n is lower, indicating that the bigger error is brought in calculation of crack propagation time. This article has not considered intermetallic compounds (IMC) that caused by the combination reaction between different metal materials. Therefore, the impact of IMC on the crack propagation speed is not considered in solder joint degradation modeling at Section IV. But actually, IMC has poorer brittleness, and the crack propagation speed in IMC is faster than that in a single material [52]. So when the crack is assumed to propagate at a uniform speed, the error will be introduced. This means model t_n of FM1 and FM2 is bigger than real t_n. So test and model t_n of FM1 and FM2 is expressed in Figure 11. Results show that test t_n is indeed a bit smaller than model t_n under most circumstances which verified conjecture of error source.

For solder joints and chip reliability model, due to IMC is not considered causing η of FM1 and FM2 is larger than the actual value, so we can qualitatively analyze that the reliability of FM1, FM2 solder joints and chips is greater than actual value too, according to equations (18) and (26). In the

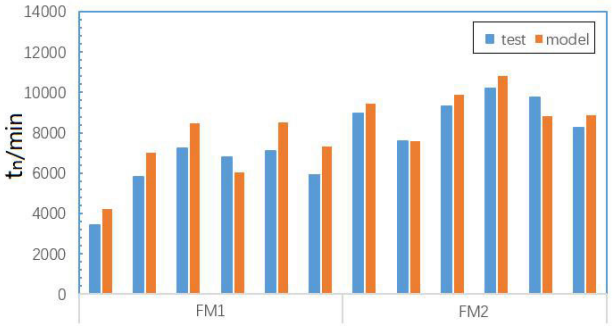

FIGURE 11. Test and model t_n of FM1,FM2.

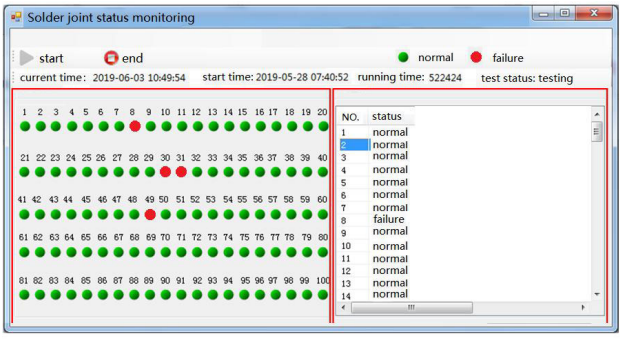

FIGURE 12. Solder joint status monitoring software.

environmental stress test, the solder joint status monitoring software, shown in Figure 12, is used to monitor the status of chip solder joints in real time. The capacitor charging time corresponding to solder failure time has been counted through a large number of previous degradation tests. Their average value, input to monitoring software, is taken as the monitoring threshold to determine whether the solder joint has failed. The normal number n_1, n_2, n_3 of these three solder joints in all samples are counted separately at intervals. n_1, n_2, n_3 is divided by the samples number N to obtain solder joint reliability. According to the finite element simulation, the solder joint is the vulnerable area of the chip. Therefore, we detect

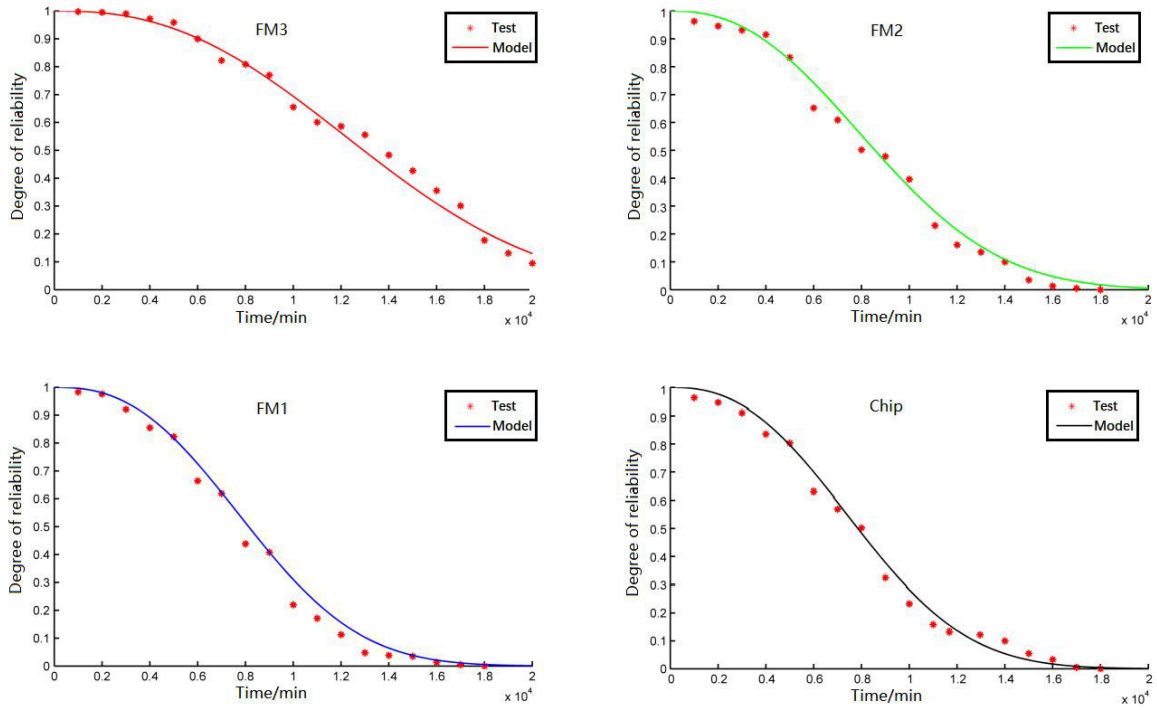

FIGURE 13. Test and model reliability of FM1, FM2, FM3 and chip.

the state of all chip solder joints. Once any solder joint fails, the chip is deemed to failed, and the chip failure time is the first solder joint failure time.. Similarly, the normal number of chip is counted at the interval and divided by N to obtain the chip reliability.

The accuracy of reliability models can be analyzed by comparing the reliability model curve with the reliability data obtained by statistical calculation, as shown in Figure 13. It can be seen the test results are consistent with the model curve, indicating that the solder joint reliability model and chip reliability model based on multiple solder joint competing failure can reflect the actual circumstances. And we can find that the reliability of model is indeed higher than the reliability of test for FM1, FM2 and chip especially during reliability rapid changing stage. This also shows that IMC is the important source of error in modeling.

VI. CONCLUSION

This article takes QFP chip solder joints as the main research object. The chip reliability model under constant temperature and random vibration are established based on the solder joint degradation mechanism and the mutually dependent competing failure theory.

First, the failure samples are obtained through chip degradation tests, and the stress-strain response of solder joints is obtained through finite element simulation. Three solder joint failure modes are distinguished based on SEM analysis, FEM analysis and test data.

Then, Coffin-Manson and Paris failure physical model is modified by the data-driven PCMD health index to establish degradation models, which provides a theoretical reference for the degradation mechanism of solder joints and a general research method for solder joint degradation modeling under coupled environment loads. As failure time is predicted as the characteristic life of two-parameter Weibull distribution, the established solder joint degradation model is linked with the solder joint reliability model. The shape parameters under different failure modes are set as changing values which simulates the solder joint degradation in actual circumstances and thus makes the solder joint and chip reliability models more accurate.

Finally, Chip reliability model based on mutually dependent competing failure of solder joints is established according to the Gumbel Copula function. The parameters of the solder joints and chip reliability models are estimated through the IFM method. The result shows that the chip reliability is close to the reliability of FM1 solder joint, but lower than the reliability of each solder joint failure mode. This means our model is more accurate than directly characterizing the chip reliability according to the most vulnerable solder joint. Verification tests are carried out to verify the accuracy of solder joint degradation models. Simultaneously, the actual reliability data of solder joints and chips are obtained to be compared with reliability model curves. Consistent results verify the effectiveness and accuracy of reliability model. And we find that the poor brittleness of IMC is the main source of errors in degradation models and reliability models.

In this article, we innovate a reliability modeling method, which provides an idea for transition from solder joint level reliability to component level reliability. Based on this

method and competitive failure theory, we can continue to study the reliability of simple and integrated components and their joint failure. It is also possible to establish the electronic system level reliability model in future studies.

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