IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 18, 2020, accepted November 7, 2020, date of publication November 10, 2020,
date of current version November 19, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3037228

A 7.6b ENOB, 16× Gain, 360mV$_{pp}$ Output Swing, Open-Loop Charge Steering Amplifier

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This work was supported in part by NSFC under Grant 62004023, in part by the National Key Research and Development Program of China under Grant 2018YFB2100100, and in part by the Department of Science and Technology of Sichuan Province under Grant 2018GZDZX0001/0002/0003.

ABSTRACT This paper presents a high-resolution, high-gain, wide-input-output-swing open-loop charge steering amplifier for pipelined successive-approximation-register (SAR) analog-to-digital converter (ADC). Compared to prior charge-steering amplifiers where every transistor is in the saturation region, the proposed amplifier uses cascode input transistors operating in the linear region, which improves its linearity and input swing. To increase the gain, the amplification time is extended by charging the load capacitance through PMOS transistors. Besides, the gain-boost structure is used to adjust the drain voltage of input transistors operating in the linear region, so that nearly the same gain at different process corners is realized. We designed two versions of the proposed amplifier. Both are in a 40-nm CMOS technology, and both achieve 7.6-bit ENOB accuracy. Compared to prior charge-steering amplifiers, ENOB is increased by 1.6-bits; gain is increased by 3.2 times (or even larger); and output swing is increased by 3.6 times.

INDEX TERMS Charge steering amplifier, open-loop, high-gain, high-accuracy, wide signal swing, pipelined successive-approximation-register analog-to-digital converter.

I. INTRODUCTION

For high-speed and high-resolution applications, a pipelined successive-approximation-register (SAR) analog-to-digital converter (ADC) [1]–[7] is a promising architecture [8]. Its first stage usually should have high resolution. However, in such ADCs, traditional closed-loop operational transconductance amplifiers are not only power-hungry for realizing fast settling and high accuracy, but also scaling unfriendly due to low intrinsic transistor gain in nanometer CMOS.

In recent years, charge steering amplifier [9] has become an attractive structure for pipelined-SAR ADCs because it benefits from noise filtering and dynamic power features [8]. Nevertheless, traditional charge steering amplifiers still have several limitations: low settling accuracy, small input-output swing, and limited voltage gain [10]. For example, to guarantee sufficient (≥6 b) settling accuracy, the input swings in [14] and [15] are limited to 25 mV and 19 mV, respectively. In [8] and [10]–[20], because the input transistors are in the saturation region, the squared relationship in I-V of MOSFET limits the linearity of the charge steering amplifiers. And if the linearity needs to be improved, the input swing is limited. The small input swing and small gain lead to small output swing, which limits the quantization resolution of the next stage SAR.

To address the above issues, a novel open-loop charge steering amplifier is proposed in this work. Cascode input transistors are in the linear region (rather than the saturation region), which improves the gain linearity and input swing, and reduces kickback noise. The simultaneous charging and discharging operation at the load capacitor makes high gain possible. Moreover, gain-boost and negative feedback are used to reduce the gain variation under process variations. Since there is a trade-off among high gain, large input-output swing, and high speed, we designed two versions of the amplifier with different performance. Designed in a 40-nm CMOS process, the first version achieves 7.6-b settling accuracy, 16 × gain, 320 mV$_{pp}$ output swing at 100 MHz clock frequency, and the second version achieves 7.7-b settling accuracy, 8 × gain, 360 mV$_{pp}$ output swing

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

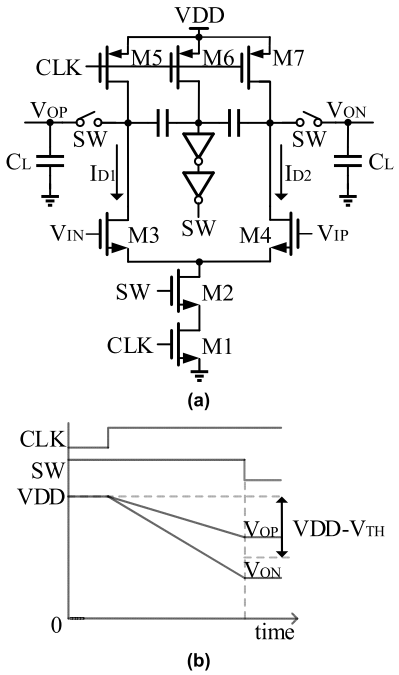

FIGURE 1. (a) Schematic and (b) timing diagram of prior charge steering amplifier [11].

at 500 MHz clock frequency. By contrast, traditional charge steering amplifiers usually achieve only 6-b settling accuracy with no more than 5 × gain and 100 mV_{pp} output swing [14], [15].

This paper is organized as follows. Section II reviews the prior charge steering amplifier. Section III analyzes the proposed charge steering amplifier. Section IV shows the post-layout simulation results, and compares it with state-of-the-art works. And finally, Section V concludes the paper.

II. PRIOR CHARGE STEERING AMPLIFIER

FIGURE 1 shows the schematic and timing diagram of a prior charge steering amplifier [11]. It is an open-loop amplifier. When CLK is low, the load capacitance C_L at output nodes is charged to *VDD*. At the rising edge of CLK, the load capacitance begins to discharge, and the voltages of output nodes (V_{OP} and V_{ON}) decrease at different rates depending on the input differential voltage. When the common-mode voltage of V_{OP} and V_{ON} crosses the threshold voltage of inverter, SW becomes low to end the discharging of load capacitance C_L, and the falling of output voltage is stopped.

The input MOS transistors are in the saturation region. And their currents I_{D1} and I_{D2} can be approximated as follows [11]:

$$I_{D1} \approx I_{D0} - \frac{g_m}{2}\Delta V_{IN} \tag{1}$$

$$I_{D2} \approx I_{D0} + \frac{g_m}{2}\Delta V_{IN} \tag{2}$$

where g_m is the transconductance, I_{D0} is the common-mode drain current, and ΔV_{IN} is the input differential signal. The voltages at V_{OP} and V_{ON} are derived as follows [11]:

$$V_{OP} \approx V_{DD} - \frac{I_{D0} - \frac{g_m}{2}\Delta V_{IN}}{C_L + C_P} t_{int} \tag{3}$$

$$V_{ON} \approx V_{DD} - \frac{I_{D0} + \frac{g_m}{2}\Delta V_{IN}}{C_L + C_P} t_{int} \tag{4}$$

$$t_{int} = \frac{(V_{DD} - V_{TH})(C_L + C_P)}{I_{D0}} \tag{5}$$

where t_{int} is the integration time, V_{TH} is the threshold voltage of inverter, C_L is the load capacitance, and C_P is the parasitic capacitance at output nodes. According to equations (3) and (4), the differential gain G_{diff} can be written as follows [11]:

$$G_{diff} = \frac{(V_{OP} - V_{ON})}{\Delta V_{IN}} \approx \frac{g_m t_{int}}{C_L + C_P} \tag{6}$$

Substitution of (5) into (6) results in

$$G_{diff} = \frac{g_m (V_{DD} - V_{TH})}{I_{D0}} \tag{7}$$

From these equations, we can see several limitations of the charge steering amplifier of FIGURE 1. Firstly, equations (1) and (2) are accurate only when the input differential signal ΔV_{IN} is small (small-signal analysis is valid). Secondly, the transconductance linearity from input voltage to output current deteriorates dramatically with the increase of input differential signal. This is due to the squared relationship, rather than linear relationship, in MOSFET I-V. Thirdly, according to equation (7), the differential gain G_{diff} is limited to a small value (no more than 5 in simulation), inherently due to the limited values of supply voltage and g_m/I_D [10]. Because both high gain and high settling accuracy are required in a residual amplifier of pipelined SAR ADC, we propose a high-gain and high-accuracy charge steering amplifier in the next section.

III. PROPOSED CHARGE STEERING AMPLIFIER

The proposed open-loop amplifier includes three parts: core circuit, gain-boost circuit, and common-mode feedback circuit. The core circuit is an amplifier with high settling accuracy, large gain, and large input-output swing. The gain-boost circuit is used to set the drain voltages of input transistors to a fixed value, thus achieving a relatively constant gain with small gain variations under process variations. The common-mode feedback circuit stabilizes the output common-mode voltage under process variations.

A. CORE CIRCUIT AND ITS PRINCIPLE

The schematic and timing diagram of the core amplifier are shown in FIGURE 2 and FIGURE 3, respectively. In FIGURE 2, the input transistors (M1 and M2) are in the linear region, and the cascode transistors (M3 and M4) are in the saturation region. This topology helps improve the gain linearity significantly, as will be explained later. For

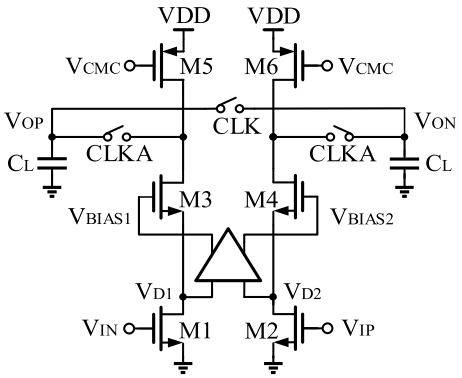

FIGURE 2. Schematic of the core circuit.

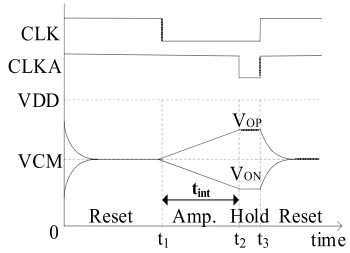

FIGURE 3. Timing diagram of the core circuit.

easy understanding, the operation is divided into three phases (reset phase, amplification phase, and hold phase), as shown in FIGURE 3. During both the reset phase and amplification phase (during $0\sim\ t_2$), the load capacitance C_L is charged through the P-end branch (M5∼6) and discharged through the N-end branch (M1∼4). Since the charging rate is the same as the discharging rate, the output common-mode voltage is always fixed at V_{CM} (0.6 V in this work). In the reset phase (during $0\sim t_1$), CLK and CLKA are high. Thus, the output nodes V_{OP} and V_{ON} are connected and reset to V_{CM}. At the falling edge of CLK (time t_1), V_{OP} and V_{ON} are disconnected. Then, V_{OP} and V_{ON} rise and fall at the same speed according to the input differential signal. The output differential signal increases as time goes on until CLKA becomes low (time t_2), which disconnects the capacitance C_L from the charging and discharging branches (M1∼6). After that, V_{OP} and V_{ON} remain unchanged until the next reset phase begins (time t_3). Compared to the prior structure of FIGURE 1(a), the proposed structure uses an extra P-end branch to charge the load capacitors during the amplification phase. Thus, the common-mode detector of the prior structure is no longer needed in this work, and the amplification time (integration time) can be longer because the voltages of output nodes will not drop quickly to *GND*. Longer amplification time also helps increase the voltage gain, as will be explained below.

B. GAIN ANALYSIS

Unlike the prior structure of FIGURE 1, the input transistors M1∼2 of this work are in the linear region. The currents through these input transistors can be calculated as follows:

$$I_{D1} = \mu_n Cox \frac{W}{L}\left[\left(V_{IN\_CM} - \frac{\Delta V_{IN}}{2} - V_{TH1,2}\right) \times V_{DS1} - \frac{1}{2}V_{DS1}^2\right] \quad (8)$$

$$I_{D2} = \mu_n Cox \frac{W}{L}\left[\left(V_{IN\_CM} + \frac{\Delta V_{IN}}{2} - V_{TH1,2}\right) \times V_{DS2} - \frac{1}{2}V_{DS2}^2\right] \quad (9)$$

where V_{IN_CM} is the input common-mode voltage. The drain-source voltages V_{DS1} and V_{DS2} are similar, as they are clamped through the gain-boost circuit (as will be discussed later). And V_{DS1} and V_{DS2} are also insensitive to voltage variations at V_{OP} and V_{ON}, which are isolated by M3 and M4. As a result, equation (9) minus (8) leads to

$$\Delta I_{OUT} = I_{D2} - I_{D1} = \mu_n Cox \frac{W}{L} \cdot \Delta V_{IN} \cdot V_{DS1,2} = g_m \Delta V_{IN} \quad (10)$$

where g_m is the transconductance of input transistors operating in the linear region. According to equation (10), if $V_{DS1,2}$ is constant, then there will be a linear relationship between the input voltage and output current. To this end, a gain-boost circuit is used to make $V_{DS1,2}$ relatively constant (as will be discussed later), and a cascode structure (M3∼4) is used to make $V_{DS1,2}$ insensitive to output voltage variations.

Now let us calculate the gain. The current and voltage at the output have the following relationship

$$\Delta I_{OUT} \cdot t_{int} = (C_L + C_P) \cdot \Delta V_{OUT} \quad (11)$$

where C_L is the load capacitance, C_P is the parasitic capacitance at the output nodes, and t_{int} is the integration time. Substituting (10) into (11), the voltage gain G_{diff} can be calculated as

$$G_{diff} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{g_m t_{int}}{(C_L + C_P)} \quad (12)$$

As can be seen, the voltage gain is proportional to the integration time t_{int} and transconductance g_m of input transistors. The advantage of this work is that, because the P-end branch (M5∼6) is charging the output nodes V_{OP} and V_{ON}, the output nodes do not go to ground quickly. Thus, the integration time t_{int} can be larger than the prior work of FIGURE 1 (larger by 3.6 times in simulation). In prior work of FIGURE 1, V_{OP} and V_{ON} fall quickly and make input transistors go into linear region. By contrast, in our work, because the output common-mode voltage is fixed, M3 and M4 in FIGURE 2 will not go into the linear region quickly. This makes our t_{int} much longer. As a result, this work achieves 16 × gain at a 100 MHz clock frequency and 900 fF load capacitance (post-layout simulation). By contrast, the gain of prior works is usually no more than 5 (e.g., [11], [14], and [15]).

Besides, the proposed amplifier also has large input swing. This is because the g_m of input transistors is independent of input signals [see equation (10)]. This is not like the prior

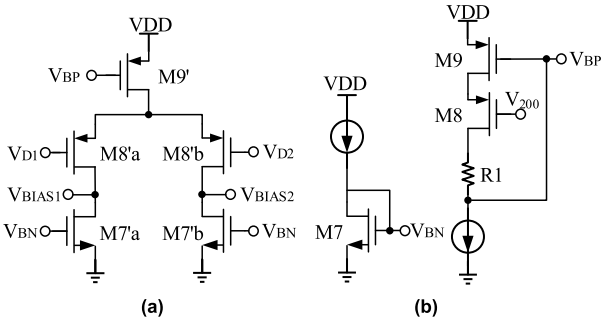

FIGURE 4. Gain-boost circuit: (a) amplifier, and (b) biasing circuit.

work of FIGURE 1, where the g_m of input transistors changes significantly with the input signal, as the input transistors are in saturation region. Post-layout simulation shows that our input swing is increased by 2 times than the prior work of FIGURE 1.

C. GAIN-BOOST CIRCUIT

Since the prior charge steering amplifier operates in the open-loop state, its voltage gain is sensitive to process, supply voltage, and temperature (PVT) variations. To solve this issue, we use an extra gain-boost circuit to reduce the gain variations in our amplifier. Its principle is explained below.

FIGURE 4(a) and (b) show the amplifier and biasing circuit of the proposed gain-boost circuit, respectively. Both M9 and M9' in FIGURE 4 are in the linear region. This gain-boost circuit works together with M3∼4 of FIGURE 2, in order to constitute a negative feedback loop. Because M9 (M8) in FIGURE 4 have the same size as M9' (M8'), V_{D1} and V_{D2} in FIGURE 4 (and in FIGURE 2 as well) are clamped to $V_{200} =$ 200 mV. This constant V_{D1} and V_{D2} lead to a relatively constant g_m of input transistors [see equation (10)] as well as a relatively constant voltage gain G_{diff} [see equation (12)], even under process variations.

D. COMMON-MODE FEEDBACK

FIGURE 5 shows the output common-mode feedback circuit. All transistors in the left part (M1'∼4' and M56') have the same sizes as the core amplifier (M1∼6 in FIGURE 2), and thus they also have the same operating point. The right part (M10∼13) of FIGURE 5 is used to clamp the node V_O to $V_{600} = 600$ mV. Because this V_O is equal to the output common-mode voltage of FIGURE 2, this output common-mode voltage is also clamped to 600 mV automatically.

IV. POST-LAYOUT SIMULATION RESULTS

The proposed amplifier has the advantages of high settling accuracy, high gain, and large input-output swing. However, there is a trade-off between high gain and high frequency, as high gain means longer amplification time and slower frequency. To be suitable for different applications, two versions of the proposed amplifier are designed in a

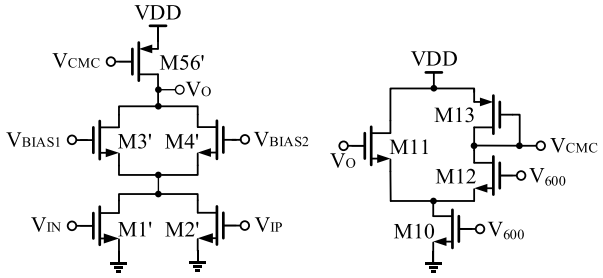

FIGURE 5. Common-mode feedback circuit.

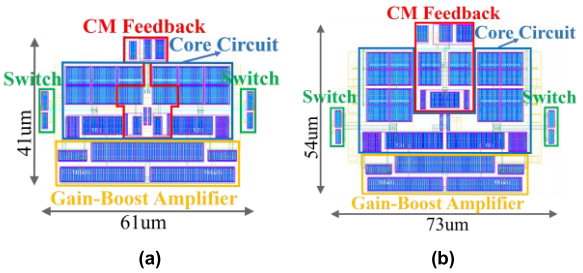

FIGURE 6. Layout of (a) the 100 MHz version and (b) the 500 MHz version.

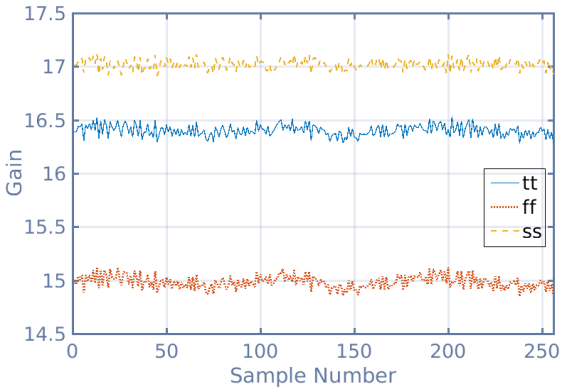

FIGURE 7. Gain at different corners.

40-nm CMOS process under a 1.1V supply voltage. Both versions guarantee high settling accuracy (ENOB≥7.5). But the clock frequencies are 100 MHz and 500 MHz, respectively. FIGURE 6 shows the layout of the 100 MHz version and 500 MHz version, respectively. The area is 0.0025 mm^2 and 0.0039 mm^2, respectively.

A. GAIN AND OUTPUT COMMON-MODE VOLTAGE

Gain and output common-mode (CM) voltage of 256 sampling points (at the Nyquist input frequency) are obtained. FIGURE 7 and FIGURE 8 show these gain values and output CM voltages of the 100 MHz version at different corners, respectively.

In FIGURE 7, the gain is between 15× to 17× (±6.6% variation) under process variations. By contrast, the gain of prior charge steering amplifier (FIGURE 1) is between 3.66 × to 5.14 × (±16.8% variation) under process

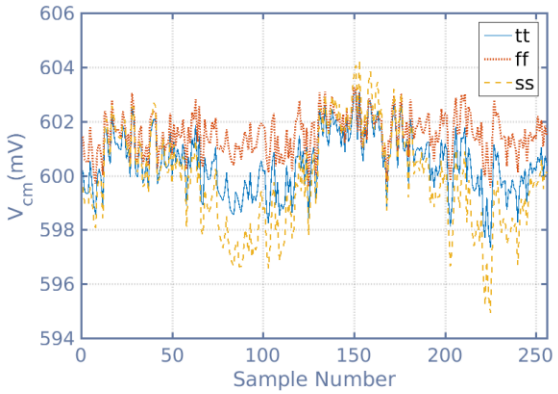

FIGURE 8. Output CM voltage at different corners.

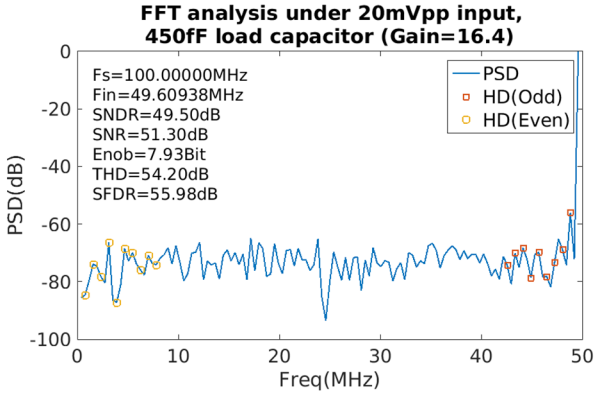

FIGURE 9. FFT spectrum of the 100 MHz version with transient noise.

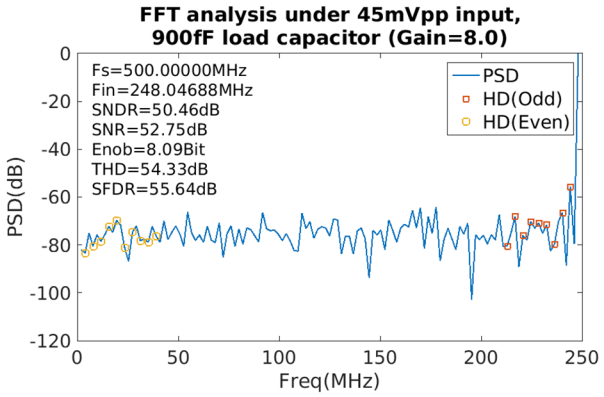

FIGURE 10. FFT spectrum of the 500 MHz version with transient noise.

TABLE 1. Gain and ENOB at different corners.

The 100M version at 20 mV_{pp} input and 900 fF load capacitor						
Corner	tt	ff	ss	fs	sf	range
Gain	16.4	15.0	17.0	16.7	15.8	15.0-17.0
ENOB	7.93	7.69	8.12	7.67	8.08	≥7.67

The 500M version at 45 mV_{pp} input and 450 fF load capacitor						
Corner	tt	ff	ss	fs	sf	range
Gain	8.04	7.85	7.87	8.04	7.85	7.85-8.04
ENOB	8.09	7.73	8.22	7.88	8.29	≥7.73

variations. These simulation results show that the proposed structure achieves a much larger gain and much smaller gain variation than the prior structure. This smaller gain variation comes from the input transistors in the linear region as well as the drain voltages clamped to 200 mV.

In FIGURE 8, the output CM voltages are between 595 mV and 605 mV. This means a ±5mV variation in CM voltage in the 100 MHz version. Meanwhile, in the 500 MHz version (not shown), the output CM voltage variation is also less than ±5 mV. This validates the effectiveness of the common-mode feedback circuit.

B. ENOB

To calculate the accuracy by FFT analysis, an ideal sample-and-hold circuit is applied in front of the charge steering amplifier.

FIGURE 9 and FIGURE 10 show the spectrum of the two versions with transient noise added and under tt corner. With Nyquist input signal, the 100MHz version achieves 16.4× gain and 7.9 bits ENOB at 20 mV_{pp} input signal, and the 500MHz version achieves 8.0× gain and 8.1 bits ENOB at 45 mV_{pp} input signal. Here, the input-output swing is still limited, because we must ensure that the amplifier output does not saturate under large gain.

TABLE 1 shows the gain and ENOB of the two versions at different corners. As can be seen, both two versions have more than 7.6 bits ENOB at each corner. And in the 500MHz version, the gain is very stable (between 7.85 × to 8.04 ×, ±1.2% variation in gain).

TABLE 2 summarizes the circuit performance and compares it with the state-of-the-art charge steering amplifiers in pipelined-SAR ADCs. For fair comparison, we re-designed the circuit of [11] and [15] using the same 40nm CMOS process, and provide their post-layout simulation results. Compared to [11], [14], and [15], this work not only significantly increases gain, but also increases the settling accuracy by 1.6 bits. Moreover, it allows large input and output swings without compromising accuracy, achieving up to 360 mV_{pp} output swing, which is at least 3.6 times larger. This large output swing helps improve the quantization resolution of the next stage SAR. These advantages mainly come from the cascode input transistors in linear region as well as the P-end branch for extending the integration time.

Although [10] has a 16× gain just like this work. It comes from a double integration technique to boost its gain of [10]. However, this means that the small input swing and deteriorated linearity issues of conventional charge steering amplifiers still exist in [10]. Besides, its gain linearity deteriorates, also because how much the

TABLE 2. Performance comparison.

	[10] JSSC 2014	[11]* *(FIGURE 1)*	[14] JSSC 2012	[15]* JSSC 2017	**This work**	
Technology (nm)	28	40	40	40	**40**	
Supply Voltage (V)	1.0	1.1	1.1	1.1	**1.1**	
Fs (MS/s)	80	1500	250	500	**100**	**500**
Load Capacitance (fF)	140	450	600	450	**900**	**450**
Input Signal (mV_{pp})	11	20	25	20	**20**	**45**
Output Signal (mV_{pp})	176	92	100	100	**320**	**360**
Voltage Gain	16	4.6	4	5	**16**	**8**
Settling Accuracy (bits)	-	6	6	6	**7.6**	**7.7**
Power Consumption (mW)	-	1.9	0.4	1.5	**2.1**	**3.3**

* *re-designed and post-layout simulated*

gain can be boosted depends on how much non-linearity is allowed [10]. The larger the gain is, the larger the non-linearity will be. By contrast, this work can achieve high gain and high linearity simultaneously. Additionally, the proposed amplifier achieves nearly equal gain at different corners.

V. CONCLUSION

This paper proposes a novel charge steering amplifier that achieves 16× gain, over 7.6 bits accuracy, and 3.6× larger output swing without compromising accuracy compared to prior charge steering amplifiers. Because high gain, high accuracy, and large input-output swing can be realized simultaneously, the proposed circuit is well suited for pipelined SAR ADCs. Finally, post-layout simulation results validate the proposed amplifier.

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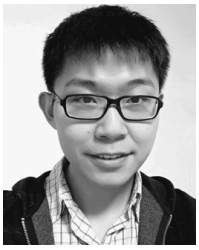

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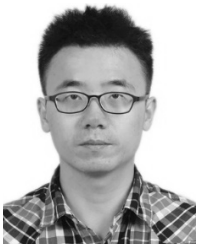

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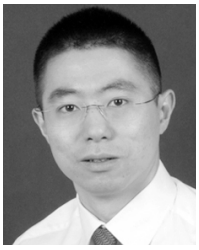

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