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A High-Efficiency Low-Power Rectifier for Wireless Power Transfer Systems of Deep Micro-Implants

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ABSTRACT In this article, the so-called bootstrapping rectifier (BSR) proposed by Hashemi *et al.* is re-analyzed, and a novel high-efficiency low-power rectifier called Opto-Coupled Dynamic Gate-Control (OCDGC) rectifier is presented based on the bootstrapping structure. Circuit analysis of BSR shows that the rectifier design has inherent problems that cause a high forward voltage drop and limit its power conversion efficiency (PCE). The BSR is simulated and fabricated in TSMC 0.18 μm process, and both simulation and experiment results prove the analysis. Inspired by the idea of bootstrapping structure, the presented OCDGC rectifier utilizes an opto-coupler to control the on-off switching of the active diode to maximize input power and prevent reverse leakage. A feedback loop is also introduced in the rectifier to limit the forward voltage drop. The proposed design is simulated in the TSMC 0.18 μm process. Simulation results show that, with a 3 MHz input, OCDGC rectifier is able to achieve more than 80% PCE at an input power down to 0.55 mW and achieve a forward voltage drop less than 0.1 V. More than 20% PCE improvement is achieved compared with the PCE of BSR.

INDEX TERMS Active diode, active rectifier, deep micro-implants, forward voltage drop, low power, opto-coupler, power conversion efficiency, rectifier, reverse current, wireless power transfer.

I. INTRODUCTION

Implanted electronic devices are increasingly being used in medical treatment and diagnostics. Wireless power transfer (WPT) is a desirable option for powering such devices as it removes the requirement for batteries or subcutaneous wiring, avoiding the risk of infection or chemical battery leakage. This has distinct advantages for the safety and convenience of patients, potentially extending the life of the implanted device and reducing the need for further surgical intervention. WPT also allows, in principle, larger numbers of sensors to be implanted, which is crucial to provide rich 3D information for the clinicians involved in therapy. Multiple sensors become very inconvenient (and generally impossible) with wiring.

In recent decades, WPT has been used in a wide range of implantable medical devices (IMDs), for cochlear [1]–[3], cardiac [4]–[7], retinal [8]–[10], spinal [11], [12], cortical [13]–[15], and peripheral implants [16]–[18]. Meanwhile, many wireless power capsule-dedicated implants have been developed for biopsy [19], [20], therapy [21], locomotion [22]–[25] and visual prostheses [26], [27] applications.

In a WPT system, the rectifier (or AC to DC converter) is a vital component. It converts AC power from the receiver coil (for the magnetic coupling resonance WPT) to DC power for the load. For wireless powered deep micro-implants, the power budget can vary from a few hundreds of microwatts to several milliwatts. This proposes a challenge to the design of rectifier because the operational power of the rectifier is restricted by the power budget of the receiver. Conventional rectifiers such as the junction-diode bridge rectifiers (shown in Fig 1) are not commonly used in a WPT system because of their high forward voltage drop (V_{FWD} = 0.7V) in rectification. Schottky diodes can be a replacement because of their lower V_{FWD}, but they will also experience heavy leakage and require special fabrication process that may increase chip cost [29]. To overcome the disadvantage of the junction-diodes, diode-connected Metal-Oxide-Semiconductor (MOS), as shown in Fig 2, has been used in the rectifiers of WPT systems [30], [31]. This MOS is

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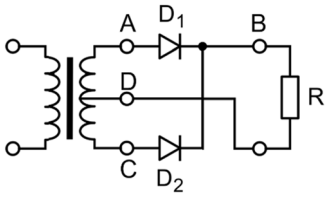

FIGURE 1. Conventional junction-diode rectifier [28].

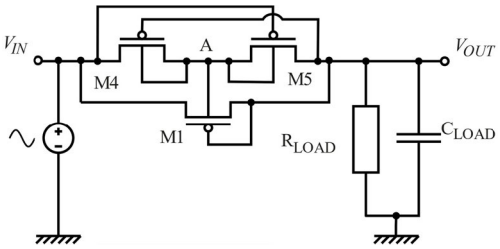

FIGURE 2. Diode-connected PMOS rectifier.

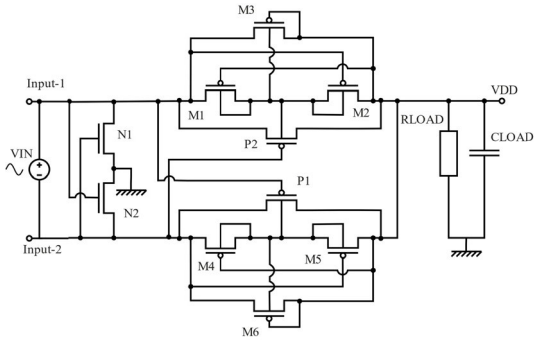

FIGURE 3. Self-synchronous rectifier.

fabricated using special processes and has zero threshold. However, they will experience large leakage currents when reverse biased. In other studies, active rectifiers have been proposed to avoid the problem of the threshold of MOS, in which the MOS gate is connected to an active node instead of the source of the MOS. The forward voltage drop V_{FWD} then becomes the voltage drop between the source and drain of the MOS instead of its threshold voltage. Unlike rectifiers operating in GHz frequencies, in which parasitic leakage is the main issue, and multiple stages are used to reduce leakage [32], the main issue of active rectifiers operating in a few MHz is the mismatching between the on-off time of active switch and the crossover time of input and output voltages, which leads to reverse leakage loss. Therefore, control circuits are designed to minimize the reverse leakage loss. One of the most basic active rectifiers is the self-synchronous rectifier [33], as shown in Fig 3, which utilizes a cross-gate structure to avoid latch-up problems. The problem of the synchronous circuit is that the on-off time of the switches is controlled by the input voltage and will not always be at the time when V_{IN} and V_{OUT} cross each other. Therefore, the reverse current will be high and reduce power conversion efficiency (PCE) [34]. To solve the problem, comparator-based active rectifiers have been proposed [35]–[39], as shown in Fig 4. The comparators

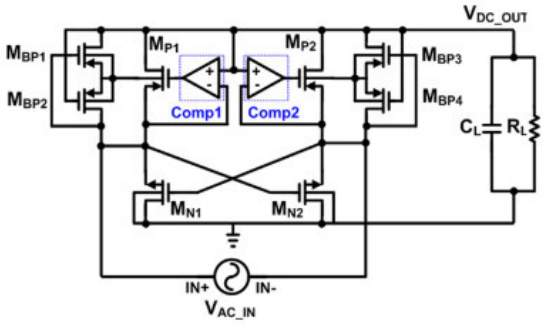

FIGURE 4. Comparator-based active rectifier [38].

compare the VAC and VDC of the rectifier and control the on-off of the MOS so that the MOS can be forced to turn on and turn off when V_{IN} and V_{OUT} cross each other. However, the comparators will experience delays at a high operational frequency due to parasitic resistance, parasitic capacitance, system offsets and mismatches [40]. Therefore, the rectifiers should be compensated with extra control schemes, which will increase the circuit complexity and power consumption [41], [42]. These rectifiers are more suitable for WPT systems with a power budget more than 40 mW at the receiver circuit and can experience start-up problem or low PCE at deeply-implanted micro-receivers [43].

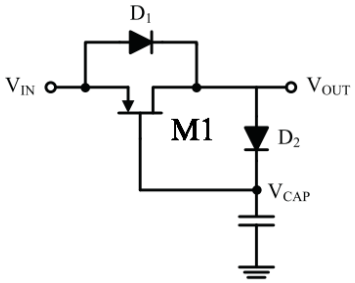

FIGURE 5. Bootstrapping rectifier basic structure [44].

Another solution to reverse current leakage is using a so-called bootstrapping structure [44], as shown in Fig 5. This circuit structure does not require comparators and, thus, is more suitable for deep micro-implants with small power budgets and do not have to face problems, such as start-up and delays. However, unlike described in [44] and [45], the bootstrapping structure has inherent problems that cause the measured PCE much lower than the simulated results, which are neither mentioned nor analyzed in either of the papers.

II. OPERATION AND PROBLEMS OF BOOTSTRAPPING STRUCTURE

A. ANALYSIS OF BASIC BOOTSTRAPPING RECTIFIER (BSR)

As shown in Fig 5, the MOS gate is controlled by the voltage at the bootstrapping capacitor V_{CAP}. When $V_{IN} > V_{CAP} + |V_{thM1}|$, the PMOS will turn on; when $V_{IN} < V_{CAP} + |V_{thM1}|$, PMOS M1 will turn off. The symbols are defined in Table 1.

TABLE 1. Definition of Symbols.

Symbol	Definition	Symbol	Definition
V_{IN}	Rectifier input voltage	V_{OUT}	Rectifier output voltage
V_{CAP}	Bootstrapping capacitor voltage	V_{thM1}	M1 threshold voltage
V_{thD2}	D2 threshold voltage	V_{sdM1}	M1 source to drain voltage
I_{sdM1}	M1 source to drain current	V_{sgM1}	M1 source to gate voltage
V_{CAP}	Rectifier forward drop voltage	R_{Load}	Rectifier load resistance

Because

$$V_{CAP} = V_{OUT} - V_{thD2}, \tag{1}$$

the turn-off condition of M1 becomes

$$V_{IN} < V_{OUT} + (|V_{thM1}| - V_{thD2}). \tag{2}$$

When $|V_{thM1}| \geq V_{thD2}$, PMOS M1 will turn off as soon as V_{IN} drops below V_{OUT}. In this way, no reverse current will flow when $V_{IN} < V_{OUT}$, and there will be no reverse leakage loss.

However, due to the bootstrapping structure, PMOS M1 is unable to operate efficiently when $V_{IN} > V_{OUT}$, and the value of V_{OUT} is dependent on the load.

Normally, the value of the bootstrapping capacitor is much less than the output capacitance of the rectifier, so the rise of V_{CAP} can be assumed to be faster than the rise of V_{OUT}. Therefore, when $V_{IN} > V_{OUT}$ and V_{IN} is increasing, the voltage V_{CAP} will become

$$V_{CAP} = V_{IN} - (V_{sdM1} + V_{thD2}). \tag{3}$$

The circuit has the following feedback loop:

$$I_{sdM1} \uparrow \rightarrow V_{OUT} \uparrow \rightarrow V_{sdM1} \downarrow \rightarrow V_{CAP} \uparrow \rightarrow V_{sgM1} \downarrow \rightarrow I_{sdM1} \downarrow$$

In the circuit, because $V_{OUT} - V_{CAP} = V_{thD2} \leq |V_{thM1}|$, PMOS M1 is in saturation region.

$$I_{sdM1} = \frac{\beta}{2} \times \left(V_{sgM1} - |V_{thM1}|\right)^2 \tag{4}$$

$$V_{sdM1} = V_{IN} - V_{OUT} \tag{5}$$

$$V_{sgM1} = V_{IN} - V_{CAP} \tag{6}$$

where $\beta = k'_p \frac{W}{L}$. k'_p is a process parameter, W and L are the effective width and length of a PMOS.

By combining (3) (4) (5) (6), the current through PMOS M1 has the following equation,

$$I_{sdM1} = \frac{\beta}{2} \times (V_{IN} - V_{OUT} + V_{thD2} - |V_{thM1}|)^2. \tag{7}$$

Because the value of V_{thD2} is approximately equal to the value of $|V_{thM1}|$, (7) can also be written as

$$I_{sdM1} \approx \frac{\beta}{2} \times (V_{IN} - V_{OUT})^2. \tag{8}$$

From (8), when the difference between V_{IN} and V_{OUT} becomes smaller, current I_{sdM1} will decrease. Therefore, the output voltage and the output current of the rectifier are inherently dependent on the load. For a rectifier load, which is equivalent to a capacitor and a resistor in parallel, because of the feedback loop, the value of V_{OUT} will be such that the resulting load resistor current

$$I_{Load-R} \approx I_{sdM1}, \tag{9}$$

assuming that the current through diode D2 is negligible.

Because

$$I_{Load-R} = \frac{V_{OUT}}{R_{Load}}, \tag{10}$$

by combining (8)(9)(10), the value of I_{sdM1} can be calculated.

$$I_{sdM1} = \frac{\beta V_{IN} R_{Load} + 1 - \sqrt{2\beta V_{IN} R_{Load} + 1}}{\beta R_{Load}^2} \tag{11}$$

From (9)(10)(11), the output voltage of the rectifier thus equals to

$$V_{OUT} = V_{IN} - \left(\frac{\sqrt{2V_{IN}\beta R_{Load} + 1} - 1}{\beta R_{Load}}\right). \tag{12}$$

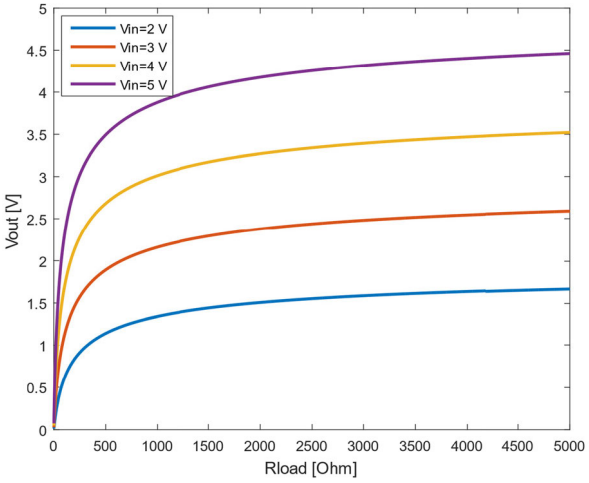

FIGURE 6. Calculated V_{OUT} of bootstrapping rectifier versus load resistance. $\beta = 400 \times 15.4\mu A/V^2$.

From (12), it can be seen that the forward voltage drop V_{FWD} of the bootstrapping rectifier is dependent on the input voltage and the load resistance. The calculated V_{OUT} versus the load resistance in different input voltage is shown in Fig 6. For the same input voltage, as the load resistance decreases, V_{FWD} increases. V_{FWD} also increases with the increase of V_{IN}. At $R_{Load} = 5k\Omega$, V_{FWD} increases from 0.33V for $V_{IN} = 2V$ to 0.53V when $V_{IN} = 5V$. The only way to reduce V_{FWD} without changing the load or input voltage is by increasing β. However, the saturation effect of V_{OUT} at a high R_{Load} shows that the increase of β will also have a similar effect.

In [44]–[46], the authors confused the turn-off condition, as shown in formula (2), of the bootstrapping rectifier with the steady-state value of V_{OUT}, ignoring the fact that the PMOS

M1 is unable to operate efficiently due to formula (3), and the output voltage is dependent on the load resistance due to formula (12), which result in a high V_{FWD} and a low PCE, as shown in Fig 6.

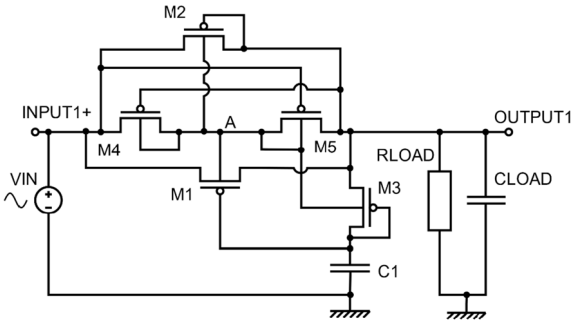

FIGURE 7. Practical Half-Wave bootstrapping rectifier.

B. SIMULATION AND MEASUREMENT RESULTS

A full-wave practical basic BSR, with its half-wave structure shown in Fig 7 was simulated and fabricated. In the circuit, C1 is the bootstrapping capacitor, and M1 is the active diode for rectification. M2 is a diode-connected PMOS to avoid latch-up. M3 is a diode-connected PMOS to charge C1. The substrate of M3 is connected to point A. The PMOSs M4 and M5 make a Dynamic Bulk Switching (DBS) circuit to define the substrate voltage of the PMOS M1. The gate of M5 is connected to the input, and the gate of M4 is connected to the output. The source of M4 is connected to the input, and the source of M5 is connected to the output. The drains of M4 and M5 are connected to each other.

During operation, the voltage at point A will be approximately equal to the higher voltage of either the input or the output. When V_{IN} is more than V_{OUT}, M4 will turn on, and M5 will turn off. The voltage V_A at point A will then be equal to V_{IN}. Because M5 is turned off, almost no current will flow through M4. V_{ds} of M4 can then be neglected. When V_{OUT} is higher than V_{IN}, M5 will turn on, and M4 will turn off. V_A will be equal to V_{OUT}. Therefore, the voltage V_A at point A will be equal to the higher voltage of input and output.

The full-wave basic BSR was simulated in Cadence SpectreD simulator and fabricated using a TSMC 0.18μm CMOS 6-Metal/2-Poly high voltage mixed-signal based 2nd generation BCD process. M1 and M3 are enhancement-mode PMOSs with W/L = 10μm/400nm, 8 fingers and 8 multipliers. M4, M5 and M2 are enhancement-mode PMOSs with W/L = 10μm/400nm, 2 fingers and 1 multiplier. The value of C1 is 10pF. This chip is mounted in a PLCC 84 package. The PMOSs used are the same type, which is a high voltage PMOS with a maximum allowed V_{ds} = 12 V, which is sufficient for the wireless power implants. The maximum allowed V_{gs} is 5V. It is a multi-finger PMOS with a minimum finger of two. The substrate connection of this PMOS is floating and thus can satisfy the requirement of the circuit for substrate voltage definition.

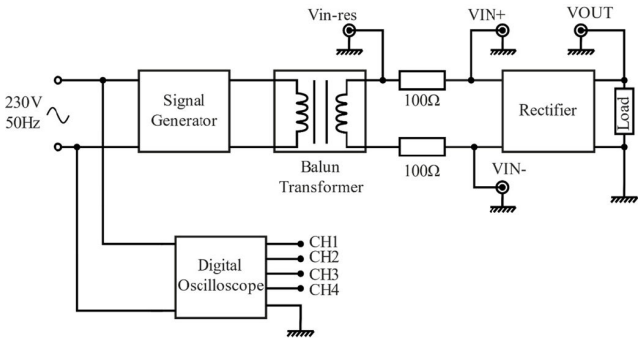

FIGURE 8. Measurement setup of bootstrapping rectifier.

The measurement setup is as shown in Fig 8. In the measurement setup, a wideband balun transformer is connected at the output of the signal generator to provide a floating input for the full-wave rectifier. Two 100Ω resistors are connected between the two output ports of the transformer and the two input ports of the rectifier, respectively, for input current measurement. The probes to measure V_{IN-res} and VIN + are set to the differential mode for balanced measurement. The input current is thus calculated as $I_{IN} = \frac{V_{IN-res} - V_{IN+}}{100\Omega}$ (A).

The input power to the rectifier is $\int_0^T v_{in}(t)\, i_{in}(t)\, dt$ at the steady working state. The output power was calculated as the integral of the squared measured output voltage divided by the load resistance over the same period as the input measurement. The voltage conversion ratio (VCR) was calculated as the ratio of the RMS output voltage to the peak amplitude of the input voltage. The amplitude of input voltage at the rectifier ranges from 1.5V to 5V. The input frequency is 8MHz. The load of the rectifier is a 5kΩ resistor and a 34pF load capacitor with the output pad parasitic capacitance, package and PCB parasitic capacitance and test probe capacitance in addition. The load capacitor is a smoothing capacitor which can store excess energy from the rectifier and reduce the ripples of output voltage.

The measured PCE and the measured VCR of the full-wave basic bootstrapping rectifier (basic BSR) are shown in Fig 9, together with the simulated PCE and simulated VCR. The higher VCR at higher V_{IN} seems to conflict with the higher V_{FWD} at higher V_{IN}, but it is untrue because the VCR is a measurement of RMS V_{OUT} in a full cycle, but the V_{FWD} is only related to the instantaneous V_{OUT} when $V_{IN} > V_{OUT}$.

As shown, the PCE of the measurement result is similar, but not identical, to the simulated output efficiency. The measured PCE and VCR are lower than the simulation results. The reason is that the bootstrapping capacitor becomes overcharged for low input voltages. Because there is no discharging path for the bootstrapping capacitor, the voltage at the bootstrapping capacitor has no way to decrease except for parasitic leakage. Once the capacitor has a high voltage, it will keep the voltage for a certain period before the parasitic leakage of the capacitor drains it out. During the period, whose length depends on the quality of the capacitor, the gate voltage of the PMOS M1 remains at a high voltage level even if a low voltage is input into the circuit. Therefore, the PMOS

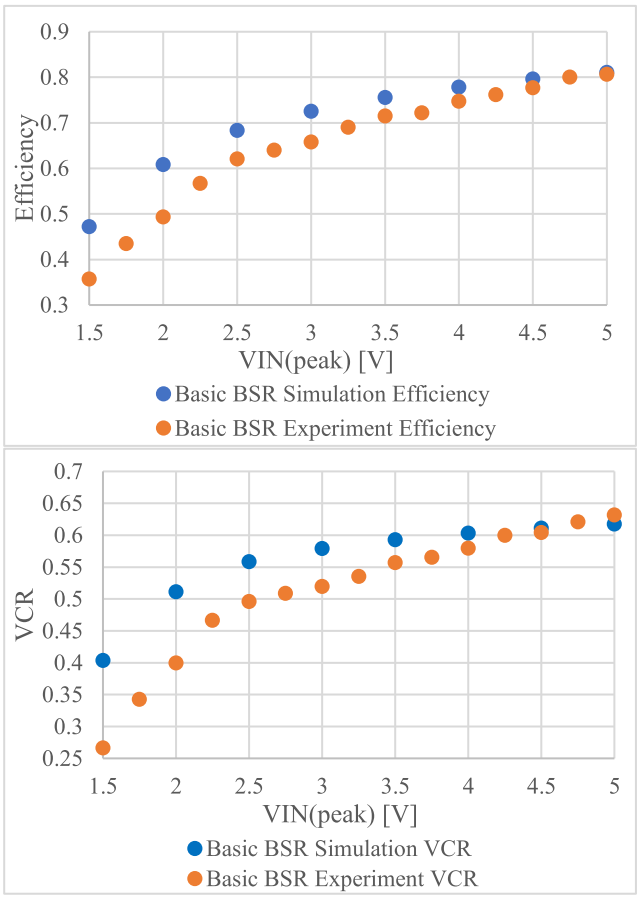

FIGURE 9. Simulated and experiment PCE and VCR with no pre-set voltage.

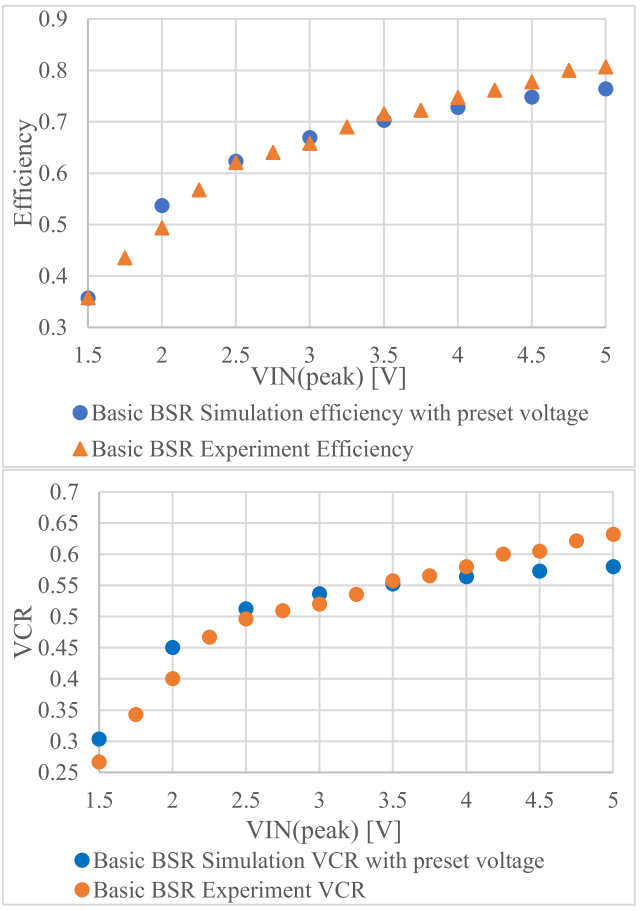

FIGURE 10. Simulated and experiment PCE and VCR. Simulation result with 2V pre-set voltage.

M1 will not be able to fully turn on at low input voltages, causing a lower measured PCE.

In Fig 9, the voltage at the bootstrapping capacitor resets to 0V for each measurement, so this problem will not occur. Further simulations showed that, if an initial voltage of more than 2V is pre-set at the bootstrapping capacitor or the output capacitor, the RMS output voltage will decrease by 0.1V to 0.2V depending on the value of input voltage. The simulated PCE and VCR of the BSR with a pre-set bootstrapping capacitor voltage are shown in Fig 10 and compared with the experiment results.

With the pre-set capacitor voltage, both the simulated PCE and the simulated VCR have closer results to the measured ones. The maximum difference of the PCE is less than 5% between simulation and measurement results. The most outstanding differences are when $V_{IN} = 2V_{peak}$ and $5V_{peak}$, which have both 4.3% difference of efficiency. The simulated RMS output voltages with a pre-set voltage agree to the measurement results with less than 5% of VCR difference. The VCR simulation results are closer to the experiment results when V_{IN} is between $2.5V_{peak}$ and $4V_{peak}$, with an average difference of 1.3%.

As a summary, the bootstrapping rectifier is a simple solution to reverse leakage problem of active rectifiers. However, it inherently suffers from a few problems such as high V_{FWD}, load-dependent V_{OUT}, and low PCE and VCR at low V_{IN}. To solve these problems, a novel rectifier is proposed based on the bootstrapping structure with the use of opto-coupler in the control circuit.

III. OPTO-COUPLED DYNAMIC GATE-CONTROL RECTIFIER

A. CIRCUIT ANALYSIS

The circuit diagram of Opto-Coupled Dynamic Gate-Control (OCDGC) Rectifier is shown in Fig 11. In the circuit, D1, M2 and D2 are the opto-coupler, where D1 and D2 are light-emitting diodes (LED), and M2 is an opto-transistor. The current gain of the opto-coupler is set to 1. C1 and C2 are the bootstrapping capacitors, which are charged with the current from D1 and D2, respectively. PMOS M31 and M32 are connected in parallel with C1 and C2, respectively, to provide a discharging path. The gate of M31 and M32 is connected to Point B, which is derived from the bottom right circuit (the Point B circuit) in Fig 11. The bulk of M31 is connected to Point A because its threshold voltage is intended to be higher, whereas the bulk of M32 is connected to its source. The resistor in the Point B circuit is chosen to minimize the current in the branch and to make sure the voltage at

point B is

$$V_B = V_{OUT} - 2V_{thD}. \tag{13}$$

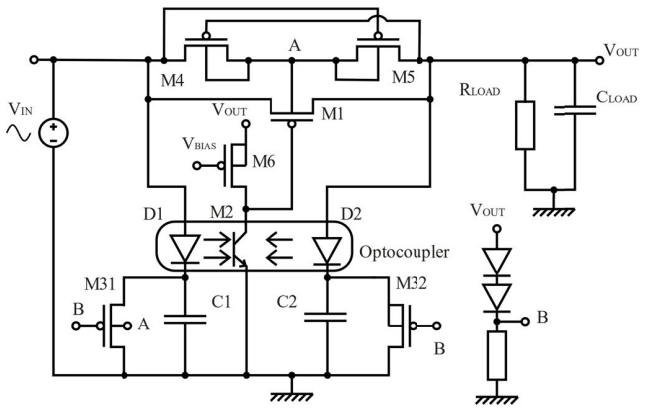

FIGURE 11. Half-wave OCDGC rectifier.

PMOS M6 and opto-transistor M2 form an amplifier circuit with VDD being the rectifier V_{OUT}. The output of the amplifier is connected to the gate of PMOS M1 for on-off switching. The gate voltage of M6 is the bias voltage of the amplifier and is set to match the current from M2. PMOS M1, M4 and M5 are the same as the ones in Fig 7, in which M4 and M5 are the DBS circuit, and M1 is the active diode for rectification.

In the circuit, D1, C1, M31, M2, M6 make a control circuit (CTL1), and D2, C2, M32, C2 and M6 make a second control circuit (CTL2).

The threshold voltages of the MOSs and diodes should meet the following conditions:

$$|V_{thM31}| + V_{thD1} = 2V_{thD} + V_{sdM1-set} \tag{14}$$

$$|V_{thM32}| + V_{thD2} = 2V_{thD} + V_{set} \tag{15}$$

where V_{thM31} and V_{thM32} are the threshold voltages of PMOS M31 and M32. V_{thD1} and V_{thD2} are the threshold voltages of LED D1 and D2. V_{thD} is the threshold voltage of the diodes in the Point B circuit. $V_{sdM1-set}$ is the target maximum value of V_{sdM1}(i.e. V_{FWD}, the rectifier forward voltage drop) that is decided by the circuit designer.

It should be noted that the non-linear characteristic of diode D1 and D2 is the key in the operation of OCDGC rectifier because this make sure that the values of $V_{sdM1-set}$ and V_{set} can remain constant during operation to keep the forward voltage drop within the desired range.

The waveforms of V_{OUT}, V_{IN} are shown in Fig 12, in which V_{IN} is $4V_{\text{peak}}$ $R_{Load} = 5\text{k}\Omega$, and $C_{Load} = 100\text{pF}$.

B. OPERATION OF CTL1

1) FROM T1 TO T2

V_{IN} increases and charge C1 through D1. LED D1 emits light, which causes M2 to turn on. M6 and M2 make an inverting amplifier, and the value of M1 gate voltage V_{gM1} thus drops from V_{OUT} to near ground voltage, which turns on M1 and let current flow from rectifier V_{IN} to V_{OUT}.

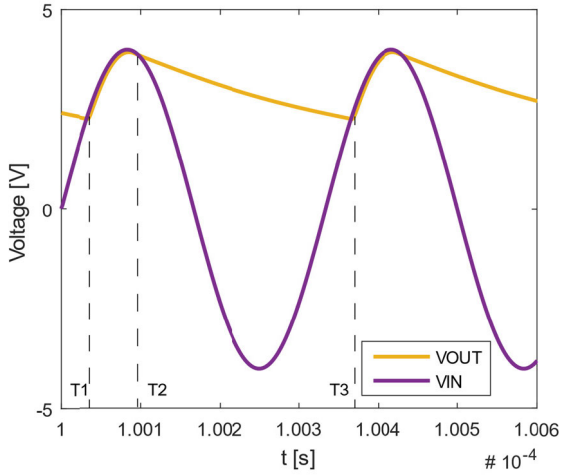

FIGURE 12. Simulated waveforms of V_{OUT}, V_{IN} of OCDGC rectifier. T1, T2, T3 are the turn-on, turn-off time of active diode M1. V_{IN} is 4 V_{peak}.

The voltage at C1 V_{C1} is

$$V_{C1} = V_{IN} - V_{thD1}. \tag{16}$$

The voltage at V_{OUT} is

$$V_{OUT} = V_{IN} - V_{sdM1}. \tag{17}$$

At PMOS M31,

$$V_{sgM31} = V_{C1} - V_B. \tag{18}$$

From (13) (16) (17) III-B2,

$$V_{sgM31} = 2V_{thD} - V_{thD1} + V_{sdM1}. \tag{19}$$

From (14), if the load resistance decreases, causing V_{OUT} to decrease, there forms a feedback loop.

$$\begin{aligned} V_{OUT} \downarrow \rightarrow V_{sdM1} \uparrow \rightarrow V_{sdM1} > V_{sdM1-set} \rightarrow V_{sgM31} \\ > |V_{thM31}| \rightarrow I_{M31} \uparrow \rightarrow I_{D1} \uparrow \rightarrow I_{M2} \uparrow \rightarrow V_{sgM1} \\ \downarrow \rightarrow I_{sdM1} \uparrow \rightarrow V_{OUT} \uparrow \end{aligned}$$

If V_{OUT} decreases and causes $V_{sdM1} > V_{sdM1-set}$, PMOS M31 will on, letting more current flow through LED D1, which will result in a lower V_{sgM1} and a higher I_{sdM1}, causing V_{OUT} to increase.

If $V_{sdM1} < V_{sdM1-set}$, due to formula (14), $V_{sgM31} < |V_{thM31}|$, PMOS M31 will be kept close, no current will flow through M31.

In this way, V_{FWD} of the rectifier can be maintained within the target range $V_{sdM1-set}$ when the load resistance is changed. The range of change of load resistance is dependent on the value of $V_{sdM1-set}$, the voltage at the gate of M1, the current through D1 and M2, and the $V_{sg} - I_{sd}$ response of M31.

2) AT T2

V_{IN} begins to drop but is still higher than V_{OUT}.

If $V_{sdM1} < V_{sdM1-set}$, M3 remains off, and there is no discharging path for C1. The voltage at C1 remains at

$$V_{C1} = V_{IN}\,(max) - V_{thD1}. \tag{20}$$

Therefore, $V_{IN} - V_{C1} < V_{thD1}$, D1 turns off, and no light will emit. If D2 also works properly and turns off, no current will flow through M2, and the voltage at gate of M1 V_{gM1} will be equal to V_{OUT}. V_{sgM1} will be less than $|V_{thM1}|$, M1 will turn off.

If $V_{sdM1} > V_{sdM1-set}$, M3 is turned on. However, because V_{IN} drops faster than V_{OUT} at the falling edge, $V_{sdM1} < V_{sdM1-set}$ will eventually happen, and M1 will turn off as well.

Therefore, at T2, M1 will turn off before V_{IN} drops below V_{OUT}, preventing any reverse current from flowing. However, it should be noted that, because the time gap between T2 and the $V_{IN} - V_{OUT}$ crossover point is very small, and the time for V_{gM1} to rise from near ground voltage to V_{OUT} is dependent on the slew rate of the amplifier M6-M2, the value of $V_{sdM1-set}$ should be properly chosen to make sure PMOS M1 is turned off before the $V_{IN} - V_{OUT}$ crossover point.

3) AFTER $V_{IN} - V_{OUT}$ CROSSOVER POINT AND BEFORE T3

V_{OUT} drops due to the discharging of load capacitance, but V_{C1} still equals to its value at T2 $V_{C1}(T2)$ because of no discharging path.

At PMOS M31, due to (13) III-B2,

$$V_{sgM31} = V_{C1}(T2) - (V_{OUT} - 2V_{thD}). \tag{21}$$

When $V_{sdM1} < V_{sdM1-set}$ at T2, $V_{C1}(T2)$ equals to III-B3,

$$V_{sgM31} = 2V_{thD} - V_{thD1} + V_{IN}\,(max) - V_{OUT}. \tag{22}$$

After $V_{IN} - V_{OUT}$ crossover point, when V_{OUT} decreases, and meets the condition that

$$V_{IN}\,(max) - V_{OUT} > V_{sdM1-set}, \tag{23}$$

M31 will turn on due to (14) (22), and C1 will discharge.

When $V_{sdM1} > V_{sdM1-set}$ at T2, $V_{C1}(T2)$ will be less than the value at III-B3, and condition (23) becomes

$$V_{IN}\,(T2) - V_{OUT} > V_{sdM1-set}. \tag{24}$$

M31 will turn on again, and C1 will discharge.

At this moment, because $V_{IN} < V_{OUT}$, $V_{sgM31} > |V_{thM31}|$ and (14), $(V_{IN} - V_{CAP})$ will be less than V_{thD1}. D1 will not conduct, and M1 will not turn on.

Because the C1 discharging rate is faster than the discharging rate of load capacitance, and M31 will turn off when $V_{sgM31} < |V_{thM31}|$, the value of V_{C1} between the $V_{IN} - V_{OUT}$ crossover point and T3 will follow V_{OUT} to drop, and thus equals to

$$V_{C1} = V_{OUT} - V_{thD1} + V_{sdM1-set} \tag{25}$$

4) AT T3

V_{IN} increases and crossovers V_{OUT} again. This is the optimum moment for M1 to turn on. If M1 turns on before T3, because $V_{IN} < V_{OUT}$, reverse current will flow, reducing PCE. If M1 turns on much later than T3, the operation time of the rectifier will be so short that the load may not be able to receive enough power.

For M1 to turn on, D1 needs to conduct, and V_{IN} needs to meet the condition that

$$V_{IN} - V_{C1} \geq V_{thD1} \tag{26}$$

Because of III-B4,

$$V_{IN} - V_{C1} = V_{thD1} + V_{IN} - V_{OUT} - V_{sdM1-set}. \tag{27}$$

Therefore, when $V_{IN} - V_{OUT} \geq V_{sdM1-set}$, condition III-B5 will be met, D1 will conduct, and M1 will turn on. Because $V_{sdM1-set}$ is a small value, the delay of M1 turn-on time from T3 will be short.

5) SUMMARY OF CTL1

As a summary, circuit CTL1 in OCDGC rectifier can achieve the following functions:

(1) Turn on active diode M1 at V_{IN} rising edge when V_{IN} crossovers V_{OUT}, avoiding reverse leakage.
(2) Maintain rectifier forward voltage drop within the target range when M1 is on.
(3) Turn off M1 near the $V_{IN} - V_{OUT}$ crossover point at the falling edge of V_{IN}, avoiding reverse leakage.

C. OPERATION OF CTL2

The operation of CTL2 is similar to CTL1, but its operation is dependent on CTL1.

1) FROM T1 TO T2

When V_{OUT} increases, D2 conducts and C2 is charged. D2 will emit light, more current will flow in M2, and M1 will turn on more.

At the moment,

$$V_{C2} = V_{OUT} - V_{thD2} \tag{28}$$

Because of equations (13) (15) and III-C2,

$$V_{sgM32} = 2V_{thD} - V_{thD2} < |V_{thM32}|, \tag{29}$$

PMOS M32 will turn off.

2) FROM T2 TO T3

V_{OUT} decreases, and because M32 is off from T1 to T2, the voltage at C2 is

$$V_{C2}\,(T2) = V_{OUT}\,(max) - V_{thD2}. \tag{30}$$

Therefore,

$$V_{OUT} - V_{C2}\,(T2) < V_{thD2}. \tag{31}$$

D2 stops conducting.

At PMOS M32,

$$V_{sgM32} = V_{C2} - V_B = V_{C2} - (V_{OUT} - 2V_{thD}) \quad (32)$$

Because of equations (15) (31) (33),

$$V_{sgM32} > 2V_{thD} - V_{thD2} > |V_{thM32}| \quad (33)$$

PMOS M32 will turn on and discharges C2.

Like the value of V_{C1} at this period, V_{C2} will also follow V_{OUT} to drop.

$$V_{C2} = V_{OUT} - V_{thD2} + V_{set} \quad (34)$$

From (34), because $V_{OUT} - V_{C2} < V_{thD2}$, D2 will not conduct even though C2 discharges through PMOS M32.

D. SUMMARY OF OPERATION OF OCDGC RECTIFIER

As a summary, when the conditions (14) (15) are met, the proposed rectifier is expected to operate with low V_{FWD} and load-independent V_{OUT}. Because of the amplifier M6-M2, the gate voltage of M1 is switched between V_{OUT} and near ground voltage, maximizing the forward current and blocking any reverse current. The major design concern is the selection of $V_{sdM1-set}$, which is related to the turn-on and turn-off time of active diode M1 and the range of forward voltage drop. Another design concern is the inverting amplifier M6-M2. The bias voltage of M6 should match the current through M2. The slew rate of the amplifier should be large enough to make sure the active diode can turn off before $V_{IN} - V_{OUT}$ crossover point. Because the current through M2 is related to the currents charging C1 and C2, the size of C1 and C2 should also be chosen with care.

IV. SIMULATION RESULTS OF OCDGC RECTIFIER

The proposed rectifier is simulated with TSMC 0.18μm CMOS 6-Metal/2-Poly high voltage mixed-signal based BCD process in Cadence SpectreD simulator. The same type of PMOS is used as the ones used in the simulation and fabrication of basic bootstrapping rectifier in II. The W/L size of active diode M1 is 10μm/400 nm, with 8 fingers and 8 multipliers. The size and multipliers of M1 are sufficiently large to reduce the conduction heat loss during operation. PMOS M6 is also 10 μm/400nm with 2 fingers and 2 multipliers. PMOS M4, M5, M31, M32 are of the same size, with 1 finger and 1 multiplier. The optocoupler formed by D1, D2 and M2 has a current gain of 1 and a bandwidth of 10MHz. Both C1 and C2 are integrated Metal to Metal capacitors and are set to 10pF. The diodes in the Point B circuit are diode-connected PMOSs of the same type to M1. The resistors in the Point B circuit is 1MΩ. The load resistance is 5kΩ, and the load capacitance is 100pF. The operational frequency is 3MHz. The value of $V_{sdM1-set}$ is 0.1V and V_{set} is also 0.1V. The input voltage varies from 1V to 5V, which corresponds to the likely output voltage range of receiver coil of WPT systems for deep micro-implants.

The simulated waveforms of V_{OUT}, V_{IN} is shown in Fig 12 and the simulated waveforms of current through active diode

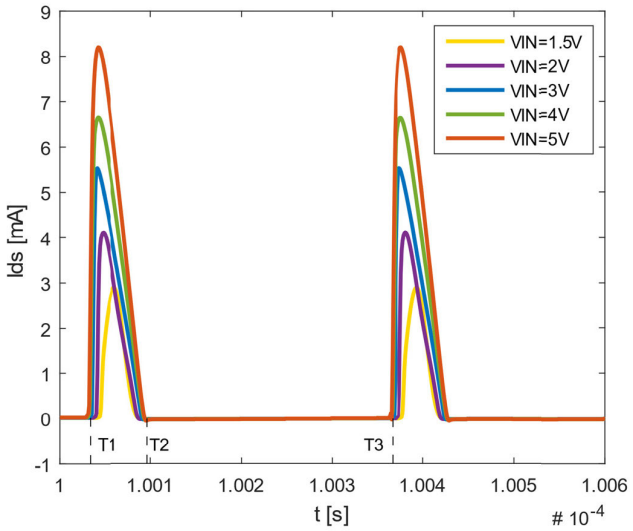

FIGURE 13. Waveforms of current through active diode M1. T1, T2, T3 are the turn-on, turn-off time of active diode M1.

M1 is shown in Fig 13. As shown, M1 begins to conduct at T1 when V_{OUT} and V_{IN} crossover and stops conducting at T2.

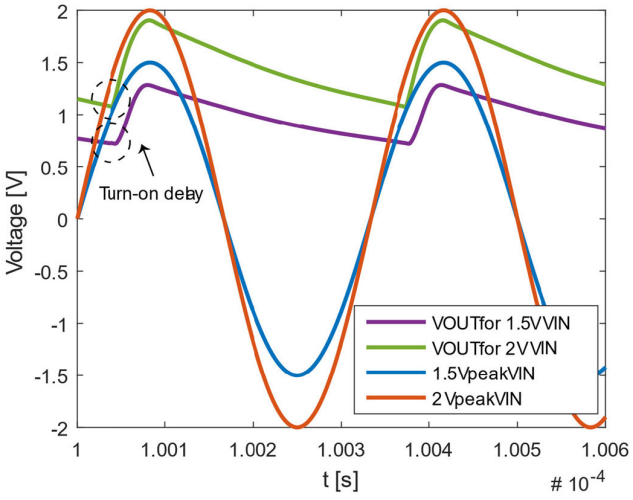

FIGURE 14. Simulated waveforms of V_{OUT}, V_{IN} for $2V_{peak}$ and $1.5V_{peak}$ input. The output voltage rise is after the $V_{IN} - V_{OUT}$ crossover point, which is due to the turn-on delay of M1.

The M1 turn-on time for $V_{IN} = 1.5\ V_{peak}$ and $2V_{peak}$ is delayed, which results in lower values of V_{OUT}, as shown in Fig 14. This is because the voltage at the gate of M31 is V_B, which is obtained from formula (13). Because the threshold voltage of the diode-connected PMOS V_{thD} is about 0.55V, the value of V_{OUT} will have to be more than 1.1V to control M31, otherwise M31 will remain off, and C1 will be unable to discharge between T2 and T3. Thus, V_{C1} will be higher than the value obtained in formula III-B4, and the value of V_{IN} to make D1 conduct will need to be higher, which results in a delay in the turn-on time of active diode M1. For $V_{IN} = 1.5V_{peak}$, because of the lower V_{IN} and higher V_{C1}, the current through D2 is unable to match the current through M6, which results in a higher M1 gate voltage V_{gM1}. Moreover,

because V_{OUT} is lower than 1.1V for most of the conduction time, PMOS M31 is unable to turn on to increase the current through D2. These two reasons cause M1 to turn on less and results in a higher forward voltage drop V_{FWD}. This is much improved for $V_{IN} = 2\text{V}_{\text{peak}}$, where V_{OUT} catches up with V_{IN} quickly after the turn-on delay, and V_{FWD} remains within the value of $V_{sdM1-set}$.

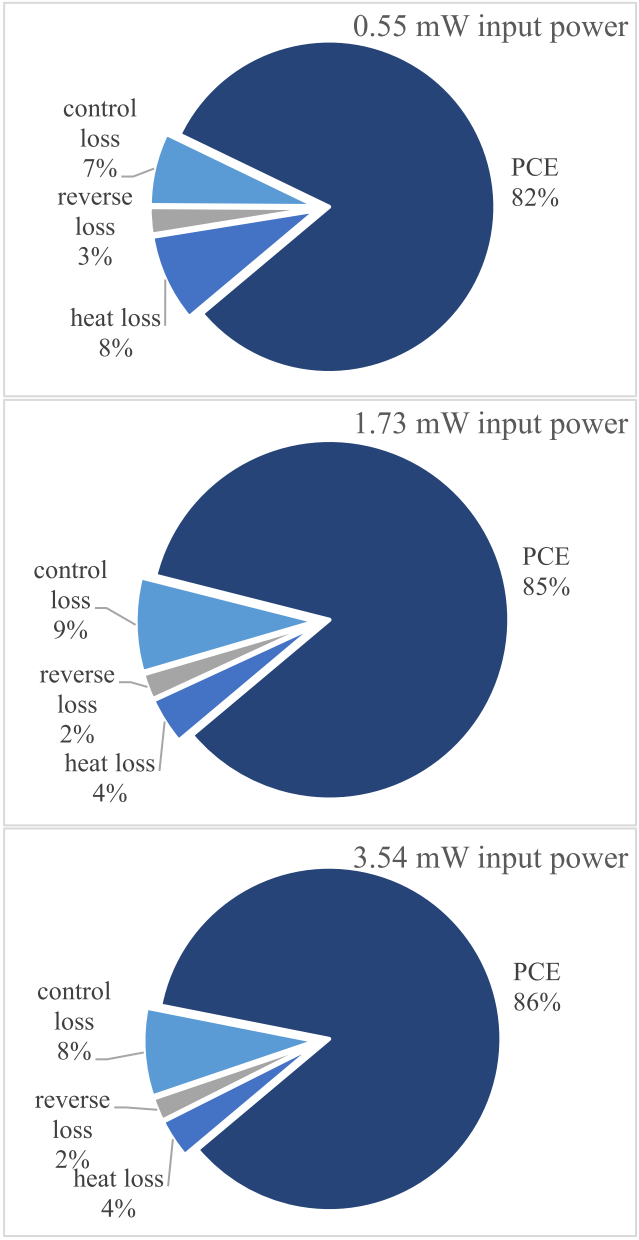

FIGURE 15. Power distribution of OCDGC rectifier.

The proposed rectifier is able to operate in a high efficiency at a small input power. The power distribution of OCDGC rectifier is shown in Fig 15. The PCE of OCDGC rectifier is more than 80% for input power more than 0.55mW. The main sources of loss are control loss and heat loss. The heat loss is between 4% and 8%. Because of the small proportion of heat loss, the self-heating effect of the rectifier is minimal and its effect to PCE is negligible. The heat loss is mainly from the conduction of active diode M1. For small input power, e.g. 0.55mW, the heat loss is the highest loss because the M1 turns on less due to the mismatch of amplifier current and M31 turn-on problem as mentioned above. For a higher input power, the control loss is the highest loss, which mainly comes from the operation of amplifier M6-M2, and the charging and discharging of C1 and C2. The power consumption of amplifier M6-M2 can be reduced by reducing the current through M6 and M2, but this will also reduce the slew-rate of the amplifier, which may result in a longer turn-on/off time of active diode M1 and reduce the overall PCE. The reverse leakage loss of OCDGC is minimal, with less than 3% of input power. This loss is mainly from the inherent leakage of PMOS M1 when it is turned off.

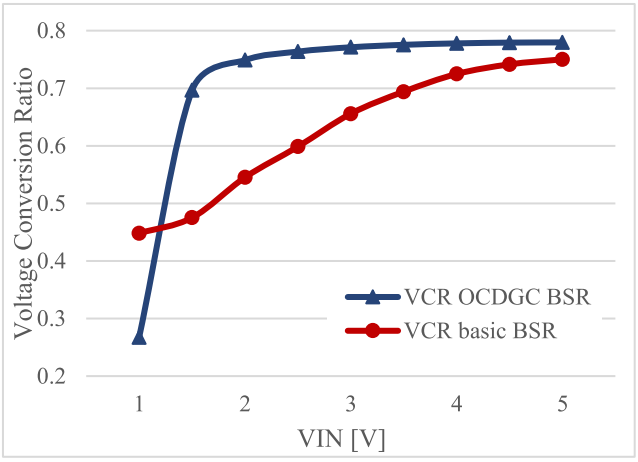

FIGURE 16. Simulated voltage conversion ratio versus input peak voltage of OCDGC rectifier and basic bootstrapping rectifier at 3 MHz.

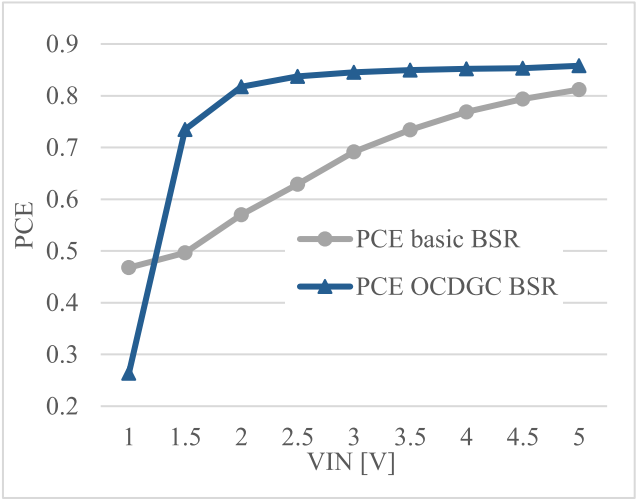

FIGURE 17. Simulated power conversion efficiency versus input peak voltage of OCDGC rectifier and basic bootstrapping rectifier at 3MHz.

Comparisons of voltage conversion ratio (VCR) and PCE are shown in Fig 16 and Fig 17 between OCDGC rectifier and basic bootstrapping rectifier (basic BSR). As shown, OCDGC rectifier has a lower VCR and PCE than basic BSR at 1V_{peak}

input, but higher VCR and PCE for $1.5V_{peak}$ and higher input. The improvement in PCE is from 4% at $5V_{peak}$ to 24% at $1.5V_{peak}$. The improvement in VCR is from 2% at $5V_{peak}$ to 22% at $1.5V_{peak}$.

Overall, simulated results show that the proposed OCDGC rectifier is able to operate with more than 80% PCE at input power from 500μW to more than 3.5mW with minimal reverse leakage loss. The problem is that the output voltage should be higher than 1.1V for the feedback loop of the rectifier to operate and for the rectifier to work in the high-efficiency mode. Comparisons with prior works with similar input power are shown in Table 1. Even though the VCR is lower in this work, but the PCE of this work is higher with a lower input power. Also, the V_{FWD} (0.05 V to 0.1V) of the proposed rectifier is much smaller than the V_{FWD} of the prior designs.

TABLE 2. Comparison With Prior Works.

	TBCAS' 10 [14]	TCAS-II' 06 [35]	TCAS-II' 12 [47]	TBCAS' 12 [45]	This work
Process	0.5 µm	0.35 µm	0.18 µm	0.18 µm	0.18 µm
C_{Load}	N/A	200 pF	10 µF	200 pF	100 pF
R_{Load}	N/A	1.8 kΩ	1 kΩ	2 kΩ	5 kΩ
V_{IN}	3.55 V	1.5-3.5 V	0.9-2 V	0.8-2.7 V	1.5-5 V
V_{OUT}	3.12 V	1.2-3.22 V	0.45-1.78 V	0.3-2 V	1.4-4.95 V
P_{OUT}	7.05 mW	5.76 mW	3.2 mW	2 mW	0.55-3.54 mW
VCR	87.9%	78%-92%	82%-89%	60%-89%	70%-78%
PCE	80.2%	65%-89%	60%-81.9%	37%-80%	73%-86%

V. CONCLUSION

In this article, the so-called bootstrapping rectifier proposed in [44]–[46] have been analyzed, and the reasons for its lower PCE in the experiment results have been pointed out and verified with simulations and experiments. A so-called OCDGC rectifier was presented in this article inspired by the idea of bootstrapping structure. Circuit analysis and simulation results show that OCDGC rectifier is able to operate at an efficiency over 80% with an input power down to 0.5mW. The forward voltage drop of the rectifier can be set by the circuit designer based on application requirement and can be maintained when output voltage drops out of the target range. The proposed OCDGC rectifier is suitable for WPT systems for deep micro-implants with a receiver power budget around 1mW and with a rectifier input voltage more than 1.5V.

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