IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received September 30, 2020, accepted October 25, 2020, date of publication November 5, 2020,
date of current version November 17, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3035974

Active Radiation-Hardening Strategy in Bulk FinFETs

ANTONIO CALOMARDE [1], **ANTONIO RUBIO** [1], **(Senior Member, IEEE), FRANCESC MOLL** [1], **(Senior Member, IEEE), AND FRANCISCO GAMIZ** [2], **(Senior Member, IEEE)**
[1]Department of Electronic Engineering, Universitat Politècnica de Catalunya (UPC), BarcelonaTech, 08034 Barcelona, Spain
[2]Department of Electronics and Computer Technology, Universidad de Granada, 18071 Granada, Spain

Corresponding author: Antonio Calomarde (antonio.calomarde@upc.edu)

This work was supported in part by the Spanish Ministry of Economy (MINECO), and in part by European Regional Development Fund (ERDF) under Project TEC2016-75151-C3-R.

ABSTRACT In this article, we present a new method to mitigate the effect of the charge collected by trigate FinFET devices after an ionizing particle impact. The method is based on the creation of an internal structure that generates an electrical field that drives the charge generated by the ion track out of the sensitive device terminals. This electrical field is generated with the insertion of complementary doped regions near the active region of the device. We analyze the influence of the distance of those regions to the device, their depth into the substrate and their doping concentration to determine the optimal implementation which minimizes the collected charge. The impact on the device performance in terms of leakage current, threshold voltage, maximum transconductance and subthreshold voltage swing has also been investigated. Our results show that the added structures introduce negligible effects in performance degradation and total leakage current, at the cost of a small increase in area. The simulations performed with technology computer-aided design numerical (TCAD) tools in 22nm bulk FinFET technology show that the amount of charge collected by the device terminals can be reduced up to 50% for a linear energy transfer (LET) of 60 MeV-cm^2/mg.

INDEX TERMS Charge collection, single event cross section, radiation hardening, soft error, single event transient (SET), single event upset (SEU), FinFET, 3D TCAD modeling.

I. INTRODUCTION

The aggressive scaling of CMOS technology has greatly increased the susceptibility to radiation-induced soft error (SE) effects due to the low level of charge stored in the devices and low signal-to-noise margins [1].

Single Event Upset (SEU) error rate is strongly influenced by the sensitive area, so as technologies advance to deeper nodes, the Soft Error Rate (SER) is reduced. However, the short distances between transistors make multiple transistors more vulnerable to a single ion strike resulting in multiple upsets [2].

The dynamics of the charge generated in a device by a radiation particle has been properly evaluated [3]. After the ion reaches the silicon surface, it generates a track that leaves a dense plasma of electron-hole pairs along its path. If the electron-hole plasma is generated in a region with an electric field, electrons and holes are separated and a current spike can be observed at sensitive circuit nodes, as free carriers are collected. This current spike has two components: a prompt component due to charge collection in the original depletion region and the funnel region [3], and a delayed component due to carrier diffusion up to the depletion region where it is quickly collected by the junction electric field.

The change in device structure from planar to FinFET impacts the sensitive area and the charge collection process after an ion strike [4]. In conventional CMOS devices all the area under the device collects the charge produced by the ion, but in the bulk FinFET only the area under the fin collects the charge generated by the ion impact (Fig. 1). Thus, the FinFET sensitive area is reduced. However, FinFET SET improvement decreases for LET $\geq$ 10 MeV-cm^2/mg as shown in [5]. In that same work, it is recommended that radiation-hardening techniques should be taken into consideration before FinFET-based circuits are potentially used in space missions Bulk and SOI FinFET SRAM cells have comparable critical charges, but the larger collection volume of the bulk cell may result in upsets for lower linear energy transfer (LET) particles, as well as a larger sensitive area (SEU cross section). However, SOI cells suffer from enhanced hole trapping in the buried oxide that leads to larger

The associate editor coordinating the review of this manuscript and approving it for publication was Nagarajan Raghavan.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

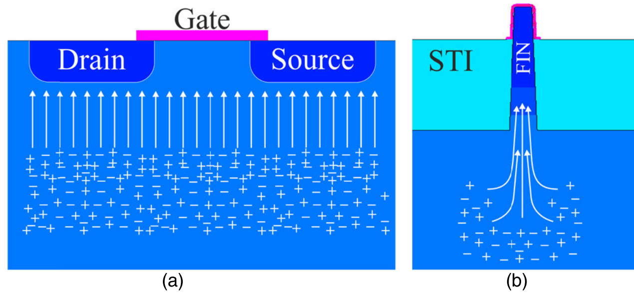

FIGURE 1. Charge collection mechanism after an ion strike in (a) planar MOS and (b) FinFETs.

I-V shifts, due to the threshold-voltage shifts caused by the irradiation.

In CMOS processes, several techniques have demonstrated their efficiency to mitigate charge collection at a node and charge sharing between nodes after an ion strike. Guard rings and guard drains are two of the most used device-level methods. A guard ring is an n+ (or p+) diffusion region surrounding a device in the n-well (or p-substrate), and a guard drain is a reverse biased diode placed near the drain region [6].

Well configuration is another technique with a great impact on the collected charge by the active devices [7]–[11]. An example can be found in [2], where different well configurations are analyzed in three technology nodes, having an apparently inconsistent behavior due to different charge collection mechanisms.

Previous papers have analyzed these techniques in planar CMOS processes [6], [12]–[17], but to the best of our knowledge and beliefs, none of them studies its effects in FinFETs at device-level, and the possible electrical characteristics degradation of the device caused by the insertion of the diffusion regions. This work is an extension and deeper study of [18].

In this context, the present work introduces an efficient mechanism to reduce the charge collected in FinFETs technology. The structure of the paper is as follows: Section II introduces the device models and the simulation environment used to simulate the charge collection process. Section III presents the technique oriented to the reduction of the charge collected by an active device. Section IV find the optimal depth, position and doping concentration of the additional regions and section V analyzes the performance in front of an ion impact in the near area around the fin, and finally, Section VI presents the general conclusions.

II. SIMULATION FRAMEWORK

Three-dimensional (3D) Technology Computer Aided Design (TCAD) simulations of devices are useful and adequate in providing insight into physical mechanisms produced by single and multiple events. In this work, 3D TCAD simulations with Synopsys Sentaurus TCAD tool suite [19] were used to evaluate and demonstrate our improved technique charge collection mechanisms and single-event transient (SET) pulse widths at the nanoscale node here analyzed (22 nm).

The devices evaluated here (Fig. 2) are elements of a high-performance 22nm bulk-FinFET process, with High-k/Metal gate scheme with a nominal V_{dd} of 1 V. FinFET doping profiles and dimensions are obtained from [20], which is based on process emulation, and from [21]. Both devices (PFin and NFin) have been calibrated to fulfill the ITRS high performance requirements for the technology node evaluated in this work [22]. Electrical characteristics such as drain current vs. gate voltage ($I_D - V_G$), drain current vs. drain-source voltage ($I_D - V_{DS}$), and threshold voltage (V_T) are also calibrated to achieve the performance published in [23], where both, the ITRS and designed I-V curves are compared. The substrate thickness has been chosen to be 0.5 μm. Dodd *et al.* studied the impact of substrate thickness [24] in CMOS technology, arriving at the conclusion that the best results are obtained with a lower thickness, due to the reduction of the ion path, and consequently, the charge deposited which diffuses up to the depletion region. We have checked that these results are also true in the case of FinFETs.

Impact ionization, drift-diffusion transport model, concentration dependent Shockley-Read-Hall (SRH), high-field mobility degradation, density-gradient quantum corrections and Coulomb scattering models were used in all the simulations performed along the study.

A. ION TRACK

The selected incident point of the ion track crosses the device at the body-drain junction, where the electric field is maximum, to simulate the transistor worst case, i.e. the maximum drain collected charge and bipolar amplification (bipolar gain), normal incidence strike, as shown in Fig. 3 (dashed lines), with the device biased in OFF.

The choice of the spatial and temporal ion track parameters is an important step in the modelling process of single event hits in nanoscale technologies [25]–[27]. Although only comparisons between the simulations for a conventional FinFET structure and the modified structure proposed in this work are made, we have tried to adjust the parameters of the ion track to the most accurate values.

The electron-hole pair column created in the device by the ion strike is modeled using a carrier-generation function [28]:

$$G(l, w, t) = G_{LET}(l)\, R(w, l)\, T(t) \quad (1)$$

where $G_{LET}(l)$ is the linear energy transfer generation density, and $R(w, l)$ is a function describing the radial variation and $T(t)$ a function describing the temporal variation of the generation rate.

The linear energy transfer (LET) value is considered constant along the ion track ($G_{LET}(l) = \text{constant}$).

The spatial distribution of the generation rate $R(w, l)$ along the impact ion track can be defined using an exponential or a Gaussian function. In our case, we preferred to use a Gaussian ion track structure because it is more frequently used in device simulation studies, and because it provides a more realistic ion track structure, as experimentally validated in [29]. Previous studies [4] conclude that for FinFET technology

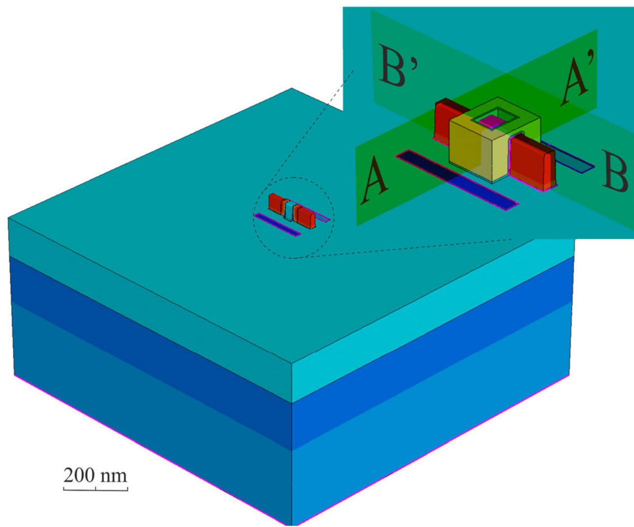

FIGURE 2. Three-dimensional TCAD 22nm bulk trigate FinFET with the two-doping trench (TIE) and reference cuts used in some figures.

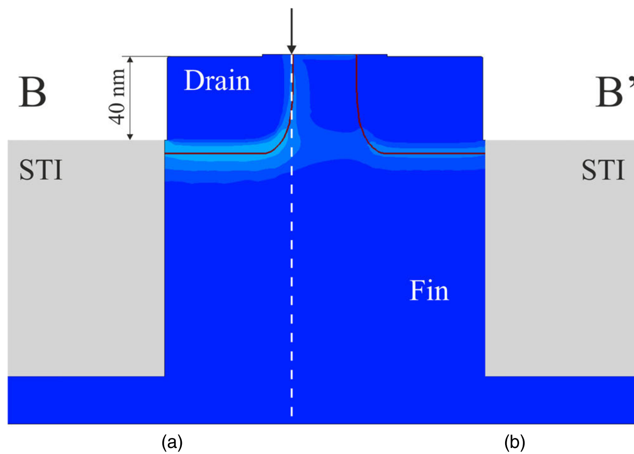

FIGURE 3. Vertical cut of the Fin region (B-B'). Arrow line is the incident point of the ion track. The ion path crosses at the position of maximum diffusion area (dashed line). Drain in the left side. Brown line is the junction line, and colors correspond to intensity of electric field.

the characteristic ion-track radius of the Gaussian function should have a value close to 10 nm for the best accuracy of the results.

The temporal evolution $T(t)$ from (1) is defined by a Gaussian function:

$$T(t) = \frac{2 \cdot e^{\left(-\left(\frac{t-t_0}{\sqrt{2}\cdot t_{hi}}\right)^2\right)}}{\sqrt{2}\cdot t_{hi}\sqrt{\pi}\left(1+erf\left(\frac{t_0}{\sqrt{2}\cdot t_{hi}}\right)\right)} \quad (2)$$

The moment of the heavy ion penetration (t_0) has been chosen to obtain zero generation at initial and final simulation time. In order to understand the implications of the characteristic width, t_{hi}, in the collected charge, simulation results of several t_{hi} from 0.6 ps to 1.2 ps are presented in Table 1. The characteristic widths (in ps) are shown in the left column, while the right column shows the collected charge by the drain terminal (in fC.) for a LET of 10 MeV-cm^2/mg. The relationship between both quantities is approximately linear in the simulated range.

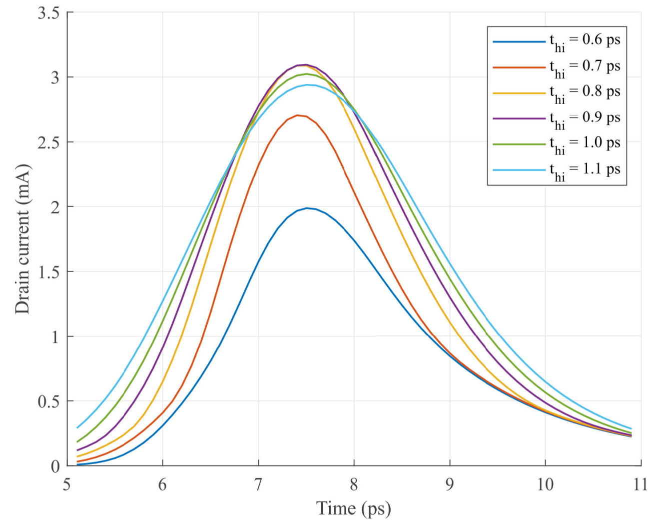

FIGURE 4. Drain current with NFIN in off, spatial radius of 10 nm, t_{hi}. from 0.6 ps to 1.1 ps, 10 MeV-cm^2/mg.

TABLE 1. Collected charge vs. ion temporal characteristic width.

Characteristic Width (ps)	Collected charge (fC)
0.6	5.52
0.7	6.81
0.8	8.26
0.9	8.97
1.0	9.46
1.1	9.87
1.2	10.21

To understand this behavior, we analyze the temporal function generation rate for these values. Lower t_{hi} values provide higher peak values and a narrower shape, with the same charge generated by the ion track in all the cases. For very small values of t_{hi}, $T(t)$ would approach to a Dirac Delta function, while for large values of t_{hi}, $T(t)$ would mean a constant generation of electron-hole pairs, but all the shapes cover the same area.

The transient responses of the simulated drain current for each one of the t_{hi} values of Table 1 are shown in Fig. 4, with a LET of 10 MeV-cm^2/mg, $t_0 = 7$ps., and a track radius of 10 nm. Drain peak current increases with t_{hi} increasing from 0.6 ps to 0.8 ps, and it decreases for t_{hi} increasing from 0.9 ps to 1.1 ps. The shape of the drain current vs time curve is also widening (delayed), i.e., the maximum peak value is obtained for a value of t_{hi} between 0.8 and 0.9 ps, while the total charge collected by the drain increases with t_{hi}, obtaining values above those observed in previous experimental works. Based on the expected values of total collected charge [30]–[33], we conclude that the best fit for t_{hi} is 0.8 ps for the evaluated device.

III. CHARGE COLLECTION METHOD

The charge collection mechanisms in FinFETs after an ion strike have been extensively studied in [4]. As shown in Fig. 1, when a dense plasma of electron-hole pairs is generated by the ion, the only path to reach the fin from the substrate is the sub-fin region.

The strategy of our proposal is to collect the generated charge by the ion track out of the sensitive terminals before it arrives to the device terminals. Typically, the drain node of the device is the most sensitive terminal, the source terminal is usually less sensitive and tied to power rails (or another drain) in a wide variety of logical gates, and gate terminal is driven by the output of the previous stage and thus also connected to power rails. In this section, our study concentrates on the NFET device.

To mitigate the effect of the charge generated by the ion, we induce an electric field capable of redirecting a significant part of this charge away from the sensitive terminals, and finally to collect it by an additional terminal. In the physical realization, two alternatives can be considered: the first one, a horizontal electric field in the transversal direction under the fin; and in the second one, a vertical electric field from the channel of the device to the substrate is superposed. Both solutions have been studied, but better results were obtained with the horizontal field implementation [18]. Therefore, only last option is presented in this article.

The easiest way to generate this electrical field consists of the use of the depletion region of a PN junction. A simplified model of the peak and width of the electrical field in an abrupt PN junction is given by the following expression [34]:

$$|E_{PK}| = \sqrt{\frac{2q\varphi_b}{\varepsilon_{si}} k \frac{1}{1/N_A + 1/N_D}} \tag{3}$$

With a width:

$$\omega = \sqrt{\frac{2\varepsilon_{si}\varphi_b}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{4}$$

where N_A and N_D are the acceptor and donor density in P and N region respectively, ϕ_b is the built-in potential. The peak value of the electric field is found right at the interface between both regions. The whole depletion region is allocated in the N and P regions with a distribution given by:

$$N_A\omega_p = N_D\omega_n \tag{5}$$

The longitudinal electric field is generated from two narrow trenches (or ties), added at each side of the device active region, and parallel to the fin, one with N+ doping (NTIE) and the other with P+ (PTIE), as shown in Fig. 2 and Fig. 5.

To design the position and intensity of the electric field, we will use the three previous equations, where the position and the doping profile of both tie trenches play an important role.

It follows from equation (5) that the doping concentration of the added trenches must be greater than the doping concentration of the contiguous area (substrate), in order to ensure that the electric field remains mostly on the desired area to capture the electron-hole pairs generated by the ion. As illustrated in Fig. 1, the region of interest where the induced electric field should be present is below the fin, so that electron-hole pairs generated by the strike are swept away from the fin structure.

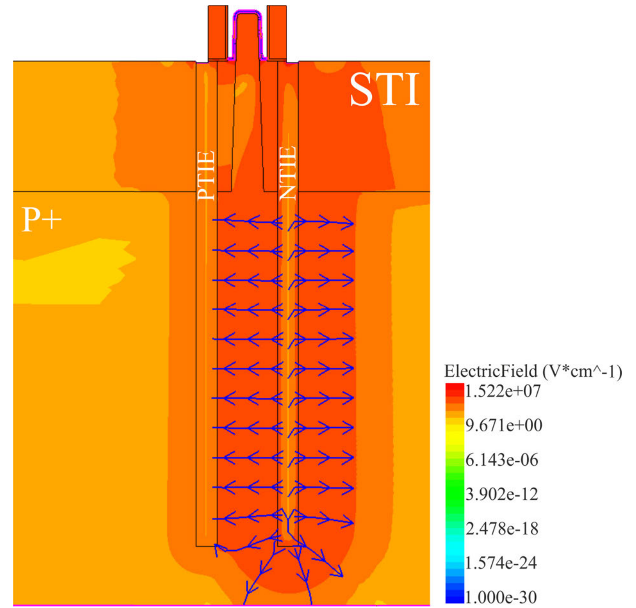

FIGURE 5. FinFET type N 2D cross section (A-A' of Fig. 2) with the well ties in both sides of the device. NTIE is the trench with N++ doping, and PTIE the P++ trench. Arrows point out the direction of the electric field.

In this work, the two trench ties are biased to ground, but it is possible to increase the width and intensity of the electric field by reverse biasing the junction between the NTIE trench and the substrate with $V_{NTIE} > 0$, and the junction of the PTIE trench and the substrate with $V_{PTIE} < 0$.

The longitudinal electric field generated is shown in the same figure (Fig. 5), and according to the previous discussion, this electric field is located under the fin. The direction of the arrows follows the direction of the electric field, and the colors, the intensity of the electric field. Only the streamlines of highest electric field are represented, which are found in the junction NTIE-substrate.

In order to verify the efficiency of the added ties in the reduction of the collected charge, we made a comparison of the same device with and without the ties (Fig. 6), with an ion impact with a LET = 10 MeV-cm^2/mg, incidence normal outside of both ties. In the two figures are exposed the electron density from the cross-section A-A' (referred to Fig. 2) after 3 ns of ion impact. The impact point and the track (in this case) are represented by the arrows. As expected, the conventional solution, on the left side of the Fig. 6, has a radial symmetric electron density distribution around the ion track, while on the right side, with the same ion conditions, the electron density distribution is substantially reduced in the region below the fin due to the effect of the presence of the right tie (N type), which capture an important quantity of the electrons generated by the ion, avoiding the diffusion to the drain region (and, also, to the complete fin structure). The results for the hole density are quite similar to the ones shown for the electron density. Additional ion entry points and tracks have been studied, obtaining similar results. Even in the worst case, when the ion strike occurs right in the drain region of the fin, the two tie trenches trap a large

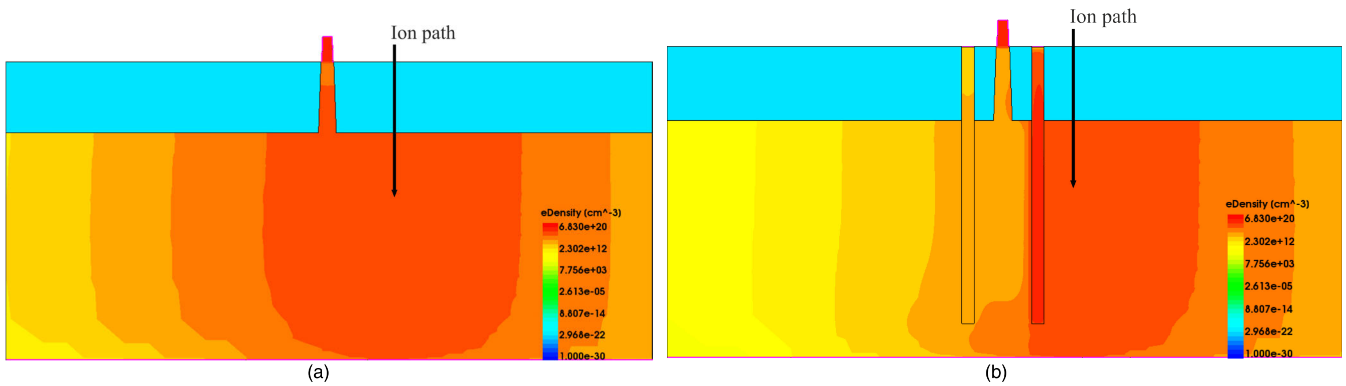

FIGURE 6. Comparison of electron density after 3 ns of an ion hit, LET of 10 MeV-cm^2/mg of a 2D cross section (A-A′ of Fig. 2), and in both cases, the incident point on the right of the fin, normal incidence. (a) without TIE trenches, (b) TIE trenches at each side of the fin.

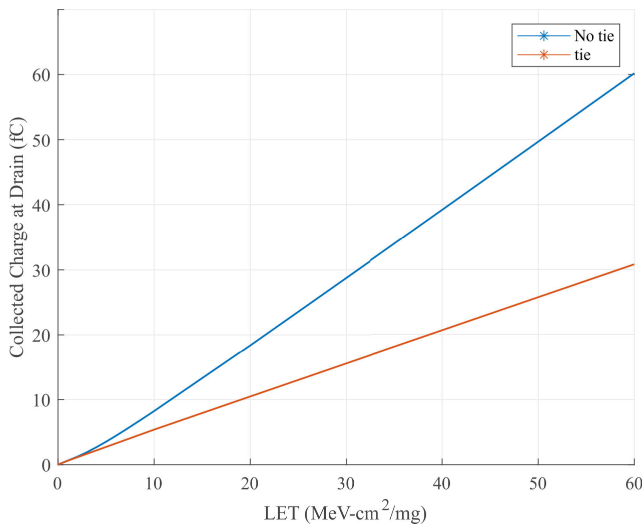

FIGURE 7. Collected charge at drain terminal after an ion impact from 1 to 60 MeV-cm^2/mg. without doping trench (blue line) and with doping trenches (orange line).

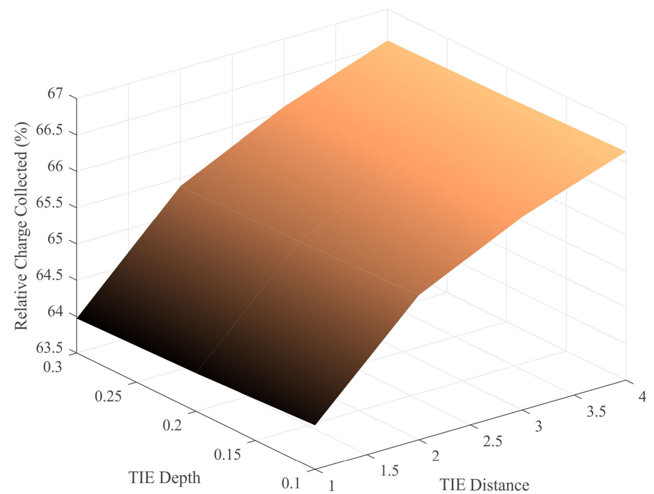

FIGURE 8. Relative charge collected by the drain terminal compared with the conventional design, changing the distance and the depth of the tie trenches.

portion of the generated charge, preventing its diffusion to the sensitive terminals of the device.

In order to quantify the percentual charge captured by the two trenches, simulation of strikes of heavy-ion data from 0.1 to 60 MeV-cm^2/mg have been performed. Results are shown in Fig. 7. The blue line is added as reference (no trench ties added) to be able to compare with our solution (orange line). In both cases, the relationship between LET and the collected charge at the drain follows a linear dependence between 10 and 60 MeV-cm^2/mg, but the slope for our solution is lower, which implies that less charge is collected in the drain, reaching on the order of 50% for the range analyzed.

IV. INFLUENCE OF VARIATION OF DEPTH AND DISTANCE

In the previous section, the ability to capture electron-hole pairs by tie trenches has been demonstrated, obtaining better results for higher values of LET's, while, for the best analyzed case, it can reach up to 50% for a LET of 60 MeV-cm^2/mg.

A. TIE TRENCHES GEOMETRY

To optimize and minimize the collected charge by the active terminal, we will evaluate the distance to the fin, depth and doping concentration of the highly doped regions (tie-trenches) to determine the optimal solution.

Simulations have been performed changing the distance of the tie trenches starting from the fin, and the depth, from the bottom of the STI (Shallow Trench Isolation) to near the bottom of the substrate. The relative charge collected by the drain terminal compared with the conventional design is shown in Fig. 8 for a LET = 10 MeV-cm^2/mg. Tie trench (TIE) depth is measured from the bottom side of the STI, up to the bottom face of the substrate. A lower value means less depth from the STI. The TIE distance is measured from the corresponding lateral side of the fin structure in units of ''fin width''.

According to the results obtained, the depth of the tie trenches has a minimal influence in the collected charge. Only a small reduction of the charge is observed for deeper tie trenches. No more than a 0.2 % from the lowest to the highest depth. This minimal influence, in our case, is due to the use of twin-well process: the charge generated outside the well is mainly diffused to the substrate, and thus deeper tie trenches are not necessary.

The most significant parameter which affects the collected charge is the distance to the fin, observing that the TIE

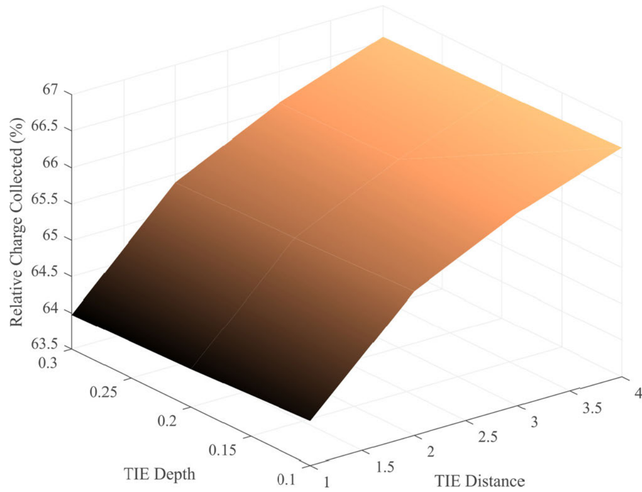

FIGURE 9. Relative leakage current vs the variation of the depth and distance of both ties (relative to the configuration without ties).

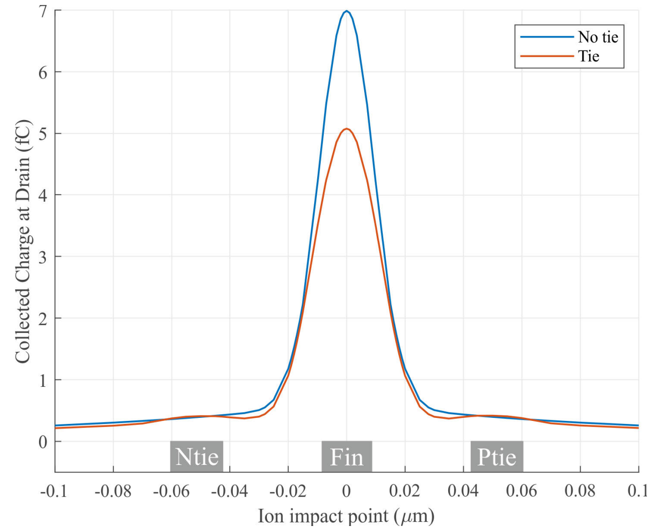

FIGURE 10. Collected charge by the drain vs ion impact point relative to the distance to the fin center, direction (A-A', Fig. 2), with a LET 10 MeV-cm^2/mg, crossing over the middle of the gate, with and without tie trenches.

trenches must be as close as possible to the fin, as allowed by the design and manufacturing rules.

B. ELECTRICAL PARAMETERS

To verify the limitations, drain current saturation, drain leakage current, threshold voltage, subthreshold voltage swing and the maximum transconductance of the device for the same trench tie distances and depth have been extracted from the simulations.

The saturation current, the leakage current and the maximum transconductance have low variance with the position and depth of the trench ties, except at a distance less than 2 times the width of the fin, reducing all these values about a 1%, as it is shown in Fig. 9 for the current in off state. These variations are due to the increase in similar proportion of the threshold voltage of the device. In all the simulations, no apparent changes affecting the subthreshold voltage swing were observed when the tie trenches were inserted in all cases.

Another parameter that can be modified is the doping concentration of the trenches. The increase in the doping concentration produces an increase in the electric field and should therefore reduce the collected charge. Several simulations have been performed observing a lower reduction of the charge collected when the doping concentration is increased. This reduction is produced at the moment of the carried diffusion of the electron-hole generated by the ion track. The minimal doping concentration in the NTIE and PTIE used in these cases is 10^{19} cm^{-3} inserted in a P substrate with 10^{15} cm^{-3}. Values under 10^{19} cm^{-3} have a drastic reduction of the efficiency in the charge captured by the inserted trenches, due to the low insertion of the depletion region in the sub-fin area.

C. LEAKAGE CURRENT

The two tie trenches added introduce a new element which contributes to the total leakage current which can be inappropriate for low power applications. In order to verify if this technique is applicable to low power design, we measured the current of the two tie trenches giving a value related to the device leakage current of $I_{off}/10^{10}$ in the worst case (the highest doping concentration of the tie trenches).

These values are insignificant compared with the device power consumption in its off state. Furthermore, the use of these trenches relies heavily on the importance of the propagation of the SEE, caused by the ion impact, in the digital chain up to a memory element (or the same memory element), i.e., should not be used in all the devices of the system, and only in those cases where the impact of an ion can cause a SEU.

V. ION IMPACT POINT

All the previous analyses were made for a strike point at the device drain. In this section we test several impact points around the device to observe the effects of the tie trench on the collected charge in the drain terminal.

To obtain the behavior in this case, a set of simulations have been carried out in the direction of the cross-section A-A' (referred in Fig. 2), in two cases, over the gate (Fig. 10 and Fig. 12), and over the drain (Fig. 11).

In these figures, the total charge collected by the drain with and without tie trench is shown as a function of the position of the ion impact point across the reference A-A' relative to the center of the fin. The position and width of the fin and the two tie trenches are shown for reference. In the result set of Fig. 10 and Fig. 11 a LET of 10 MeV-cm2/mg has been used, and 60 MeV-cm^2/mg for Fig. 12.

From the data shown in Fig. 10, Fig. 11 and Fig. 12(a), it is observed that the shape of the collected charge in the three cases follows the same pattern, and is repeated for the rest of the cuts in the direction AA'. The highest charge collected by the drain is found when the impact point of the ion is over the fin structure or very close (around two times the fin width), and its maximum value in the middle of the fin

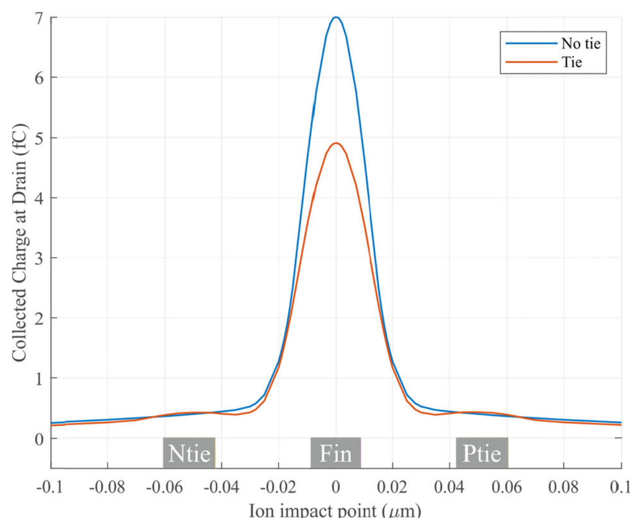

FIGURE 11. Collected charge by the drain vs ion impact point relative to the fin center, direction (A-A', Fig. 2), with a LET 10 MeV-cm^2/mg crossing over the middle of the drain.

(along curve A-A '). Outside the fin area, the total charge captured by the drain is practically negligible (approximately 30 times less in the worst case), for all cases (with or without trenches), so outside the fin area, the probability of creating a SET (Single Event Transient) is quite low, and relegated to ions with a very high LET.

The efficiency of the tie trenches is shown in the right of Fig. 12(b) for a LET of 60 MeV-cm^2/mg and impact over the middle of the gate. Inside the fin or nearest (the section of highest charge collected by the drain), the efficiency is maximum, arriving to values of a 73% and a 58% (LET 10 and 60 MeV-cm^2/mg respectively) over the drain region, and a 70% for a LET of 10 MeV-cm^2/mg when the impact is over the drain, and compared for the solution without trench ties. These efficiencies decrease as increases the distance from the midpoint of the fin, and is proportional to the charge collected by the drain.

Outside the fin area, with the use of tie trenches, the collected charge is 15% lower on average, except in the area where the tie trenches are located, where their efficiency is drastically reduced in these regions with an increase of about a of 5% in the P doping tie area (PTIE). This unexpected behavior has been analyzed, and it is due to the modification of the electric field by the ion track in the tie trench, and, although part of the inserted charge is absorbed in the same area, it is also expelled outside the tie trench, and consequently, absorbed by the rest of the terminals. This reduction has minimal impact in the total efficiency because it is produced outside the fin area, where the charge collected is a 30% lower than in the fin.

The continuous shrinkage of technology nodes involves an increase in multiple upsets, having a relevant importance at the nanoscale [2]. Outside the area between the two trenches, the charge collected by the collector is reduced around a 17% for a LET of 10 and 60 MeV-cm^2/mg, improving the resilience to multiple upsets.

There is also agreement between the results of Fig. 7 and Fig. 10, Fig. 11 and Fig. 12, since in all cases for higher LETs, the efficiency of the trenches improves, obtaining greater absorption of the generated charge by the ion track.

The charge collected by the drain when the ion impact point is moved along the cut B-B' (see Fig. 2) is depicted in Fig. 13. The limits of the drain and source regions are also shown, in order to be able to reference the position of the impact.

According to previous works, the most sensitive region is limited to the drain area, but our results also show that, in addition to this region, the portion of the gate region near the drain is also sensitive, and furthermore, it is the most sensitive area of all the structure of a bulk FinFET, with or without tie trenches. The reduction of the charge

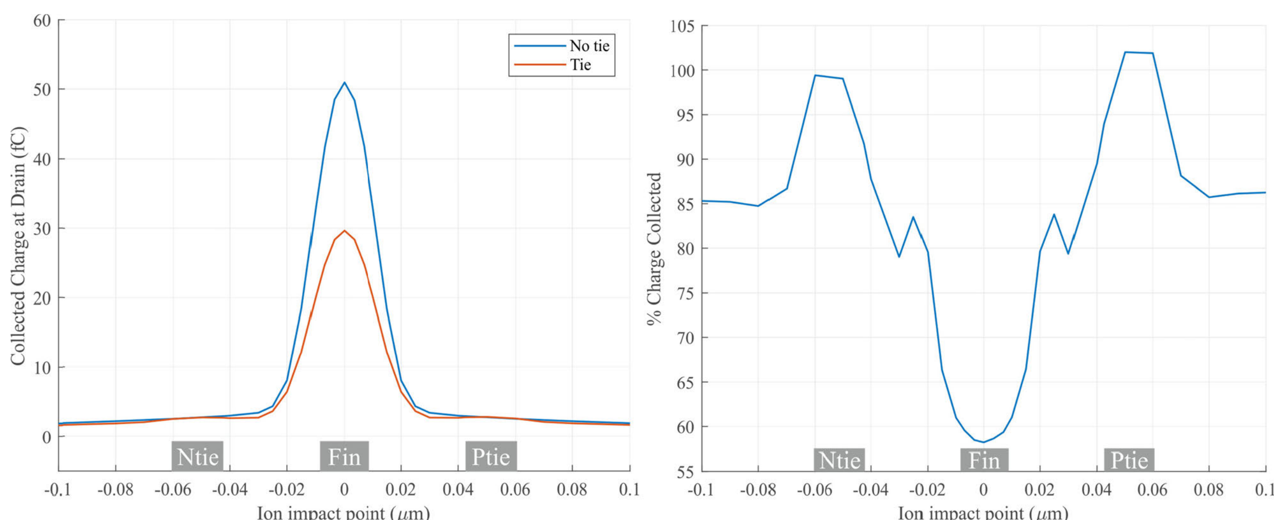

FIGURE 12. Collected charge by the drain vs ion impact point relative to the fin center, direction (A-A', Fig. 2), crossing over the middle of the gate, and LET 60 MeV-cm^2/mg. (a) Charge with and without tie trenches, (b) Relative charge collected with the insertion of the tie trench.

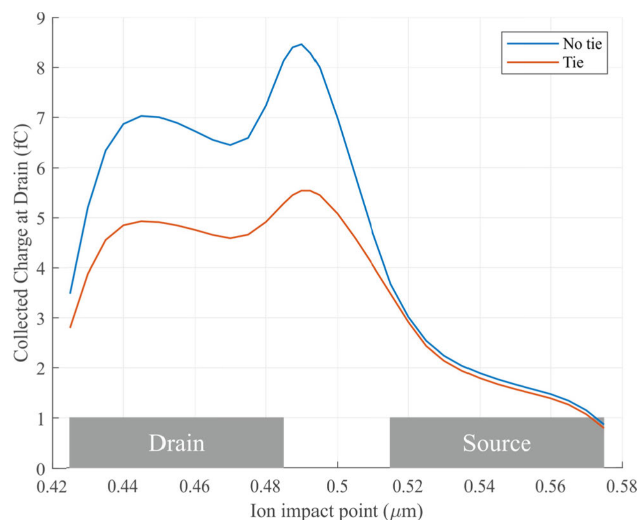

FIGURE 13. Collected charge by the drain vs ion impact point relative to the fin center, LET 10 MeV-cm2/mg. charge with and without tie trenches along the cut B-B′ (see Fig. 2).

collected by the drain in this region is about a 30% in the drain region, and up to a 35% in the gate area, near the drain.

The use of a composition of Fig. 10 to Fig. 13 allows us to conclude that the most sensitive region of bulk FinFET is limited to the fin structure, and located between the drain and the gate region of the fin. In this region, the use of the tie trenches allows to reduce the charge collected by the drain up to a 35 % for a LET of 10 MeV-cm^2/mg, and a 50% for a LET of 60 MeV-cm^2/mg.

VI. CONCLUSION

This article proposes a new method to mitigate the charge collected on the sensitive terminals of a bulk FinFET device generated by an ion track. The proposal is based on the creation of an electric field that redirects the excess of carriers towards terminals not affecting the information processed by the devices. The electric field is created through two trench ties with a P+ and N+ doping profile and placed at both sides of the device.

The depth, distance and doping of the tie trenches have been analyzed. The depth of the tie trenches has a minimal influence in the collected charge, allowing to reduce the difficulty in manufacturing process the proposed solution. The TIE trenches must be as close as possible to the fin, as allowed by the design and manufacturing rules.

The incorporation of these trenches increases slightly the global power consumption of the system. It has been shown in the present work that the contribution of the tie current related with the device in its off state is $I_{off}/10^{10}$, which is a negligible part compared with the device in its lower power consumption state.

Drain current saturation, drain leakage current, threshold voltage, subthreshold voltage swing and the maximum transconductance have been analyzed, with minimal impact when the tie distance is greater than 2 times the fin width.

The reduction of charge collected by the drain terminal of a bulk FinFET when an ion impact is produced can be as much as 50% when the trench-ties proposed in this work are incorporated in the device structure, for a LET = 60 MeV-cm^2/mg. This efficiency is reduced for lower LET's.

The greatest charge collected by the drain is obtained when the ion impact point is on or around the fin. In this region, the tie trenches have shown the highest efficiency, and outside this region, the collected charge is negligible in both cases, with or without the tie trenches.

As future work we will evaluate the use of the trenches in complex gates and multi fin devices, and the impact in the charge collected, leakage and area overhead.

REFERENCES

[1] D. Munteanu and J.-L. Autran, "Modeling and simulation of single-event effects in digital devices and ICs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1854–1878, Aug. 2008.
[2] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. A. Reed, R. D. Schrimpf, J. K. Wang, N. Vedula, B. Bartz, and C. Monzel, "Impact of technology scaling on SRAM soft error rates," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3512–3518, Dec. 2014.
[3] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.
[4] P. Nsengiyumva, L. W. Massengill, M. L. Alles, B. L. Bhuva, D. R. Ball, J. S. Kauppila, T. D. Haeffner, W. T. Holman, and R. A. Reed, "Analysis of bulk FinFET structural effects on single-event cross sections," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 441–448, Jan. 2017.
[5] P. Nsengiyumva, D. R. Ball, J. S. Kauppila, N. Tam, M. McCurdy, W. T. Holman, M. L. Alles, B. L. Bhuva, and L. W. Massengill, "A comparison of the SEU response of planar and FinFET d flip-flops at advanced technology nodes," *IEEE Trans. Nucl. Sci.*, vol. 63, no. 1, pp. 266–272, Feb. 2016.
[6] B. Narasimham, J. W. Gambles, R. L. Shuler, B. L. Bhuva, and L. W. Massengill, "Quantifying the effect of guard rings and guard drains in mitigating charge collection and charge spread," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3456–3460, Dec. 2008.
[7] H. Jianguo, H. Yibai, and L. Ge, "SET response of the selectively implanted deep N-Well —Comparison with dual well and triple well," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 3, pp. 370–375, Sep. 2015.
[8] T. Uemura, T. Kato, R. Tanabe, H. Iwata, J. Ariyoshi, H. Matsuyama, and M. Hashimoto, "Exploring well-configurations for minimizing single event latchup," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3282–3289, Dec. 2014.
[9] I. Chatterjee, B. Narasimham, N. N. Mahatme, B. L. Bhuva, R. D. Schrimpf, J. K. Wang, B. Bartz, E. Pitta, and M. Buer, "Single-event charge collection and upset in 40-nm Dual- and triple-well bulk CMOS SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2761–2767, Dec. 2011.
[10] N. J. Gaspard, A. F. Witulski, N. M. Atkinson, J. R. Ahlbin, W. T. Holman, B. L. Bhuva, T. D. Loveless, and L. W. Massengill, "Impact of well structure on single-event well potential modulation in bulk CMOS," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2614–2620, Dec. 2011.
[11] J. R. Ahlbin, M. J. Gadlage, D. R. Ball, A. W. Witulski, B. L. Bhuva, R. A. Reed, G. Vizkelethy, and L. W. Massengill, "The effect of layout topology on single-event transient pulse quenching in a 65 nm bulk CMOS process," *IEEE Trans. Nucl. Sci.*, pp. 3380–3385, Dec. 2010.
[12] B. Narasimham, B. L. Bhuva, R. D. Schrimpf, L. W. Massengill, M. J. Gadlage, W. T. Holman, A. F. Witulski, W. H. Robinson, J. D. Black, J. M. Benedetto, and P. H. Eaton, "Effects of guard bands and well contacts in mitigating long SETs in advanced CMOS processes," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 3, pp. 1708–1713, Jun. 2008.
[13] X. Xu, Y. Xiong, M. Tang, Z. Li, and Y. Zhou, "Failure mechanisms of guard-drain in mitigating n-hit single-event transient via 45-nm CMOS process," in *Proc. 12th IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Oct. 2014, pp. 1–3.
[14] T. R. Young and C. L. Hee, "TID and SEE hardened n-MOSFET layout on a bulk silicon substrate which combines a DGA n-MOSFET and a guard drain," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2015, pp. 1–4.

[15] B. Narasimham, R. L. Shuler, J. D. Black, B. L. Bhuva, R. D. Schrimpf, A. F. Witulski, W. T. Holman, and L. W. Massengill, "Quantifying the reduction in collected charge and soft errors in the presence of guard rings," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 1, pp. 203–209, Mar. 2008.

[16] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3253–3258, Dec. 2006.

[17] M. P. Baze, S. P. Buchner, and D. Mcmorrow, "A digital CMOS design technique for SEU hardening," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2603–2608, 2000.

[18] A. Calomarde, E. Amat, A. Rubio, F. Moll, and F. Gamiz, "Active charge collection strategy for radiation environment at device level," in *Proc. 16th Eur. Conf. Radiat. Its Effects Compon. Syst. (RADECS)*, Sep. 2016, pp. 1–4.

[19] *Sentaurus TCAD*, Synopsys, Mountain View, CA, USA, 2019.

[20] *Three-Dimensional Simulations of Raised Source-Drain FinFET*, Synopsys, Mountain View, CA, USA, 2019.

[21] H. Kawasaki, "Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4.

[22] *International Technology Roadmap for Semiconductors—ITRS 2.0 Home Page*. Accessed: Apr. 12, 2016. [Online]. Available: http://www.itrs2.net/

[23] C. C. Wu, D. W. Lin, and, "High performance 22/20nm FinFET CMOS devices with advanced high-K/metal gate scheme," in *IEDM Tech. Dig.*, Dec. 2010, pp. 600–603.

[24] P. E. Dodd, M. R. Shaneyfelt, E. Fuller, J. C. Pickel, F. W. Sexton, and P. S. Winokur, "Impact of substrate thickness on single-event effects in integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1865–1871, 2001.

[25] M. Murat, A. Akkerman, and J. Barak, "Electron and ion tracks in silicon: Spatial and temporal evolution," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3046–3054, Dec. 2008.

[26] T. Makino, D. Kobayashi, K. Hirose, Y. Yanagawa, H. Saito, H. Ikeda, D. Takahashi, S. Ishii, M. Kusano, S. Onoda, T. Hirao, and T. Ohshima, "LET dependence of single event transient pulse-widths in SOI logic cell," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 1, pp. 202–207, Feb. 2009.

[27] M. Raine, A. Valentin, M. Gaillardin, and P. Paillet, "Improved simulation of ion track structures using new Geant4 Models—Impact on the modeling of advanced technologies response," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2697–2703, Dec. 2012.

[28] *SentaurusTM Device User Guide*, Synopsys, Mountain View, CA, USA, Mar. 2019.

[29] M. P. R. Waligórski, R. N. Hamm, and R. Katz, "The radial distribution of dose around the path of a heavy ion in liquid water," *Int. J. Radiat. Appl. Instrum.*, vol. 11, no. 6, pp. 309–319, Jan. 1986.

[30] F. El-Mamouni, E. X. Zhang, N. D. Pate, N. Hooten, R. D. Schrimpf, R. A. Reed, K. F. Galloway, D. Mcmorrow, J. Warner, E. Simoen, C. Claeys, A. Griffoni, D. Linten, and G. Vizkelethy, "Laser- and heavy ion-induced charge collection in bulk FinFETs," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2563–2569, Dec. 2011.

[31] F. El-Mamouni, E. X. Zhang, D. R. Ball, B. Sierawski, M. P. King, R. D. Schrimpf, R. A. Reed, M. L. Alles, D. M. Fleetwood, D. Linten, E. Simoen, and G. Vizkelethy, "Heavy-Ion-Induced current transients in bulk and SOI FinFETs," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2674–2681, Dec. 2012.

[32] N. Seifert, S. Jahinuzzaman, J. Velamala, and N. Patel, "Susceptibility of planar and 3D tri-gate technologies to muon-induced single event upsets," in *Proc. IEEE Int. Rel. Phys. Symp. Process.*, May 2015, pp. 211–216.

[33] N. Seifert, B. Gill, S. Jahinuzzaman, J. Basile, V. Ambrose, Q. Shi, R. Allmon, and A. Bramnik, "Soft error susceptibilities of 22 nm tri-gate devices," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2666–2673, Dec. 2012.

[34] Simon M. Sze, *Semiconductor Devices: Physics and Technology*, 3rd Ed. Hoboken, NJ, USA: Wiley, 2012.