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New Type Single-Supply Four-Switch Five-Level Inverter With Frequency Multiplication Capability

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ABSTRACT This paper focuses on the problems of a large number of components and complex structure for traditional five-level inverters. In order to solve the problem, a novel single-supply four-switch five-level inverter topology is proposed. Based on the H4 two-level full bridge inverter, one coupling inductor and two diodes are added to constitute the proposed topology. By means of the LPS-PWM modulation strategy with frequency doubling ability, one pair of complementary power switches operate at power frequency, and the other pair of high-frequency switches operate at the half of the output sine wave modulation frequency, which effectively reduces the switching loss and electromagnetic interference resulting from high switching frequency. In addition, three kinds of extended circuits of four-switch five-levels are proposed. A comprehensive comparison against the state-of-the-art topologies in terms of the required number of components is performed to attest the outperforming merits of the proposed topology. Finally, various experimental results are presented to validate the feasibility and operability of the proposed topology.

INDEX TERMS Four-switch five-level inverter, reduce switch count, frequency doubling, THD.

I. INTRODUCTION

Inverter is the key to realize DC-AC. Multilevel inverter has the advantages of low Total Harmonic Distortion (THD) rate, low switching voltage stress and small output filter over the various types of sine wave inverter [1]–[3]. Thus, it is widely used in new energy generation, HVDC transmission, active power filter, high-power motor drive, flexible AC transmission and other fields [4]–[6]. The classical multilevel inverter (MLI) topologies include cascaded H-bridge (CHB) multilevel inverter [7], Neutral Point Clamped (NPC) multilevel inverter [8] and flying capacitor (FC) multilevel inverter [9]. However, at least eight power switches are required in the classic five-level inverter, which also needs more power components and auxiliary drive circuits. With the number of MLI levels increases, the number of components will also increase, which makes the MLI system bigger, more complex and less efficient. At the same time, it is difficult to solve the capacitor voltage balance problem existed in NPC and FC topologies [10], [11].

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Researchers are trying to increase the number of output voltage levels and reduce the number of switches to further improve the efficiency and the quality of output voltage waveform [12]–[22]. An ANPC topology and decoupling algorithm are introduced in [12], which solve the problem of unbalanced neutral point potential of NPC topology capacitor. Moreover, the clamping capacitances required by traditional NPC topology are also reduced, only three capacitors and eight power switching devices are needed to realize five-level output. However, it is noted that the input DC voltage of this topology should be twice as high as the peak output voltage, which limits its application. Recently, the topology which is combined FC and NPC in [13] can realize NPC capacitor neutral point potential balance and output larger voltage with less switches. However, six switches and three capacitors are still needed in this topology. A MLI topology based on switched capacitor (SC) is proposed in [14]–[16], whose number of components is reduced by outputting a higher voltage than the input in a charge pump like manner [23]. The five-level topology based on SC introduced in [14] has twice the output voltage gain, and the voltage stress of some power switches are declined to reduce

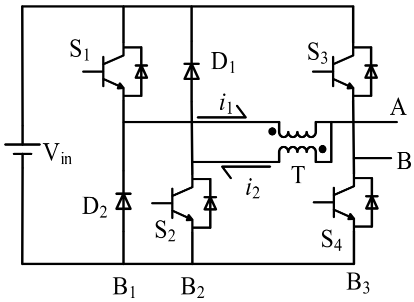

FIGURE 1. Main circuit of coupled inductance five-level inverter.

the switching loss. With a large number of components, the topology consists of two capacitors, seven power switching devices and four independent diodes. The number of independent diodes is further reduced in [15]. The switched capacitor five-level topology proposed in [16] with only one capacitor as auxiliary component has twice the output voltage gain, and the voltage stress of all power switches does not exceed the input voltage. However, more power switches are needed in this topology, and it does not have the ability of frequency doubling. At the same time, the switching frequency of the power switch is high and the switching loss is serious. In [19], a five-level inverter using coupling inductors is proposed, which can achieve five-level output using only four-switches. However, four independent diodes and two reverse polarity coupled inductors are also needed in this topology. As a result, the volume and cost of the inverter system are increased.

In this paper, a novel four-switch five-level inverter and its modulation strategy are proposed. Only one coupling inductor and two diodes are added to the proposed topology which is based on the H4 full bridge inverter. It is conducive to the reduction of inverter system volume and the improvement of efficiency that the number of components and gate driving circuit are reduced. A double frequency LPS-PWM modulation strategy combined level shift and phase shift modulation is designed. The strategy is easy to implement, and the equivalent switching frequency is doubled.

This paper is organized as follows: in the second part, the topology of the proposed four-switch five-level inverter is discussed in detail, the current ripple on the coupling inductor is calculated, and the multi-carrier level pulse width modulation technology for pulse generation by gate driving circuit is discussed. In the third section, three kinds of extended circuits are given. The comparisons between the proposed topologies and advanced topology are given in the fourth part. In the fifth part, the results and analysis are given. On the experimental platform based on STM32H750VBT6, the experiments are carried out to verify its performance. Finally, the conclusion is given in the sixth part.

II. FOUR-SWITCH FIVE-LEVEL INVERTER TOUPOLOGY

A. OPERATION PRINCIPLES

The topology of four-switch five-level inverter consisted of three legs B_1-B_3 is shown in Fig. 1. The switches S_1 on the leg B_1 and S_2 on the leg B_2 work at high-frequency PWM, and the switches S_3 and S_4 on the leg B_3 work at the fundamental

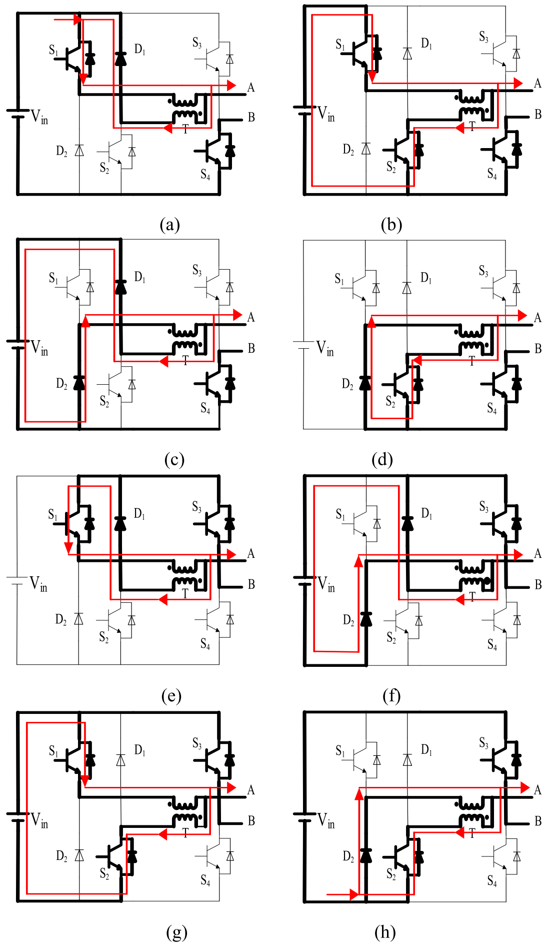

FIGURE 2. Operation modes. (a) State A, (b) State B, (c) State C, (d) State D, (e) State E, (f) State F, (g) State G, (h) State H.

frequency for voltage polarity reversal. The switching frequency of S_1 and S_2 is only half of the modulation frequency of the output sine wave. The end points of the upper and lower windings of the reverse polarity coupling inductor are respectively connected to the midpoint of the leg B_1 and leg B_2, and the freewheeling path is formed by diodes. It does not need to set the dead time for the high frequency leg, so that the reliability of the inverter system can be improved.

As shown in Fig. 2, all kinds of operation states of the four-switch five-level inverter are given.

State A: when the circuit is in the state shown in Fig. 2(a), the switches S_1 and S_4 are on, the upper winding current of the reverse polarity coupling inductor flows in through S_1, while the current of the lower winding flows out through D_1. Ignoring the forward voltage drop of diode D_1, the bus differential mode voltage V_{AB} is

$$V_{AB} = \mathrm{V_{in}} \tag{1}$$

At this time, the voltage stress of switches S_2, S_3 and diode D_2 are $\mathrm{V_{in}}$.

State B: when the circuit is in the second working state shown in Fig. 2(b), S_1, S_2 and S_4 are on, the upper winding

TABLE 1. Switching states of thr five-level invertor.

State	V_{AB}	S_1	S_2	S_3	S_4
A	V_{in}	1	0	0	1
B	$V_{in}/2$	1	1	0	1
C	$V_{in}/2$	0	0	0	1
D	+0	0	1	0	1
E	-0	1	0	1	0
F	$-V_{in}/2$	0	0	1	0
G	$-V_{in}/2$	1	1	1	0
H	$-V_{in}$	0	1	1	0

current of the reverse polarity coupling inductor flows in through S_1, and the lower winding current of the reverse polarity coupling inductor flows out through S_2. The bus voltage V_{AB} is

$$V_{AB} = \frac{V_{in}}{2} \tag{2}$$

In this state, the voltage stress of switch S_3 and diodes D_1 and D_2 are V_{in}.

State C: when the circuit is in the third working state shown in Fig. 2(c). S_4 is on, the upper winding current of the reverse polarity coupling inductor flows in through D_2, and the winding current under the reverse polarity coupling inductor flows out through D_1. Without considering the forward voltage drop of diodes, the bus voltage V_{AB} is

$$V_{AB} = \frac{V_{in}}{2} \tag{3}$$

At this time, the voltage stress of switches S_1, S_2 and S_3 are V_{in}.

State D: when the circuit is in the fourth working state shown in Fig. 2(d). S_2 and S_4 are on, the upper winding current of the reverse polarity coupling inductor flows in through D_1, and the winding current under the reverse polarity coupling inductor flows out through S_2. The bus voltage V_{AB} is

$$V_{AB} = 0 \tag{4}$$

At this time, the voltage stress of switches S_1, S_3 and diode D_1 are V_{in}.

States E, F, G and H are the four working states of the proposed topology when the output voltage level is in negative half cycle, corresponding to the four working states D, C, B and A respectively.

The corresponding relationship between the working state of four-switch five-level inverter and the switches is shown in Table 1. The switching frequency of S_1 and S_2 is half of the operating frequency of voltage level V_{AB}. Switches S_3 and S_4 used for symbol reversal work at the fundamental frequency, and the switching losses are neglected. Therefore, the total switching loss can be reduced. In the table, "1" indicates on and "0" indicates off.

B. CURRENT RIPPLE ON COUPLED INDUCTOR

The duty cycle of S_1 is d_1 and the duty cycle of S_2 is d_2. The input voltage V_{in} and the sinusoidal voltage V_0 output to the load can be regarded as ordinary step-down inverter when the inverter operates in continuous conduction mode. There are the following equations.

$$d_1 = \begin{cases} \dfrac{V_0}{V_{in}} & V_0 \geq 0 \\ 1 + \dfrac{V_0}{V_{in}} & V_0 < 0 \end{cases} \tag{5}$$

$$d_2 = 1 - d_1 \tag{6}$$

When the switches S_1 and S_2 are on at the same time, the voltage on the upper and lower sides of the coupling inductor both are $V_{in}/2$, and the current ripple is positive. When the switches S_1 and S_2 are off, the voltage on upper and lower sides of the coupling inductor are $-V_{in}/2$, and the current ripple is negative, so:

$$L\frac{\Delta i}{\Delta t} = \frac{1}{2}V_{in} \tag{7}$$

$$\Delta i_1 = \begin{cases} \dfrac{V_{in}d_2}{2Lf_s} & d_2 < 0.5 \leq d_1 \\ \dfrac{V_{in}d_1}{2Lf_s} & d_1 < 0.5 \leq d_2 \end{cases} \tag{8}$$

$$\Delta i_1 = \Delta i_2 \tag{9}$$

where L is the coupling inductance, Δi_1 and Δi_2 are the ripple current of i_1 and i_2 at the upper and lower sides of the coupling inductor, respectively. f_s is the switching frequency.

C. MODULATION STRATEGY

There are two kinds of multi-carrier PWM modulation methods: level shift pulse width modulation (LS-PWM) [24], [25] and phase shift pulse width modulation (PS-PWM) [26]. However, the inverter with redundant switching states cannot be modulated by these two modulation strategies. In [27], the LPS-PWM modulation method combining LS-PWM and PS-PWM is proposed, which is applied to a seven-level inverter. A kind of LPS-PWM modulation which is suitable for the proposed five-level inverter topology is designed in this paper.

The modulation strategy for the proposed five-level inverter is shown in Fig. 3. The voltage levels of carrier e_1 and e_3 are the same as the voltage levels of e_2 and e_4, respectively, but the phases of the two carriers at the same voltage level differ by π. The sinusoidal modulated signal waveform $e_s = A_{ref}\sin 2\pi f_{ref}t$ shares the same axis with these carriers. A_{ref} is the amplitude of the sinusoidal signal waveform $|A| < 2A_c$, and f_{ref} is the frequency of the sinusoidal signal waveform. According to the relationship between e_s and e_k(k = 1,2,3,4), the process of five-level modulation is divided into four sectors: $R_1 \sim R_4$, the state of two levels appears alternately in each sector.

In Fig. 3, when $e_s \geq e_2$, the switch S_1 is ON, when $e_s \leq e_1$, the switch S_2 is ON, when $e_s \geq e_4$, the switch S_1 is ON, when

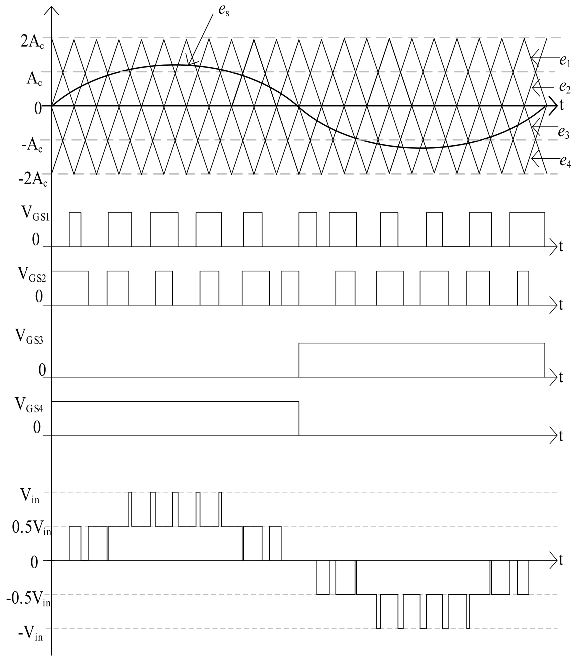

FIGURE 3. The modulation scheme of the proposed five-level inverter.

$e_s \leq e_3$, the switch S_2 is ON. The driving signals of switches S_3 and S_4 are fundamental wave.

The amplitude of the output voltage waveform V_0 is determined by the ratio of the amplitude of the reference sinusoidal signal waveform e_s and the amplitude of the carrier. Therefore, the modulation index M is defined as:

$$\mathrm{M} = \frac{\mathrm{A}_{ref}}{2\mathrm{A}_c} \tag{10}$$

III. EXTENDED TOPOLOGY

The basic unit of the four switch five level inverter topology shown in Fig. 1 can be extended in three different ways, which will be discussed below.

Extension I: As shown in Fig. 4, symmetrical capacitors and switches are added in the basic unit in this method. When a group of symmetrical capacitors and switches are added in the topology, the inclusion of a DC power supply increases the output voltage level by eight.

The total rated voltage of switching semiconductor devices in the topology can be reflected by the total standing voltage (TSV), it can be defined as

$$\mathrm{TSV} = \frac{\sum_{i=1}^{n} V_{b\_sw,i} + \sum_{j=1}^{m} V_{b\_d,j}}{V_{0\_\max}} \tag{11}$$

where $V_{b\_sw,i}$ and $V_{b\_d,j}$ represents the maximum shielding voltage of each switch and diode in the topology, respectively. V_{o_max} is the maximum output peak voltage.

The equation of switch number (N_{SW}), the number of drive circuits (N_{gd}), the number of capacitors (N_C) and the number of levels (N) expressions of multilevel topology are given, where k is a positive integer variable and the voltage at both

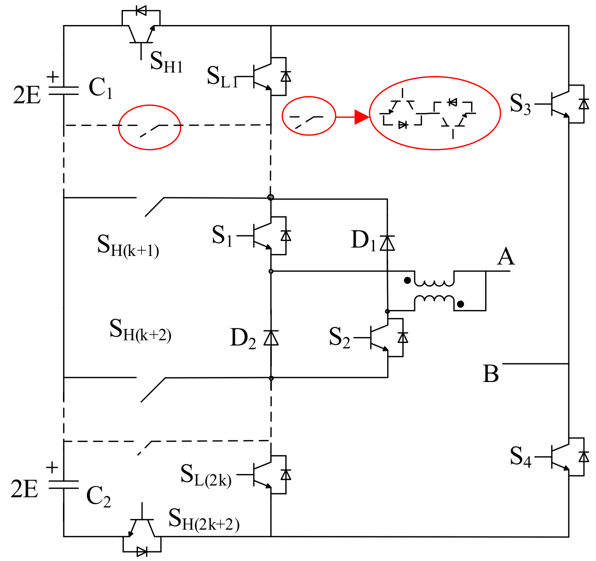

FIGURE 4. Extension I of the four-switch five-level inverter.

ends of each capacitor is 2E.

$$\left.\begin{aligned} \mathrm{N}_{sw} &= (6k+6) \\ \mathrm{N}_{gd} &= (4k+6) \\ \mathrm{N}_C &= (2k) \\ \mathrm{N} &= (8k+1) \end{aligned}\right\} \tag{12}$$

The TSV of each switch in the extended topology in Fig.4 can be calculated as

$$\left.\begin{aligned} \mathrm{V}_{S3} &= 4kE \\ \mathrm{V}_{S1} = \mathrm{V}_{D1} &= 2kE \\ \mathrm{V}_{SH(k+1)} &= 2kE \\ \mathrm{V}_{SH1} = \mathrm{V}_{SL_k} &= 2E \end{aligned}\right\} \tag{13}$$

Therefore, the total TSV of extension I is given as

$$\mathrm{TSV} = (2k^2 + 22k + 4)E = \frac{(2k^2 + 22k + 4)}{4k}\mathrm{V}_{\mathrm{in}} \tag{14}$$

Extension II: As shown in Fig.5, compared with extension I, a capacitor is added in this method.

In this extension, the number of the output voltage level increases by eight for each additional group of symmetrical capacitors and switches. The different equations of this topology shown in Fig. 5 are given as follow

$$\left.\begin{aligned} \mathrm{N}_{sw} &= (6k+6) \\ \mathrm{N}_{gd} &= (4k+6) \\ \mathrm{N}_C &= (2k+1) \\ \mathrm{N} &= (8k+5) \end{aligned}\right\} \tag{15}$$

The TSV of each switch in the extended topology in Fig.5 can be calculated as

$$\left.\begin{aligned} \mathrm{V}_{S3} &= (4k+2)E \\ \mathrm{V}_{S1} = \mathrm{V}_{D1} &= (2k+2)E \\ \mathrm{V}_{SH(k+1)} &= 2kE \\ \mathrm{V}_{SH1} = \mathrm{V}_{SL_k} &= 2E \end{aligned}\right\} \tag{16}$$

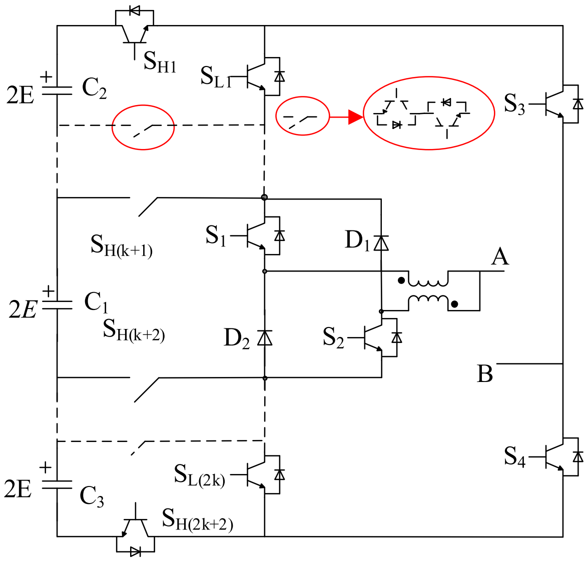

FIGURE 5. Extension II of the four-switch five-level inverter.

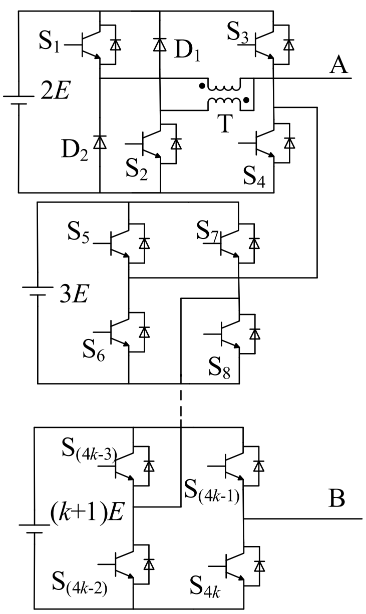

FIGURE 6. Extension III of the four-switch five-level inverter.

Therefore, the total TSV of extension II is given as

$$\mathrm{TSV} = (2k^2+22k+16)E = \frac{(2k^2+22k+16)}{4k+2}\mathrm{V_{in}} \tag{17}$$

Extension III: As shown in Fig. 6, different types of DC are added to the cascade expansion III according to the actual demand, the number of levels also varies greatly. When the type and number of DC both are k, there are the following relationships.

$$\left.\begin{array}{c} \mathrm{N}_{sw} = 4k \\ \mathrm{N_{gd}} = 2k+2 \\ \mathrm{N_{DC}} = k \\ \mathrm{N} = (k^2+3k+1) \end{array}\right\} \tag{18}$$

TABLE 2. Different equations of the proposed topologies.

Extension	N_{SW}	N_{gd}	N_C	N_{DC}
I	$\frac{3}{4}N+\frac{21}{4}$	$\frac{1}{2}(N+11)$	$\frac{1}{4}(N-1)$	1
II	$\frac{3}{4}N+\frac{9}{4}$	$\frac{1}{2}(N+7)$	$\frac{1}{4}(N-5)$	1
III	$4\sqrt{N+1.25}-6$	$2\sqrt{N+1.25}-1$	0	$\sqrt{N+1.25}-1.5$

The TSV of each switch in the extended topology shown in Fig. 6 can be calculated as

$$\left.\begin{array}{c} \mathrm{V}_{S(4k-3)} = \mathrm{V}_{S(4k-2)} = \mathrm{V}_{S(4k-1)} = \mathrm{V}_{S4k} = (k+1)E \\ \mathrm{V_{D1}} = \mathrm{V_{D2}} = 2E \end{array}\right\} \tag{19}$$

Therefore, the total TSV of extension III is given as

$$\mathrm{TSV} = (2k^2+6k+2)E = 4+\frac{4}{k^2+3k}\mathrm{V_{in}} \tag{20}$$

Three extensions of the proposed basic unit have been summarized in Table 2 with equations in terms of the number of levels N.

IV. COMPARATIVE STUDY

In order to evaluate the advantages and disadvantages of the proposed topology, the comparisons of the proposed topology and other recently reported five level inverters are given in Table 3. The comparisons include the number of power switches ($\mathrm{N_{SW}}$), the number of DC sources at the input side ($\mathrm{N_{DC}}$), the number of independent diodes ($\mathrm{N_d}$), the number of capacitors ($\mathrm{N_{cap}}$), the number of reverse polarity coupling inductors ($\mathrm{N_T}$) and the topological TSV.

The proposed topology has the same number of power switches as that in [19], however, the number of independent diodes and reverse polarity coupled inductors is half of that, so the proposed topology has advantages in volume and loss.

Compared with the five-level topology reported in [12]–[18], the proposed topology has less power switches and gate drive circuits. The TSV of the proposed topology is only larger than that of the topology proposed in [13] and [16]. However, the topology described in [13] and [16] does not have the ability of frequency doubling. Therefore, under the same output waveform quality, the high-frequency switching frequency of the topology introduced in this paper is only half of that in [14], so switching loss and electromagnetic interference caused by high switching frequency can be reduced.

The comparisons between Extension III and these topologies proposed in [28]–[34] have been given. As shown in Fig. 7, the curves that the number of switches, driving circuits and input DC voltage sources change with the increase of levels are compared respectively. The relationship between the number of switches and voltage levels is shown in Fig. 7(a). When the number of levels continues to increase, fewer switches are required in the proposed topology. The curves of required gate drive and the number of levels is shown in Fig. 7(b). Compared with other cascaded multilevel expansion, the proposed topology has less number of gate

TABLE 3. Comparison of key features between the new topology and the recently reported five-level inverter.

Ref.	N_{SW}	N_{DC}	N_d	N_{cap}	N_T	TSV
[12]	8	1	0	3	0	6
[13]	6	1	0	3	0	5
[14]	7	1	4	2	0	6.5
[15]	7	1	1	2	0	6
[16]	9	1	0	1	0	4.5
[17]	6	2	1	2	0	11
[18]	8	2	0	4	0	10
[19]	4	1	4	0	2	8
Proposed	4	1	2	0	1	6

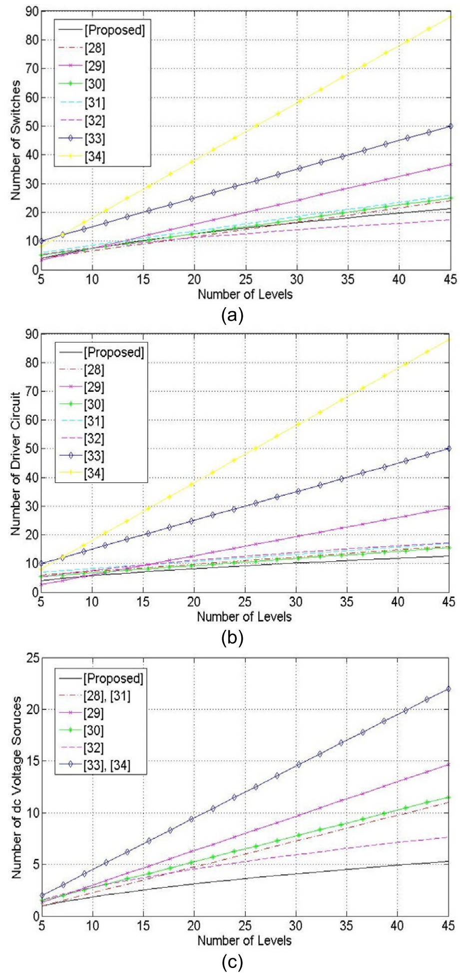

FIGURE 7. The relationships between the number of levels of expansion-III and (a) the number of switches, (b) the number of gate drive circuits and (c) the number of DC voltage sources.

drivers. Fig. 7 (c) shows the lower number of dc voltage source requirement of the proposed topology compared to other topologies.

In addition, the extension I and II of the proposed topology have been compared with several other expansion circuits introduced in other literatures in Fig. 8. The curves of the number of switches and the number of gate drives with the number of levels are shown in Fig. 8(a) and (b), respectively. It should be noted that the number of gate drives of the proposed topology is consistent with the number of the switches. When the number of levels continues to increase, the number of switches and gate drives required by the proposed topology is significantly less than that of other types of single source extended circuits. The curves of the number of capacitors with the number of levels are shown in Fig. 8(c), the results show that the proposed topology also has more advantages.

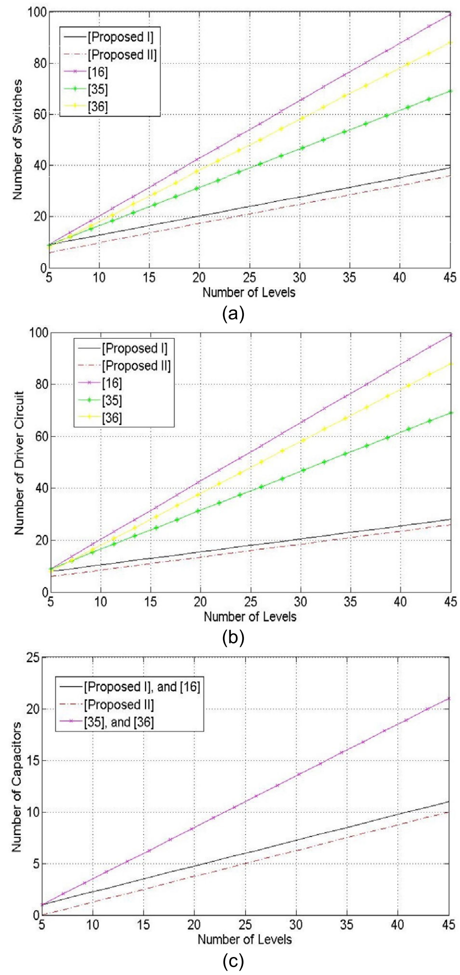

FIGURE 8. The relationships between the number of levels of expansion- I, II and (a) the number of switches, (b) the number of gate drive circuits and (c) the number of DC voltage sources.

V. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

As shown in Fig. 9, the MATLAB simulation model of 2kW four-switch five-level inverter is designed, where i and i_0 are the currents flowing through the output filter inductor and the load respectively. The simulation parameters of four-switch five-level inverter are designed in Table 4. According to the data sheet of R6030ENX, the conduction resistance r_{s1}-r_{s4} and drain-source capacitance C_{S1}-C_{S4} of MOSFET S_1-S_4 are determined. According to the data sheet of DSEI30,

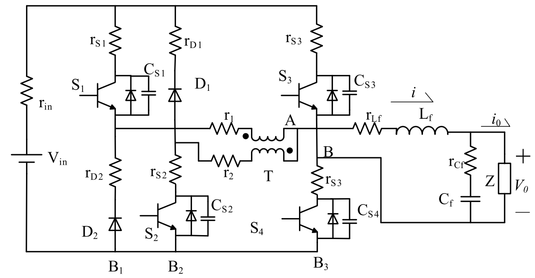

FIGURE 9. Simulation model of the proposed inverter.

TABLE 4. Simulation parameters of the proposed inverter.

Parameters	Value
Input Voltage V_{in}	320V(rin:50mΩ)
Modulation index M	0.9375
Output load Z	Z_1:22.5Ω Z_2:20.25Ω+31.22mH Z_3:20.25Ω+324.55μF
MOSFETs S_1-S_4	r_{S1}-r_{S4}:0.115Ω C_{S1}-C_{S4}:1900pF
Independent Diode D_1-D_2	V_F:1.01V r_{D1}-r_{D2}:7.1mΩ
Coupled Inductance L	2mH(r1-r2: 50mΩ)
Filter Capacitor C_f	16μF(r_f: 21.9mΩ)
Filter Inductor L_f	0.25mH(r_{Lf}: 20mΩ)
Switching Frequency f_s	16kHZ
Frequency of the sinusoidal signal waveform f_{ref}	50HZ

the conduction resistance r_{d1}-r_{d2} and the forward conduction voltage drop of independent diodes D_1-D_2 are determined.

The simulation results of the proposed inverter in unity power factor and non-unit power factor (i.e. cos $\varphi = \pm 0.9$) are shown in Fig. 10. The FFT analysis under different loads is shown in Fig. 11. The THD of the five-level differential mode voltage V_{AB} in Fig. 11(a) is 30.63%, and according to [37], the calculation expression of THD is described as.

$$\text{THD}, \% = \frac{57.7}{(\text{n}-1)\text{M}}, \% \tag{21}$$

where n is non-negative level count. Therefore, the voltage THD at the modulation index of 0.9375 is estimated as 30.77%, which is well agreed with the experimental results.

When the output load is Z_1, the output current is in phase with the output voltage. As shown in Fig. 10(a), the THD of the current output current and the output voltage are both 0.36%. The simulation results of V_0 ahead of i_0 (i.e. cos $\varphi =$ 0.9) is shown in Fig. 10(b) when the output load is inductive load Z_2. The THD of current output current and output voltage are 0.08% and 0.26% respectively. The THD of the output current in Fig. 10(b) is further reduced because the inductive load acts as a filter. In Fig. 10(c), the simulation results show that when the output load is capacitive load Z_3, V_0 lags i_0 (i.e. cos $\varphi = -0.9$). The THD of output current and output voltage are 0.46% and 0.42% respectively. The FFT of corresponding output voltage are shown in Fig. 10(b), (c) and (d) when the load is Z_1, Z_2 or Z_3.

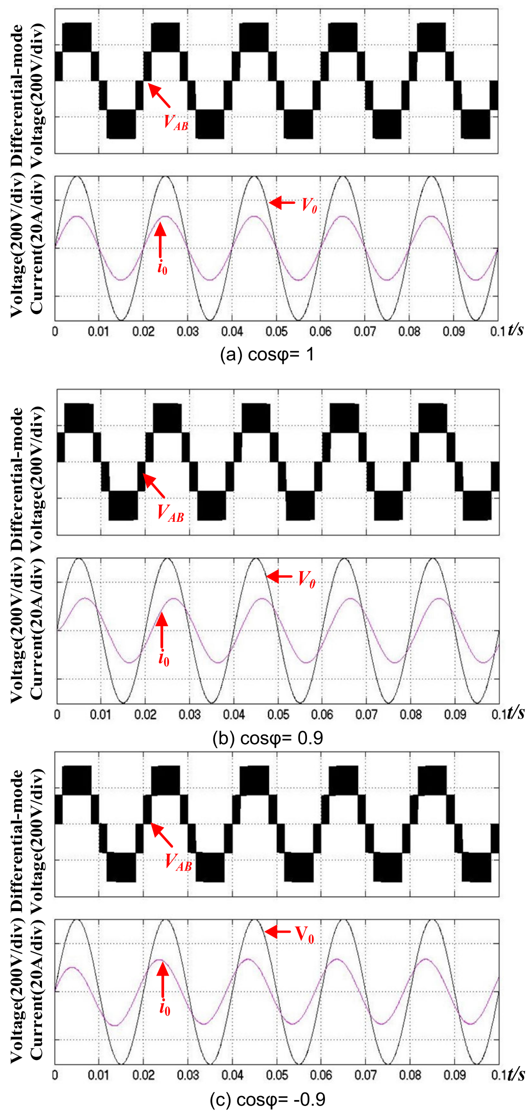

FIGURE 10. Simulation results of the reactive power adjustment capability of the five-level topology. (a) cosφ = 1. (b) cosφ = 0.9. (c) cosφ = −0.9.

Fig. 12 shows the key waveform of four-switch five-level inverter when a load is suddenly added. The waveform diagrams of differential mode voltage V_{AB}, output voltage V_0 and output current i_0 under the condition of sudden change from no-load to inductive load Z_2 are given in Fig. 12(a). The output voltage is stable and the output current can be smoothly transited. The current waveforms on the upper and lower sides of the reverse polarity coupling inductor and on the output filter inductor L are shown in Fig. 12(b). The leakage inductance current of the reverse polarity coupling inductor changes according to the sinusoidal law, the self-current balance on the leakage inductance is realized.

As shown in Fig. 13, the dynamic changes of M in the four-switch five-level inverter are listed when the load is

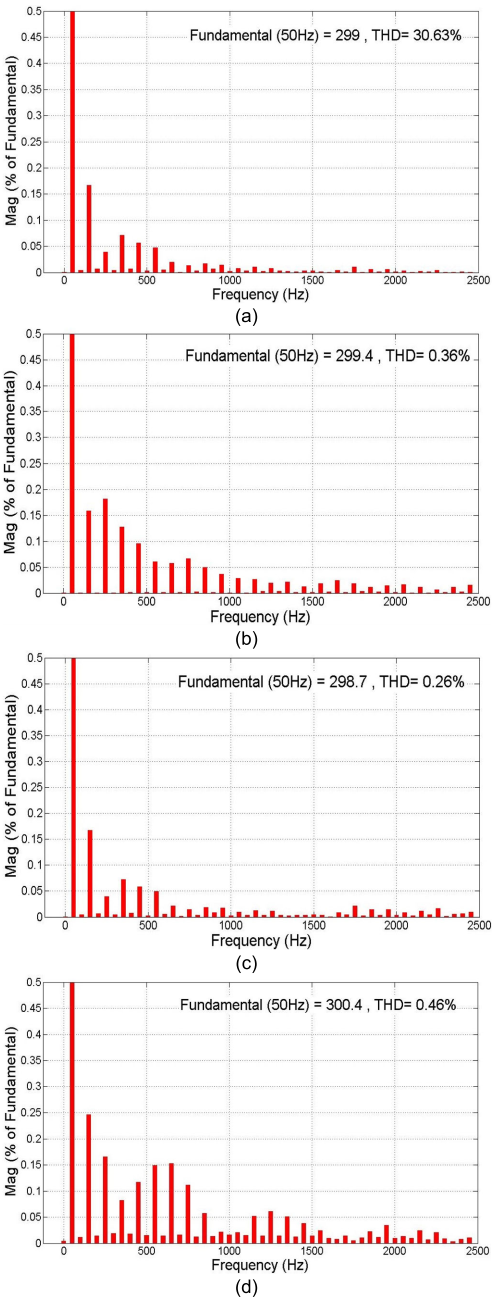

FIGURE 11. FFT of simulation results with (a) output five-level voltage V_{AB}. (b) output voltage V_0 with Z_1. (c) output voltage V_0 with Z_2. (d) output voltage V_0 with Z_3.

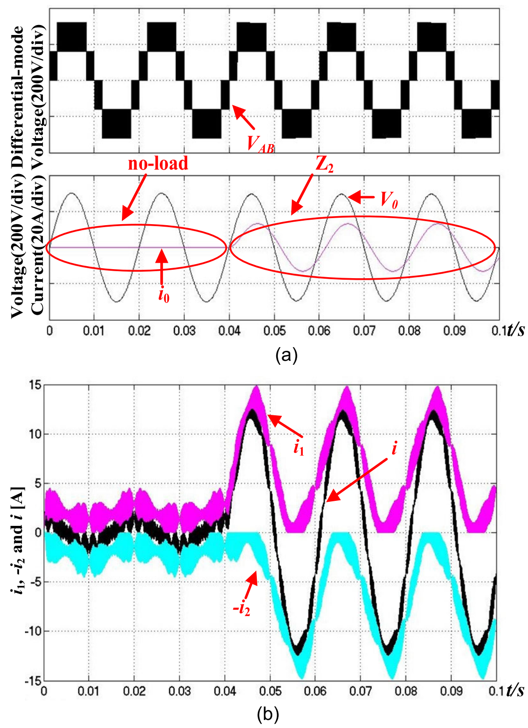

FIGURE 12. Simulation waveform when the load is suddenly changed. (a) Differential mode voltage V_{AB}, output voltage V_0, and current i_0 (b) current i_1, i_2, and i at unit power factor.

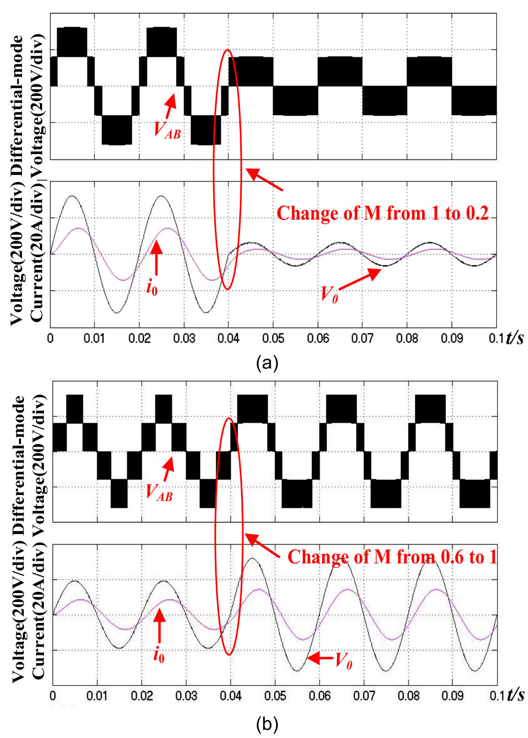

FIGURE 13. Simulation results of propose topology when M is changed from. (a) 1.0 to 0.2 (b) 0.6 to 1.0.

Z_2. In Fig. 13(a), the modulation index increases from 0.2 to 1, while in Fig. 13(b) the modulation index is reduced from 1 to 0.6. In Fig. 13(a), although the number of levels is reduced when the modulation degree is 0.2, the dynamic performance does not decrease.

The curve of output efficiency changing with power is shown in Fig. 14 when the output load is reduced from 450Ω to 9Ω. When the output power $P_0 = 1.11$kw, the maximum power conversion efficiency is 98.4%. The comparison curves of output voltage harmonic distortion rate between H4 full bridge inverter topology and proposed topology under different modulation index are shown in Fig. 15 when load is Z_1. When H4 full bridge inverter topology and proposed

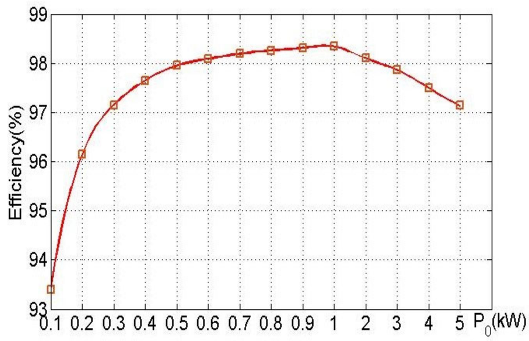

FIGURE 14. Efficiency of the proposed topology.

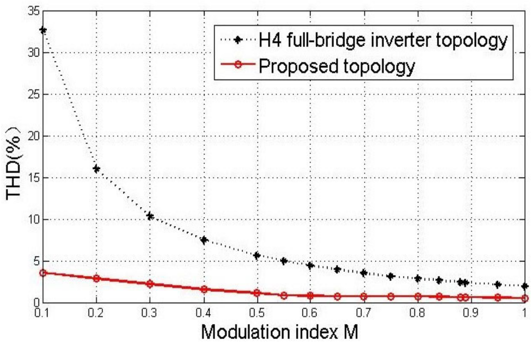

FIGURE 15. The THD comparison of H4 inverter topology and proposed topology.

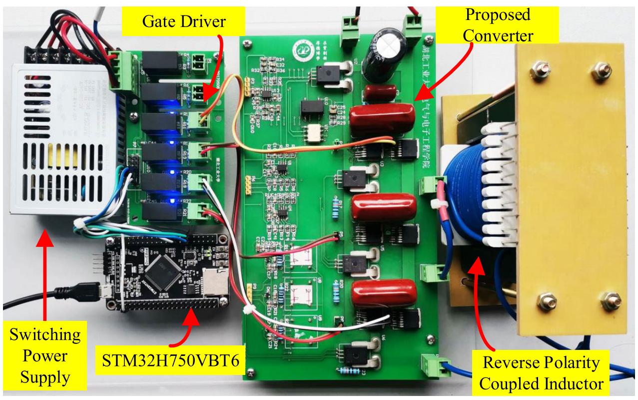

FIGURE 16. Hardware setup of the proposed inverter.

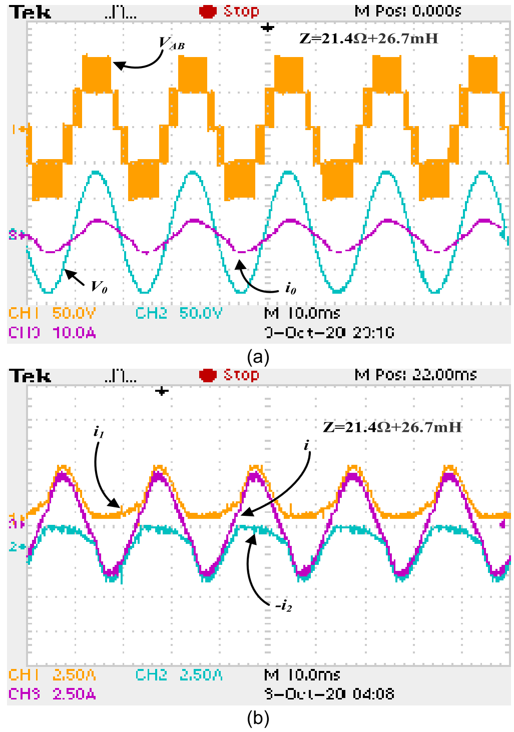

FIGURE 17. Experimental results of the proposed five-level inverter topology. (a) Differential mode voltage V_{AB}, output voltage V_0 and output current i_0. (b) Current on both sides of reverse polarity coupling inductor.

topology under the same switching frequency, same filter inductance and filter capacitor, the output voltage THD of the proposed topology is significantly lower than that of the common H4 inverter topology, which means that under the same input voltage and the same THD standard, the output voltage regulation range of the proposed topology is wider than that of the H4 inverter topology.

B. EXPERIMENTAL RESULTS

In order to verify the correctness and feasibility of the proposed five-level inverter topology and the modulation strategy, as shown in Fig. 16, a small experimental prototype based on STM32 microprocessor was built. The control of the system is realized by STM32H750VBT6 single chip microcomputer. The DC side voltage is 100V, the AC side voltage peak value is 88V (50Hz), the load $Z = 21.4\Omega + 26.7$mH, the filter inductance is 1.1mH, and the filter capacitance is 8μF. The reverse polarity coupling inductor adopts double winding in parallel, the leakage inductance is 4.35μH, the magnetizing inductance is 2.38mH, and the switching frequency is 8kHz.

The experimental results of four-switch five-level topology are shown in Fig. 17. As shown in Fig. 17(a), the output voltage level, filtered output voltage and output current waveform of the inverter system are presented. It should be noted that the output current i_0 is slightly distorted due to the saturation of the load inductance. The current waveforms of the upper and lower sides of the reverse polarity coupler are shown in Fig. 17(b). Because of the unidirectional current conduction of diodes D_1 and D_2, the current i_1 and $-i_2$ are unipolar, and the changes of current i_1 and $-i_2$ are consistent with the theories.

The experimental results of four-switch five-level topology with dynamic modulation in inductive load are shown in Fig. 18. In Fig. 18(a), the modulation index is reduced from 0.9 to 0.2, while in Fig. 18(b) the modulation index increased from 0.6 to 0.9. When the modulation index is dynamic, the waveform of output voltage and output current are smoothly, which means the dynamic performance is good. The experimental results when the load is suddenly changed are given in Fig. 19. The experimental results when the load is suddenly

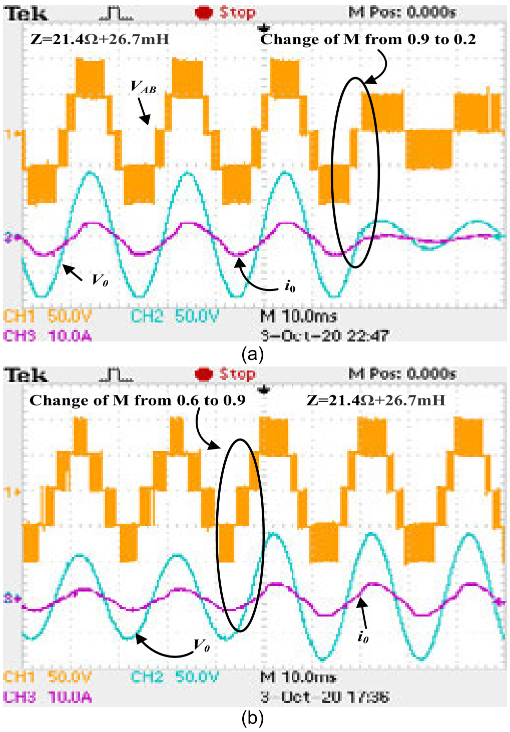

FIGURE 18. Experimental results of propose topology when M is changed from. (a) 0.9 to 0.2 (b) 0.6 to 0.9.

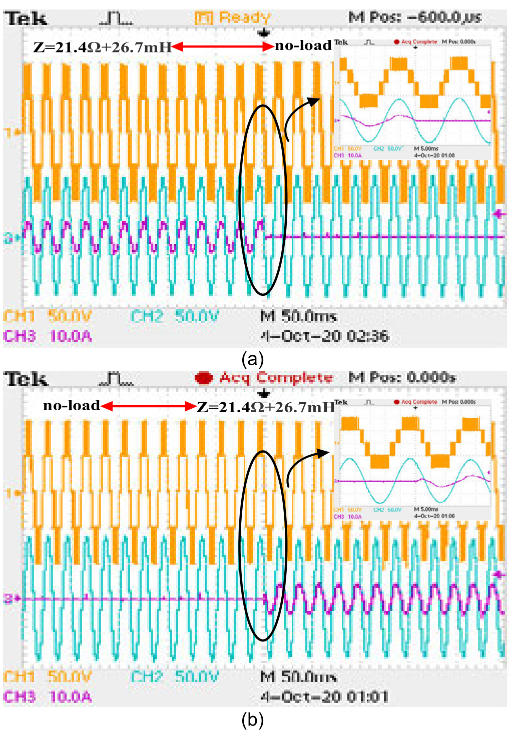

FIGURE 19. Experimental waveform when the load is suddenly changed, (a) the load is suddenly increased. (b) the load is suddenly reduced.

changed to no-load are shown in Fig. 19(a). Fig. 19(b) shows the experimental results when the load is suddenly added, and the experimental waveform is consistent with the simulation.

VI. CONCLUSION

This paper presented a novel five-level inverter topology with frequency doubling and expansion capability. The operation principle, the modulation method, analysis of the voltage stress on the coupling inductor, the comparison, simulation and experimental results of the three kinds of extended topologies are given. The number of components of the proposed five-level inverter is less than that of other five-level topologies. Because of the frequency doubling ability of the proposed topology, the switching loss is further reduced. In the simulation, the power loss analysis has been carried out, and the maximum efficiency of the proposed five-level topology reaches 98.4% when the output power is 1.1kW. In addition, three different multilevel extension circuits which have certain advantages in the number of devices are presented based on the proposed topology. In the simulation and experiment, the circuit has been confirmed by inductive load. It should be noted that the output current of the experiment is slightly distorted due to the saturation of the load inductor. In addition, the experimental results are completely consistent with the simulation results when the modulation index changes or load is suddenly changed.

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