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A Body Channel Communication Technique Utilizing Decision Feedback Equalization

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ABSTRACT This article presents the body channel communication technique that first adopts decision feedback equalisation. For the first time, we characterised post-cursor intersymbol interference of a single-bit pulse response of a human body channel for decision feedback equalisation achieving the first body channel communication faster than 100 Mb/s. In the proposed technique, an 8-tap decision feedback equaliser is utilised at the receiver to compensate for intersymbol interference of the body channel. The experimental results show that the proposed prototype transceiver achieved the highest data rates of 150 Mb/s and 10 Mb/s along 20-cm and about 100-cm body channels, respectively. Compared to the previous best result measured for the same body-channel distance of about 100 cm, the data rate is improved by ten times, showing that the proposed technique can significantly increase the speed of body channel communication.

INDEX TERMS Body-channel communication (BCC), decision feedback equalization (DFE), human-body communication (HBC), intra-body communication (IBC), wireless body area network (WBAN).

I. INTRODUCTION

Wireless body area networks (WBANs) refer to heterogeneous networks composed of computing devices such as wearables or implantable biomedical devices for applications dedicated to the human body [1]–[3]. In the earliest IEEE WBAN standardisation [4], the target applications were initially centred around low-power medical [5]–[8] and healthcare systems [9]–[11]. Nowadays, many other applications emphasise data rate and energy efficiency, rather than power consumption [2]; for instance, consumer electronics for entertainment purposes [3] (e.g., wearable audio player [12], wearable VR/AR [13], real-time multiplayer gaming platforms [14]), and context-aware environment (e.g., ambient intelligence [15]). To satisfy the requirements for these high-end applications (beyond 100 Mb/s data rate), the recent research focus is on improving communication systems' performance.

Body-channel communication (BCC) – synonymously known as human-body communication (HBC), which uses the human body as a signal-transmission medium, is now a widely-accepted physical layer (PHY) owing to its superiority in terms of power consumption and data rate [16]. Following the first successful BCC implementation using an IC chip [17], researchers have developed many more BCC transceivers with advanced schemes [16]–[29]. In general, two approaches have been investigated in designing BCC transceivers: RF communication and digital baseband

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communication. For instance, RF BCC transceiver [24] has achieved a maximum data rate of 80 Mb/s at the total energy cost of 78.8 pJ/b based on a dual-band BPSK modulation. An example which uses digital baseband communication is the work that applies Walsh coding [25] aiming to make the best use of available human-body channel bandwidth as efficiently as possible; this transceiver has achieved a maximum data rate of 60 Mb/s at the energy cost of 181 pJ/b. In general, transceivers that use RF modulation schemes tend to be bulkier (e.g., 5.76 mm^2 [24]) due to their high implementation complexity. In contrast, digital transceivers have simpler architectures and require less chip area (e.g., 1.122 mm^2 [26]), but achieve slightly lower data rates. However, the achievable data rates, energy efficiency, and hardware costs of the state-of-the-art transceivers are not yet sufficient for high-end applications.

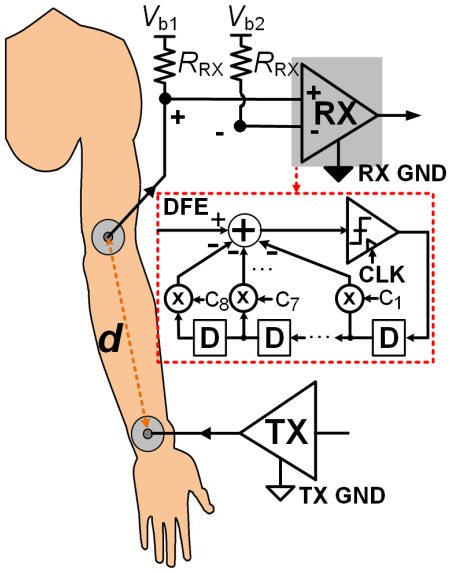

FIGURE 1. DFE-based BCC Transceiver. TX drives the human body via an electrode. Data signal passes through a human-body channel with the transmission path distance *d*. RX implements decision feedback equalisation to recover transmitted data. RX bias voltages V_{b1} and V_{b2} are applied externally with RX input impedance R_{RX}. Note the two separate reference grounds for TX and RX.

This work presents a BCC transceiver that significantly improves data rate and energy efficiency by adopting an equalisation technique. First, the time-domain channel pulse response was simulated using the *S*-parameters extracted from frequency-domain measurement. By thoroughly analysing the obtained channel information, it was found that the human-body communication (HBC) channel showed similar characteristics with ac-coupled interconnects such as transmission lines on FR4 boards [30]–[32] for high-speed chip-to-chip serial communications. Using this result, we designed and tested a BCC transceiver, which employs an equalisation technique typically implemented for high-speed serial links or optical communications – decision feedback equalisation (DFE). The proposed BCC transceiver exploits capacitively-coupled digital baseband communication with an analogue equalisation at the receiver (Figure 1). Comparisons with galvanic coupling BCC (GC-BCC), and the justifications of capacitive coupling BCC (CC-BCC) will be discussed in Section II. The transmitter (TX) is a simple inverter-based voltage-mode source-series terminated (SST) driver, whereas the receiver (RX) is a full-rate, resistively-loaded, current-summing, 8-tap decision-feedback equaliser.

The transceiver, fabricated in 65-nm CMOS technology, achieved the highest data rate of 150 Mb/s (16.6 pJ/b) along a 20-cm-long body channel, and also offered reliable operation at 100 Mb/s (23.5 pJ/b) over an arm-to-arm transmission ($d \sim 1.0$ m). For both modes of operation, the minimum achievable BER was 10^{-6}.

The paper is organised as follows. Section II describes and gives implications of the measured frequency- and time-domain characteristics of an HBC channel. Section III presents the proposed BCC TRX. Section IV describes the use of the fabricated chip for BCC implementation. Section V gives and discusses the implementation results. Finally, Section VI concludes the paper.

II. HUMAN-BODY COMMUNICATION CHANNEL

In a realistic BCC scenario, the TX and RX must have their own separate floating reference grounds, which should also be fully isolated from the earth ground. In other words, the return path should be closed through the environment, and not through the earth-grounded equipment. Therefore, throughout the experimental procedures, external earth-ground loops must be avoided absolutely, because they lead to invalid measurement results. Extensively investigated in the previous study [33], signals feeding through return paths provided by the external earth-ground loops cause significantly increased channel gain. Some of the earliest work [17] did not take the ground isolation into consideration, and hence obtained invalid frequency-domain measurements; for instance, the transmission gain across a 15-cm channel on the human forearm showed only about ∼6 dB attenuation [17], which is a greatly deviated value compared to one measured with the proper experimental setup that has accounted for ground decoupling (25-30 dB) [24]. For all experimental procedures in our work, ground isolation was achieved using appropriate methods, which will be explicitly described accordingly.

The target channel was the human body with attached Ag AgCl electrodes (3MTM Red DotTM 2239) separated by distance d = 20cm/≈100cm (Figure 1). Capacitive-coupling approach, i.e., a single signal electrode for TX and RX individually, was selected for the least transmission loss [34], [35]. The counterpart to the capacitive approach, commonly referred to as galvanic coupling (two electrodes), offers better environmental resilience at the cost of increased signal attenuation. The signal transmission path is fully confined by the human body between the TX and RX signal electrodes, whereas the return path is closed through the surrounding environment. To select an optimal signalling scheme and a TRX topology for the target HBC channel,

the channel's frequency and time-domain characteristics were carefully analysed.

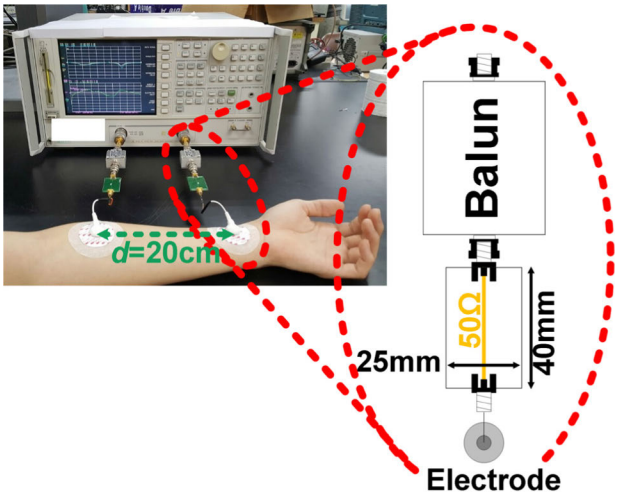

FIGURE 2. Frequency-domain human body channel characteristics measurement setup.

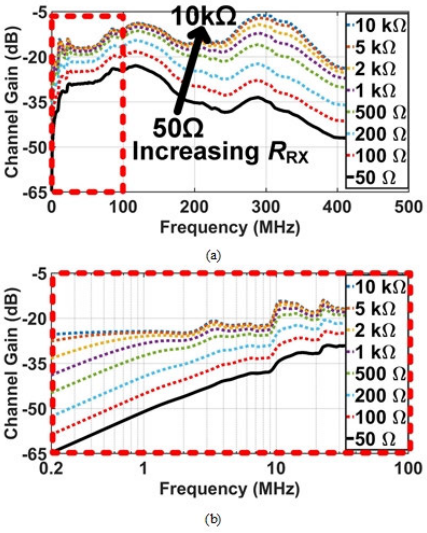

FIGURE 3. Simulated HBC channel gain vs. frequency for various R_{RX}: (a) linear 200 kHz ≤ f ≤ 500 MHz; (b) semi-log 200 kHz ≤ f ≤ 100 MHz. Black solid line: measured S_{21} parameter; coloured dashed-lines: simulated channel gains with increasing R_{RX}.

A. FREQUENCY-DOMAIN CHARACTERISTICS

The frequency-domain characteristics of the HBC channel were obtained using a network analyser (HP8753ES, Hewlett Packard Inc.). The measurement setup (Figure 2) was similar to the one in [35], except that the utilised ground-decoupling balun transformers (FTB-1-1, Mini-Circuits Inc.) had wider bandwidths of 200 kHz to 500 MHz. Two identical PCBs, each of which had a 50 Ω transmission line, resembled a TX and an RX [36], [37]. The electrodes with snap wires were connected to the 50 Ω transmission lines of the PCBs whose grounds were deliberately left floating (capacitive coupling). Calibration was performed to de-embed undesired properties such as the 50-Ω transmission line and parasitic elements of the transformers. The electrodes were included in the target HBC channel characteristics, and thus not de-embedded because they are part of the channel in the realistic scenario. However, the electrode lead wires were unavoidably included in the measured network S parameters in addition to the target HBC channel characteristics; de-embedding of these properties requires further studies to extract the HBC characteristics exclusively.

The results shown in Figure 3 were measured based on the experimental setup illustrated in Figure 2. The S-parameters extracted with 50-Ω R_{RX} are shown as the black solid line, and were loaded onto Spectre, from which S_{21} for different R_{RX} were simulated (dashed lines). The extracted S-parameters were used as the basis for transceiver simulations.

The HBC channel transmission gain H(f) across the frequency range of 200 kHz ≤ f ≤ 500 MHz (Figure 3a) showed an overall band-pass nature: a DC-blocking region, a relatively flat band for f < 150 MHz, and a gradual low-pass zone beyond 150 MHz. The capacitive elements of the human body [38] and the capacitive return path together give rise to the DC-blocking property just as in high-speed AC-coupled interconnects [30], [31]. Due to the series RC connection through the human body's capacitive elements, and the RX termination impedance R_{RX}, the cut-off frequency of the DC-block region decreased as R_{RX} increased (Figure 3b). The band-path region of H(f) increased with R_{RX} [26]. This can be interpreted as the voltage division between R_{RX} and other impedances $Z_{other}(f)$ such as electrodes and the human body:

$$H(f) = 20\log\left|\frac{R_{RX}}{R_{RX} + Z_{others(jf)}}\right| \quad (1)$$

For R_{RX} < 1 kΩ, $Z_{other}(f)$ is dominant in (1), and thus $H(f)$ is approximately linearly proportional to R_{RX}. As R_{RX} gets increased further, it becomes the dominant term, thus reducing the effect of the proportional increment of $H(f)$, until it gets saturated at R_{RX} of 10 kΩ. Above R_{RX} of 2 kΩ, peaking at around 20 MHz was observed, which corresponds to complex intersymbol interference (ISI) in time-domain. Figure 4a shows how S21 varies with increasing d. A significant change occurred between d = 30 cm and about 100 cm, because the longer transmission path includes the torso of the human subject. Figure 4b describes the S21 measured under three different coupling configurations. The experimental setup for galvanic coupling was replicated from [35] using the same PCBs (Figure 2), with the electrode pitch of about 5 cm. As discussed earlier, the S21 with PCB ground connection creates an earth-ground loop and gives completely invalid results. Capacitive-coupling electrode configuration shows a better performance than galvanic configuration, confirming the previous studies [33]–[35] and our choice. However, since the return path is formed by capacitive coupling between the device ground planes, it is imperative to carefully consider the impacts of the return path for overall BCC performance.

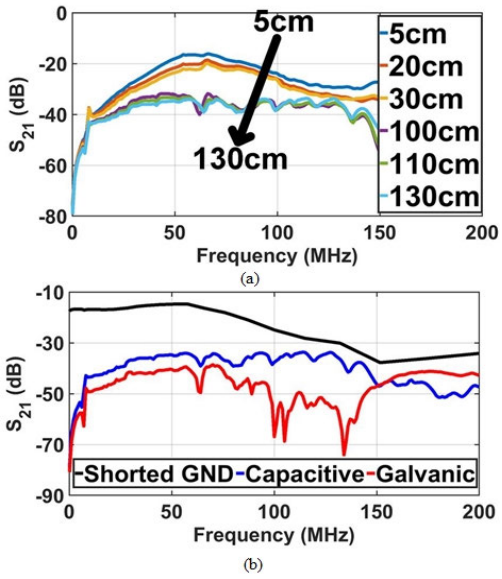

FIGURE 4. Measured S_{21} vs frequency with (a) various d in capacitive coupling; and (b) three different electrode cconfigurations for $d \approx 100$ cm.

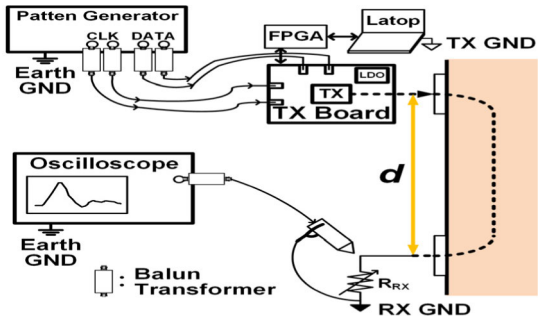

FIGURE 5. Single-bit pulse response measurement setup.

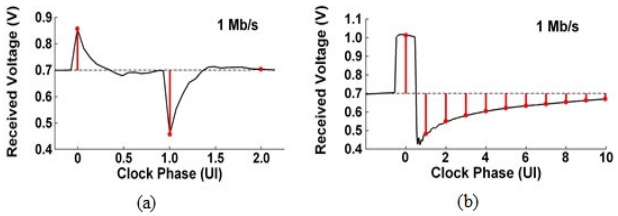

FIGURE 6. Single bit pulse responses of a 20-cm human body channel (a) with, and (b) without ground isolation. The transmitted pulse width is 1μ s, which corresponds to 1 Mb/s BCC. R_{RX} of 1 k Ω is used. DC bias voltage of 0.7 V is shown.

These considerations include the sizes of the ground planes, the distance between the ground planes, and environmental factors.

Note that for both results shown in Figure 3 and 4 were obtained with R_{RX} of 50 Ω, because the PCBs we designed (Figure 2) for frequency characteristics measurement had 50 Ω transmission lines, for matching with the termination impedance of the balun transformers. Mismatched impedances will give rise to the inclusion of unwanted characteristics.

B. TIME-DOMAIN CHARACTERISTICS

Unlike the frequency-domain measurements, there has been hardly any attempt to measure time-domain characteristics of the HBC channel because most of the previous BCC TRXs use RF schemes, in which the bandwidth availability is the primary concern. For DFE-based TRXs, however, time-domain information, especially the pulse-response, is critical to examine and assess the significance of ISIs.

For the first time, the time-domain properties of the HBC channel were characterised for decision feedback equalisation by measuring single bit pulse responses (SBPRs) under various conditions. Because no available equipment can solely satisfy the ground isolation requirements, i.e., high-speed equipment's chassis is always earth-grounded strictly for safety reasons, we used our fabricated TRXs and customised PCBs to measure SBPRs (illustrated in Figure 5). A single bit pattern "…00100…" was produced and fed into the TX by a pattern generator (GB1400-TX, Tektronix Inc.); all output ports of the pattern generator were connected to the TX board through ground-decoupling balun transformers. While the TX periodically transmits a 1-UI-wide pulse, the received waveforms were measured using an oscilloscope at human body channel distances of 20 cm and about 100 cm. Note that the probe to the oscilloscope input port is also connected via a balun transformer (with probe ground lead connected to the RX ground). The measurement without ground isolation gave a wholly different and invalid response compared to the measurement with ground isolation, proving the importance of ground isolation (Figure 6).

With ground isolation, SBPRs (Figure 7) were measured for various pulses whose widths (data rate) range from 100 ns (10 Mb/s) to 5 ns (200 Mb/s). The measured SBPRs showed the properties of the DC-blocking, the low-pass filtering, and irregularly uneven time-domain ISIs. At low speed (1 Mb/s), the SBPR in Figure 6a clearly showed the typical DC-blocking nature: a positive peak at the rising edge of the transmitted pulse, followed by a negative peak at the falling edge of the transmitted pulse; each peak resembles pulse signal through a series capacitor. As the pulse width (the corresponding data rate) was reduced from 1 μs (1 Mb/s) to 100 ns (10 Mb/s), the separated two peaks gradually got closer until they became overlapped (Figure 7b), after which the trailing post-cursors of the second peak started to dominate. As the pulse width was reduced to 6.67 ns, or equivalently as the corresponding data rate was increased to 150 Mb/s, the uneven in-band region of the frequency response caused the irregularly shaped post-cursor ISI (Figures 7c-d). This post-cursor ISI can be compensated by DFE as long as the number of post-cursor ISI taps does not exceed the DFE tap count. At a data rate of 150 Mb/s or below, significant post-cursor ISI taps were within eight taps of the SBPRs (Figure 6a) and Figures 7a-d), suggesting that an 8-tap DFE

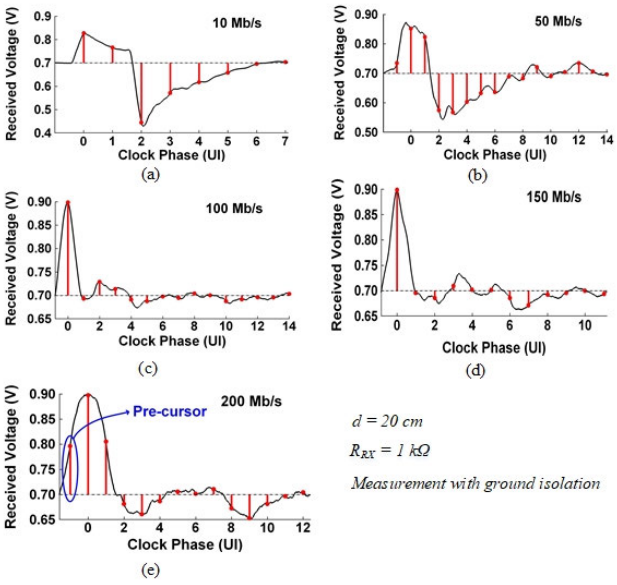

FIGURE 7. Human body channel's responses to single bit pulses whose widths (the corresponding data rates in BCC) are (a) 100 ns (10 Mb/s), (b) 20 ns (50 Mb/s), (c) 10 ns (100 Mb/s), (d) 6.67 ns (150 Mb/s), and (e) 5 ns (200 Mb/s), respectively. The channel distance is 20 cm. R_{RX} of 1 k Ω is used. DC bias voltage of 0.7 V is shown.

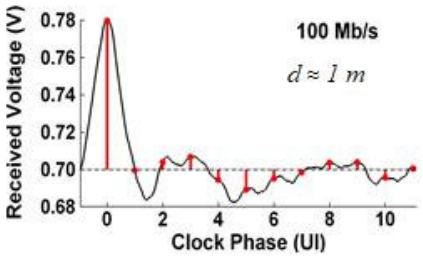

FIGURE 8. An about 1-m human body channel's response to a single bit pulse whose width is 10 ns, which corresponds to 100 Mb/s BCC. R_{RX} of 1 k Ω is used. DC bias voltage of 0.7 V is shown.

can enable 150 Mb/s BCC though the 20-cm body channel. At a higher data rate of 200 Mb/s (Figure 7e), the 9th and higher post-cursor ISI taps of the SBPR became not ignorable, implying that 200 Mb/s BCC requires more than eight DFE taps. In addition, it was interesting to observe a large pre-cursor of the SBPR at 200 Mb/s (Figure 7e), which cannot be compensated by DFE. Based on the time-domain SBPR measurement (Figure 7), we decided to implement an 8-tap DFE to target 150 Mb/s through a 20-cm body channel. Similarly, SBPR at the ∼100 cm channel (Figure 8) showed that an 8-tap DFE could achieve 100 Mb/s through an about 100-cm human body channel. Note that the measured raw SBPRs have zero DC voltage, as the signals were measured with an oscilloscope with baluns. The DC voltage of 0.7 V shown in Figures 6-8 was to reflect the bias voltage at the RX inputs (Figure 1), which was present *de facto*. This RX bias voltage is required for the proper operation of the RX main amplifier (Section III.C).

To summarise, we have extracted the frequency-domain S parameters for the frequency range of 250 kHz to 500 MHz, with which the transceiver was simulated and designed accordingly. Moreover, we have characterised time-domain pulse responses of the human body communication for the first time. The time-domain single-bit pulse responses were used as the basis for DFE tap coefficients (described in Section IV). All experiments were performed with careful experimental setup designs to provide isolated floating ground references (described in Section IV).

III. TRANSCEIVER DESIGN

A. DECISION FEEDBACK EQUALISATION

Previously reported BCC transceivers adopted either RF modulation [16], [20]–[24], [28] or digital baseband signalling [17]–[19], [25], [26], [29] without significant compensation for channel distortion, by assuming relatively flat frequency band. RF-based TRXs modulate data onto the flat frequency bands. Assuming that the channel has a narrow bandwidth, BW, the theoretical data rate would be limited to η·BW, where η (bit·s^{-1}·Hz^{-1}) is the spectral efficiency of the modulation scheme. For example, the RF TRX [24] has achieved 80 Mb/s at most with two 40 MHz bands by exploiting BPSK, which has η of 1 bit·s^{-1}·Hz^{-1}. However, the performance is severely limited by the in-band distortion for a long channel because the exploited RF schemes have all assumed an ideally flat frequency band. In addition, the high complexity of the circuit for narrowband modulation requires significant power consumption [24].

In contrast to the RF TRXs, the digital baseband TRXs have mostly utilised the wider baseband. In reality, however, the mid-band channel is not flat, which is the main reason for the degradation of TRX performance. A simple analogue equaliser has been used [26] to compensate for high-frequency path loss to expand usable bandwidth. However, the benefit is severely limited due to its poor capability of equalising the complex characteristics (Figure 7 and Figure 8) of the HBC channel. For example, a typical analogue equaliser [14] cannot compensate for all the irregularly shaped ISIs (Figure 7d) due to its limited degrees of tuning freedom. Moreover, while the galvanic-coupling implementation gives resilience to environmental changes, due to increased attenuation TRX in [29] reports successful communication only at a 1 cm channel.

All previous research works have assumed a relatively flat frequency band at which communications are achieved. As a result, the performance was severely limited; in fact, hardly any work has ever attempted significantly to restore in-band distortions to efficiently expand usable bandwidths. DFE, which is well known for its supreme channel flattening capability, can therefore be used to compensate for the non-flat band of the HBC channel to a great extent [27]. We, for the first time, employed DFE to a BCC TRX to compensate for the in-band channel distortion.

Typically, DFE is implemented at RX actively to compensate for ISI caused by an uneven frequency response of

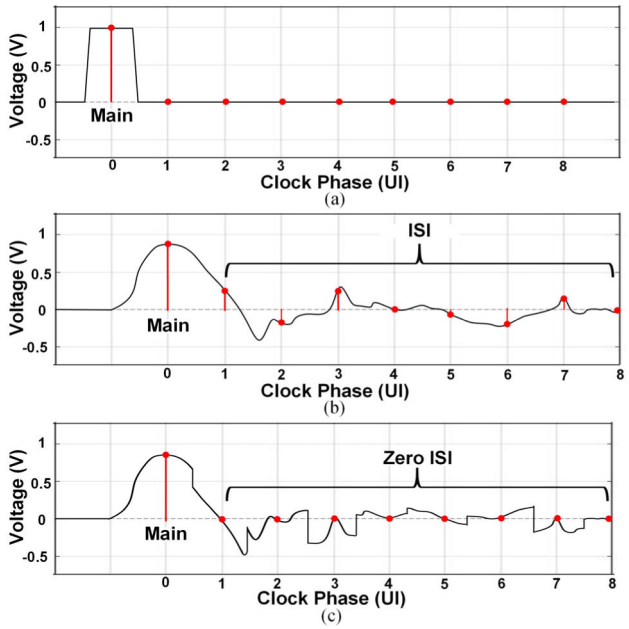

FIGURE 9. Example (a) transmitted, (b) received, and (c) after-DFE pulses for transmission of the isolated one-bit pattern: "…0001000…".

the channel. A simple block diagram of DFE is depicted in Figure 1, and the simulated waveforms are plotted in Figure 9. In time-domain, the non-flat band appears as post-cursor ISIs, which limit the performance. Even though the transmitted pulse is a clean one unit-interval (UI) square pulse (Figure 9a), the received pulse (Figure 9b) has many post-cursor ISIs due to channel distortion. Decision errors are simply unavoidable as trailing ISIs from previously transmitted data interfere with current (and future) signals. DFE improves communication performance by actively cancelling these ISIs based on the previous bit decision. Assuming that DFE properly cancels ISIs, the slicer output is the correct decision bit (Figure 1). A series of flip flops delay the correct bits (representing '1' or '−1') by multiples of the symbol interval. Each bit of the sequence corresponds to the polarity of the corresponding ISI tap that must be cancelled by DFE (Figure 9b). These bits are multiplied by the DFE coefficients that correspond to the ISI tap values (Figure 9b), and then are subtracted from the incoming signal by the summer (Figure 1). After the summer, the output signal is, in principle, ISI-free (Figure 9c), and thus the following slicer can correctly determine the received bits as initially assumed. As a result, DFE effectively eliminates ISIs and improves data rates significantly.

B. TRANSMITTER CIRCUIT

The TX (Figure 10a) is a voltage-mode non-return-to-zero (NRZ) driver, whose driving strength can be digitally controlled by an inverter driver and source-series terminated (SST) driver banks. The TX consists of 40 SST drivers and one inverter DRV1 with a huge driving strength. The driver's impedance can be controlled from 25 Ω to 1 kΩ.

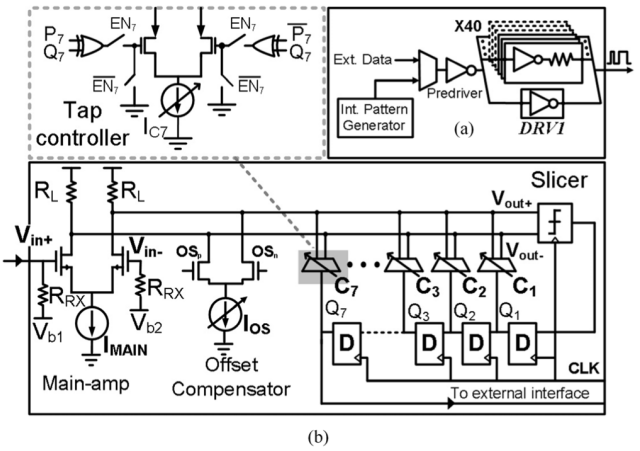

FIGURE 10. Schematics of the proposed (a) voltage-mode TX; and (b) DFE RX.

The PMOS and NMOS of SST drivers were sized such that the pull-up and pull-down resistances were 10% of the series impedance (1 kΩ) to preserve linearity. The purpose of the configurable output driving strength is to account for variations between human subjects (channel adaptability), and to find optimal driving strength required for minimum power dissipation.

The TX sends out a non-return-to-zero (NRZ) binary digital data directly onto the body. The DC components contained in NRZ data would be eliminated entirely after passing through the human body (Figure 3). However, the loss of DC information is irrelevant to receiver operation and, therefore, does not require special attention here.

Our design complies with the safety standard, which is introduced by the International Commission on Non-Ionizing Radiation Protection (ICNIRP) and the IEEE International Committee on Electromagnetic Safety [39]–[41]. These standards provide regulatory guidelines on human exposure to electric, magnetic, and electromagnetic fields in the RF regime based on potential tissue-heating effect. The external fields produced by electronic devices induce an electrical current in biological tissues, which can cause tissue heating. The restriction imposed for our frequency band-of-interest (150 MHz) is stated in a localised specific absorption rate (SAR) of 2 $W{\cdot}kg^{-1}$ and 4 $W{\cdot}kg^{-1}$ for general public exposure around for head and extremities, respectively [40]. However, in the case of BCC, wherein the current is directly applied to the tissue via electrodes, incident power density would be the more appropriate metric than SAR. The power density safety level, computed based on SAR, is stated as 10 $W{\cdot}m^{-2}$ [41] at our frequency of interest. With the 3M 2239 electrode having a sensor area of 2.45 cm^2, the maximum incident power would be 2.45 mW. We performed simulations using the measured S-parameter model of a human body channel (Figure 3) to examine if the TX meets the safety limitations. The simulated average incident powers across all configurations of our TX fall below 2.45 mW, confirming the safety (Figure 11). Note that this value does not

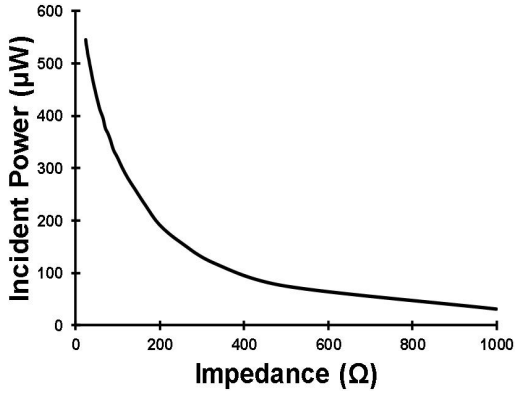

FIGURE 11. Simulated incident power to the human body versus different TX driving impedances.

consider the locations on which electrodes are placed. A more rigorous model of the whole body would provide localised power in particular areas on the body. Moreover, no results have shown evidently harmful biological effects besides the tissue-heating effect, which is why the safety requirement in these types of wearable devices is less stringent than in implantable medical devices.

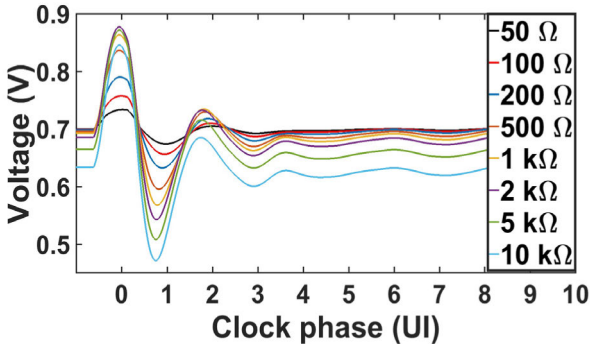

FIGURE 12. Simulated SBPRs at 100 Mb/s for R_{RX} 50Ω to 10 k Ω.

C. RECEIVER CIRCUIT

The number of DFE taps and the RX termination impedance R_{RX} were co-optimised. As observed in frequency-domain characteristics (Figure 3) of the human-body channel, R_{RX} affects both the transmission gain and the flatness of the frequency response [26], associated with the required DFE tap count. In this design, the DFE tap count was determined by an evaluation based on time-domain channel simulations for various R_{RX} values using the S-parameters extracted from the frequency-domain measurement (Figure 3). Simulated SBPRs at 100 Mb/s for several R_{RX} values (Figure 12) describe two things: the received voltage increase as R_{RX} increase, confirming the investigation in [26]; and as also examined in equation (1), R_{RX} above 1 kΩ also complicates post-cursor ISIs due to the introduced peaking (Figure 3). Therefore, R_{RX} imposes the trade-off between the signal amplitude and the post-cursor ISIs. The ideal eye height

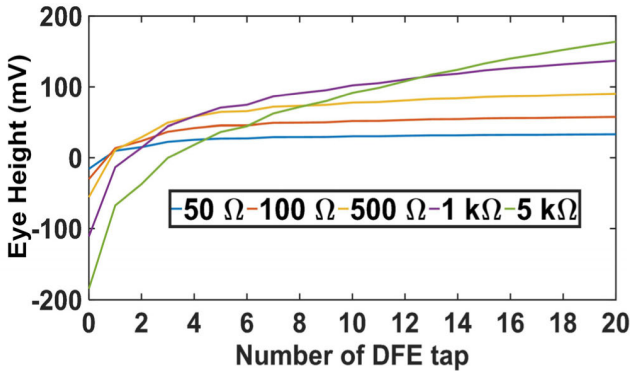

FIGURE 13. Eye height versus number of DFE taps for R_{RX} 50Ωto 5 kΩ.

(Figure 13) versus DFE tap counts was calculated using the optimal DFE tap coefficients that were mathematically computed from Figure 9 using the method in [42]. The required number of DFE taps increases with R_{RX} due to the increased complexity of the post-cursors ISI profiles. Considering the trade-off and hardware costs, an eight-tap DFE with R_{RX} of 1 kΩ was chosen to be implemented. Of course, by simply adding more number of DFE taps, the performance can be further enhanced. However, only insignificant improvement is expected (Figure 13). The proposed BCC TRX (Figure 1) therefore, exploits a capacitively-coupled 8-tap DFE RX terminated with 1 kΩ.

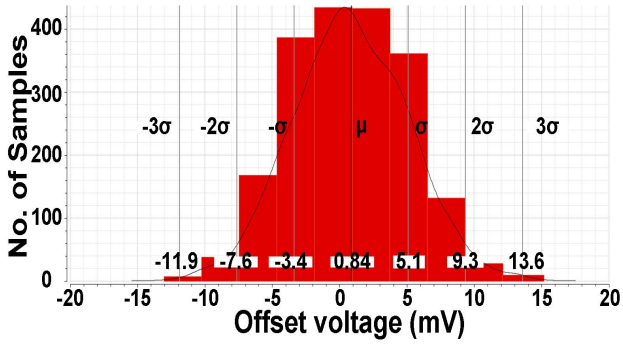

FIGURE 14. Comparator (slicer) Monte Carlo simulation results. μ = 0.84 mV, σ = 4.2 mV, N = 2000.

The RX circuit (Figure 10b) is a full-rate, resistively-loaded, current-summing, 8-tap decision-feedback equaliser. The RX consists of a main amplifier, an offset compensator, a sense amplifier, a DFE retimer, and tap controllers. The main amplifier sets up the main cursor current, while also amplifying the received voltage with a gain of about two. The offset compensator cancels slicer offset errors caused by transistor mismatch, and also enables the *in-situ* measurement of eye diagram [43]. The strong-arm sense amplifier makes decisions based upon the summed (equalised) differential voltages. The Monte Carlo simulations confirm practically tolerable designs within mismatch and process variations (Figure 14). Typical master-slave D-flip flops are used as the

DFE retimer. The currents can be tailored according to the shapes of pulse responses at a particular data rate. The DFE taps are designed such that the coefficients can be configured ranging 200% of the required range in simulation using the measured channel characteristics. Lastly, the polarity of the i^{th} tap is digitally controlled by the exclusive-or logic function of polarity input Pi and the delayed-decision bit Qi. Whenever not used, taps are turned off completely by feeding '0' to the enable inputs ENi, instead of setting the tail current to '0' which would have caused unwanted currents to flow by the NMOS differential pair and the parasitic capacitors at the drain nodes of the tail current sources.

D. PERIPHERALS

The peripheral blocks of the chip include a 96-bit snapshot, a digital scan I/O, an internal pattern generator, and data buffers. The snapshot takes a 'snapshot' of a consecutive 96-bit sequence of the internal pattern generator (TX) or sliced data (RX). The scan I/O block allows the bidirectional flow of control bits. The internal pattern generator has two functionalities: user-defined programmable data pattern which can be invoked once or rotated continually, and a pseudo-random-bit-sequence generator (PRBS31). The data buffer interfaces the recovered data of the RX to an external environment, e.g., error detector equipment or CDR. The peripheral circuit blocks serve as configuration and test blocks that do not affect the transceiver core operation.

IV. IMPLEMENTATION

BCC Implementation of the fabricated transceiver requires (1) essential prerequisites preceding the main experiment, and (2) conducting the main experiment.

A. EXPERIMENTAL PREREQUISITES

Prerequisites for the main experiment include chip fabrication and packaging, full-custom PCB design, and preparation of a proper experimental setup.

1) CHIP FABRICATION AND PACKAGING

To prove the concept of BCC exploiting DFE, the proposed TRX was fabricated in 65-nm bulk CMOS technology. Figure 15 shows the micrograph of the fabricated chip with the layout of the TRX. The TRX core measured 5600 μm^2, of which the TX driver core and the RX DFE core occupied about 3500 μm^2 and 2100 μm^2, respectively. The fabricated chip was packaged with chip-on-a-board (COB) technology.

2) PCB DESIGNS

The PCB designs (Figure 16) must fulfil the ground isolation and high-speed signal integrity requirements. Two separate on-board low-dropout (LDO) regulators (TPS7A88, Texas Instrument Inc.) were included as isolated power sources for the TX and RX boards, respectively, to avoid using earth-grounded power supply units. LDO regulators are powered from USB ports of two battery-powered laptop computers. Whenever earth-grounded high-speed equipment made

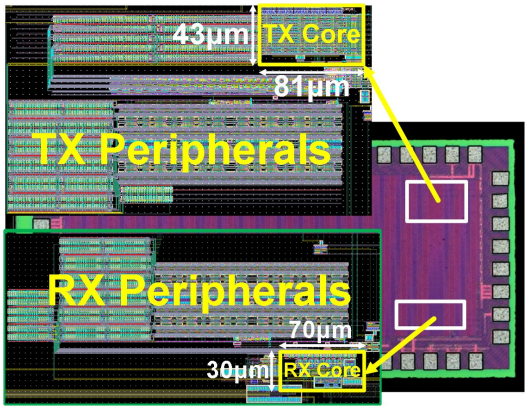

FIGURE 15. Chip micrograph (1 mm × 2 mm) of the DFE BCC TRX. TX core occupies 3500μ m^2; RX core occupies 2100μ m^2.

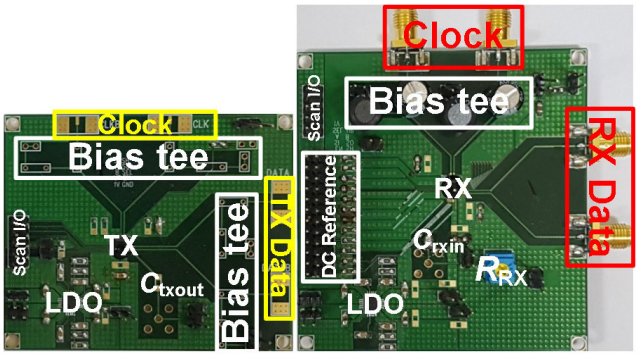

FIGURE 16. BCC PCB implementation of (a) TX (21 cm^2); and (b) RX (49 cm^2). Two separate LDOs are used as isolated power sources. On-board bias tees ensure CML voltage swing for data and clock inputs.

connections (e.g., clock or data) with the boards, the balun ground decoupling transformers were used. As the fabricated chip required CML-level voltage swings of 0.5-1.0 V for clock and data inputs, an on-board bias tee was implemented.

As the target data rate of the proposed transceiver was about 100 Mb/s regime, a special effort was required in designing the custom PCBs. Four-layer FR4 PCBs with ENIG surface were fabricated. The 50-Ω differential transmission lines had widths of 0.356 mm (14 mils) with the stated PCB specification. The ground copper planes of the TX and RX were 70 mm × 30 mm, and 70 mm × 70 mm, respectively.

B. EXPERIMENT SETUP

The aspects of the experimental setup (Figure 17) involve ground isolation, equipment management, transceiver configurations, and handling of the human under test. First, two separate laptops controlled firmware of FPGAs independently for TX and RX to ensure ground isolation. Throughout the experimental procedures, the laptops operated with batteries, i.e., should not be ac-powered. A GPIB/LAN gateway (Agilent E5810B, Agilent Technologies Inc.) provided remote access of equipment through a wireless network.

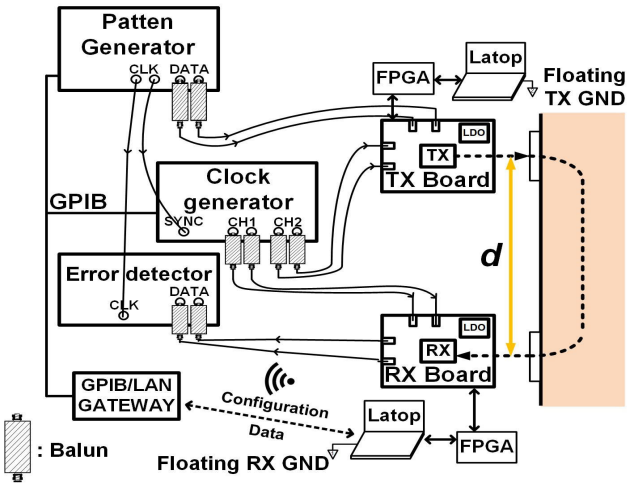

FIGURE 17. Overall experiment setup to achieve ground isolation. TX and RX boards have LDOs for isolated power supply. Balun transformers are used whenever the boards are driven with output ports of high-speed equipment. GPIB/LAN gate way sets up an internal wireless network for configuring and acquiring data from the equipment.

Using the internal network, the laptops configured and acquired data from the equipment using the IEEE-488 Standards (GPIB). The differential DATA outputs of the pattern generator (GB1400-TX, Tektronix Inc.) were used as the TX data. The CLK output was used as a reference clock source of an error detector (GB1400-RX, Tektronix Inc.), and the CLK_BAR output was used as a synchronisation clock of a pattern generator (81134A, Agilent Technologies Inc.), from which the transceiver clocks were driven. The pattern generator 81134A provided delay control (1-ps resolution) between the two available channels, by which the phases of TX and RX clocks were adjusted.

The transmitter configuration includes the number of drivers to be enabled and the selection of data source (internal or external pattern generator). The receiver configurations involve RX bias voltages, control of DFE tap currents and corresponding polarities, and an offset current. The digital control bits were configured using a serial scan I/O block. The RX bias voltages and DFE tap currents were adjusted by external DACs.

C. BCC EXPERIMENT

The main BCC experiment was divided into three stages: *in-situ* mapping of receiver input-referred voltage, application of particle-swarm-optimisation (PSO) algorithm for tap coefficient optimisation, and an eye diagram measurement. Before the main experiment, we performed a safety experiment.

1) SAFETY EXPERIMENT

A safety limit test was first performed for the BCC TX with a real human subject. The primary safety concern for these types of wearable devices (and other NFC devices) is associated with the possible tissue-heating effect caused by a current induced by electric fields produced by the devices. In the cases of BCC, however, an electrical current is directly applied to the body. Therefore, the safety guideline set by ICNIRP in terms of power and power density would be more appropriate than SAR to assess safety in BCC. It is worth mentioning that since the BCC frequency response is attenuative, the power is maximum at the TX. To check whether the proposed TX satisfies the safety limit, the incident power localised on the electrode area was estimated by measuring the difference in current consumptions of the TX with and without the electrode attachment on the human arm (Figure 18). In the test, the maximum incident power (power density) of the TX was measured approximately 300 μW (1.18 W·m^2) satisfying the safety limit of 10 W·m^{-2}, which was discussed in Section III.B.

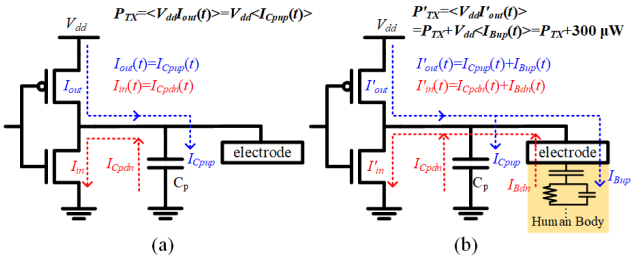

FIGURE 18. An indirect safety verification method to estimate TX incident power by measuring TX's power consumption (a) without, and (b) with attaching the electrode to the human body. TX's incident power is less than the power consumption increments with electrode attachment: P'_{TX}- P_{TX} = 300 μW; < · > is the operator of time average.

There are, however, some caveats in the estimated power density. First, it does not consider the positions on which the electrodes are attached in the body. For example, more stringent safety requirement should be set near the head area. Second, the estimate merely gives an averaged value over the total electrode area. Therefore, it must be ensured that the localised power at any points in the electrodes should be below the safety limit. Lastly, the measured power does not indicate the worst-case value. The proposed TX can inject a huge amount of current into the human body in case the TRX grounds become shorted. While it is highly unlikely for shorting of TRX grounds to occur (as TX and RX are distant), it is still necessary to be aware of this issue to prevent the worst-case scenario from happening at all. Considering all these caveats collectively, future studies should look into the safety requirement further.

2) IN-SITU MAPPING OF RX INPUT-REFERRED VOLTAGE

To perform *in-situ* mapping of RX input-referred voltage, Vin+ of the receiver was swept from 0.5 V to 0.9 V for a fixed Vin- of 0.7 V (i = 1 to n; where n depends on incremental step sizes). For each i^{th} Vin+ voltage iteration, the DAC voltage that controls offset compensator current was swept (j = 1 to m). With the slicer output connected to GB1400-RX, BERs were measured for all combinations of V^i_{in+} and $V^j_{DAC,offset}$. A BER of 0.5 would indicate that

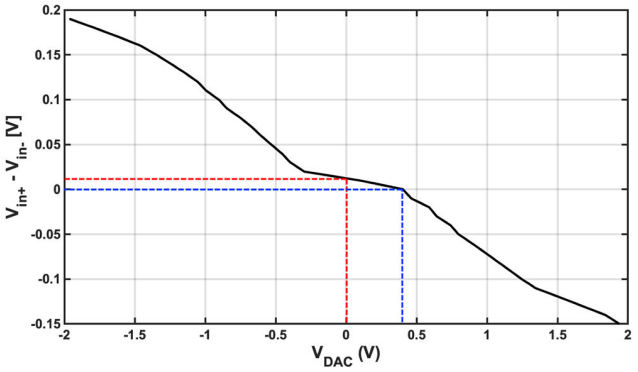

FIGURE 19. Input-referred differential voltage mapping for slicers. The slicer has an input-referred offset error of ∼12 mV; The offset error is compensated at V_{DAC} of ∼0.4 V.

Vin+ is equal to Vin- (0.7 V), i.e., the input-referred differential voltage is 0 V. Completing all combinations of iterations, we obtained a matrix that maps input-referred differential voltages to the offset compensator DAC voltages. Figure 19 shows the input-referred differential voltage (Vin^+ -Vin^-) versus the DAC voltage V_{DAC}. Using this mapping matrix, we were able to compensate for a slicer offset error, and an *in-situ* eye diagram was measured.

3) PARTICLE SWARM OPTIMISATION FOR DFE COEFFICIENTS

Coarse DFE tap coefficients were initially obtained from the pulse response at a particular target data rate and channel distance. These coefficients may not be of optimal values, and therefore to enhance the robustness of the transceiver, we used an optimisation routine based on the particle swarm optimisation (PSO) algorithm [44]. PRBS data were invoked and transmitted through the human body at the chosen d. At the fixed offset current, at which the slicer error was corrected, the RX clock phases were adjusted. For each clock phase iteration, BER was measured. Therefore, for a given particle (tap coefficient combinations), a horizontal bathtub curve was measured. The PSO was allowed to run until the particles approximately converged to one position, at which the eye width would be the maximum. This procedure was repeated once for the target data rate of 150 Mb/s at $d = 20$ cm, and another for the data rate of 100 Mb/s at $d = \sim 1.0$ m.

4) IN-SITU EYE DIAGRAM MEASUREMENT

An input-referred eye diagram was measured using the optimised combinations of the DFE tap coefficients (and corresponding tap currents). The process is essentially similar to the one performed for PSO. The eye height was determined by changing the offset current DAC voltage. For each vertical sweep point, the RX clock phase was adjusted. For all sets of swept VDAC/phase combinations, BER was measured. Using the mapping table obtained earlier, we measured the complete *in-situ* eye diagram.

V. IMPLEMENTATION RESULTS

We have demonstrated that the DFE technique would be applicable for BCC implementation with our proposed transceiver. Eye diagrams (Figures 20a and 20c) of the BCC TRX were measured *in-situ* for the first time in this work while communicating at 150 Mb/s through a 20-cm-long human limb (Figure 19b), and at 100 Mb/s through an about 100-cm arm-to-arm body channel. The recorded eye heights and widths (Figure 19d) at BER $< 10^{-6}$ were 35 mV and 0.17 UI ($d = 20$ cm); and 45 mV and 0.22 UI ($d \approx 100$ cm). The TX driver core operating at 150 Mb/s and 100 Mb/s consumed 0.49 mW and 0.35 mW respectively, whereas the RX DFE core consumed about 2.0 mW regardless of the data rate; this corresponds to total TRX core energy costs per-bit of 16.6 pJ/b (150 Mb/s @ $d = 20$ cm) and 23.5 pJ/b (100 Mb/s @ $d \approx 100$ cm). For both modes of operation, the measured BER was 10^{-6}. It is worthwhile mentioning that without DFE enabled, no successful communications at these high data rates were viable, i.e., completely closed eye diagrams.

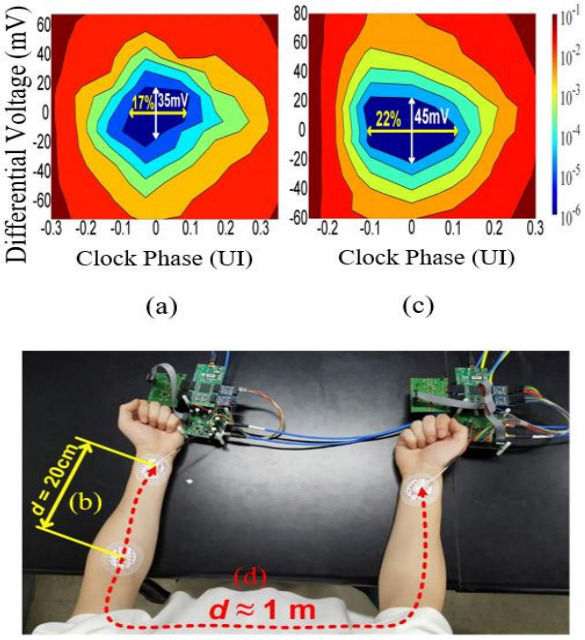

FIGURE 20. Eye diagrams measured *in-situ* (at the RX electrode) and the measured human body channels; (a) eye diagram measured at 150 Mb/s for (b) a 20-cm human arm channel. (c) eye diagram measured at 100 Mb/s for (d) an about 1-m human arm-to-arm channel.

Compared with prior implementations, our experimental results clearly showed that the proposed DFE technique can greatly improve BCC. Our experimental results are summarised and compared with other works in Table 1. The proposed TRX is the first BCC TRX utilizing DFE, and achieved 150 Mb/s, which is the fastest data rate reported to-date. Compared with the previous record (100 Mb/s) [29], which employed galvanic coupling, the proposed TRX improved the maximum data rate by 1.5 times with the 20-fold increase in the test channel distance. Slightly lower data rates of 80 Mb/s

TABLE 1. System summary and comparison to other designs.

	[18][a]	[20][b]	[26][a]	[24][c]	[28][a]	[29][b]	**This work[a]**	
Technology [nm]	180	180	65	65	65	180	**65**	
Scheme	Capacitive + 3-Level PPM	Capacitive + AFH-FSK	Capacitive + 3-Level Walsh Code	Capacitive + Coherent BPSK	mHBC + OOK	Galvanic + Bipolar RZ	**Capacitive + DFE**	
Channel Distance [cm]	25	180	-	-	150	1	**20**	**≈ 100**
Max. Data Rate [Mb/s]	10	10	60	80	5	100	**150**	**100**
Power [mW]	2.6	4.6	10.87	6.3	0.059	3.155	**2.49[d],[e]**	**2.35[d],[f]**
Incident Power [mW]	-	-	-	-	-	-	**< 0.30**	
Energy/bit [pJ/b]	260	460	180	78.8	11.9	31.55	**17[d]**	**24[d]**
Bit Error Rate	10^{-4}	10^{-5}	10^{-5}	10^{-5}@40Mb/s	-	10^{-9}	**10^{-6}**	**10^{-6}**
Eye Height (mV)	-	-	-	-	-	1000[g]	**35[h]**	**45[h]**
Eye Width (UI)	-	-	-	-	-	0.79[g]	**0.17[h]**	**0.22[h]**
Sensitivity [dBm][i]	-	-65 @ 10^{-5}	-58 @ 10^{-5}	[j]-40 @ 10^{-5}	-56[k]	[l] @ 10^{-9}	**-30 @ 10^{-6}**	
Area [mm^2]	2.0	2.30	1.12	5.76	0.12	1.258	**0.00558[d]**	

[a]Human subject; [b]Bionic arm; [c]Subject unspecified; [d]TRX datapath only; [e]TX Power of 0.49 mW; [f]TX power of 0.35 mW; [g]recovered data eye diagram; [h]RX input-referred eye diagram; [i]at specified BER; [j]40 Mb/s; [k]unspecified BER; [l]unspecified sensitivity

and 60 Mb/s with capacitive coupling have been demonstrated in [24] and [26], respectively. However, channel distances are not clearly reported [24], [26]. Because ISI and the channel attenuation greatly increase with the channel distance, the performance difference would be much larger if similar channels were used in these works. For more fair comparisons, we also compared the proposed TRX with the prior works [18], [20] that were measured for similar channel distances. Although a slightly shorter 20-cm channel is used in this work, the maximum data rate of 150 Mb/s in this work is fifteen times as fast as the data rate of 10 Mb/s achieved in [18]. For similar about 100-cm-long channels, the proposed TRX achieved 100 Mb/s, which is ten times as fast as the data rate of 10 Mb/s reported in [20]. These results show that DFE has the potential to enable breakthrough improvement in BCC performance. One last thing to mention is that our design (and as most baseband-based BCC) has low sensitivity compared to the RF-based BCC because the performance of our design is mostly limited by ISIs caused by channel distortion rather than by low SNR as in RF circuit design. Despite the low sensitivity, our design has achieved reliable communication with BER of 10^{-6}.

VI. CONCLUSION

The first body channel communication technique utilising DFE was presented. To exploit DFE in BCC, the post-cursor ISI of a single bit pulse response of human body channels has been characterised and analysed in detail for the first time in this work. Based on this analysis, an inverter-based TX and an 8-tap DFE RX were implemented in 65-nm CMOS technology. The proposed DFE-based BCC TRX has achieved maximum data rates of 150 Mb/s and 100 Mb/s while communicating over the 20 cm and about 100 cm human-body channels, respectively. The achieved data rate of 150 Mb/s is about 1.5 times as fast as the previous record, even with a ∼20-fold channel distance. Compared with the prior arts measured for similar distances, our work has achieved substantial improvements in data rates (15 × @ d ≈ 20 cm and ∼10 × @ d ≈100 cm). The implementation results show that the DFE technique, which has been exploited for the first time, could be the key enabler of a BCC transceiver that operates at several hundreds of megabits per second for many innovative body-area network applications, including, for instance, on-body ultra-definition-video streaming, real-time gaming, and many others.

Further improvement is possible in the future. First, the pulse response above 200 Mb/s (Figure 7e) suggests that the data rate can be improved by increasing the number of DFE taps and adopting a few-tap feed-forward equalisation (FFE) to account for pre-cursor ISI. Second, many existing techniques can be borrowed from wireline communication or more advanced communication systems for efficient channel adaptation and equalisation: for example, sign-sign least-mean-square algorithm in adaptive high-speed wireline transceivers, or pilot symbol-based channel estimation from advanced communication technologies like OFDM. Third, because our transceiver used a simple non-return-to-zero (NRZ) scheme for data transmission, i.e., uncoded signalling that contains dc components, employing encoding schemes with suppressed dc components such as Manchester coding or 8b/10b coding would enhance the data rate further. Moreover, safety issues in terms of potential electrode dissolution due to unbalanced can be resolved by coding methods that ensure DC balance. Fourth, the presented BCC TRX chip did not have implementations of clock path elements in this version, as the scope of our work was to test and validate the feasibility of DFE on BCC. In typical wireline transceiver design nowadays, the circuitries for clock path elements are well-established [45]–[47]. However, note that the relatively low target data rate (compared to the state-of-the-art Gb/s serial links) for BCC applications does not impose complex requirements in the clock path elements. Therefore, perhaps as simple as demonstrated in [48] would be sufficient to implement CDR. Lastly, the limitation of

the capacitive coupling approach and the issue with motion artefacts could be overcome by adopting on-chip real-time tap adaptation algorithms. It may not be straightforward to directly adopt existing adaptation techniques used in wireline transceivers, considering the time scale at which the channel characteristics change, i.e., HBC channel characteristics vary much more rapidly than that of wireline channels. Nevertheless, many clever methods have demonstrated successful adaptation within less than tens of milliseconds [49] (or even less [50]). Because typical human motion artefacts lie within the 0.01-5 Hz range, with appropriate modifications in the circuit designs, existing wireline adaptation algorithms can be efficiently utilised for BCC. To summarise, all these issues will help support fully functional wearable capabilities.

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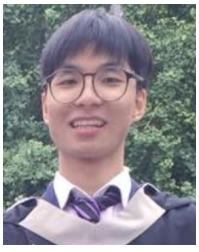

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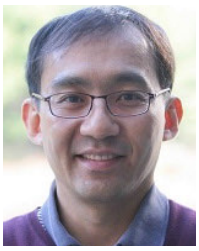

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