

Received August 26, 2020, accepted October 19, 2020, date of publication October 29, 2020, date of current version November 11, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3034665

# **Binary Memory Implemented by Using Variable Gain Amplifiers With Multipliers**

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This work was supported by the Czech Science Foundation Project under Grant 19-22248S.

ABSTRACT This work describes design process toward fully analogue binary memory where two coupled piecewise-linear (PWL) resistors are implemented using novel network topology with the voltage gain amplifiers (VGA). These versatile active devices allow slopes of individual segments of ampere-voltage (AV) characteristics associated with PWL two-terminals to be electronically adjustable via the external DC voltage. Numerical analysis of designed binary memory cell covers all mandatory parts: phase portraits, calculation of the largest Lyapunov exponent (LLE), basins of attraction for the typical strange attractors, and high-resolution circuit-oriented bifurcation sequences. A transition from the stable states toward chaotic regime through metastability is proved via real measurement. The robustness of the generated chaotic attractors is verified by captured oscilloscope screenshots.

**INDEX TERMS** Analogue binary memory, bifurcation diagram, electronic tuning, chaos, Lyapunov exponent, piecewise-linear (PWL) resistors, strange attractor.

### I. INTRODUCTION

It is well known that isolated dynamical systems having at least three degrees of freedom can exhibit complex, irregular, continuous, bounded in state space volume, random-looking, frequency-wideband motion known as a deterministic chaos. Chaos, as one of the possible solutions associated with given set of differential equations, can be understood as universal dynamic phenomena. It means that physical interpretation of individual state variables and internal system parameters are not important. Instead of this, global vector field geometry plays crucial role since folding and stretching mechanism caused by inevitable intrinsic system nonlinearity needs to apply on state trajectories simultaneously. Of course, not all trajectories can be affected since several different attractors can coexist.

General properties of the chaotic motion are interesting, at the same time due to theoretical, educational and application perspectives. Robust chaotic system generates waveform that is sensitive to the small changes of initial conditions, contains continuous scale of periodic signals, provides dense strange attractor with the non-integer geometric dimension, chaotic waveforms have increased entropy, etc. This facts have been demonstrated within hundreds of dynamical systems among all fields and research branches of physics;

The associate editor coordinating the review of this manuscript and approving it for publication was Pavlos I. Lazaridis.

for example in classical mechanics [1]–[3], math description of the chemical reactions [4], [5] and fluid dynamics [6], [7], in frame of the simplified population growth models [8], during analysis of climate model [9]–[11], in optics [12], [13] and, of course, analogue electronics. However, all chaotic systems represent simplified models of the real situations with a finite number of state variables. It is well known that probability of chaotic steady state solution rises with increased order of analyzed system. Therefore, considering very complex behavior of real events, chaos probably belongs to relatively common motion.

In the case of chaotic circuits, more detailed specification of chaos sources can be applied. Lumped analogue circuits were subject of research from the viewpoint of investigation of chaotic behavior for the last four decades. Robust strange attractors were reported in dynamics of standard structures of oscillators such as Colpitts [14], [15], Hartley [16], [17], Wien-bridge topology [18], [19], and many others. Regions with chaotic solution were detected in the phase locked loops [20], [21] and frequency filters [22], [23]. In the latter case, it turns out that both parameters of the input harmonic signal, amplitude and frequency, can continuously switch between chaotic and regular operational regimes of filtering two-port. Power electronics and switching circuits can be (and often are) subjects of nonlinear dynamics, unpredictable behavior, and chaos as well. Evolution of various strange attractors was revealed in the case of DC-DC converters



having different topologies [24]–[26]. Chaotic phenomena can be observed, both numerically and experimentally, inside simple nonlinear switched capacitors circuits [27], [28]. Logic networks and gates are not excluded from potentially chaotic systems [29]. Recent paper [30] presents evolution of chaos in fundamental class C amplifier having a single bipolar transistor modeled by admittance-type equivalent twoport. Several very simple chaotic circuits with one or two bipolar transistors and three accumulation elements are discussed in [31]. Of course, both Colpitts and Hartley oscillator topologies are members of this group of autonomous systems. Paper [32] shows that chaos in oscillating circuit can be detected thanks to the automatic gain control loop. Detailed study [33] suggests construction of robust chaotic system via closed loop of nonlinear active two-port and arbitrary realization (passive and active) of low-pass frequency filter. There, fundamental filter parameters, that is pole frequency and quality factor, are used as natural bifurcation parameters. This list of chaotic circuits is by no means complete; it continues to grow every day. Due to the problem topicality further investigation in this research area can be expected.

This paper is organized as follows. Next section provides mathematical model of binary memory system and its linear analysis. Third section is focused to show numerical analysis results that are widely considered as common standard if new chaotic dynamical system is presented [34]. Fourth section describes individual analog building blocks that are utilized in design process of chaotic oscillator. Active realization of memory including limitations coming from utilization of the commercially available variable gain multipliers is subject of section five. This section also gives experimental verification of the binary memory via measured period doubling route-to-chaos scenario. Finally, open research areas are suggested and concluding remarks are stated; where overall properties of developed chaotic memory are summarized.

# **II. MATHEMATICAL MODEL OF MEMORY**

One of the simplest circuit concepts of a multi-state memory system is based on series or anti-series connection of several resonant tunneling diodes (RTD) [35]–[37] as demonstrated in Fig. 1a). AV curve of RTD with properly adjusted bias point via voltage  $V_{\rm bias}$  can be approximated by PWL function having following properties: 1) it is scalar function having at least three linear segments, 2) exhibits both positive and negative slopes, 3) is odd-symmetrical with respect to a non-zero center. Of course, number of linear segments determine maximal amount of the stable states of memory.

Although configuration of static memory mentioned above is old chaos was discovered quite recently, see work [38] and [39] for details. Evolution of chaos is allowed if a very high-frequency models of micro-scale RTDs are considered [40]. In this case, connection of two ideal diodes with non-zero threshold voltage is supplemented by a lead inductance and two parasitic capacitances as depicted in Fig. 1b). Biasing voltage can be removed by introducing linear transformation of the coordinates, namely by using simple shift of

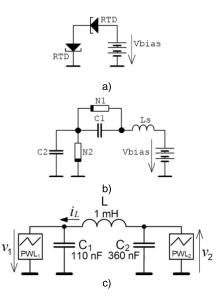


FIGURE 1. Binary memory based on the coupled RTDs: a) fundamental concept, b) equivalent circuit with high-frequency models of both RTDs, c) rearrangement of real-valued components.

the state space origin. Consequently, both active PWL resistors can be odd-symmetrical with respect to zero. Obviously, such shape of nonlinearity represents significant simplification of design process. Schematic provided in Fig. 1c) demonstrates simple lumped electronic circuit to be implemented in the upcoming section of this paper. Note that all accumulation elements are real-valued, i.e. denormalized to time constant  $\tau=10~\mu s$  and utilize impedance norm  $\xi=1000$ . Note that both  $\tau$  and  $\xi$  can be chosen arbitrarily. Dynamics of this memory is described by following set of ordinary differential equations:

$$C_1 \frac{d}{dt} v_1 = i_L - f_1(v_1),$$
 (1a)

$$C_2 \frac{d}{dt} v_2 = i_L - f_2(v_2),$$
 (1b)

$$L\frac{d}{dt}i_L = -v_1 - v_2,\tag{1c}$$

where scalar PWL functions are of the form:

$$|v_k| \le \frac{V_{sat}^k}{A_k} \to f_k(v_k) = \left(\frac{1 - A_k}{R_k}\right) v_k,$$

$$v_k > \frac{V_{sat}^k}{A_k} \to f_k(v_k) = \frac{1}{R_k} \left(v_k - \frac{V_{sat}^k}{A_k}\right)$$
(2a)

$$+\frac{1-A_k}{R_k} \cdot \frac{V_{sat}^k}{A_k},\tag{2b}$$

$$v_{k} < -\frac{V_{sat}^{k}}{A_{k}} \rightarrow f_{k}(v_{k}) = \frac{1}{R_{k}} \left( v_{k} - \frac{V_{sat}^{k}}{A_{k}} \right) - \frac{1 - A_{k}}{R_{k}} \cdot \frac{V_{sat}^{k}}{A_{k}}, \tag{2c}$$

where formulas for saturation voltages  $V_{sat}^k$ , slope resistors  $R_k$  and amplifications  $A_k$  will be defined later. Fixed points are all real solutions of a nonlinear algebraic problem dx/dt = 0. Number and location of equilibria depends only



on the shape of AV curves of PWL resistors. Dynamical system (1) can possess one, three or five fixed points. Their locations are uniquely determined by solution for which holds:

$$v_1 = -v_2,$$
 (3a)

$$i_L = f_1(v_1) = f_2(-v_2).$$
 (3b)

Obviously, we always have equilibrium located at state space origin, i.e.  $\mathbf{x}_e = (0, 0, 0)^T$ . In fact, PWL functions divide state space into nine affine segments. Presence of the fixed point in each segment is conditioned by existence of solution of following equations:

$$v_{1} = -v_{2} = \left(\frac{R_{2}}{R_{1} + R_{2} - R_{1}A_{2}}\right) V_{sat}^{1} \wedge v_{1}$$

$$> \frac{V_{sat}^{1}}{A_{1}} \wedge |v_{2}| < \frac{V_{sat}^{2}}{A_{2}}, \qquad (4a)$$

$$v_{1} = -v_{2} = -\left(\frac{R_{2}}{R_{1} + R_{2} - R_{1}A_{2}}\right) V_{sat}^{1} \wedge v_{1}$$

$$< -\frac{V_{sat}^{1}}{A_{1}} \wedge |v_{2}| < \frac{V_{sat}^{2}}{A_{2}}, \qquad (4b)$$

$$v_{1} = -v_{2} = -\left(\frac{R_{1}}{R_{1} + R_{2} - R_{2}A_{1}}\right) V_{sat}^{2} \wedge |v_{1}|$$

$$< \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} > \frac{V_{sat}^{2}}{A_{2}}, \qquad (4c)$$

$$v_{1} = -v_{2} = \left(\frac{R_{1}}{R_{1} + R_{2} - R_{2}A_{1}}\right) V_{sat}^{2} \wedge |v_{1}|$$

$$< \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} < -\frac{V_{sat}^{2}}{A_{2}}, \qquad (4d)$$

$$v_{1} = -v_{2} = -\left(\frac{R_{1}V_{sat}^{2} - R_{2}V_{sat}^{1}}{R_{1} + R_{2}}\right) \wedge v_{1}$$

$$> \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} > \frac{V_{sat}^{2}}{A_{2}}, \qquad (4e)$$

$$v_{1} = -v_{2} = -\left(\frac{R_{1}V_{sat}^{2} + R_{2}V_{sat}^{1}}{R_{1} + R_{2}}\right) \wedge v_{1}$$

$$< -\frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} > \frac{V_{sat}^{2}}{A_{2}}, \qquad (4f)$$

$$v_{1} = -v_{2} = \left(\frac{R_{1}V_{sat}^{2} + R_{2}V_{sat}^{1}}{R_{1} + R_{2}}\right) \wedge v_{1}$$

$$> \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} < -\frac{V_{sat}^{2}}{A_{2}}, \qquad (4g)$$

$$v_{1} = -v_{2} = \left(\frac{R_{1}V_{sat}^{2} - R_{2}V_{sat}^{1}}{R_{1} + R_{2}}\right) \wedge v_{1}$$

$$< \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} < -\frac{V_{sat}^{2}}{A_{2}}, \qquad (4g)$$

$$v_{1} = -v_{2} = \left(\frac{R_{1}V_{sat}^{2} - R_{2}V_{sat}^{1}}{R_{1} + R_{2}}\right) \wedge v_{1}$$

$$< \frac{V_{sat}^{1}}{A_{1}} \wedge v_{2} < -\frac{V_{sat}^{2}}{A_{2}}, \qquad (4g)$$

Jacobi matrices for individual segments can be expressed as:

$$\mathbf{J}_{inner}^{inner} = \begin{pmatrix} \frac{1 - A_1}{R_1 C_1} & 0 & \frac{1}{C_1} \\ 0 & \frac{1 - A_2}{R_2 C_2} & \frac{1}{C_2} \\ -\frac{1}{L} & -\frac{1}{L} & 0 \end{pmatrix}, \tag{5a}$$

$$\mathbf{J}_{inner}^{outer} = \begin{pmatrix} \frac{1-A_1}{R_1C_1} & 0 & \frac{1}{C_1} \\ 0 & \frac{1}{R_2C_2} & \frac{1}{C_2} \\ -\frac{1}{L} & -\frac{1}{L} & 0 \end{pmatrix}, \quad (5b)$$

$$\mathbf{J}_{outer}^{inner} = \begin{pmatrix} \frac{1}{R_1C_1} & 0 & \frac{1}{C_1} \\ 0 & \frac{1-A_2}{R_2C_2} & \frac{1}{C_2} \\ -\frac{1}{L} & -\frac{1}{L} & 0 \end{pmatrix}, \quad (5c)$$

$$\mathbf{J}_{outer}^{inner} = \begin{pmatrix} \frac{1}{R_1 C_1} & 0 & \frac{1}{C_1} \\ 0 & \frac{1 - A_2}{R_2 C_2} & \frac{1}{C_2} \\ -\frac{1}{L} & -\frac{1}{L} & 0 \end{pmatrix}, \tag{5c}$$

$$\mathbf{J}_{outer}^{outer} = \begin{pmatrix} \frac{1}{R_1 C_1} & 0 & \frac{1}{C_1} \\ 0 & \frac{1}{R_2 C_2} & \frac{1}{C_2} \\ -\frac{1}{I} & -\frac{1}{I} & 0 \end{pmatrix}. \tag{5d}$$

Subscript and superscript associated with the square matrix J mark segment of first and second PWL resistor, respectively. Characteristic polynomial can be expressed as follows:

$$\lambda^{3} - \left(\frac{\alpha_{1}}{R_{1}C_{1}} - \frac{\alpha_{2}}{R_{2}C_{2}}\right)\lambda^{2} + \left(\frac{1}{C_{1}L} + \frac{1}{C_{2}L} + \frac{\alpha_{1}\alpha_{2}}{R_{1}R_{2}C_{1}C_{2}}\right)\lambda - \frac{R_{1}\alpha_{2} + R_{2}\alpha_{1}}{R_{1}R_{2}C_{1}C_{2}L} = 0, \quad (6)$$

where  $\alpha_k = 1$  in the outer segment and  $\alpha_k = 1 - A_k$  in the inner segment of the k-th PWL resistor. Roots of polynomial (6) can be evaluated using Cardan rules, both symbolically and numerically form. Symbolic formulas are very complicated and will not be provided. However, numerical evaluation of roots of polynomial (6) is part of optimization routine as it will be clarified in upcoming section.

# III. NUMERICAL ANALYSIS

Numerical results presented in this paper were obtained using three programs: Mathcad 15 mostly dedicated for graphical visualization, Matlab 2018 for implementation of calculation routines, and Orcad Pspice utilized for circuit simulations. For numerical integration process, fourth order Runge-Kutta method with the fixed time step was chosen.

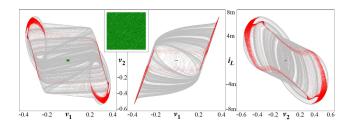


FIGURE 2. Different projections of a typical strange attractor produced by memory:  $v_1$  vs  $v_2$  plane (left),  $v_1$  vs  $i_L$  plane (middle),  $v_2$  vs  $i_L$  plane (right). Sensitivity to small changes of initial conditions: initial (green) and final (red) states after evolution time 100  $\mu$ s, small plot is zoomed area  $v_1 \in (-10, 10)$  mV,  $v_2 \in (-10, 10)$  mV with  $10^4$  randomly generated initial conditions with uniform distribution.

Figure 2 demonstrates a typical shape of the "maximally complex,,strange attractor generated by the binary memory.

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(4h)



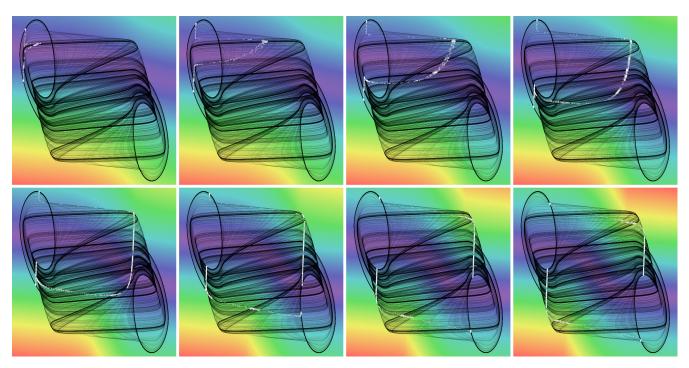


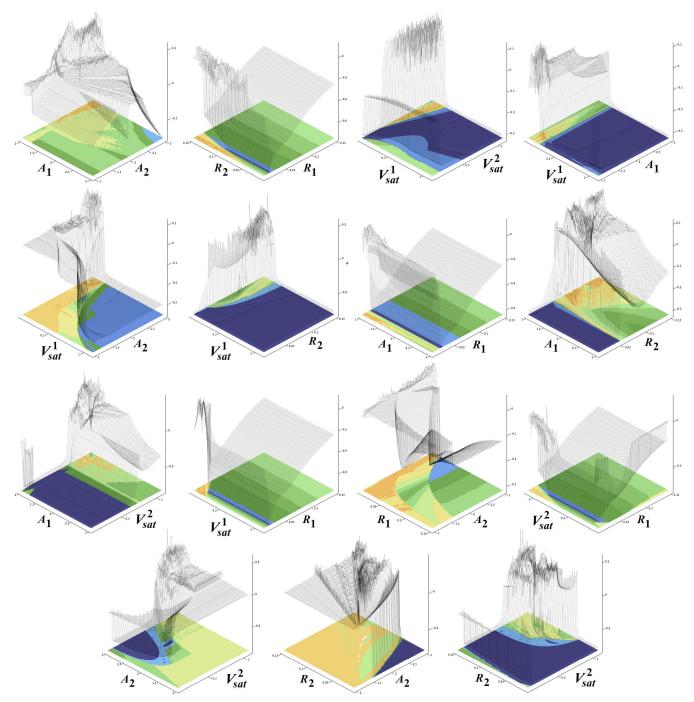
FIGURE 3. Rainbow-scaled contour plot of kinetic energy distribution,  $v_1$  vs  $v_2$  plane projection of typical chaotic attractor (black) and return maps (white dots) plotted for following list of Poincaré sections:  $i_L = -7$  mA,  $i_L = -6$  mA,  $i_L = -5$  mA,  $i_L = -4$  mA,  $i_L = -3$  mA,  $i_L = -2$  mA,  $i_L = -1$  mA, and  $i_L = 0$  mA.

This plot also shows a high degree of unpredictability of dynamical flow. Distribution of kinetic energy in state space occupied by the typical double-scroll attractor generated by memory is provided by means of Fig. 3. Here, low speed of system evolution is marked by blue colour, average kinetic energy is denoted by green areas, high and very high system movement can be expected in yellow and red regions. Note that only horizontal slices for the negative current  $i_{\rm L}$ are provided. It is because origin-centred symmetry of the vector field. This means that plots for the positive values of current  $i_L$  looks analogically. Figure 4 provides plots of LLE as two-dimensional functions of all combinations of the parameters in the hexagonal space. This six-dimensional hyperspace was dedicated for search-for-chaos routine where fitness function was suitable combination of three basic properties of a state attractor, namely: 1) boundedness of the attractor, 2) positive value of LLE, and 3) existence of three unstable fixed points. Optimization itself is based on a nongradient evolutionary-inspired algorithm. Stability of equilibrium points is tested via calculation of roots of (6). From the viewpoint of chaos formation third criterion seems to be irrelevant because many chaotic dynamical systems having degenerated equilibrium structures [41]-[43], with variable equilibrium [44] or even without equilibrium objects (points, lines, curves) [45] have been already discovered. It has been already proved that chaos is not restricted to unstable fixed points, see [46], [47] for details. On the other hand, existence of three fixed points represents situation that is close to the operation as common binary memory.

Discovered strange attractors belong to the class of selfexcited, rendering a choice of initial conditions very simple: in the close neighbourhood of origin that is unstable for all combinations of system parameters considered during search procedure. Of course, Fig. 4 shows only a small fragment of parameter's hyperspace addressed by optimization procedure used in this work. It is focused on area where robust chaos was finally localized. Set of numerical values that leads to a very dense double-folded strange attractor are:  $C_1=110$  nF,  $C_2=360$  nF, L=1 mH,  $V_{\rm sat}^1=200$  mV,  $A_1=1.2$ ,  $R_1=14$   $\Omega$ ,  $V_{\rm sat}^2=1$  V,  $A_2=3$ ,  $R_2=130$   $\Omega$ . Eigenvalues associated with fixed points in the outer regions of the vector field depends primarily on the slopes of PWL resistors.

Used method for numerical calculation of LLE with Gram-Smith orthogonalization excludes wrong misinterpretation of the chaotic dynamics as numerical artefact or a long chaotic transient. Variations of solution with respect to the resistance  $R_2$  is visualized by means of Fig. 5. In these plots, the initial conditions were chosen symmetrically as  $\mathbf{x}_0 = (0.01, 0, 0)^T$ and vector  $\mathbf{x}_0 = (-0.01, 0, 0)^T$  for orange and blue trajectory respectively. State orbits were integrated up to the final time 100 ms with fixed time step 1  $\mu$ s. Intersections of plotted PWL functions mark  $v_1$  coordinates of the fixed points. Note that mentioned qualitative change of memory behavior starts and ends with attraction fixed points. Between corner values of the resistance  $R_2$ , that is 50  $\Omega$  and 600  $\Omega$ , several different limit cycles can be observed. Further increasing value of resistor  $R_2$  does not admit turning dynamical system into chaotic regime. Also note that outer fixed points can be located within either inner or outer segments of second PWL function. For  $R_2 = 50 \Omega$  eigenvalues associated with these equilibrium points are given by linearization matrix  $\mathbf{J}_{outer}^{outer}$  and numerical eigenvalues are  $\lambda_{1,2} = -3.488 \cdot 10^4 \pm j \cdot 4.918 \cdot 10^4$ ,





**FIGURE 4.** Topographically scaled surface-contour plot of LLE as function of two circuit parameters taken from full set  $\{A_1, R_1, V_{\text{sat}}^1, A_2, R_2, V_{\text{sat}}^2\}$ , high-resolution plots with uniform parameter step 0.01.

 $\lambda_3 = -6.351 \cdot 10^5$ , i.e. a state orbit spirals toward outer fixed points quickly. Therefore, what we have here, is a true binary memory with two mirrored basins of attraction.

Table 1 shows symbolically transitions between state space segments described above (situation a – first row). For chaos evolution, outer fixed points should be located within inner segment created by the second PWL resistor, i.e. where eigenvalues are defined by  $\mathbf{J}_{outer}^{inner}$ . For resistance  $R_2$  larger

than 70  $\Omega$  state space geometry can be divided into nine affine segments and described by transitions in situation b (second line of Table 1). Obviously, chaotic orbit eventually visits all regions of the state space. For upper boundary  $R_2 = 600 \Omega$  eigenvalues calculated for the outer equilibrium points are still defined by  $\mathbf{J}_{outer}^{inner}$  and one can obtain easily  $\lambda_{1,2} = -2.479 \cdot 10^3 \pm \mathrm{j} \cdot 5.197 \cdot 10^4$  and  $\lambda_3 = -6.351 \cdot 10^5$ , i.e. state orbit tends toward outer fixed points following spiral



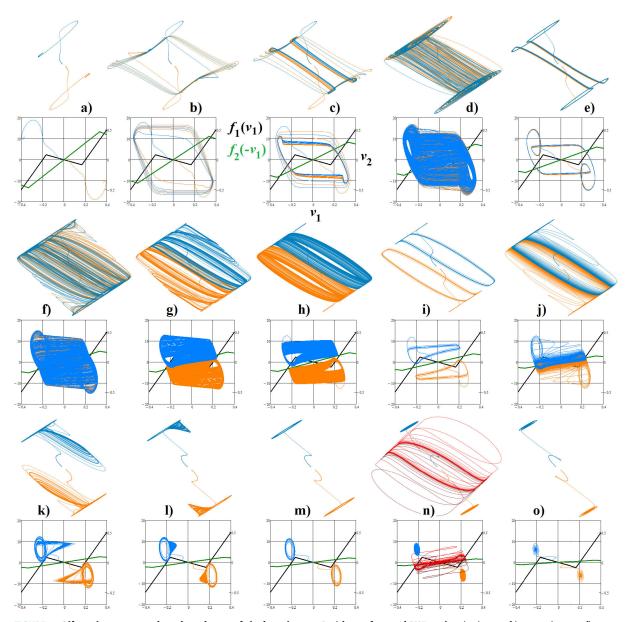


FIGURE 5. Bifurcation sequence based on change of single resistance  $R_2$  (slope of second PWL resistor): a) 50  $\Omega$ , b) 60  $\Omega$ , c) 80  $\Omega$ , d) 90  $\Omega$ , e) 110  $\Omega$ , f) 130  $\Omega$ , g) 140  $\Omega$ , h) 150  $\Omega$ , i) 170  $\Omega$ , j) 230  $\Omega$ , k) 250  $\Omega$ , l) 280  $\Omega$ , m) 320  $\Omega$ , n) 410  $\Omega$ , and o) 600  $\Omega$ .

movement. In this case, transitions between segments could be characterized by situation c (third line of Table 1).

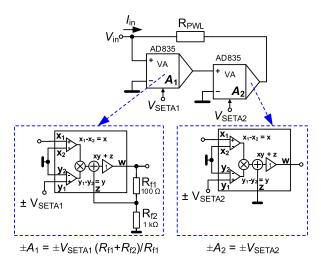
Note that several different attractors coexist within dynamics of binary memory. Figure 5n) shows four different  $\omega$ -limit sets: two fixed points and two mirrored limit cycles. Evolution of the latter cases is achieved by choosing initial conditions as  $\mathbf{x}_0 = (0.1, 0, 0)^T$  for brown colour and vector  $\mathbf{x}_0 = (-0.1, 0, 0)^T$  for red trajectory. The same limit cycles can be observed for the higher values of resistor  $R_2$ .

As part of numerical investigation, basin of attraction for chaotic and non-chaotic attractors was calculated. To do this, systematic state space grid of volume 10 V  $\times$  10 V  $\times$  10 mA having density 100 mV  $\times$  100 mV  $\times$  1 mA of the initial

conditions was constructed. Doing so, it has been verified that robust strange attractor generated by sequent numerical values of passive and active elements:  $C_1 = 110$  nF,  $C_2 = 360$  nF, L = 1 mH,  $V_{\rm sat}^1 = 200$  mV,  $A_1 = 1.2$ ,  $R_1 = 14$   $\Omega$ ,  $V_{\rm sat}^2 = 1$  V,  $A_2 = 3$ ,  $R_2 = 130$   $\Omega$ , is a global attracting set. However, question about existence of hidden attractors was not answered. To find answer, more sophisticated calculation of the initial states than generation of rough grid mentioned above needs to be performed. In fact, a pair of the hidden attractors can be expected due to the vector field symmetry. Because familiarity of analysed memory system with Chua's oscillator it is very likely that hidden limit cycles coexist with strange attractors, similarly as it was proved for this famous chaotic oscillator in paper [48].

**TABLE 1.** Transitions between state space segments.

| situation | description  |
|-----------|--|
| a         | $\mathcal{R}^3 \colon \begin{pmatrix} E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{stable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \\ \downarrow & \searrow & \uparrow & \swarrow & \downarrow \\ E_1^{unst.} \oplus E_1^{unst.} \oplus E_1^{stable} & E_2^{unstable} \oplus E_1^{unstable} & E_1^{unst.} \oplus E_1^{unst.} \oplus E_1^{stable} \\ \uparrow & \nearrow & \uparrow & & \uparrow \\ E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{stable} \oplus E_1^{stable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \end{pmatrix}$ |
| b         | $\mathcal{R}^3 \colon \begin{cases} E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{stable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \\ \downarrow & & \downarrow & \downarrow & \downarrow \\ E_2^{stable} \oplus E_1^{stable} & & E_2^{unstable} \oplus E_1^{unstable} & \oplus E_2^{table} \oplus E_1^{stable} \\ \uparrow & & \uparrow & & \uparrow \\ E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{stable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \end{cases}$   |
| C         | $\mathcal{R}^3 \colon \begin{pmatrix} E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{unstable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \\ \downarrow & \searrow & \downarrow & \downarrow & \downarrow \\ E_2^{stable} \oplus E_1^{stable} & E_2^{unstable} \oplus E_1^{unstable} & E_2^{stable} \oplus E_1^{stable} \\ \uparrow & \swarrow & \uparrow & \searrow & \uparrow \\ E_2^{stable} \oplus E_1^{stable} & \rightarrow & E_2^{unstable} \oplus E_1^{unstable} & \leftarrow & E_2^{stable} \oplus E_1^{stable} \end{pmatrix}$  |



**FIGURE 6.** Principal configuration of fully analogue electronically adjustable active PWL resistor.

# IV. DESCRIPTION OF PWL BUILDING BLOCK

Chaotic oscillator to be implemented contains three passive elements and two PWL resistors, as evident from Fig. 1c). Circuit realization of PWL resistor with two VGAs AD835 is depicted in Fig. 6 together with implementation of VGA using one multiplier and differential stage. Theoretical shape of AV characteristics is provided in Fig. 7. Design formulas important for synthesis of the analogue chaotic system or, more precisely speaking, for synthesis of PWL resistors, will be derived in this section. Position of breakpoint voltages is symmetrical with respect to origin, namely:

$$\pm V_{break} = \pm V_{sat}^2 \frac{1}{A_1 A_2} \cong \frac{\pm V_{sat}^2}{V_{SETA1} \left(\frac{R_{f1} + R_{f2}}{R_{f1}}\right) V_{SETA2}}.$$
 (7)

Because for AD835 holds relation  $V_{sat}^2 = V_{inp} \cdot V_{SETA2}$  we obtain immediately:

$$\pm V_{break} = \frac{\pm V_{inp\_max}}{V_{SET\_A1} \left(\frac{R_{f1} + R_{f2}}{R_{f1}}\right)}.$$
 (8)

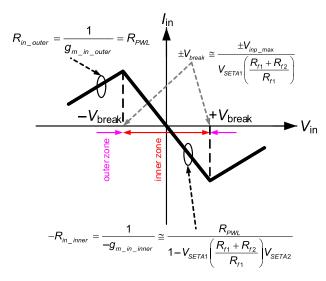


FIGURE 7. PWL AV characteristics of designed active resistor including description math formulas.

Note that this formula does not depend on the voltage  $V_{\text{SETA2}}$ . Slope of PWL AV curve in the inner segment, i.e. if  $V_{inp} < \pm V_{break}$ , can be expressed as:

$$R_{in\_inner} = \frac{1}{g_{m\_in\_inner}} = \frac{R_{PWL}}{1 - A_1 A_2}$$

$$\stackrel{\cong}{=} \frac{R_{PWL}}{1 - V_{SET\_A1} \left(1 + \frac{R_{f2}}{R_{f1}}\right) V_{SET\_A2}}.$$
(9)

In the outer segments, namely for  $V_{inp} > \pm V_{break}$  where slope of AV characteristics is positive, equivalent resistance can be formulated as:

$$R_{in\_outer} = \frac{1}{g_{m\_in\_outer}} = R_{PWL}.$$
 (10)

Using these formulas and parameters defined above leading to the so-called "chaotification" of a binary memory system, numerical values of both PWL resistors are provided via Table 2. AV characteristics of both PWL resistors ready



TABLE 2. Theoretical and practical numerical values associated with implementation of both active PWL resistors.

|  | PWL <sub>1</sub> | PWL <sub>2</sub>        |
|--|------------------|-------------------------|
| Des  | ign target       |                         |
| V <sub>break</sub> [V]   | ±0.167           | ±0.333                  |
| $g_{	extsf{m_in_outer}}/R_{	extsf{in_outer}}[	extsf{mS}/\Omega]$ | +71.4 / 14       | +7.8 / 128              |
| $g_{m \; in \; inner} / R_{in \; inner} [mS  /  \Omega]$         | -14.3 / -70      | -15.6 / <del>-</del> 64 |
| Calculate  | ed parameters    |                         |
| V <sub>SETA1</sub> PWL [V]                                       | 0.76             | 0.39                    |
| VSETA2_PWL [V]   | 0.14             | 0.71                    |
| $R_{PWL}[\Omega]$ (round up)                                     | 14 (15)          | 128 (120)               |

for implementation in the memory were experimentally confirmed via laboratory measurement.

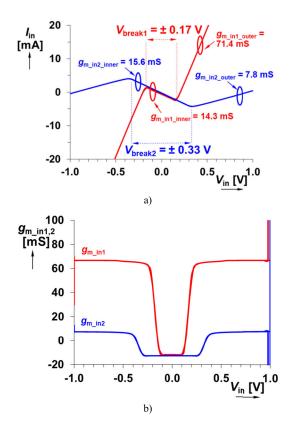


FIGURE 8. Measured AV curves of both designed PWL resistors:
a) interesting numerical values within required state space volume,
b) corresponding conductance slopes as functions of input voltage.

Results are graphically summarized by means of Fig. 8. To preserve smooth, visually friendly shape of modelled chaotic attractor, segments of AV curves of both PWL resistors need to be straight lines without ripples or overshoots. Linearity is represented by constant derivatives, the input admittances of PWL blocks. To verify such feature, measurement was done using small step of input voltage, success visible in Fig. 8b).

### **V. REALIZATION, SIMULATION, AND EXPERIMENTS**

Fully analogue circuit realization of binary memory cell is provided in Fig. 1c) where two PWL resistors described in Fig. 6 are utilized. Numerical values associated with AV

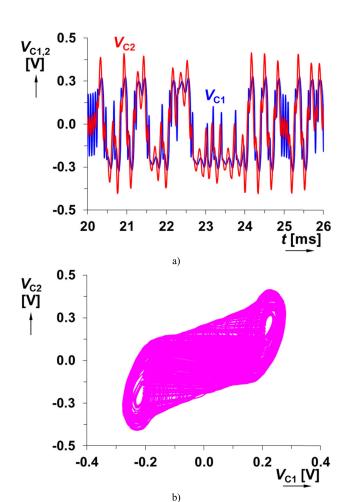


FIGURE 9. Selected Orcad Pspice circuit simulation results associated with chaotic regime of binary memory: a) generated signals in time domain, b) corresponding plane projection.

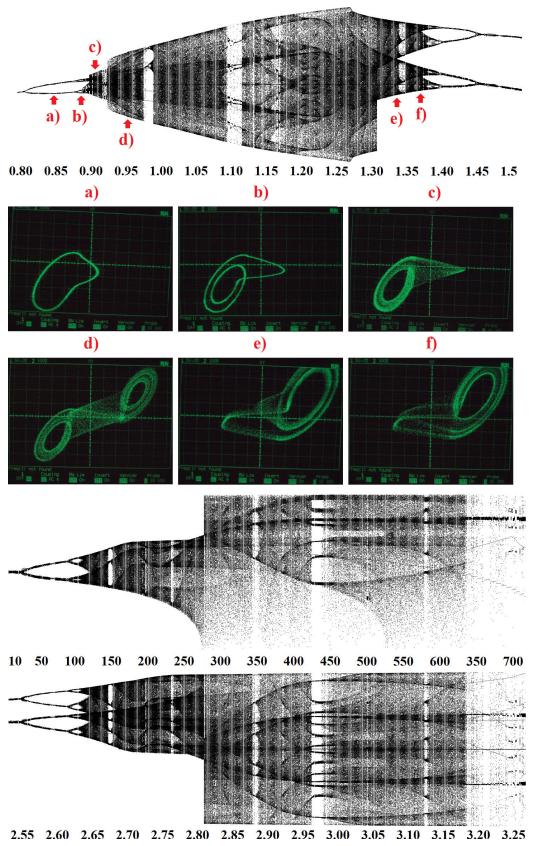
characteristics of both PWL resistors are given within Tab. 2. At the first stage, chaos in binary memory cell was confirmed by Orcad Pspice circuit simulator, see Fig. 9 for few selected results. Chaotic circuit was implemented using breadboard and fed by symmetrical  $\pm 5$  V. This limited supply voltage is allowed thanks to the small state space volume occupied by desired strange attractor, check Fig. 2. Figure 10 illustrates one-dimensional bifurcation diagrams calculated with respect to three key internal parameters of PWL resistors. Chaotic waveforms  $v_1$  and  $v_2$  generated by the chaotic binary memory are visualized by means of Fig. 11. Evidently, chaotic motion is a combination (repetition) of two spiral movements. This corresponds to two saddle-spiral types of equilibrium points.

Of course, dynamical system (1) can be implemented as the lumped circuit using alternative approach. For example, voltage mode [49] as well as current mode [50] chaotic circuit can be designed using analogue computer concept.

### VI. RESULTS AND DISCUSSION

Firstly, this manuscript introduces elegant realization of low voltage two-terminal device having the odd-symmetrical





**FIGURE 10.** Calculated one-dimensional bifurcation diagrams and associated state attractors captured by oscilloscope: variable  $A_1 \in (0.8, 1.5)$  (upper plot), variable  $R_1 \in (10, 700)$   $\Omega$  (middle plot), variable  $A_2 \in (2.55, 3.25)$  (lower plot).



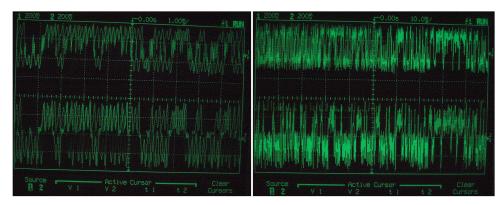


FIGURE 11. Generated chaotic waveforms in time domain visualized in two different time scales, captured oscilloscope screenshots.

PWL AV characteristics. Slopes of AV curve can be adjusted in wide range via external DC voltage source. Such universal circuit component can be utilized not only in realization of chaotic networks but design of analog nonlinear circuits in general. Potential signal processing applications are limited by finite supply voltage and frequency response of integrated circuit AD835.

### VII. CONCLUSION

This paper provides circuitry realization of binary memory that is fully adjustable via external electronic signals. This external control can smoothly change fundamental nature of memory: from stable states, through limit cycles, chaotic oscillations back to a pair of the stable states. Therefore, constructed memory can work as binary. In addition, can generate robust chaotic waveforms with significant entropy suitable for practical applications. Existence of different solutions including strange attractors is proved by numerical analysis as well as experimental measurement. Very good harmony between theoretical and practical results is obtained.

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