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An Active Resistor With a Lower Sensitivity to Process Variations, and Its Application in Current Reference

VILEM KLEDROWETZ, JIRI HAZE, ROMAN PROKOP, AND LUKAS FUJCIK
Department of Microelectronics, Brno University of Technology (BUT), 61600 Brno, Czech Republic
Corresponding author: Vilem Kledrowetz (kledrowetz@vutbr.cz)

ABSTRACT A novel active resistor circuit offering less sensitivity to process and temperature variations without any extra trimming is proposed. The circuit consists of two accurately matched, high resistance polysilicon (hripoly) resistors and a voltage-controlled MOS resistor, and it is designed for the industrial temperature range (−20 °C to 85 °C) in the TSMC 180 nm general-purpose process. The actual performance of the circuit is analyzed by using the Corner and Monte Carlo analyses that comprise two thousand samples for the global and local process variations. The maximum error in the resistor value is ±6.2 %, with the standard deviation of $\sigma = 1.2$ %. The proposed active resistor reduces the maximum error from ±15 % to ±6.2 % when the both the process and the temperature variations are considered without trimming. As an application, a transconductor and a current reference based on the novel active resistor are introduced, and their accuracy-related performance is studied.

INDEX TERMS Active resistors, current reference, process variation, transconductor.

I. INTRODUCTION

At present, increasingly more integrated circuits (IC) require high accuracy components. One of the most important parts of an IC is the resistor. Most processes offer several types of resistors optimized for different applications. Polysilicon resistors are available in the CMOS and BiCMOS processes. The poly used for constructing MOS gates is heavily doped to improve the conductivity and has a sheet resistance of between 25 and 50 Ohms per square; lightly doped polysilicon can exhibit sheet resistances of hundreds or even thousands of Ohms per square.

A resistor's Ohm value depends on numerous factors, including the variability, temperature, nonlinearity, and contact resistance; other factors of importance in this respect involve, above all, the resistor's dimensions and sheet resistance. The dimensions of a resistor vary because of photolithographic inaccuracies and nonuniform etch rates. The sheet resistances differ due to fluctuations in the film thickness, doping concentration, doping profiles, and annealing profiles [1]. Modern processes maintain the sheet resistance within ±20 %. Such a tolerance is markedly poorer than that of comparable discrete devices. As a result, the direct implementation of resistors in analog CMOS circuits is usually avoided because of low sheet resistance and accuracy limitations; moreover, the Ohm value is fixed and cannot be tuned [2]. Integrated circuits can nevertheless achieve a high degree of precision matching. If one component value increases by 20 %, then all precisely matched devices based on the same material experience similar increases [3], with the maximum deviation up to ±0.1 %. The ratio between two similar components can be controlled to deliver a rate better than 0.1 %; therefore, analog integrated circuits usually depend on matching to obtain a significant part of their precision. In some cases, the circuit parameters markedly associate with the accuracy of a single resistor (Brokaw reference, V-I converter, RC integrator, etc.). Thus, after being manufactured, each integrated circuit must be adjusted by trimming the value of one or more devices. Integrated circuits generally utilize diverse types of trimming processes, depending upon the process and the manufacturer. One of the most popular trimming devices is the resistor. Resistors can be trimmed by using fuses, Zener zaps, EPROM trims, and laser trims. Another option is to use a digital potentiometer.

Many research papers have been published on the replacement of standard resistors by active resistors in RC filters [4]–[7], transconductors [8]–[11], and universal active resistors [12]–[16]; alternatively, digitally programmable

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OTAs (operational transconductance amplifiers) are employed for the given purpose [17]–[25] to compensate the PVT variations (the digital control action overcomes any mismatch, temperature, and process variations). Active resistor circuits embody complex structures, implemented by employing MOS transistors that are functionally equivalent to classic resistors. The class of active structures is designed mainly in view of the possibility of markedly reducing the silicon area, especially for large values of the simulated resistances. However, the structures suffer from resistance nonlinearity, limited voltage ranges, and process variation [26]–[29]. These drawbacks then limit the use of the active resistor in applications such as current and voltage references and transconductors.

The paper aims to design a floating active resistor with a low sensitivity to the process and temperature variations. The proposed circuit exploits the fact that the ratio between two components from the same material can be controlled to yield a rate better than ±0.1 %; thus, the main hripoly resistor is supplemented with another, well-matched hripoly resistor. The other resistor's variation is converted to the voltage that drives the MOSFET resistor, connected in series with the main resistor. The MOSFET's resistivity changes in a manner opposite to that characterizing the main one, depending on the process and temperature variations. The proposed solution significantly reduces the sensitivity of the circuit parameters at the process corners. The performance of the circuits is analyzed by using Cadence software.

This paper is organized as follows: In Section II, the impact of the process variation on the MOSFET's parameters is explained; Section III proposes a new active resistor and explains the basic principle; Section IV introduces the transistor level design of the circuit and demonstrates the simulation results; in Section V, the transconductor and current reference based on the novel active resistor are introduced and their accuracy-related performance studied; and Section VI highlights the major conclusions of the work.

II. IMPACT OF THE PROCESS VARIATION ON THE MOSFET PARAMETERS

In order to maintain or even improve the circuit performance criteria, such as the gain, voltage range, and current mirror's small-signal output resistances, the device threshold voltage (V_{TH}) needs to be scaled in proportion to the supply voltage. This effort has a serious side effect on the subthreshold leakage current: As the V_{TH} is scaled down, the sub-threshold drain currents at the zero gate voltage keep growing. However, the dramatic increase in the nominal leakage is accompanied by an exponential rise in the sensitivity to V_{TH} variations. The most important fluctuation sources include, for example, random dopant dispersion, line-edge roughness, oxide thickness variation, nonuniform V_{TH} by fixed charge, and variation in the implant and anneal processes [30]. Modern processes maintain the V_{TH} and β tolerances within ±20 %.

A. MODELING THE MOSFET IN THE TRIODE REGION

Several MOSFET models have been discussed in [31]. We will assume a source-referenced, simplified, strong-inversion model (SPICE LEVEL 3); this yields the drain current

$$I_{DS} = \beta\left[(V_{GB} - V_{SB} - V_{TH})(V_{DB} - V_{SB}) - \frac{1+f_b}{2}(V_{DB} - V_{SB})^2\right], \quad (1)$$

where $\beta = \mu C_{OX} W/L$, and f_b is the Taylor series expansion coefficient of the bulk charge [32], given by

$$f_b = f_n + f_s \frac{\gamma}{4\sqrt{2\phi_F + V_{SB}}}. \quad (2)$$

This model specifies the narrow width (f_n) and short channel (f_s) effects, which occur when narrow or short channel dimensions are used. In the above equation, substituting V_{DB} - V_{SB} with V_{DS}, and V_{GB} - V_{SB} with V_{GS} gives

$$I_{DS} = \beta\left[(V_{GS} - V_{TH})\, V_{DS} - \frac{1+f_b}{2} V_{DS}^2\right]. \quad (3)$$

If the channel is designed with larger W and L (greater than about 0.8 μm [33]), the narrow/short channel effects can be ignored ($f_s = 1, f_n = 0$). Since the V_{DS} is very small, namely, ($V_{DS} \ll V_{GS} - V_{TH}$), (3) can be rewritten as

$$I_{DS} = \beta\left[(V_{GS} - V_{TH})\, V_{DS} - \frac{1}{2} V_{DS}^2\right], \quad (4)$$

which corresponds to the Schichman-Hodges model (SPICE LEVEL 1). This model is simple to use in hand calculations but neglects some important effects; however, models with physical parameters (1)(3) cannot produce accurate results unless appropriate values are used for their parameters. The values of some of these parameters are usually not specified accurately by the manufacturers; thus, in the realm of circuit design, it is more desirable to express the model equations in terms of the electrical rather than the physical parameters [33].

B. MOSFET RESISTOR

The small-signal resistance (r_{DS}) follows from (4):

$$r_{DS} = \frac{\delta v_{DS}}{\delta i_{DS}} = \frac{1}{\beta\,(V_{GS} - V_{TH} - V_{DS})}. \quad (5)$$

As mentioned earlier, the V_{TH} and β are loaded with a process variation error. Assume that the V_{TH} process variation error is expressed by the parameter E_{VTH}, and the β by E_β. These error parameters are given by the following equations:

$$E_\beta = 1 + \frac{\delta\beta}{\beta}, \quad (6)$$

$$E_{VTH} = 1 + \frac{\delta V_{TH}}{V_{TH}}. \quad (7)$$

Now, (5) can be rewritten as

$$r_{DS} = \frac{1}{\beta E_\beta\,(V_{GS} - V_{TH} E_{VTH} - V_{DS})}. \quad (8)$$

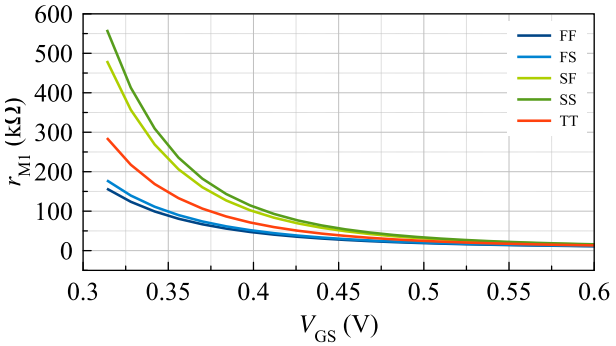

FIGURE 1. The voltage dependence of the MOSFET resistor at different process corners: V_{TH} (FF, FS, SF, SS, TT) = (0.25, 0.26, 0.30, 0.31, 0.28) V.

A plot of r_{M1} ($= r_{DS}$) as a function of v_{GS} from the Cadence corner analysis is shown in Fig. 1 for $V_{DS} = 0.2$ V and $W/L = 11/10$.

Fig. 1 indicates that the r_{DS1} variation depends on the overdrive voltage, denoted as V_{OV} ($V_{OV} = V_{GS} - V_{TH}$). The worst-case deviation from the typical r_{DS1} at $V_{GS} =$ 0.35 V is almost 100 % (TT vs. SS); the level then drops to 20 % at $V_{GS} = 0.6$ V. It should also be noted that the manufacturer specifies the maximum deviation of the high resistance poly resistor (hripoly) from the nominal value up to ±15 %. As the resistivity deviation (both MOSFET and passive hripoly) generated by the process variation becomes high, using a single resistor is significantly limited in IC design.

III. ACTIVE RESISTOR

As already mentioned in Section II, employing a single resistor is markedly limited in IC design. Within this section, a novel active resistor circuit with less sensitivity to process variation is proposed; the relevant principle is illustrated in Fig. 2.

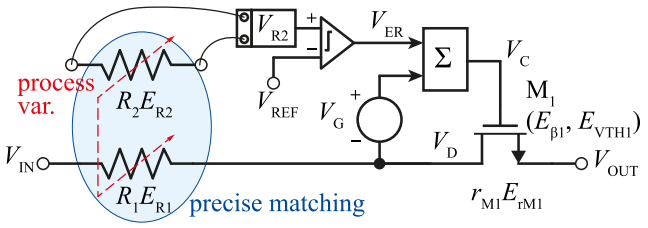

FIGURE 2. A simplified schematic of the active resistor. The parameters E_{R1} and E_{R2} represent the process variation error of the hripoly and the E_{rM1} of MOSFET (includes both $E_{β1}$ and E_{VTH1}).

The core of the circuit is composed of an R_1 (a hripoly resistor) connected in series with an M$_1$ (an NMOS transistor in the triode region). The transistor's purpose is to compensate the fluctuation in R_1 caused by process variation. The overall resistance between the V_{IN} and the V_{OUT} is equal to the sum of R_1 and r_{M1}, that is

$$R_{AR} = R_1 + r_{M1}, \tag{9}$$

and, including errors,

$$R_{AR} = R_1E_{R1} + r_{M1}E_{rM1}. \tag{10}$$

As can be seen in Fig. 2, the M$_1$ is controlled from the drain side by the $V_C - V_D$ voltage, which is in contrast with the circuit illustrated in Fig. 2. Thus, $V_{GS1} = V_D + V_G + V_{ER} - V_{OUT} = V_{DS} + V_G + V_{ER}$, where $V_{DS} = V_D - V_{OUT}$. Now, equation (4) can be rewritten as

$$I_{DS} = \beta_1 V_{DS}\left(V_G + V_{ER} + \frac{1}{2}V_{DS} - V_{TH}\right), \tag{11}$$

and the r_{M1}, including the process variation error, can be defined as

$$r_{M1} = \frac{1}{\beta_1 E_{\beta 1}\left(V_{DS} + V_{ER} + V_G - V_{TH}E_{VTH1}\right)}. \tag{12}$$

A. MINIMIZING THE EFFECT OF THE R_1 VARIATION

To minimize the E_{R1}, a second resistor (R_2) constructed from the same material (hripoly) is added to the circuit. The added R_2 is accurately matched with the R_1; therefore, the process variation affects both resistors almost equally. In the case of precise matching, the maximum mismatch error is approximately 0.1 %. Mathematically, we have

$$\frac{E_{R1}}{E_{R2}} = 1 \pm 0.001(\text{max}). \tag{13}$$

Consequently, the variation of the R_2 (V_{R2}) is compared with the reference level (if $E_{R2} = 1$, then $V_{ER} = 0$ V), and the result is converted into a voltage (V_{ER}), which is added to the values of the V_G and V_D; the relevant result (V_C) is then led to the tunable resistor comprising the NMOS transistor M$_1$.

In order to demonstrate the circuit principle and to propose a design approach, the R_{AR} is specified to be 20 kΩ and is divided into two parts: $R_1 = 10$ kΩ and $r_{M1} = 10$ kΩ. The ratio of the R_1/r_{M1} should be defined carefully. Firstly, the r_{M1} value must be large enough to counterbalance the deviation in the R_1; secondly, an appropriate r_{M1} function must be found to compensate for the R_1 fluctuation. A notable problem consists in that the linear function of the resistor R_1 is compensated by the reciprocal function (8) of the resistor r_{M1}; this relationship is substituted with a linear curve inverted with respect to the R_1 (Fig. 3).

To minimize the variation of the r_{M1}, it appears more advantageous to select a higher V_G (see Fig. 1); such a choice, however, can limit the maximum voltage range of the circuit. For the selected V_G and the required r_{M1} (10 kΩ in this case), the design of the M$_1$ W/L can be accomplished. Then, the equivalent δV_{ER}, which will produce in the r_{M1} an increase identical with the decrease in the R_1 and vice versa, can be defined mathematically from (12) with the selected V_G and r_{M1} or, more accurately, by reading from the simulation. Due to the nonlinear shape of the r_{M1} curve, the change in the δV_{ER} is not symmetrical (Fig. 3(a)); thus, the operation point (V_G, r_{M1}) is shifted to a lower r_{M1} (a higher V_G). Then, a symmetrical change can be considered (Fig. 3(b)).

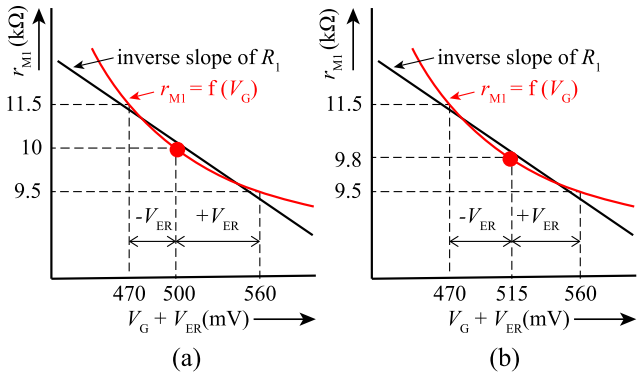

FIGURE 3. The relationship between the r_{M1} and the $V_G + V_{ER}$ with the (a) nonsymmetrical (b) and symmetrical δV_{ER}.

The sensitivity of the V_{ER} to the R_1 is assumed by using the R_2. This is mathematically expressed as

$$\delta R_1 = -\delta r_{M1}, \delta r_{M1} \mathrel{\widehat{=}} \delta V_{ER} \mathrel{\widehat{=}} V_{R2} = \delta R_2 / \delta R_1. \quad (14)$$

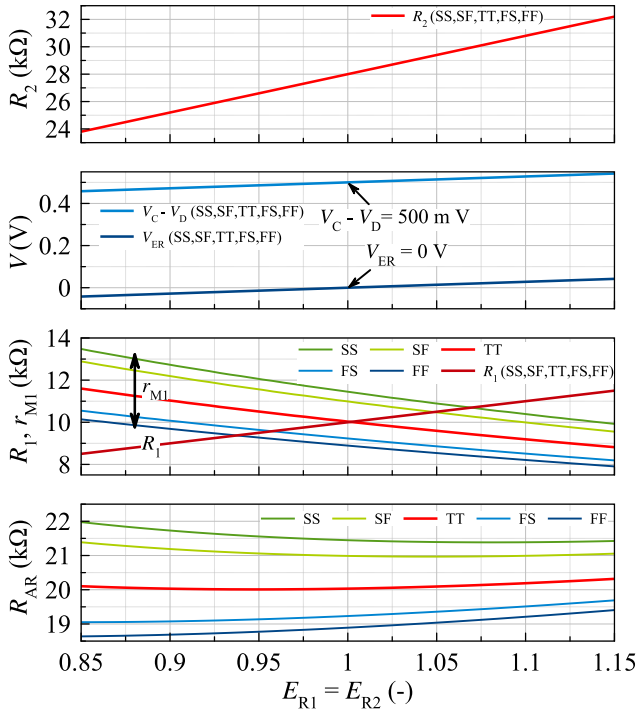

FIGURE 4. The DC sweep analysis of the circuit from Fig. 2, including the corners of the M_1 (SS, SF, TT, FS, FF).

The Cadence-based analysis of the circuit from Fig. 2 is shown in Fig. 4. The process variation in the hripoly resistors is represented by the sweep of the error coefficient E_{R1}; the mismatch errors are not included in the analysis, therefore $E_{R1} = E_{R2}$. In the hripoly, the manufacturer specifies a maximum deviation of up to ± 15 % from the nominal value; thus, the R_1 is multiplied with the E_{R1}, which changes from 0.85 to 1.15. Mathematically, this is

$$\delta R_1 = R_1 E_{R1}; \quad (15)$$

The impact of the process corners is obvious from the above results. Fig. 4 indicates that both of the illustrated voltages (V_{ER} and $V_C - V_D$) are unaffected by the process corners of the MOSFET.

B. MINIMIZING THE EFFECT OF THE r_{M1} VARIATION

However, as the V_{TH} fluctuates at the corners while the voltages are constant, the overdrive voltage (V_{OV}) is different. Thus, the V_{OV} produces fluctuation of the r_{M1} and, consequently, the R_{AR} ($20^{+10\%}_{-7.5\%}$ kΩ); this is undesirable, and the deviation should be lowered. Another NMOS transistor, denoted as M_2, is therefore added to the circuit instead of the constant voltage level shifter (V_G DC source), according to Fig. 5.

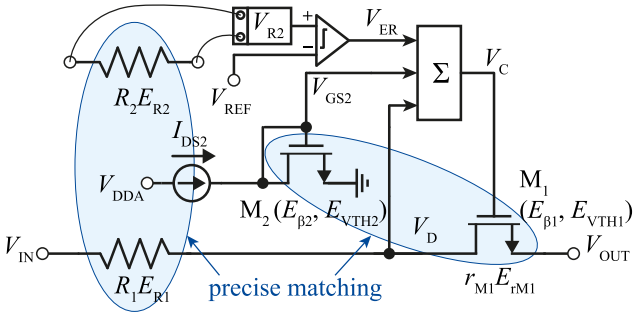

FIGURE 5. A simplified schematic of the proposed active resistor extended with the M_2.

For R_{AR}, we can write

$$R_{AR} = R_1 E_{R1} + \frac{1}{\beta E_{\beta 1} (V_{DS} + V_{ER} + V_G - V_{TH} E_{VTH1})}, \quad (16)$$

where

$$V_{ER} = V_{R2} E_{R2} - V_{REF} = I_{R2} R_2 E_{R2} - V_{REF}. \quad (17)$$

Now, the level shifter is made up of the M_2, the drain of which is shorted to its gate, forcing the transistor to operate in the saturation mode with a constant gate-to-source voltage (V_{GS2}). The transistors M_1 and M_2 are precisely matched; thus, $E_{\beta 1}/E_{\beta 2} = E_{VTH1}/E_{VTH2} = 1 \pm 0.001$. In terms of completeness, it should be noted that these transistors operate in different modes. As was mentioned earlier, the M_1 operates in the triode region, while the M_2 operates in saturation, meaning that the V_{GS2} voltage is expressed from the MOSFET drain-to-source current formula for the saturation mode as

$$V_{GS2} = \sqrt{\frac{2 I_{DS2}}{\beta_2 E_{\beta 2}}} + V_{TH} E_{VTH2}, \quad (18)$$

when the channel length modulation is ignored.

Now, assume $E_{\beta 1} = E_{\beta 2}$, $E_{VTH1} = E_{VTH2}$. By substituting (18) into (12), we obtain

$$r_{M1} = \frac{1}{\beta_1 E_{\beta 1}\left(V_{DS} + V_{ER} + \sqrt{\frac{2I_{DS2}}{\beta_2 E_{\beta 2}}}\right)} = \frac{1}{\beta_1\left(E_{\beta 12}V_{DS} + E_{\beta 12}V_{ER} + \sqrt{E_{\beta 12}}\sqrt{\frac{2I_{DS2}}{\beta_2}}\right)}. \quad (19)$$

Equation (19) shows that the $V_{TH}E_{VTH}$ parameter was cancelled out; nevertheless, the error parameter $E_{\beta 12}$ ($E_{\beta 1} = E_{\beta 2} = E_{\beta 12}$) was not fully reduced. The error of V_G is reduced to $\sqrt{E_{\beta 12}}$, and both the V_{DS} and the V_{ER} are still subject to $E_{\beta 12}$. However, as will be shown later, the V_{DS} is kept low, similarly to the V_{ER}. We can write $(V_{DS}, V_{ER}) \ll V_G$. An analysis of the circuit from Fig. 5 is shown in Fig. 6.

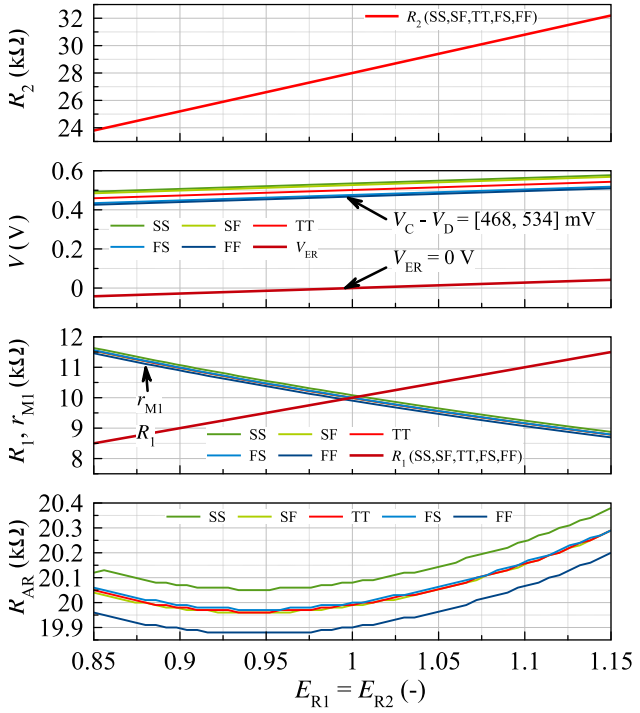

FIGURE 6. The DC sweep analysis of the circuit from Fig. 5, including the corners of the MOSFETs (SS, SF, TT, FS, FF).

As is presented in Fig. 6, the $(V_C - V_D)$ voltage is not permanently constant (Fig. 4) but varies according to the M_1 parameters' fluctuation (β_1, V_{TH1}). Thanks to this property, it is possible to minimize the r_{M1} fluctuation and, consequently, the R_{AR}, whose fluctuation decreases from $20^{+10\%}_{-7.5\%}$ kΩ to $20^{+2\%}_{-0.75\%}$ kΩ.

Equation (16), where the R_{AR} is described, can be modified to read

$$R_{AR} = R_1 E_{R1} + \frac{1}{\beta_1 E_{\beta 1}\left(V_{DS} + V_{ER} + \sqrt{\frac{2I_{DS2}}{\beta_2 E_{\beta 2}}}\right)}. \quad (20)$$

C. MINIMIZING THE EFFECT OF THE V_{DS} VARIATION

The preceding portions of the section discussed the impact of the process variation on the R_{AR}; however, as shown in (19), the MOSFET resistance depends on the V_{DS}. When the $V_{IN} - V_{OUT}$ increase, the V_{DS} grows too, and, consequently, the R_{AR} (r_{M1}) will decrease, as illustrated in Fig. 7.

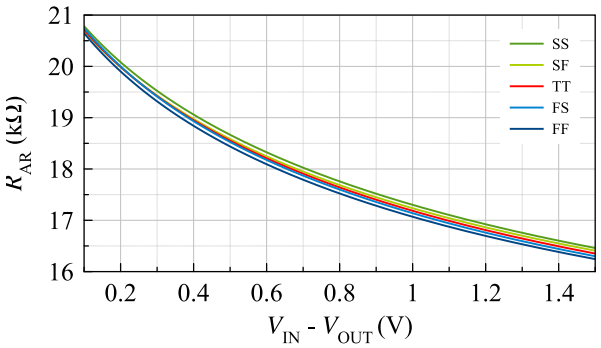

FIGURE 7. The R_{AR} as a function of the voltage on the active resistor ($V_{IN} - V_{OUT}$) for different MOSFET process corners (SS, SF, TT, FS, FF).

Fig. 7 demonstrates that the R_{AR} decreases from 20.8 kΩ at $V_{IN} - V_{OUT} = 100$ mV down to 16.3 kΩ at $V_{IN} - V_{OUT} = 1.5$ V; this variation becomes excessively large, and the impact of different V_{DS} must be suppressed. The body effect can be used to perform such a step. The simplest solution is to connect the bulk of the M_1 to a voltage source, whose voltage will decrease with increasing V_{DS}. This configuration can be implemented by using the circuit in Fig. 8.

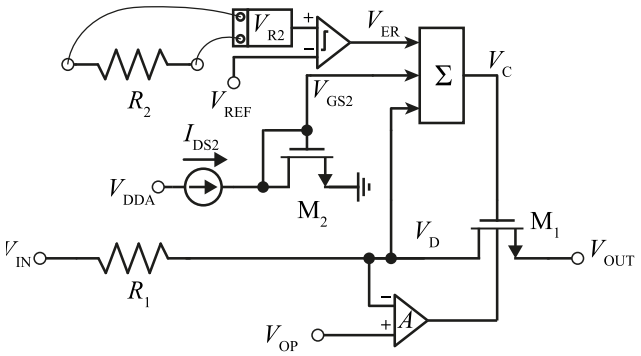

FIGURE 8. A simplified schematic of the proposed active resistor with the V_{DS} compensation circuit.

In Fig. 8, the V_{OP} is equal to the V_{DS} voltage at the operational point (100 mV in this case), for which the r_{M1} was designed. The operational amplifier's inverting input is connected to the V_D. When the V_D increases, the V_{BS} decreases, resulting in a higher V_{TH1} and, consequently, lower V_{OV}; the entire process then causes the channel resistance (r_{M1}) to increase. Mathematically, this is expressed as

$$R_{AR} = R_1 E_{R1} + \frac{1}{\beta_1 E_{\beta 1}\left(V_{DS} + V_{ER} + \sqrt{\frac{2I_{DS2}}{\beta_2 E_{\beta 2}}} - \delta V_{TH1}\right)}, \quad (21)$$

where

$$\delta V_{TH1} = \gamma \left(\sqrt{2\,|\phi_F| + V_{SB1}} - \sqrt{2\,|\phi_F|} \right). \tag{22}$$

Thus, in (21), $V_{DS} - \delta V_{TH1} = 0$ should be satisfied.

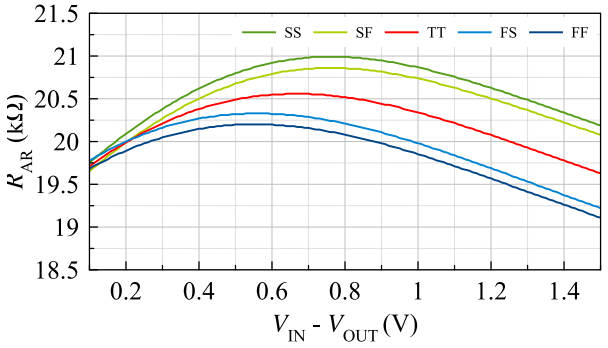

FIGURE 9. The R_{AR} with the V_{DS} compensation circuit as a function of the voltage on the active resistor ($V_{IN} - V_{OUT}$) for the different MOSFET process corners (SS, SF, TT, FS, FF).

Fig. 9 shows the results of the improved circuit. The fluctuation varies from 19.1 kΩ to 21 kΩ over the process corners. The lowest fluctuation occurs at the lowest $V_{IN} - V_{OUT}$ voltages due to the lower V_{DS}. The impact of the V_{DS} comprising $E_{\beta 1}$ ($= E_{\beta 12}$) was demonstrated in (19). In order to minimize this error, a R_{AR} design with a smaller proportion of the r_{M1}, under the conditions described in this section, should be chosen.

A simple procedure to implement the V_{DS} compensation circuit will be outlined in the next section.

IV. CIRCUIT DESIGN ON THE TRANSISTOR LEVEL

In this section, the implementation the active resistor at the transistor level will be described. The circuit utilizes the band-gap reference (IP core), which provides the V_{REF} and bias voltages (V_{BN}, V_{BP}) for the current sources. The circuit power supply is 1.5 V. The R_{AR} value is set to be 50 kΩ and will be employed in the practical examples comprised within Section IV. As mentioned in the previous section, there are two major requirements on the MOSFET resistor (r_{M1}): The r_{M1} value must be large enough to have the ability to counterbalance the deviation in the R_1, and an appropriate r_{M1} function must be found to compensate for the R_1 fluctuation. In Section III-A, we showed that the V_{DS} voltage significantly affects the resistor accuracy. In order to minimize the V_{DS} fluctuation, the MOS resistance (r_{M1}) is designed to be as small as possible. The minimum value of the r_{M1} is given by the maximum R_1 deviation, which is 15 % for the TSMC 180 nm technology. However, the r_{M1} cannot reduce its resistance to zero, and thus a higher value must be chosen (see Section III-A).

Fig. 11 shows a complete schematic of the active resistor. The summing block, together with the level shifter block, is implemented by using a differential difference amplifier (DDA), whose output voltage (V_C) can be determined from the formula

$$V_C = V_{R2} - V_{REF} + V_D + V_{GS2}. \tag{23}$$

The measurement of the R_2 deviation is performed via a simple series connection of the current reference source (M_{I3b}) and the R_2 with one node grounded. Then, the voltage at the second node of the R_2 is measured (V_{R2}) and led to the DDA differential input, where it is compared with the reference voltage (V_{REF}). The difference ($V_{R2} - V_{REF}$) corresponds to the V_{ER} from Fig. 8 and is zero in the case of a typical process.

The voltage level shifter consists of the M_2 and a current source (M_{I4b}). The shift voltage was expressed in (18), where $I_{DS2} = I_{B2}$. The bias voltages for both the current sources (M_{I3b}, M_{I4b}) and the reference voltage (V_{REF}) are generated from the IP core cell.

In designing the R_{AR}, the basic problem rests in the approach to dividing it into smaller parts in order to achieve the maximum voltage range and to minimize the effect of the V_{DS} (Section III-C).

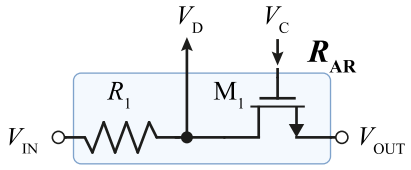

FIGURE 10. The basic implementation of the R_{AR}.

If we assume that the V_{OUT} is grounded and the R_{AR} consists of resistors, as is shown in Fig. 10, the circuit minimum input voltage ($V_{IN(min)}$) is affected most strongly by the input voltage range of the DDA and the I_{B2} current source. Since the I_{B2} is implemented by using a NMOS transistor, its operation in the saturation region must be guaranteed. The voltage on the bottom noninverting DDA input is given as

$$V_D = V_{IN} \frac{r_{M1}}{R_{AR}} \tag{24}$$

With the hripoly resistor tolerance of 15 %, the value of the r_{M1} should be $r_{M1} \geq 0.15\, R_{AR}$. Fig. 11 indicates that the r_{M1} is set to be 20 ± of R_{AR}. In this case, the minimum voltage between the drain-source of the M_{I4b} ($V_{IB2(min)}$) is 100 mV, which corresponds to $V_{IN(min)} = 500$ mV. In order to reduce the $V_{IN(min)}$, the R_1 is divided into two identical resistors (R_{1A} and R_{1B}), as illustrated in Fig. 12.

Then, (24) can be rewritten as

$$V_D = V_{IN} \frac{r_{M1} + R_{1B}}{R_{AR}}. \tag{25}$$

Now, if $V_{IB2(min)} = 100$ mV, $V_{IN(min)} = 167$ mV. The $V_{IN(min)}$ significantly decreases and can be mathematically described as

$$V_{IN(min)} = V_{IB2(min)} \frac{R_{AR}}{r_{M1} + R_{1B}}. \tag{26}$$

This expression is valid only for zero difference between the V_{R1} and the V_{REF}. In order to cancel out the requirement

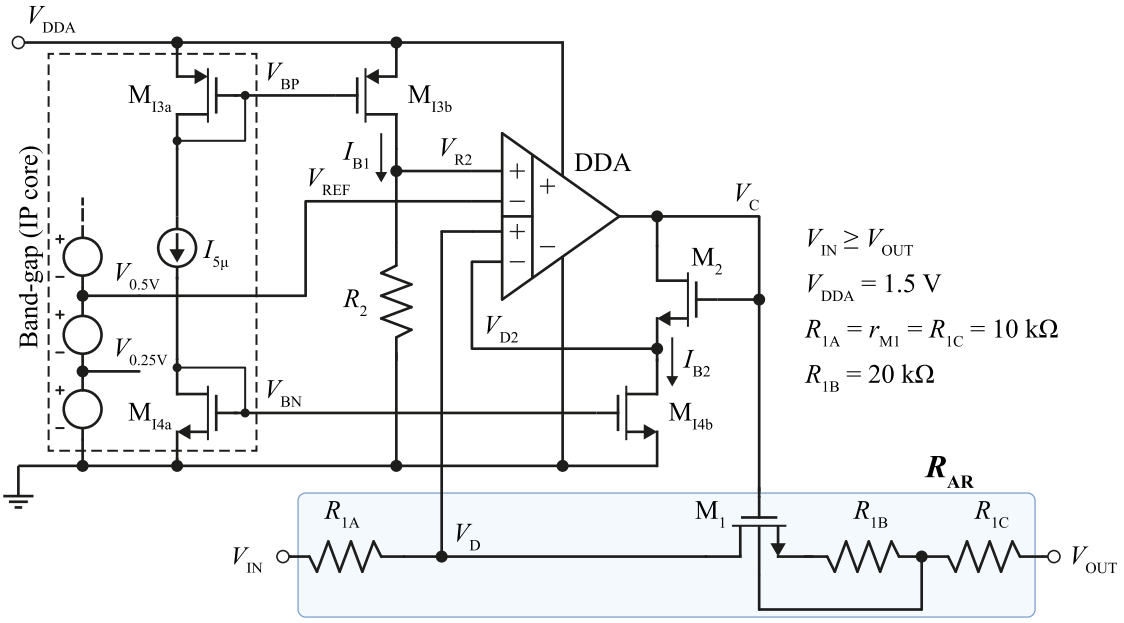

FIGURE 11. The circuit implementation of the proposed active resistor.

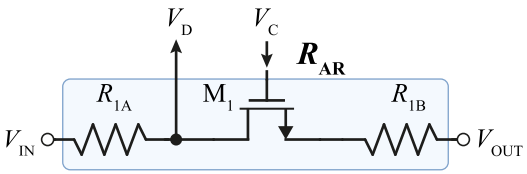

FIGURE 12. An advanced implementation of the R_{AR}.

for $V_{IN(min)} = 0.175$ V, the differential voltage is set to $V_{IB2(min)}$. Mathematically, this is

$$V_{R2} = V_{IB2(min)} + V_{REF}. \tag{27}$$

The maximum voltage across the R_{AR} ($V_{IN(max)}$) is limited by the maximum DDA output voltage (V_C), which is almost equal to the V_{DDA}. For the V_C, we have

$$V_C = \frac{V_{IN(max)}\,(R_{AR} - R_{1A})}{R_{AR}} + V_{R2} - V_{REF} + V_{GS2}. \tag{28}$$

The $V_{IN(max)}$ can be derived from (28):

$$V_{IN(max)} = \frac{(V_C + V_{REF} - V_{R2} - V_{GS2})\,R_{AR}}{R_{AR} - R_{1A}}. \tag{29}$$

Fig. 7 demonstrates the impact of different V_{DS} on the R_{AR}, which decreases with increasing V_{DS}. Therefore, the resistor R_{1B} is subdivided into two parts, R_{1B} and R_{1C}, when the body terminal of the M_1 is connected in between, as illustrated in Fig. 11. Then, as the V_{DS} rises, the threshold voltage (V_{TH1}) increases, decreasing the V_{OV1}. This results in a rising r_{M1}, and the effect is in the direction opposite to that of the V_{DS} effect. As a result, the R_{AR} becomes almost constant even when the V_{DS} varies. As mentioned earlier, the $V_{IN(min)}$ is affected by the input voltage range of the DDA, and the $V_{IN(max)}$ is limited by the maximum output voltage of the DDA. To meet the design requirements, as mentioned above, we chose the current mirror DDA topology with the PMOS input pair. Also, note that this is the ideal output structure for a wide swing amplifier because no cascodes are employed.

A. IMPACT OF THE CIRCUIT NONIDEALITIES

In addition to the above error sources, many other sources occur in the transistor level circuit from Fig. 11. The error sources can be divided into two parts: reference source errors and DDA nonideal parameters.

The IP core band-gap circuit output voltage and current tolerance is ±1 %. The reference voltage $V_{REF} = 750$ mV leads directly to the DDA input, whereas the current reference sources are additionally influenced by the current mirror mismatch errors (pairs M_{I3a} - M_{I3b} and M_{I4a} - M_{I4b}). Another negative property is the finite output resistance. In order to reduce the impact of these errors, MOSFETs are designed with large lengths. The reference current I_{B1} including the errors is given as

$$I_{B1} = I_5 E_{BG} \frac{W_{I3b} L_{I3a}}{L_{I3b} W_{I3a}} E_M\,(1 + \lambda V_{DSI3b}), \tag{30}$$

where E_{BG} is the band-gap current (I_5) tolerance (±1 %), E_M is the matching error of the pair M_{I3a} - M_{I3b} (±0.6 %), and λ is the channel length modulation of the M_{I3b}. (0.009 V^{-1}).

The maximum error of the I_{B1} (10 μA) calculated from (30) corresponds to 0.2 μA. This current is converted into the V_{R2} error offset, which is 10 mV. When the V_{REF} error is ±1 %, the worst-case V_{ER} offset is given by the sum

of the V_{R2} and V_{REF} errors, which amounts to 15 mV. In the Cadence simulation, a 15 mV V_{REF} offset corresponds to a 200 Ω error in R_{AR}.

The error of the other current source, I_{B2}, generates an error in the DC voltage shift, due to a different current through the M_2; such a scenario then results in a different V_{GS2}. From (30), the maximum error is 0.08 μA, which corresponds to the V_{GS2} increase of 3.37 mV and the r_{M1} of +50 Ω (data from the simulator).

The relationship concerning the DDA output voltage was shown in (23). The accurate version includes nonideal parameters, such as the common-mode rejection ratio ($CMRR$), DC voltage open-loop gain (A_V), and voltage offset (V_{OFF}); this version is defined by [34].

$$V_C = A\,(V_{R2} - V_{REF} + BV_D - V_{OFF}) + V_D + V_{GS2}, \quad (31)$$

where

$$A = 1 + \frac{2}{CMRR} - \frac{1}{A_V}, \quad (32)$$

and

$$B = \frac{1}{CMRR} - \frac{1}{A_V}. \quad (33)$$

For the DDA parameters $A_V = 65$ dB, $CMRR = 82$ dB, and $V_{OFF} = \pm 1.2$ mV, the V_C error calculated by using (31) is −14 mV ($V_{OFF} = -1.2$ mV) or +6 mV in the case of $V_{OFF} = +1.2$ mV.

All of the errors were converted into a V_C offset. The worst case scenario would materialize if the errors were added together, even though the probability of such a situation is very low. Thus, 32.5 mV is the maximum offset error, which causes the deviation of up to 430 Ω in R_{AR}. All of the effects described above are included in the analysis in Section IV-B.

B. SIMULATION RESULTS

The process-compensated active resistor was designed with the TSMC 180 nm technology. The performance of the circuits was analyzed with Corner and Monte Carlo; the latter analysis comprised two thousand samples for the global and local process variations. Power supply variations affect the parameters of the DDA and the band-gap; these effects are included in the errors mentioned in Section II. The DC power supply voltage was set to equal $V_{DDA} = 1.5$ V, and all the transistors were of a medium V_{TH}. To analyze the circuit in the full voltage range, the terminal V_{OUT} was grounded in all of the following cases, even though any voltage can be connected to it; however, the condition of $V_{OUT} \leq V_{IN}$ must be satisfied. Next, the R_{AR} (50 kΩ) is subdivided into four parts ($R_{1A} = R_{1C} = r_{M1} = 10$ kΩ and $R_{1B} = 20$ kΩ), as illustrated in Fig. 11. The bias currents are set to be $I_{B1} = 10$ μA, $I_{B2} = 4$ μA. The DDA unity gain bandwidth is 2 MHz, and the DC open loop gain amounts to 65 dB.

Fig. 13(a) shows the R_{AR} as a function of $(V_{IN} - V_{OUT})$ in the fifteen process corners. Fig. 13(a) indicates that the input voltage range is the range of 0.1 V - 1.2 V. The resistance (R_{AR}) differs from its desired value by not more than 4 % at $V_{IN} = 1.2$ V. The linearity error is shown in Fig. 13(b). The maximum deviation from 50 kΩ is 0.35 % in the typical process conditions.

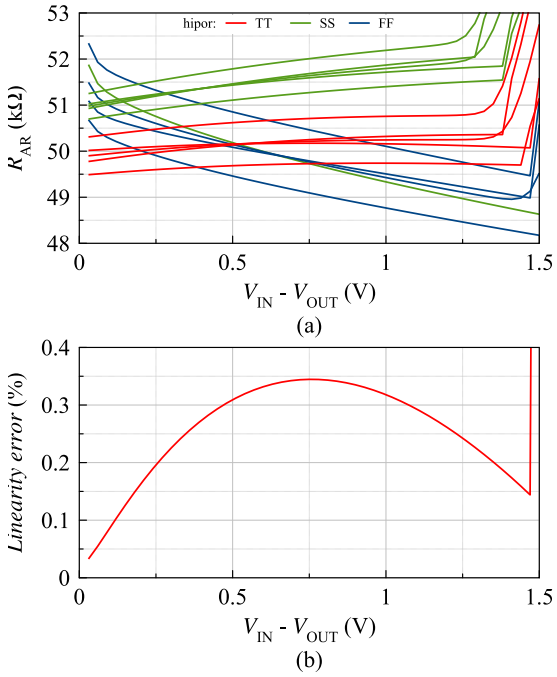

FIGURE 13. The voltage dependence of (a) the R_{AR} in the different process corners (MOSFET: SS, SF, TT, FS, FF; hipor: SS, TT, FF), and (b) the linearity error in the typical corners.

The Monte Carlo analysis comprising two thousand samples for the global and local process variations to determine the standard variation is shown in Fig. 14. There are six plots for different $(V_{IN} - V_{OUT})$ and temperatures. The lowest value is $\sigma = 289.5$ Ω at $(V_{IN} - V_{OUT}) = 0.2$ V and T = 27 °C; the highest value corresponds to $\sigma = 603$ Ω at $(V_{IN} - V_{OUT}) = 1.2$ V and $T = -20$ °C, constituting the deviation of only 1.2 % from the nominal value.

Fig. 15 shows the R_{AR} as a function of temperature in the different process corners. As shown in Fig. 15, the maximum temperature coefficient of the proposed current reference circuit is $TCR = 620$ ppm/°C over the industrial temperature range.

V. APPLICATION EXAMPLE

In this section, two practical application examples demonstrating the functionality of the novel active resistor are introduced: One illustrates the use of the proposed resistor in a transconductor circuit, whose gm accuracy depends on the resistor accuracy, and the other exposes the use of the same resistor in designing a high accuracy current reference circuit. The designed current reference is compared to that presented in similar papers related to the topic (Table 1).

A. TRANSCONDUCTOR

The transconductor is a versatile building block employed in many analog and mixed-signal circuit applications, such as continuous-time filters, delta-sigma modulators,

TABLE 1. The parameters of the proposed current reference compared to the data presented within similar papers.

Ref.	Process (μm)	V_{DD} (V)	I_{REF} (μA)	Power (μW)	Type of resistor	Area mm^2	σ/mean (%)	TC (ppm/°C)	T range (°C)	Max. var. (%)	Measured/ Simulated	Trim./ Cal.
[38]	0.18	1.5	1.7	-	R	-	-	-	-40 - 150	±15.67	Sim.	No
[39]	0.18	2	10	80	MOS	-	4.26	170	-20 - 120	-	Sim.	No
[40]	0.35	1.5	0.00914	0.109	MOS	0.035	2.16	44	0 - 80	±6.5	M.	No
[41]	0.18	1.8	3	78.29	MOS	0.0066	1.69	1088	0 - 100	±8.56	Sim.	No
[41]	0.18	1.8	3	78.9	MOS	0.007	-	1080	0 - 100	±3.17	Sim.	Trim.
[43]	0.18	-	51.2	-	R(external)	0.0312	2.7	-	-	-	M.&Sim.	No
[44]	0.18	1.5	0.001	0.0045	MOS	0.322	0.25	289	-20 - 80	±1.57	M.	Cal.
[45]	0.18	0.9	0.371	2	MOS	-	16.1	2251	-40 - 100	-18/+12.6	Sim.	No
[46]	0.18	0.8	0.0166	0.0486	R	0.054	4.65	241	-40 - 120	-8.8/+17	M.&Sim.	No
This work	0.18	1.5	10	150	R-MOS	0.0297	1.634	32	-20 - 85	±5.5	Sim.	No

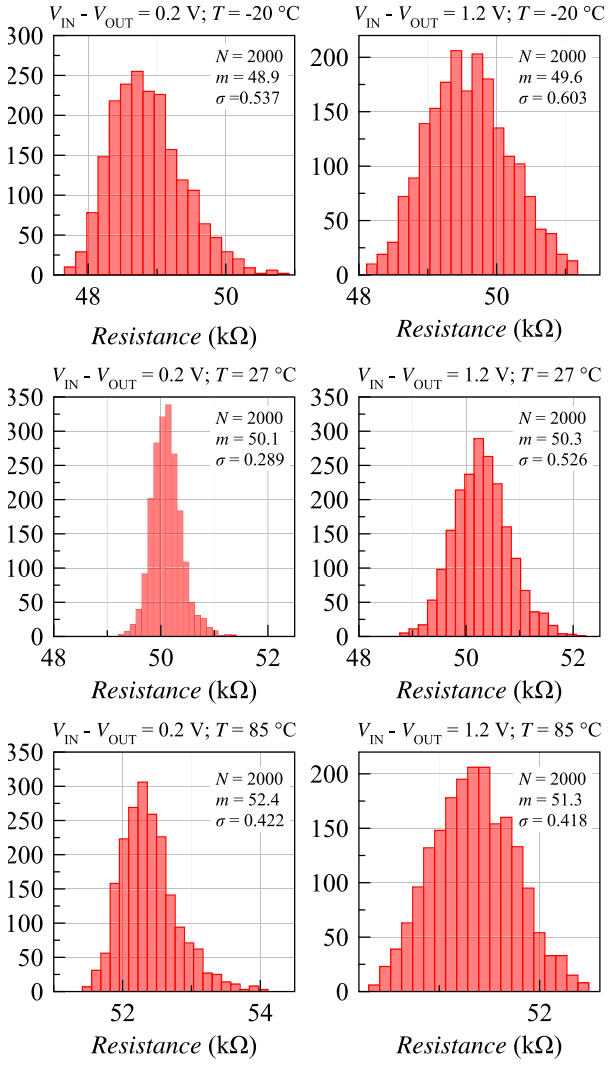

FIGURE 14. The histograms of the R_{AR} for different ($V_{IN} - V_{OUT}$) and temperatures.

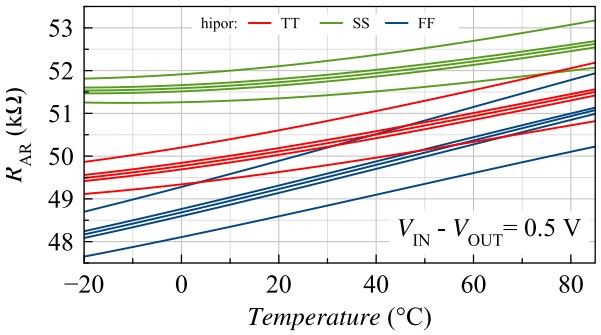

FIGURE 15. The resistance (R_{AR}) as a function of temperature in the different process corners (MOSFET: SS, SF, TT, FS, FF; hipor: SS, TT, FF).

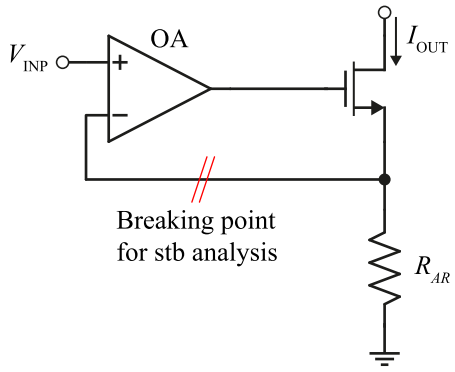

FIGURE 16. A simplified schematic of the transconductor.

data converters, current references and FPAAs (field programmable analog arrays). The transconductor performs voltage-to-current conversion. Linearity is one of the most critical requirements in the designing of transconductors. Fig. 16 shows the basic transconductor circuit allowing the input voltage to control the output current.

Because of the virtual short between the input terminals, the inverting input is bootstrapped to within microvolts (or millivolts) of the noninverting input. Since the voltage V_{INP} appears across the R_{AR}, the output current is $I_{OUT} = V_{INP}/R_{AR}$. The output current (I_{OUT}) accuracy (and g_m) depends on the accuracy of the resistor and the operational amplifier's parameters. The previous sections pointed to poor accuracy of IC passive resistors. In this context, one option lies in using trimming to produce accurate resistors, while another one is to employ off-chip discrete resistors, which exhibit high accuracy (typically 1 % or less); these components, however, must be used externally. Such a condition implies a higher cost and also raises other issues, including the number of pins that can be utilized to connect

the resistor to the internal circuitry. Yet another option then consists in utilizing a switched-capacitor technique.

To obtain high accuracy, a novel R_{AR} resistor with 50 kΩ is applied; the circuit is identical with that presented in Section IV. Then, we have $g_m = 1/R_{AR} = 20\ \mu$S. The accuracy of the g_m is proportional to that of the resistor. The impact of the operational amplifier is negligible with respect to its very high gain (100 dB), *CMRR* (>100 dB), and offset (0.5 mV). The parameter g_m is given by

$$g_m = \frac{I_{OUT}}{V_{IN}} = \frac{A_V}{R_{AR}\,(A+1)} + \frac{V_{OFF}}{V_{INP}R_{AR}}, \tag{34}$$

where A_V is the open-loop gain of the operational amplifier and V_{OFF} denotes the of the operational amplifier's offset.

The results from the 250 corner analysis runs (where $V_{INP} = 500$ mV) are $I_{OUT(min)} = 9.6\ \mu$A and $I_{OUT(max)} = 10.2\ \mu$A, with the standard deviation being $\delta I_{OUT}(\sigma) = 69.5$ nA (0.7 %). Next, the outcome of the spectral analysis is shown in Fig. 17; the amplitude of the input sinewave equals 200 mV, with the frequency amounting to 100 Hz. The resulting parameters are: $SNDR = 70.6$ dB, $SFDR = 73.6$ dB, and $THD = 0.02$ %.

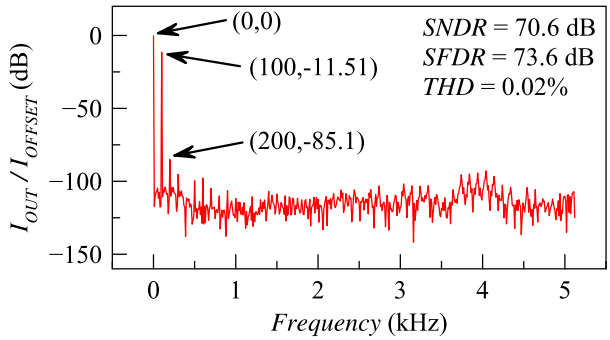

FIGURE 17. The spectral analysis of the transconductor.

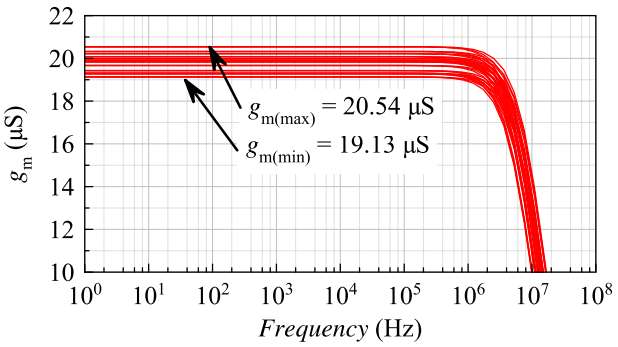

FIGURE 18. The closed-loop transfer function magnitude response of the transconductor (45 corners: MOSFET, hipor, and mimcap).

The frequency response of the transconductor is represented in Fig. 18; the figure includes the corner analysis comprising the process variation of the MOSFET, hipor resistors, and mimcaps. These individual branches of the analysis counted 45 runs altogether.

The operational amplifier finds use in a simple voltage follower configuration. However, this is not the optimal arrangement in terms of the capacitive loading and potential risk of oscillations; thus, the system stability must be evaluated from the open feedback loop.

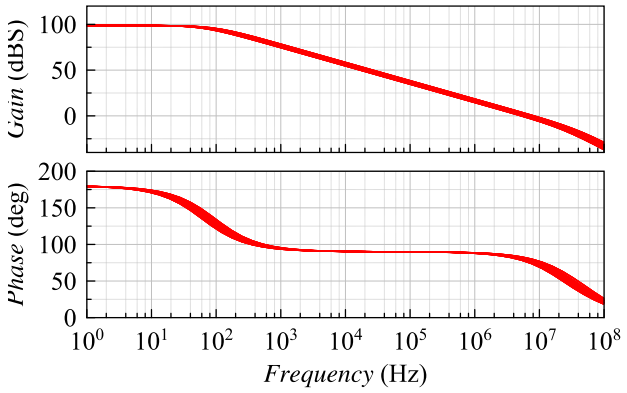

FIGURE 19. The transconductor open loop gain stability analysis in the different process corners (MOSFET, hipor, mimcap).

The results in Fig. 19 demonstrate that the proposed system is stable (phase margin > 60 dB); in the relevant schematic, the breaking point for the stability (stb) analysis is shown.

B. SELF-BIASED CURRENT REFERENCE

This section will introduce a self-biased current reference circuit that takes advantage of the novel active resistor. Multiple current references with high accuracy and low-temperature variations can be found in several relevant papers and books [35]–[38], [38]–[41]; however, most articles do not discuss the process variations.

The proposed self-biased current reference circuit is shown in Fig. 20. The basic part of the circuit is Beta-multiplier reference. The Beta-multiplier embodies an example of a circuit that uses positive feedback. The addition of the resistor R_{AR1} reduces the closed loop gain (a positive feedback system can be stable if its closed loop gain is smaller than one). By decreasing the size of the resistor, however, we increase the gain of the loop and push the feedback system closer to instability. An example of when this could occur is the scenario where the parasitic capacitance between the source of M_2 and ground is large (effectively shorting the M_2 source to ground). If the resistor, for instance, is bonded off-chip to set the current, the bias circuit is likely to oscillate [42]. In any self-biased circuit, there are two possible operating points; therefore, a start-up circuit is included in Fig. 20.

To obtain the V_{DDA}, V_{BP}, and V_{BN}, the external band-gap reference is not used. All of the signals are generated inside the circuit. The increase in the output resistance of the current mirrors (M_1 - M_2, M_3 - M_4) is achieved by adding six transistors (M_5 - M_{10}); this significantly helps to lessen the sensitivity to the power supply. The maximum fluctuation of 5 % is considered in the analyses. The bias voltages V_{BP} and V_{BN} are generated by the V_{GS4} and V_{GS1}. The current

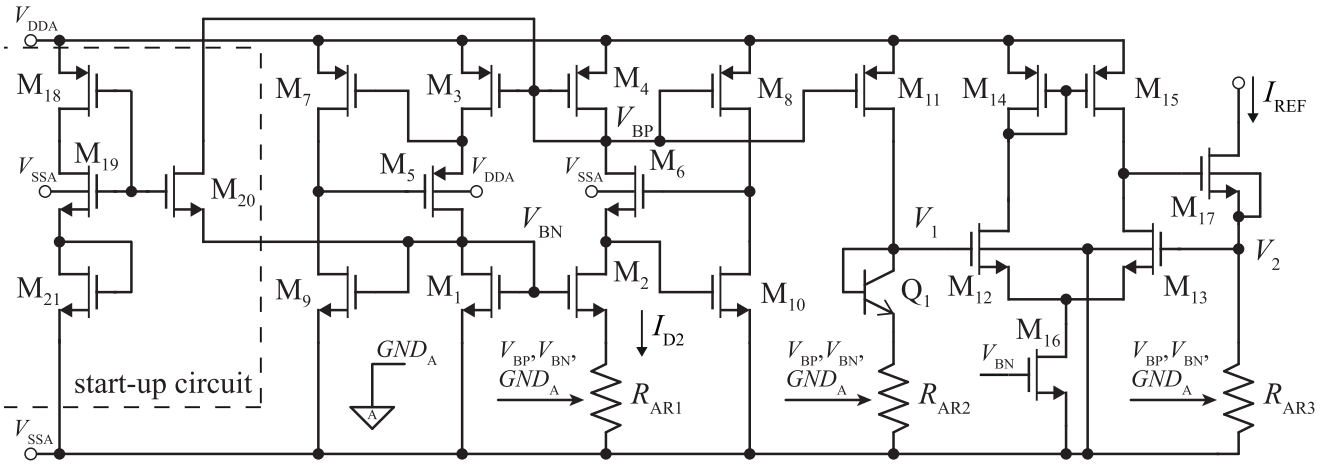

FIGURE 20. The transistor-level schematic of the proposed current reference. The circuit power supply is ($V_{DDA} - V_{SSA}$) = 1.5 V and $GND_A = (V_{DDA} - V_{SSA})/2$.

mirror consisting of the M_3 and M_4 sets the same current to flow through the M_1 and M_2. This current can be defined as

$$I_{D2} = \frac{V_{GS1} - V_{GS2}}{R_{AR1}} = \frac{\sqrt{\frac{2I_{D2}}{\beta_1}} - \sqrt{\frac{2I_{D2}}{\beta_2}}}{R_{AR1}}. \quad (35)$$

The numerator value ($V_{GS1} - V_{GS2}$) increases with temperature; thus, the I_{D2} exhibits the IPTAT character, similarly to the I_{B1} and I_{B2} (see Fig. 11), which are derived from it. Consequently, the R_{AR} decreases with temperature. These two effects act against each other, yielding a slightly positive temperature coefficient.

Then, the current I_{D2} is mirrored to the collector of Q_1 through the M_4 to M_{11}. The collector voltage, denoted as V_1, reads

$$V_1 = V_T ln\left(\frac{NI_{D2}}{I_S}\right) + NI_{D2}R_{AR2}, \quad (36)$$

where $N = W_{11}/W_4$.

The collector of Q_1 is connected to the NMOS differential-pair with an active load, which, together with the M_{17} and R_{AR3}, performs the voltage-to-current conversion. The reference current is given by

$$I_{REF} = \frac{V_2}{R_{AR3}}. \quad (37)$$

Ideally, for the temperature-independent I_{REF}, we have

$$\frac{\delta I_{REF}}{\delta T} = 0 = \frac{\delta V_2}{\delta T} + \frac{\delta R_{AR3}}{\delta T} = \frac{\delta V_{BE1}}{\delta T} + \frac{\delta R_{AR1}}{\delta T} + \frac{\delta R_{AR3}}{\delta T}. \quad (38)$$

The corner analysis comprises forty-five combinations of process corners (MOS, BJT, resistors). Fig. 21 shows the I_{REF} as a function of temperature. The worst case scenario occurs when the temperature reaches −20 °C, that is, I_{REF} (μA) ∈ [9.38, 10.48]; such a situation corresponds to 9.93 μA ±5.5 %. The Monte Carlo analysis comprising two

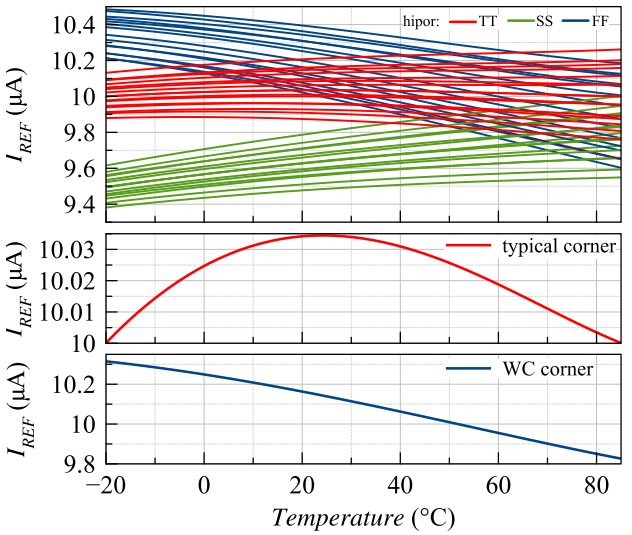

FIGURE 21. The current (I_{REF}) as a function of temperature in the different process corners (MOSFET: SS, SF, TT, FS, FF; BJT, SS, TT, FF, and hipor: SS, TT, FF). All typical corners and the worst case scenario are illustrated below.

thousand samples for the global and local process variations to determine the standard variations is shown in Fig. 22. There are four plots for different temperatures; the lowest value is σ = 89.9 nA at T = 85 °C, and the highest one corresponds to σ = 161.5 nA at T = −20 °C. This amounts to a deviation of 1.634 % as related to the mean value.

Table 1 shows the performance of the proposed current reference circuit compared to the data presented within already published papers. The deviation of the reference current is expressed as standard deviation over mean value in the fourth column. The seventh column introduces the maximum error in the reference current, considering the combined effect of the process variations and temperature change in the given range (Table 1). The maximum variation of the proposed reference current is 5.5 % without trimming.

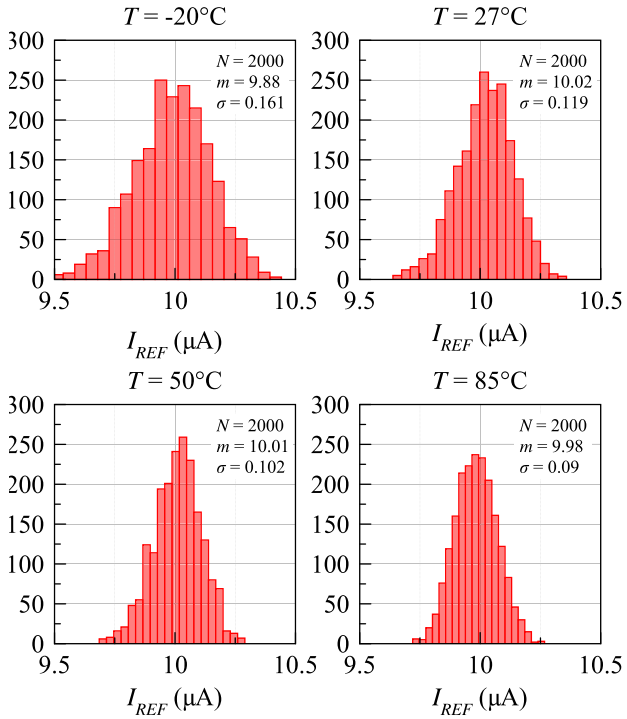

FIGURE 22. The histograms of I_{REF} for different Temperatures.

VI. CONCLUSION

A novel active resistor circuit that compensates for the process and temperature variations without any extra trimming is proposed. The corner simulations indicate that the maximum variation in the active resistor is 6.2 % and 1.2 % in terms of the process and the temperature, respectively. The standard deviation of ±0.45 % was obtained via Monte Carlo simulations. The maximum temperature coefficient of the proposed current reference circuit is $TCR = 620$ ppm/°C over the industrial temperature range. The linearity error is determined by the maximum deviation from 50 kΩ, and it amounts to 100 Ω in the typical process conditions. Two practical application examples are introduced in Section V: One illustrates the use of the proposed resistor in the transconductor circuit, whose g_m variation is less than 4.2 %, and the other demonstrates the usability of the proposed resistor in designing the high accuracy current reference circuit. Based on the Corner simulations, the maximum error in the proposed reference current is ±5.5 %, considering the combined effect of the process variations and temperature change from −20 °C to 85 °C. The highest standard deviation value is $\sigma = 161.5$ nA at $T = -20$ °C.

ACKNOWLEDGMENT

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VILEM KLEDROWETZ was born in Zlin, Czech Republic, in 1985. He received the M.Sc. and Ph.D. degrees, majoring in microelectronics circuits, in 2009 and 2014, respectively, and graduated from the Faculty of Electrotechnical Engineering and Communication, Brno University of Technology (BUT). He is currently working as a Research Fellow with the Department of Microelectronics, BUT. He is focused on the design of analog integrated circuits, especially AD and DA converters.

JIRI HAZE was born in Nachod, Czech Republic. He received the M.Sc., Ph.D., and Ass. Prof. degrees from the Faculty of Electrical Engineering and Communication, Department of Microelectronics, University of Technology, Brno, Czech Republic, in 2002, 2005, and 2009, respectively. He is currently working as an Associate Professor with the University of Technology. His research is in the field of integrated circuit design, where his interests include analog and mixed-mode integrated circuits design, signal processing, and sensor application.

ROMAN PROKOP was born in Velke Mezirici, Czech Republic. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Brno University of Technology, Czech Republic, in 1995 and 2009, respectively. He is currently working as an Assistant Professor with the Department of Microelectronics, Brno University of Technology. His research is in the field of integrated circuit design, where his interests include modern innovative analog circuits, current-mode circuits, analog signal processing, and digitally tunable analog circuits.

LUKAS FUJCIK received the M.Sc. and Ph.D. degrees in electrical engineering from the Brno University of Technology, Czech Republic, in 2002 and 2006, respectively. He is currently working as an Associate Professor with the Brno University of Technology. His research is in the field of the integrated circuit design, where his interests include oversampling $\Delta\Sigma$ modulators, digital signal processing, digital synthesis on chip, digital implementation, sensor signal digitization, and mixed-signal circuit design. He is a leader of the IC Design Research Group, Department of Microelectronics. He is the author/coauthor of more than 60 scientific articles and publications. He is/was the leader of several projects financed by the Czech Science Foundation in the field of integrated circuit design, digital signal processing, and smart sensor signal processing. He has professional activities with industries, i.e., Honeywell, S3Group, ON Semiconductor, ASICentrum, ViDiTech, and so on. He gained Rector's Award for excellent research activities in 2006.