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Technology Independent ASIC Based Time to Digital Converter

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ABSTRACT This paper proposes a design methodology for a synthesizable, fully digital TDC architecture. The TDC was implemented using a hardware description language (HDL), which improves portability between platforms and technologies and significantly reduces design time. The proposed design flow is fully automated using TCL scripting and standard CAD tools configuration files. The TDC is based on a Tapped Delay Line architecture and explores the use of Structured Data Path (SDP) as a way to improve the TDL linearity by homogenizing the routing and parasitic capacitances across the multiple TDL's steps. The studied approach also secures a stable, temperature independent measurement operation. The proposed TDC architecture was fabricated using TSMC 180nm CMOS process technology, with a 50MHz reference clock and a supply voltage of 1.8V. The fabricated TDC achieved an 111ps RMS resolution and a single-shot precision of 54ps (0.48 LSB) and 279ps (2.51 LSB), with and without post-measurement software calibration, respectively. The DNL across the channel is mostly under 0.3 LSB and a maximum of 8 LSB peak-to-peak INL was achieved, when no calibration is applied.

INDEX TERMS Application specific integrated circuit (ASIC), structured data path (SDP), time interval measurement, time-to-digital converter (TDC).

I. INTRODUCTION

Time-to-Digital Converters (TDC) have been extensively used in positron emission tomography (PET) and other experimental physics areas [1]–[3], and in high precision metrology equipment [4]. Current state-of-the-art Application Specific Integrated Circuits (ASIC) TDCs have already achieved precisions in the range of tens of picoseconds [5]–[13]. These advances have been escorted by a strong technological evolution in Field Programmable Gate Arrays (FPGA), which have become a platform of interest for TDC research applications, due to its low cost, fast development cycle and large flexibility. When analyzing ASIC and FPGA TDCs architectures, the major difference stands on the resolution defining logic element. When using a FPGA, the resources are predetermined by the device selected. When designing an ASIC, the possibility to create custom cells adds different TDC architecture implementation options, but also increases the overall design complexity.

With technology scaling down, key metrics such as performance, power consumption and area are expected to improve. However, this only holds true for digital designs, since not every analog circuit can be shrunk and thus benefit from the lower sized technologies [6]. Therefore, all-digital, synthesizable, TDC architectures have the potential to take full advantage of technology improvements and reach better performance in the long term. Moreover, modern applications demand not only high resolution and precision but also lower power consumption and small die area. For example, in automotive LiDAR applications, in order to scan a scene, a single laser-detector pair can be adopted, if a beam steering mechanism is used. However, this method reduces the maximum achievable frame rate. One possible alternative is to have multiple detectors capturing multiple reflected pulses in parallel. This solution requires multiple TDC channels and thus power and size become a major concern.

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Another major concern for industry applications is the development time, which is desirable to be as short as possible due to the highly competitive market. Usually, ASIC TDCs are systems that require carefully designed and tested cells with complex calibration circuitry. Even in full digital architectures, the cells responsible for defining the TDC resolution are designed and tested at transistor level. This greatly increases the development cycle, thus increasing costs and reducing portability between different technologies.

Although the transistor level cell design is required to achieve higher resolution and performance, when targeting new applications that require a resolution in the range of a few hundreds of picoseconds, an approach focused on portability and reduced development time is certainly advantageous. This may be achieved by adopting a full Hardware Description Language (HDL) design flow.

In this work, the authors present a study on the performance compromises and design flow adjustments required when implementing an ASIC based TDC using a technology independent HDL. The main objective was to verify if the achieved performance using Structured Data Path (SDP) (to homogenize the TDC cells' propagation delay variation) could compete with the current state of the art implementations, while fulfilling the requirements of automotive LiDAR sensors applications [14]. The proposed architecture was deployed, tested and verified in an FPGA and then migrated to ASIC, only changing, on the HDL code, the reference to the standard cell used in the fine measurement stage of the TDC, thus demonstrating its improved portability.

The remainder of this paper is structured as follows: Section II presents the proposed architecture details; Section III discusses the ASIC implementation process. After that, the layout considerations are presented; Section IV presents the experimental results obtained. The fabricated prototype limitations are also identified and explained; Section V presents the main conclusions and discusses the future work that must be done to improve the achieved results.

II. PROPOSED ARCHITECTURE

The traditional TDC development approach in ASIC technology enables high resolution and good linearity at the cost of custom designed cells, which increases the design complexity and development time. The possibility of having a simple, technology independent and synthesizable architecture, that is optimized to guarantee a resolution as low as a given technology cell propagation delay, would contribute to lower development times and increased flexibility. This synthesizable approach would also enable a full automated design flow using the traditional Computer Aided Design (CAD) tools.

Based on the authors' previous experience in FPGA TDC implementations, a TDL was used as the base architecture in the research on how to design and develop a technology independent TDC. The purpose of the presented architecture is to achieve a highly portable TDC that can be migrated seamless between platforms and technologies. To increase the performance and field of applications of the proposed TDC

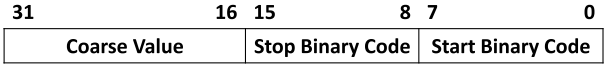

FIGURE 1. TDC output frame structure.

architecture, it is important to achieve high measurement resolutions in a large dynamic range. This can be achieved by implementing a fine and a coarse measurement stage. The fine measurement stage, implemented using a TDL-based architecture, is responsible for detecting time intervals lower than the TDC's reference clock cycle. The coarse measurement unit extends the measurement range by counting reference clock cycles, from the moment the start event is detected, until the arrival of the stop event, using a binary counter. The operation of the fine measurement stage is completely asynchronous to the remaining system, including the coarse measurement stage. Thus, a synchronization module must be implemented to guarantee proper TDC operation. Each measurement is characterized by a 32-bit binary value (Fig. 1), being the 16 most significant bits the coarse measurement result and the 16 least significant bits the fine measurement result (divided in 8-bit blocks for the start and stop events). Therefore, the final measurement value can be calculated according to (1):

$$\Delta t = n_c * T_{CLK} + \left(nf_{st} - nf_{sp}\right) * \tau \tag{1}$$

being n_c the number of counts in the binary coarse counter, T_{CLK} the reference clock period, n_{fst} the binary output of the fine measurement stage for the start event, n_{fsp} the binary output of the fine measurement stage for the stop event, and τ the LSB resolution of the fine measurement stage, in this case, the average propagation delay of the cells used to build the TDL. The fine measurement stage only covers a maximum period of one reference clock cycle, thus the maximum time interval capable of being converted by the proposed TDC will be given by $2^{nc} * T_{CLK} + T_{CLK}$. Moreover, since a single fine module is used to measure both start and stop events, the minimum time interval capable of being detected by the TDC is equal to T_{CLK}. Instead of internally calculating the time interval measurement, the output of the TDC is given in the number of counts. This enables the post-measurement processing to be performed at the software side, simplifying the TDC architecture. To reduce the pad count of the ASIC and increase the peripheral portability, a slave serial protocol interface (SPI) was implemented. The clock crossing domain, between the TDC and the SPI slave interface, is done by a FIFO memory. This module also works as a temporary store unit, where measurement data is stored until read by the master. A block diagram depicting the overview of the implemented TDC architecture is presented in Fig. 2.

A time interval is characterized by two events, the start and stop events, corresponding to the rise and fall edge of the signal being measured ('Time interval' on Fig. 3), respectively.

Upon the start event occurrence, a logic '1' starts propagating through the delay chain. The chain is sampled on the

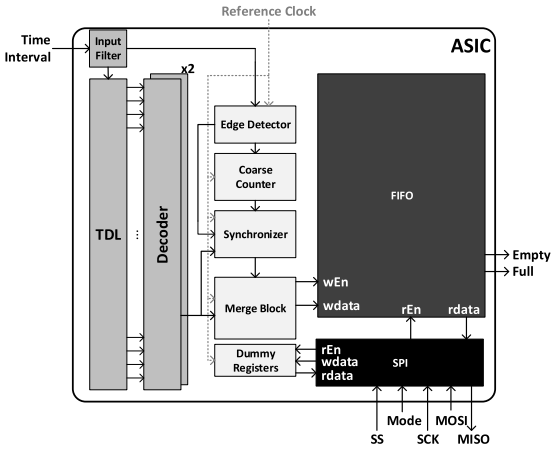

FIGURE 2. ASIC TDC block diagram.

following clock by a set of registers ('First Stage Registers' on Fig. 3) and an enable signal ('start event' on Fig. 3) for the thermometer code storing registers of the start event ('Second Stage Start Registers' on Fig. 3) is generated. These registers are enabled during one clock cycle and are used to store a stable thermometer code for the decoding stage. An analogous sequence occurs when a stop event is triggered. The 'First Stage Registers' sample the state of the TDL on the next clock after the occurrence of a stop event and the 'stop event' signal is generated to enable the 'Second Stage Stop Registers', storing a stable thermometer value on the following clock. Apart from enabling the registers where the fine measurement values are stored, the Start/Stop events, which are generated synchronously to the system clock, are used as the enable/disable signal for the coarse counter. The thermometer to binary decoding is pure combinatorial and requires less than three clock cycles to complete the conversion from thermometer to binary code. The fine measurement values ('Start Binary Code' and 'Stop Binary Code') are then merged with the synchronized coarse counter value ('sampled Coarse Counter') and a write enable signal ('End of Conversion') is generated in order to store the measured value ('TDC Value') to the FIFO memory. After receiving the stop event, a total of 5 system clocks are required until the measurement is stored in the FIFO (3 to get a stable value from the decoding stage, 1 to merge the values and 1 to write to the FIFO).

A. FINE MEASUREMENT STAGE

Since both start and stop events are asynchronous to the normal TDC operation, in order to achieve higher performance, the TDC must be capable of measuring the time interval between both time events and the following clock cycle. When multiple time events need to be captured, a TDC channel for each event is commonly used. However, in order to reduce the chip area, the proposed fine measurement channel was designed to capture both the start and stop events. The detailed view of the designed TDL is presented in Fig.4 and the details of its implementation discussed on Section III-A. It is composed by a delay line built using standard buffers. Clock buffers should be used in order to secure a homogeneous behavior when propagating a logic level '1' and logic level '0', since these cells are typically designed to have similar rising- and falling-edge timings. The delay line is sampled at each clock cycle by a set of registers connected to the outputs of the clock buffers. To reduces the probability of metastability occurrence and guarantee a stable value for the next processing stages, two other sets of registers are implemented. These are only enabled during one clock cycle after the occurrence of the respective event (start or stop).

The thermometer code outputted by the TDL is converted to a binary value through a thermometer-to-binary decoder, implemented using combinational logic based on a priority encoder. A decoder for each time event (start and stop) was implemented.

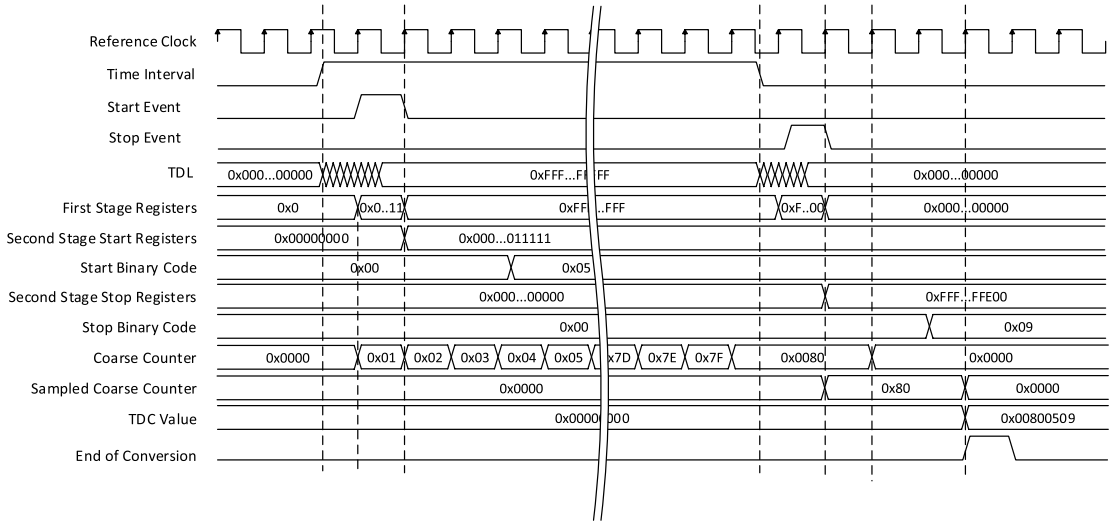

FIGURE 3. Typical measurement waveform.

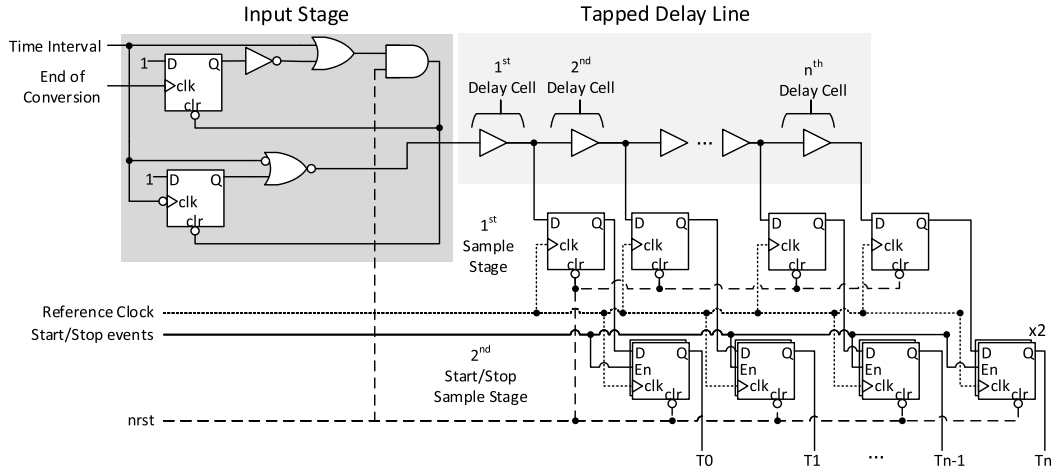

FIGURE 4. TDL RTL overview.

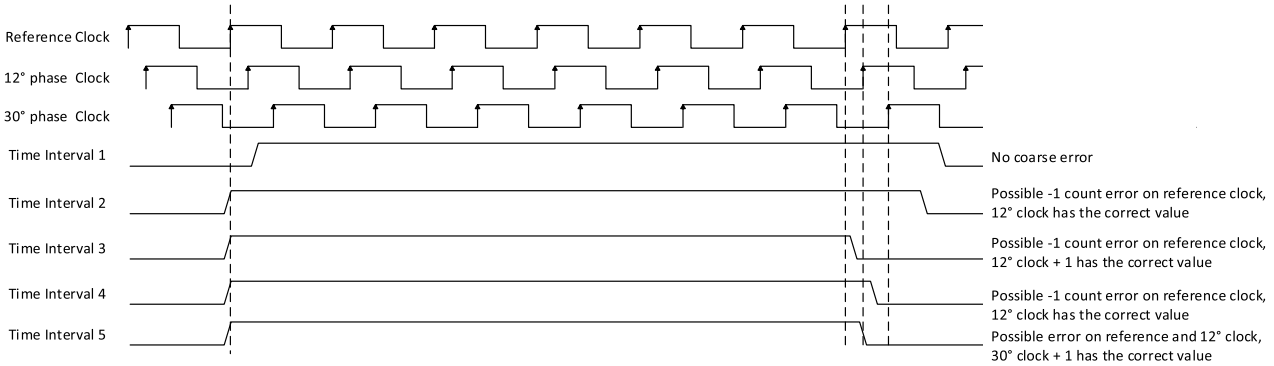

FIGURE 5. Synchronization error scenarios.

The input stage presented on Fig.4 was designed to guarantee that no new input is accepted for measurement while the TDC is still calculating and storing the previous time interval measurement. The circuit secures that the value at the input on the TDL remains at logic level '0' until the generation of the end of conversion signal. It also guarantees that it remains at '0' if the end of conversion signals arrives in the middle of a time interval pulse, to avoid only partially measuring a time interval.

B. COARSE MEASUREMENT STAGE

The coarse measurement stage is based on a binary counter with an enable signal. The counter is enabled upon the detection of a start event and starts to increment at each reference clock cycle. The counter is disabled when a stop event is detected, and the counting value is then stored in a second set of registers to be used in further operations. The start and stop events are generated by an edge detector circuit (see Fig. 2).

C. SYNCHRONIZER

The need for a synchronizer module arises from the use of two asynchronous measurement units (fine and coarse). Due to the asynchronous characteristic of the input time interval, it is possible to have a start or stop event close to the arrival of the reference clock, violating the setup or hold timings of the coarse counter and edge detection registers. In such scenarios, measurement errors equal to ± 1 reference clock cycle may be observed. This occurs due to the impossibility of ensuring the exact same routing delay of the start and stop event signals for every module of the TDC. The waveform diagram, presented in Fig. 5, depicts the possible error scenarios. Usually, a second coarse counter is included in the TDC design, with an 180° phase difference to the reference clock, to cover these metastable scenarios. However, since the proposed architecture aims to measure both start and stop events using the same channel, it is possible for the start event to arrive during the first counter metastability window while the stop event arrives during the second counter metastability window, or vice-versa. Therefore, a third counter must be used to secure a stable value in these scenarios. The fine measurement output data is used to determine if the sampling of the coarse counter was performed in a metastable scenario, and if so, which synchronization counter should be used to correct the issue.

III. TDC IMPLEMENTATION

The implementation process of the TDC was based on a technology independent HDL (Verilog). To automate the

implementation process, a set of scripts were created to configure the tools used. In this Section, some details of the TDC Register Transfer Level (RTL) implementation are presented, with special focus on the TDL description.

A. RTL IMPLEMENTATION

The use of Verilog HDL enables specifying most of the TDC Intellectual Property (IP) in a technology independent way, enhancing portability and easing integration. Due to its nature, the TDL module description needs to reference the cell that will be used to build the delay line. The TDL can be implemented using the Verilog's generator construct (see Fig. 6), enabling the automation of the multiple delay steps instantiation. All the other TDL's building blocks were implemented using technology independent constructs. To further improve the architecture portability and technology independency, the delay cell used to build the TDL can be designed as a module. This would enable the use of the command *change_link* during synthesis, allowing a different cell to be used to build the TDL depending on the technology being used and avoiding changes to the HDL code.

```
genvar i;
generate
    for(i=0; i < `NUM_STAGES; i=i+1)
    begin : delay_cell
        if(i!=0)
        begin : delay_cell
        (* dont_touch = "TRUE" *) CKBD0BWP7T delay_cell(
            .Z(tdl_val_w[i]),
            .I(tdl_val_w[i-1])
        );
        end
        else
        begin : delay_cell
        (* dont_touch = "TRUE" *) CKBD0BWP7T delay_cell(
            .Z(tdl_val_w[i]),
            .I(hit_i)
        );
        end
    end
endgenerate
```

FIGURE 6. Verilog code for the TDL generation.

According to TSMC digital library documentation, the clock buffer selected to implement the TDL steps has a typical propagation delay of 105ps and 107ps for low-to-high and high-to-low transitions, respectively. Since the reference clock for the proposed TDC has a frequency of 50MHz, a minimum of 191 delay steps must be implemented to completely cover the 20ns period. A total of 256 delay steps were defined to cover for mismatch in the propagation delay due to process variations.

B. DESIGN FLOW AND LAYOUT CONSIDERATIONS

The TDC implementation follows a typical digital scripted flow (see Fig. 7). Apart from minor changes in the typical digital design flow scripts, an extra file (SDP file) must be loaded during the place-and-route step. A multi-vendor design flow was adopted with Synopsys's Design compiler being used for synthetizing the design, Cadence's Innovus used for the TDC place-and-route and Cadence's Virtuoso

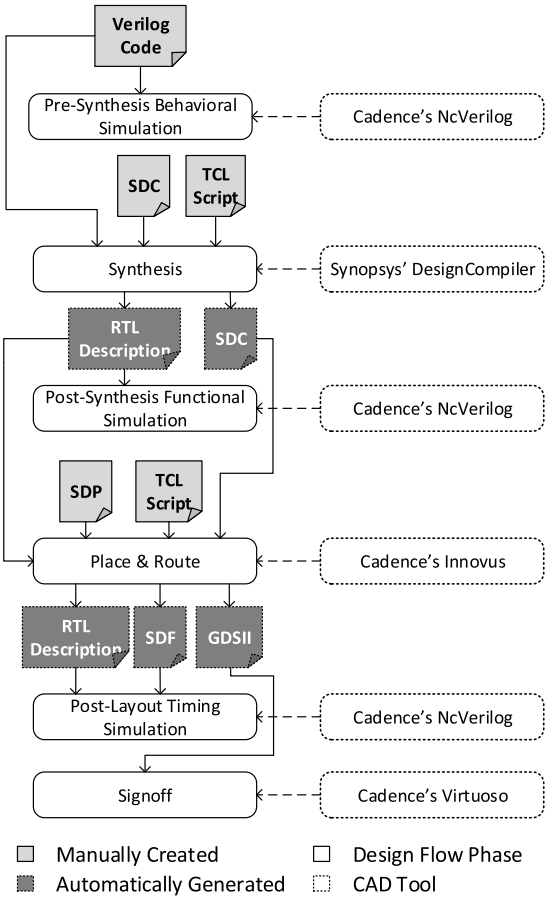

FIGURE 7. SDP design flow.

used to perform the final pad ring design, DRC (Design Rules Check) and LVS (Layout Versus Schematic) checks. During the entire process, behavioral and functional simulations were performed using Cadence's NcVerilog.

Regarding synthesis, it is required to signalize the TDL cells as being *dont_touch* elements. Otherwise, when analyzing the design, the tool will automatically optimize the delay chain and remove it from the final RTL.

Since sub-nanosecond resolution is being targeted, the effect of routing, parasitic capacitances and cell's placement starts to play an important role on the final TDL's steps propagation delays. While FPGAs offer a predetermined structure, ASIC layout placement is based on the timing constraints, typically resulting in a more clustered placement, rather than a structured and uniform one. In the same way, migration between technologies (for example from TSMC 180nm to 65nm), will result in different layouts due to different cell's size and design rules. When analyzing the literature results reported on FPGA TDL-TDC architectures, the use of Carry4 primitives is almost undisputed [15]–[17], since the dedicated routing available to sequentially connect multiple of these blocks enables high resolution to be achieved, while maintaining a reduced non-linearity. Therefore, to achieve a hardware independent ASIC TDL-TDC, similar

characteristics must be obtained. To do so, layout constraints must be used, allowing a structured and uniform placement.

The automated placement of the TDL's cells in a standardize pattern can be done using SDP files [18]. This would allow a uniform routing pattern between the TDL's steps, homogenizing the parasitic loads in each step.

An approach based on a similar concept was proposed by Chaberski *et al.* in [19], where dummy LUTs, in an FPGA platform, were configured as buffers to regulate the loads on the routings of the delay line, thus increasing the overall chain's linearity. The standard placement pattern is technology independent and secures that the tool performs an automatic and identical routing, contributing to uniform cells' propagation delays. Once the TDL is placed, the remaining design follows the standard automated placement.

As the synchronizer block needs two extra counters, with a phase shift to the reference clock, prior to the clock tree generation, extra skew groups must be created with different insertion delay times, to generate two different phase shifts. Another skew group must be created to the TDL registers to secure a low skew value between the flip-flops sampling the delay chain. Otherwise the thermometer code of the fine measurement stage may have missing codes, deteriorating the overall system's performance. After the creation of all the skew groups, the following layout steps are standard to most digital designs.

IV. EXPERIMENTAL RESULTS

In order to properly study the effect of SDP on the TDC's linearity, two different implementations were analyzed. One using the typical digital layout design flow and the other with SDP. The two resultant layouts were compared and assessed using post-layout timing simulations, as well as the exported layout timing data, on the format of a standard delay format file (SDF).

The proposed architecture, using SDP, was then fabricated in TSMC 180 nm, 6-metal CMOS process. The prototype is 1×0.89mm with a total power consumption of 36mW when operated with a 50MHz clock, at 1.8V (including SPI and FIFO modules). Considering the 5 clock periods required for completing a measurement after the stop event, a maximum sampling rate of 10MHz is achieved. The fabricated chip is presented in Fig. 8. As can be observed, the TDC channel covers less than 10% of the total chip area, being most of the area used by the 256 positions FIFO memory.

A. SDP AND NON-SDP LAYOUT COMPARISON

The resultant layout of the two different implementations (with and without SDP) is shown in Fig. 9. A detailed analysis on the non-SDP layout shows a non-uniform cell organization (coarse placement highlighted in light-blue in Fig. 9), while the SDP version not only presents a sequential placement with homogeneous distance between subsequent cells, it also shows the expected uniform routing (light-blue cells at the top right and light-blue and pink lines at the bottom right of Fig. 9).

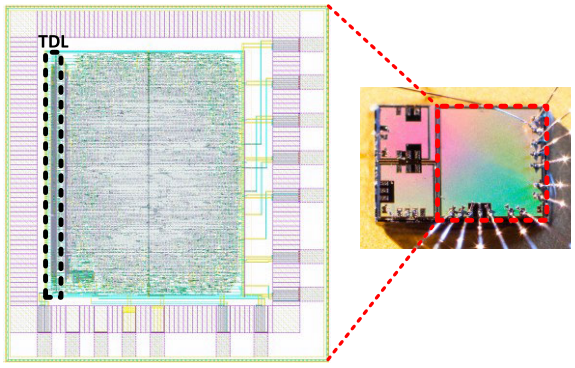

FIGURE 8. Fabricated TDC.

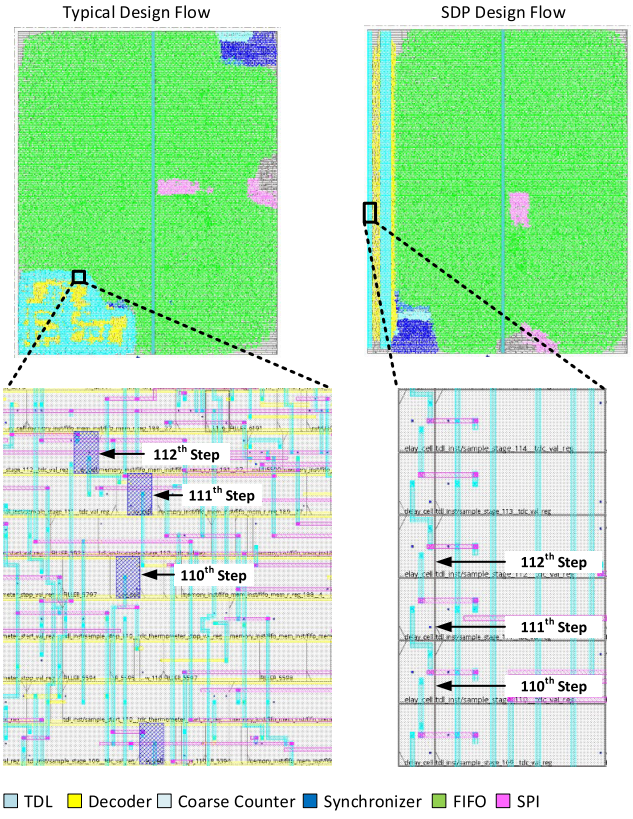

FIGURE 9. TDL layout for the different design flows.

From the exported layout timing information, it was possible to verify that,, although the routings from the two implementations are completely different, the delay introduced in the data path is identical in both scenarios (zero in the SDP case and a maximum of 1ps in the non-SDP). However, if the cells' propagation delays are compared, it is noticeable that the non-uniform routing generates large variations on the cells' propagation delays (see Fig. 11 for the propagation delay of the TDL cells normalized to a LSB of 170ps, correspondent to the worst-case scenario simulation).

The SDP layout shows a maximum variation of 1ps between steps while the non-SDP approach has a maximum

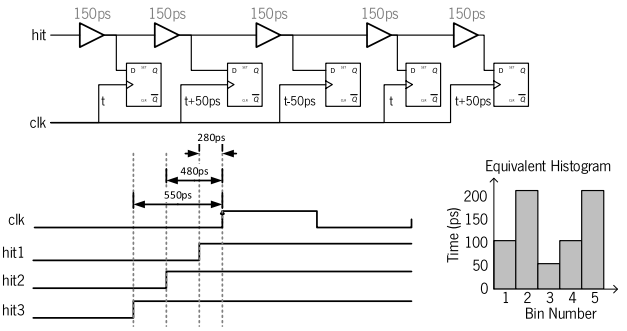

FIGURE 10. Clock insertion delay skew effect.

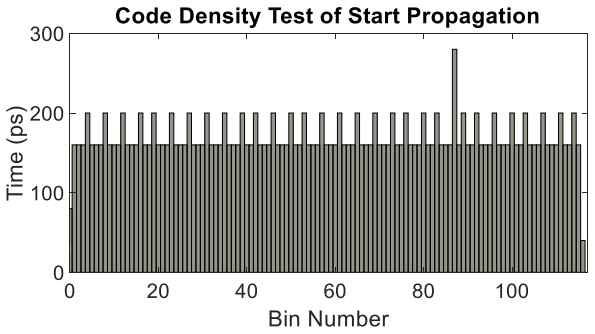

FIGURE 12. Post-layout code density test simulation.

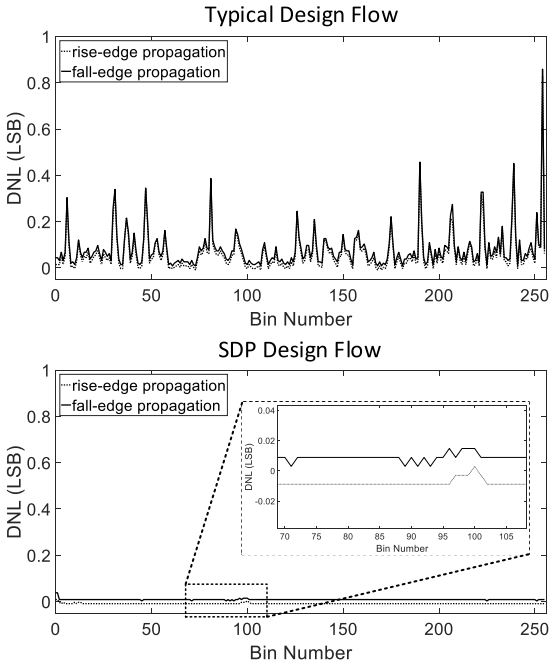

FIGURE 11. Non-SDP and SDP TDL cells' propagation delays.

of 144ps. This discrepancy between steps results in a maximum DNL of 0.85 LSB and 0.038 LSB for the non-SDP and the SDP implementations, proving the advantages of using SDP to homogenize the delay line steps delays.

Moreover, in a typical digital design flow, different placements and routings would be generated during multiple layout iterations, resulting in TDLs with completely different characteristics. This also holds true if the architecture would have to be migrated to another technology. With SDP, the TDL homogeneity is maintained across all layout iterations and potential technology changes.

Since the TDL clock distribution may play a significant role on the TDL linearity, a post-layout timing simulation was performed on the SDP layout. The simulation was designed to mimic a code density test. The results are presented in Fig. 12.

A non-linearity in the range of 0.2 LSBs was obtained with a non-linearity peak in-between the 80th and 100th steps. This increase on the non-linearity of the TDC is explained by the different clock insertion delays for the TDL sampling flip-flops. When analyzing the extracted post-layout SDF file, it is possible to verify that the non-linearity peak on the simulation matches the highest clock insertion delay.

When designing a TDL, the analysis is usually done considering the clock tree distribution as ideal, which results in a delay step equal to the propagation delay of the element used to build the TDL. However, the routings' skew in the clock tree distribution can be consider as another delay line, leading to a Vernier delay line structure, where both start and stop signals are delayed. This means that the effective step delay will vary according to its clock signal insertion delay. Moreover, due to the parallel structure of the clock tree distribution (as opposed to the serial distribution of the hit signal), when analyzing a scenario where a given step i has a higher insertion delay than the previous one i-1, the effective result is an increase of the i^{th} step's delay and a decrease on the $i^{th} - 1$ step's delay, equal to the amount of skew between the two sampling registers (see the example for a 150ps step delay given on Fig. 10 and Table 1).

TABLE 1. Example of the sampled values of Figure 10.

Hit Signal	Expected TDL Output	Real TDL Output
hit1 (280 ps)	00001	00011
hit2 (480 ps)	00111	00011
hit3 (550 ps)	00111	00111

Since the clock tree for the TDL was constrained to have a maximum of ±50ps skew, a maximum step propagation delay difference of 100ps is expected during experimental measurements. If higher linearity is required, the TDL clock tree distribution may be constrained using SDP, to reduce the skew of the clock insertion delay of the sampling flip-flops. Considering the effort required for constraining the clock tree in the SDP file, and since the non-linearity results were within an acceptable range for the targeted application, this SDP layout was considered for fabrication.

B. MEASUREMENT SETUP

A printed circuit board (PCB), was used to experimentally validate the fabricated SDP based TDC. The board

includes a microcontroller used to read the SPI slave interface of the TDC, perform software calibration (if desired), and communicate with a host computer using UART interface. A TDC from Texas Instruments (TDC7200) was also included to be used as reference for the time measurements performed. An external 50MHz crystal oscillator mounted on the PCB is used as the main clock source for the TDC ASIC. A temperature sensor, placed near to the TDC, was also included to perform measurements during temperature tests. The TDC7200 has a 55ps resolution and a 35ps single shot precision [20] and was used as a reference measure to secure that the fabricated TDC synchronization module was working properly. If the synchronization between the coarse and fine measurement modules was faulty, measurement errors greater than one clock cycle may occur. The reference TDC7200 was used to monitor the time interval (Tin on Fig. 13) generated by the waveform generator. The values measured by the TDC7200 were then compared to the ones measured by the fabricated TDC to check if the measurements errors were within a range lower than a coarse LSB, validating the synchronization module operation.

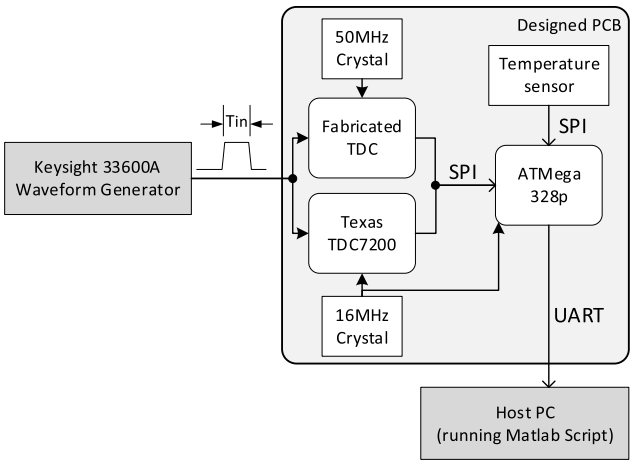

FIGURE 13. Measurement setup block diagram.

The measurement setup, depicted in Fig. 13, is composed by a Keysight 33600A waveform generator, the designed test PCB with the ASIC TDC, and a host computer running a MATLAB script for metrology. Temperature tests were also performed, during which, the test PCB was placed inside a DY60T oven from ACS (Angelantoni Test Technologies Srl).

C. CODE DENSITY TEST

In order to evaluate the real delay distribution across the implemented TDL, a code density test was performed. The function generator was configured to output a square wave signal at 999,133 kHz, a frequency unrelated with the TDC's reference clock. This creates a sliding window effect on the sampling steps of the TDC, which, in an ideal scenario, would have the same probability to be sampled. A total of 100 thousand TDC measurements were performed to reduce probabilistic errors. For brevity, only the plots for the start event sampling are presented in Fig. 14.

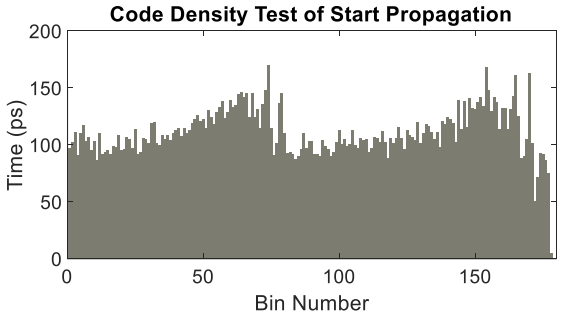

FIGURE 14. Steps' propagation delays for start event.

The maximum number of TDL cells through which the signal was able to propagate was 180, which gives an average LSB of 111ps, for start and stop propagation, at ambient temperature. Moreover, the code density test shows no zero delay steps, meaning the clock skew constraints applied to the TDL were effective on preventing missing codes. This results in an effective number of bits of 20.32 for the implemented TDC ($\log_2$(Dynamic Range/rms resolution)).

D. PRECISION

To measure the precision of the TDC, short- and long-range measurements were performed. In the short-range measurement, a square wave signal with 480,434ns up time interval was defined. A square wave with an up time of 1101,321586μs (near end-of-scale) was used as the TDC input to evaluate the effect of the reference clock skew on a long-range measurement scenario.

In both test cases, a total of 100 thousand samples were measured. The results presented in Fig. 15 show a single-shot precision of 279ps (2.51 LSB) and 305ps (2.75 LSB), for the short- and long-range measurements, respectively. Note that the TDC precision is deteriorated by the non-linearity of the TDL (see subsection E), which has a peak-to-peak INL of 6.4 LSB.

E. LINEARITY

The TDC linearity is usually characterized based on its Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). The DNL can be obtained from the code density tests results according to (2):

$$DNL_i = \tau_i - \bar{\tau} \tag{2}$$

where τ_i is the propagation delay of the ith cell propagation delay and $\bar{\tau}$ is the ideal cell propagation delay.

The INL represents the accumulated non-linearity across the TDL, thus it can be determined according to (3):

$$INL_i = \sum_{i=0}^{N-1} DNL_i \tag{3}$$

From equations (2) and (3), the DNL and INL for the TDL start and stop propagation was calculated. The results for the

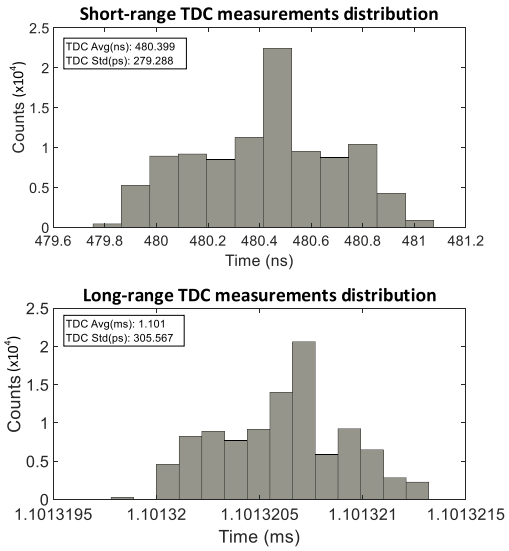

FIGURE 15. TDC's single-shot measurement precision.

start event propagation are presented in Fig. 16, showing a DNL in the range of −0.9 LSB to 0.6 LSB. For the stop event propagation, a −0.7 LSB to 0.9 LSB was obtained. It is worth noticing that most of the measured DNL is below ±0.3 LSB and that a non-linearity increase is noticeable around the 80th step, which is close to the results obtained from simulation. The INL for the start event propagation is in the range of −2.6 LSB to 3.8 LSB, while for the stop event it reached a maximum of −8 LSB.

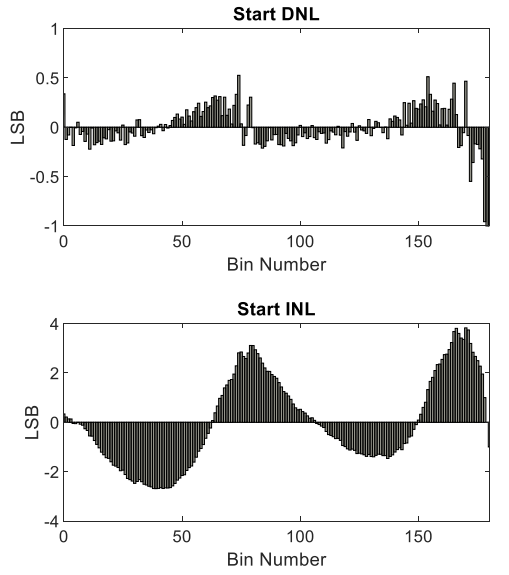

FIGURE 16. TDC's non-linearity.

Based on these results, it is possible to conclude that the clock skew constraints defined during layout are not a viable solution to achieve high linearity. Thus, it is mandatory to also constraint the TDL's clock tree distribution using SDP. Otherwise the high homogeneity achieved in the propagation delay of the cells, due to the use of SDP, is jeopardized by the variable skew of the clock tree.

F. BIN CALIBRATION

Since the design constraints applied during layout were not enough to reach a precision close to 1 LSB, a post-measurement software calibration was applied, following a bin-by-bin calibration process. Two calibration tables, one for start and another for stop, were built according to the results from the code density test. These tables store in each position the cumulative propagation delays at each step of the TDL. Thus, the table's first position will store the value obtained from the code density test correspondent to the first step, the second position will store the value from the previous position plus the obtained value from the code density test correspondent to the second step, and so forth. Since the output of the TDC is given in the number of cells that propagated the input signal, instead of directly multiplying this value by the resolution RMS value (as presented in (1)), this number is used as the index to access the calibration table, being the read value directly used to perform the time interval calculation. Thus, a multiplication operation is replaced by a calibration table access.

These tables were also used to calibrate the temperature dependency measurement results. After calibration, the single-shot precision of the TDC is improved to 54ps (0.48 LSB) and 52ps (0.47 LSB) for the short- and long-range measurements, respectively. The single-shot precision measurement results are presented in Fig. 17.

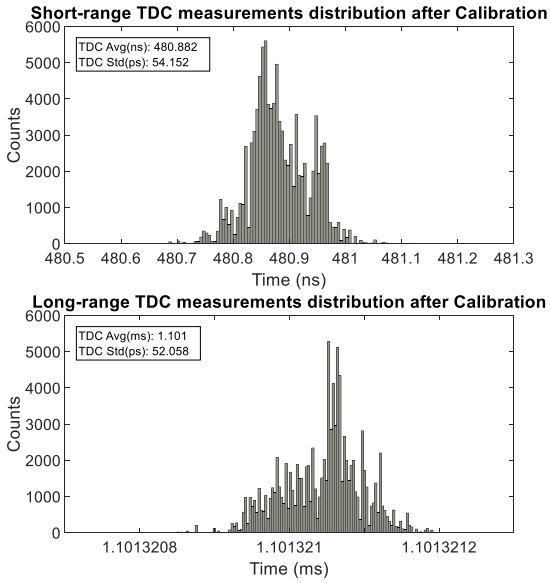

FIGURE 17. TDC's single-shot measurement precision after calibration.

G. TEMPERATURE PERFORMANCE DRIFT

In order to understand the TDC's temperature dependency, an average time interval, equal to the one used on the short-range test, was experimentally measured at different temperatures (in the range of 0° to 50°C, in steps of 5°C).

First, no calibration was applied to study the effectiveness of the proposed SDP approach on maintaining a good measurement stability with temperature variations. Afterwards, the software calibration tables were used to calibrate the measurement results.

The results obtained are depicted in Fig. 18. It is possible to verify that both calibrated and non-calibrated measurements remain stable across the tested temperature range, with less than 100ps variation in both cases. Moreover, the average LSB resolution at the worst-case temperature scenario (50°C) was 121ps, 10ps more than the value at ambient temperature, representing a small variation of 0.09 LSB. Thus, the proposed method is capable of producing a TDC which has a stable operation with temperature variation.

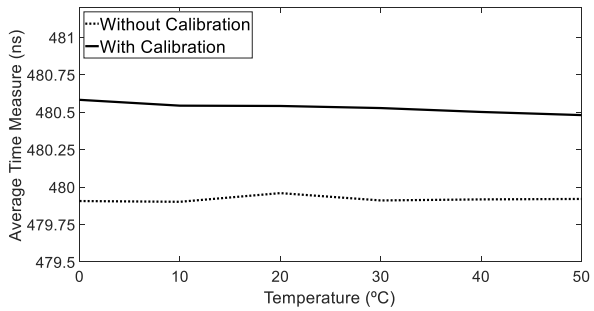

FIGURE 18. Precision variation with temperature (top) and average measurement (bottom).

H. DISCUSSION

In order to compare the proposed architecture with the state-of-the-art, the figure of merit (FOM) presented in [11] was used. The FOM presented in [21] could also be used, however, since the area is considered in this FOM, the results obtained would be highly dependent on the technology being used. According to the results presented in [11], the *ENOB* was changed by N_{linear}, which includes the quantizer resolution while considering the INL. Therefore, the final FOM is calculated according to (4):

$$FOM = \frac{Power}{2^{N_{linear}} * Rate} \tag{4}$$

The comparison is summarized in Table 2. It is important to refer that the FOM does not consider the design complexity and development time, which is the main advantage of the proposed methodology. Although the resolution and precision of the proposed TDC is not capable of competing with the most sophisticated solutions currently available, it offers a simple and portable architecture, that can be migrated in-between technologies in less than a week. Moreover, the advantages of the proposed SDP approach, to improve the cells' propagation delay homogeneity, can be applied to other synthesizable architectures, like the one presented in [22], where the authors highlight the propagation delay differences on the buffers used due to place and route mismatch. Another advantage of the proposed design not captured by the FOM is the performance repeatability. While in a typical digital design flow the TDC would be placed randomly (different layout runs would generate different cells placement), resulting in different performance characteristics, the proposed approach secures a consistent layout across multiple iterations independently of the technology being used.

When comparing the proposed TDC with architectures fabricated using the same technology, it is possible to verify that the power consumption is considerably higher. This is because the FIFO memory is also being included in the power report. If the memory is excluded and only the TDC channel is considered, the power consumption of the proposed architecture is approximately 5.4mW, according to the post-layout power reports. The implementation of a clock gating strategy for the FIFO memory may be used to reduce the power consumption of the system. This solution can easily be introduced on the design flow scripts, maintaining the methodology flexibility and the design process automatic.

As stated in Section II, if higher performance is required, both the architecture and design process presented are flexible enough to include custom-made cells [23]. A custom-made (designed at the transistor level) delay cell can be introduced during synthesis, replacing the currently instantiated standard clock buffer from TSMC digital library. This change can also be included in the design scripts keeping the process automatic.

Finally, considering the linearity achieved, which was mainly influenced by the clock tree skew distribution and not by the routing in-between TDL steps, it is expected that, in smaller technologies, like 90nm, the proposed architecture may achieve a resolution of 50.5ps (typical propagation delay for a TSMC 90nm clock buffer similar to the one used on the TDL configuration presented) and a single-shot precision of 24.2ps (considering the same relationship between the precision, linearity and resolution obtained using a 180nm technology, i.e. a single-shot precision of 0.48 LSB). Moreover, since TSMC maintains the same naming convention, in the case of the migration from TSMC 180nm to 90nm, no change would be needed in the HDL, the user would only need to change the digital library used by the CAD tools and the TDC would be automatically generated using the scripts that implement the proposed design methodology.

V. CONCLUSION AND FUTURE WORK

An integrated fully digital TDL TDC architecture implemented using technology independent HDL and a fully automated design flow has been presented. In order to validate and study the effectiveness of the proposed approach, an ASIC was fabricated using TSMC 180nm CMOS process technology. The fabricated device reached a rms resolutions of 111ps with a 279ps precision, without calibration and including other sources of measurement errors introduced by the waveform generator, input signal routing path, among others. The overall performance can be further improved when a calibration step is added, reaching a precision of 54ps. The scripts developed during this work enable the execution of

TABLE 2. Performance summary and comparison.

	This Work	[6]-12	[10]-19***	[24]-14	[25]-18	[26]-18	[7]-14	[27]-17
Technology	180nm	350nm	180nm	350nm	130nm	180nm	130nm	350nm
Architecture	TDL*	Two-Step (DLL)	Two-Step (Pulse Shrinking)	Pulse Shrinking	Phased Clocks	Two-Step (Cyclic Vernier)	Two-Step (DLL)	DLL
Resolution (ps)	111	8.878	2	40	780	377	5	320
Precision (LSB)	2.5 0.49**	1.1	0.7	0.1	0.05	0.82	0.6	0.73
DNL (LSB)	±0.8	-0.94:0.65	1.5	-	±0.05	1.41**	±0.9	±0.68
INL (LSB)	8	-2.48:0.84	4.2	±0.6	±0.05	2.31**	±1.3	±1.21
NLinear	17.43	20.89	13.62	-	16.86	11.27	-	11.23
Range	1310.72µs	4.5ns	130ns	22ns	102.4µs	355ns	-	2.5µs
Power (mW)	36 (5.4) (@1.8V)	85 (@3.3V)	18 (@1.8V)	-	6.5 (@1.5V)	0.65	43 (@1.2V)	10.9 (@3.3V)
Area (mm^2)	0.89	8.88	0.08	0.025	0.033	0.028	-	0.152
Operating F. (MHz)	50	220	-	-	320	-	781	100
Sampling Rate (MHz)	10	4	3.3	0.00001	14	0.67	-	0.3
FOM	$2.04x10^{-5}$	$1.09x10^{-5}$	$4.33x10^{-4}$	-	$3.90x10^{-6}$	$3.93x10^{-4}$	-	$1.51x10^{-2}$

*Fully designed with technology independent HDL (no custom cell design) **After calibration ***Simulation

a fully automated design flow for a TDL-TDC generation, regardless of the technology being used, which, according to the experimental results obtained, offer standard cell level resolution and a single-shot precision greater than ±3 LSB, while maintaining good thermal stability. Moreover, the proposed approach enables a much higher portability between platforms and technologies than the currently available ASIC TDC solutions, due to the fully scripted design flow and the usage of standard technology digital cells, instead of the typical custom cell design approach.

The benefits of SDP for homogenizing the cells' propagation delays was demonstrated. However, to avoid jeopardizing the advantages of SDP, it must also be applied to the clock tree of the TDL, since it was proven that clock skew constraints are not enough to keep the non-linearity of the system low.

Future work will focus on introducing the clock tree constraints in the SDP file and further research the effect of SDP in achieving performance repeatability across multiple chips.

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