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Analog Integrated Circuits Based on Wafer-Level Two-Dimensional MoS_2 Materials With Physical and SPICE Model

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ABSTRACT In this article, accurate physical and SPCIE model of wafer-level monolayer molybdenum disulfide (MoS_2) device are developed to guide the devices and circuits design, which is the foundation of high-performance analog chip design. Moreover, the proposed model considers the non-ideality of thin films and the influence of Schottky contact with higher accuracy. The mean percentage error (MPE) of the physical model simulation and measurement results is 4.49%. Based on the SPICE model implemented in this article, the amplifier circuit and current amplifying circuits are implemented to verify the manufacturing process and accuracy of the device models, which shows the MoS_2 is potential material to realize industrial applications. The MPE of the SPICE model simulation and measurement results is within 7.00% which can be utilized for our analog circuit design.

INDEX TERMS Two-dimensional (2D) material, wafer-level MoS_2, SPICE model, Schottky contact, physical model, analog integrated circuits.

I. INTRODUCTION

With the increasing demand for integration and computing ability, the feature size of CMOS transistors is continually shrinking based on Moore's law and has reached the physical limitation.

With the end of the Moore era, 2D layered materials have great potential in the next generation of electronics and optoelectronics due to their excellent optical and electrical properties. Compared with traditional bulky devices, 2D devices have unique advantages such as flexibility, transparency, foldability and lightweight that have the potential to replace rigid silicon. Thus, 2D devices can realize the design of implantable and wearable devices in the future. Graphene is the most widely studied 2D material, which has high mobility, good mechanical stability and nearly transparency properties. However, the bandgap of graphene is zero which makes the transistor difficult to turn off. Although bandgap can be artificially tuned, it will certainly increase the complexity of the process, increasing the defects and decreasing the mobility of materials. It overcomes the defect of graphene without bandgap and becomes a potential semiconductor material. With the study of transition metal dichalcogenide (TMDs), MoS_2 is a two-dimensional (2D) material that has the advantages of adjustable bandgap, high mechanical strength, thermal stability and no dangling bond on the surface. It offers significant advantages for realizing large-scale flexible systems owing to its wafer-level good transport properties and stable crystalline structure. In recent years, field-effect transistors (FETs) based on MoS_2 has been widely studied. MoS_2 has more advantages because MoS_2 becomes a direct bandgap semiconductor when the thickness is reduced to a single layer. This provides a physical foundation for the application of MoS_2 in high-performance devices.

Comparison with the MOSFET based circuits, MoS_2 circuits are widely used in various sensors such as gas detection, production of hydrogen, wearable devices and so on [1]–[9]. Due to its flexibility characteristic, it can realize flexible

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electronics which can be used to monitor biological signal from the skin of the human body by embedding smart textiles into sensors. By utilizing ultrathin 2D MoS_2 material, soft and stretchable skin-like devices can be achieved. In particular, for electrophysiological signals, soft contact between the devices and tissue can significantly reduce the impedance of the electrode-skin interface and mechanical sliding, minimizing motion artifacts. Moreover, these devices are biocompatible and can realize various circuits that they can fully wrap around the organism in 3D space without imposing any mechanical deformation as shown in FIGURE 1. Therefore, MoS_2 with high flexibility and transparency can provide new opportunities for advanced diagnosis and medical repair. It becomes an excellent potential candidate for biomedical applications also because of its in vivo biocompatibility and non-toxic biodegradation products.

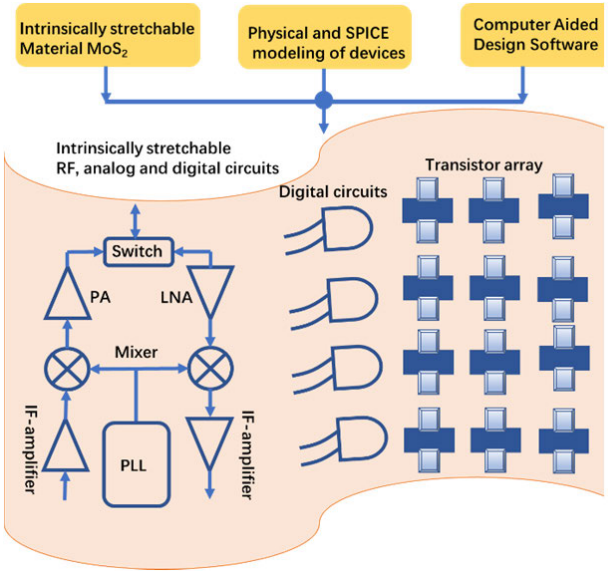


FIGURE 1. The custom design flow of a two-dimensional (2D) integrated circuit. The proposed wafer-level MoS_2 materials have tremendous application potential in digital circuits, analog circuits and even radio frequency circuits such as power amplifier (PA), low noise amplifier (LNA) and phase locked loop (PLL).

Despite various sensors, MoS_2 chip can also realize computation and storage that are the driving force for the development of integrated circuits. To fully realize the above applications, wafer-level chemical vapor deposition (CVD) growth [10]–[12] is the trend and precise models are essential for circuit design. An accurate simulation model is the profound of circuit design, which can help to avoid the performance loss from the theoretical design to the production process, thus reducing the experimental cost and accelerating the development speed. As a result, it can improve the efficiency of circuit design and shorten the cycle of circuit design. Moreover, it changes the design methodology of the 2D device by trial and error.

To date, the application of MoS_2 has been limited to single or multiple devices, because of the technical difficulty in material growth, device uniformity and yield control. Compared with the individual device on exfoliated MoS_2 material, analog circuits are implemented with wafer-level MoS_2 material. However, there is still a lack of precise physical model and SPICE model that can accurately describe the electrical characteristics of MoS_2 FETs based on chemical vapor deposition (CVD) grown process. In this work, the MoS_2 enhancement-mode (E-mode) transistor with accurate physical and SPICE modeling was realized with industrial computer-aided design tool flow to enable a complex system including several kinds of analog circuits.

The paper is organized as follows. First, a brief introduction to the gate-first process is provided. In this approach, all the components are fabricated after the MoS_2 layer transfer to maximize the design flexibility and device density. Meanwhile, fixed-charge in the gate dielectric of MoS_2 transistors with comparable results with exfoliation devices should be reduced. This makes for a MoS_2 transistor with positive threshold voltage and good statistical distribution. Second, a detailed physical model and compact SPICE models are utilized to capture the different regions of device performance (subthreshold, linear, saturation) and to predict future FET performance as the fabrication process evolves. Third, industrial design flow for the design, simulation, and layout of MoS_2-based circuits with an industry-standard IC design environment has been developed.

With the demonstrated fabrication technology, modeling, and computer-aided design flow, a platform for the co-optimization of circuits and devices using MoS_2 was built. And the fabricated analog circuits show the great promise of the technology for realizing high performance and complex MoS_2-based chip. Finally, the physical model and SPICE model are both verified and shows good agreement with measurement results. The analog integrated circuits are designed based on SPICE model and the measurement results show good performances.

II. FABRICATION AND PHYSICAL MODEL OF THE MoS_2 DEVICE

A. DEVICE MANUFACTURING PROCESS

The device manufacturing process with the chamber structure is shown in FIGURE 2(a). A crucible with molybdenum trioxide (MoO_3) power is placed in Zone-2 while the appropriate amount of sulfur powder is placed in Zone-1 which is upstream of the flow in the tube. The distance between the two zones is 30 cm. A carefully cleaning sapphire substrate is placed face-down on the MoO_3 power. The synthesis temperature for Zone-1 and Zone-2 is controlled at 180 °C and 650 °C, respectively. Continuous monolayer MoS_2 film is synthesized at atmospheric pressure with 10 min sulfuration time. The high-quality wafer-level film and its thickness are shown in FIGURE 2(b)-(c). After the film is ready, the MoS_2 FET and circuits are fabricated on the wafer-scale MoS_2 film on the sapphire substrate [12].

The contact electrodes (35 nm Au), source and drain contacts, are patterned by traditional laser writing technology

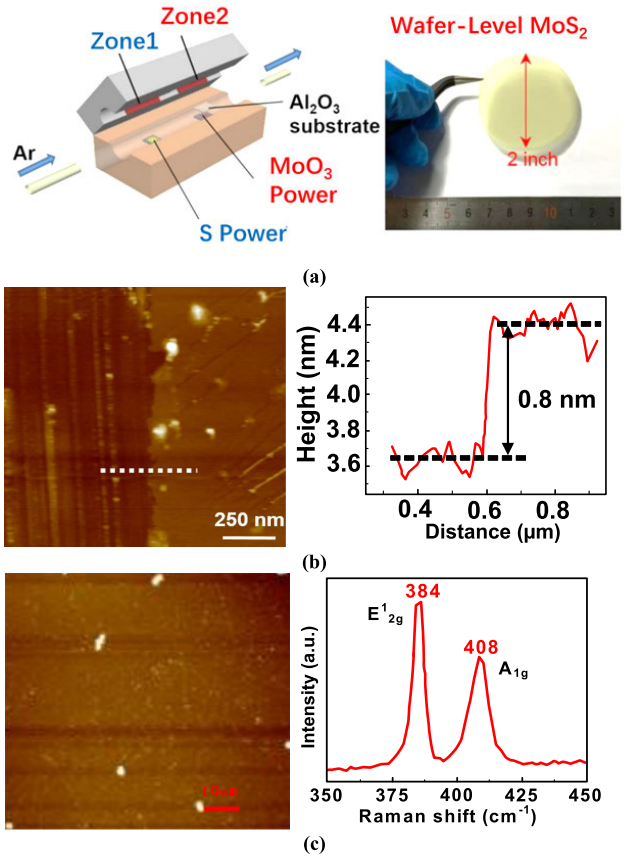


FIGURE 2. (a) MoS_2 material grown by CVD in double temperature zone and 2-inch wafer-level MoS_2 films (b) Atomic force microscopy (AFM) of the MoS_2 film (c) In the experiment, the monolayer MoS_2 were characterized by Raman spectra [12].

and subsequently deposited using Electronic Beam (E-beam) evaporation. The CF_4 plasma etching is performed to define the MoS_2 channel region. To increase threshold value and reduce the leakage current of the device, a seeding layer (2 nm SiO_2/2 nm Al_2O_3) is deposited by E-beam evaporation followed by furnace annealing in an oxygen atmosphere at 100 °C. Then 20 nm HfO_2 is grown by Atom Layer Deposition (ALD) as the main dielectric layer. After using lithography again to define the hole, SF_6 plasma etching is utilized to remove the insulating layer between metal layers followed by depositing 30 nm Au using E-beam evaporation. The last lithography and lift-off process are utilized to form the top metal layer [12], which is deposited by thermal evaporation as shown in FIGURE 3.

B. MODELING METHODOLOGY

There are currently two mainstream modeling methods for 2D material devices: finite element analysis [13], [14] and compact model analysis [15]–[22]. The finite element analysis usually refers to Technology Computer Aided Design (TCAD) simulation. The TCAD simulation can accurately simulate the geometric structure of the device with the price of a huge amount of computation. However,

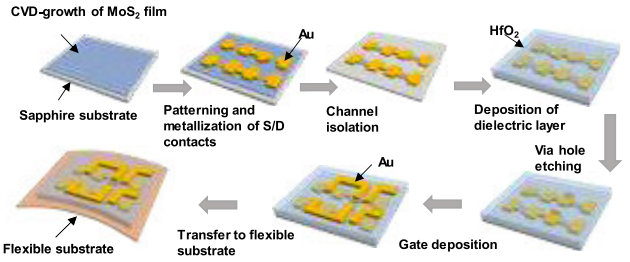


FIGURE 3. Top gate transistor manufacturing process flow.

TCAD simulation is generally used for qualitative analysis or theoretical verification. Because the defect of the two-dimensional material is difficult to control, it is necessary to use the fitting method while comparing the simulation results with the experimental data. At this point, the compact model is more effective. Besides, the compact model has obvious advantages in computing speed.

Nowadays, a 2D FET compact model based on surface potential is rigorous and standardized in terms of the mathematical procedure. For example, paper [15], [16] shows the physical model of the MoS_2 device based on the Fermi level and carrier drift-diffusion law. Paper [17]–[20] consider the nonideal effects of the interface defect that modifies the carrier concentration, and mobility. Paper [21], [22] analyzes the 2D state density of the atomic layer thickness and its influence on the quantum capacitance. Then, considering the drift-diffusion mechanism of the carrier along the single-layer MoS_2, the expression of the drain current is obtained. These physical models [15]–[22] help us understand the working principle of the devices. However, the models are all based on the exfoliated MoS_2 transistors which are still difficult to explain the performances of the device in wafer-level devices with various defects.

For the bulk silicon FETs, the current-voltage characteristics can be qualitatively discussed as [23]

$$I_{DS,bulk} = \frac{W\mu_{eff}C_{0x}}{2L}\left[2\left(V_{GS}-V_T\right)V_{DS}-V_{DS}^2\right] \quad (1)$$

where W is the channel width, L is the channel length, μ_{eff} is the effective mobility of carriers in the channel, C_{0x} is the gate oxide capacitance, and V_{GS}, V_{DS}, V_T is the gate-source voltage, drain-source voltage and threshold voltage of the FET, respectively.

It should be noticed that the $I_{DS,bulk} - V_{GS}$ relationship is linear, while the nonlinear transfer characteristics of MoS2 FETs are observed in our experiment. To include this feature of our device, some additional effects that do not exist in ideal bulk devices should be taken into consideration. In the paper, the Schottky contact and Van der Waals gap are included in our model.

Compared with the traditional ohmic contact, the single layer MoS_2 device is the Schottky contact for source and drain and the contact resistance is related to the voltage. In order to fully characterize the device, the device is divided

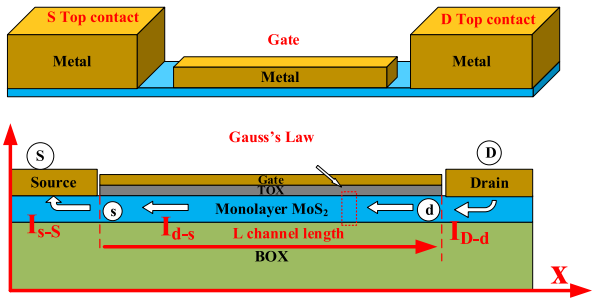


FIGURE 4. Device structure with three different regions.

into three parts: external drain connection point D to drain channel point d, drain channel point d and source channel point s, source channel point s to external source connection point S as shown in FIGURE 4. Each region can be analyzed as an independent device with different voltage and current characteristics. However, because there is no leakage on the substrate and they are connected in series, the current of these parts are the same

$$I_{D\to d} = I_{d\to s} = I_{s\to S} = I_{DS} \tag{2}$$

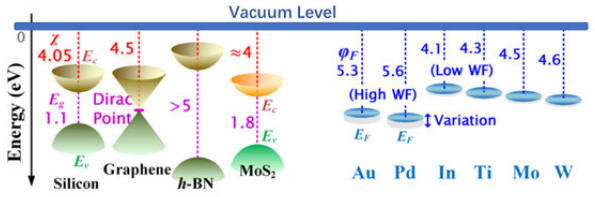


FIGURE 5. Band diagrams of different materials and selected contact metals. E_c, E_v, and E_g represent conduction band edge, valence band edge, and band gap, respectively. χ and φ_F represent electron affinities and metal work functions, respectively [24].

C. SCHOTTKY CONTACT OF SOURCE AND DRAIN

Based on the types of contact between the source/drain metal and MoS_2 as shown in FIGURE 5 [24], the energy band structure from metal to MoS_2 is analyzed. According to the strength of the interaction, metal contact with 2D materials can be divided into two types of physical adsorption and chemical adsorption which is known as metal alloying as shown in FIGURE 6. The contact between metal and MoS_2 is similar to physical adsorption. The energy band structure of the 2D material at the interface does not change, only the Dirac point deviates from the center position. Because there is no hanging bond on the surface of 2D material, the potential barrier of the contact interface is produced by the Van der Waals gap between metal and 2D material. Considering the work function and adsorption type of Au and MoS_2, there will be a potential barrier at the contact interface. The Van der Waals gap will hinder the carrier movement and form a large contact resistance.

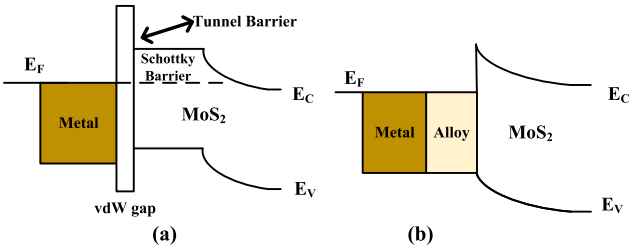


FIGURE 6. Energy band of the device: (a) physical adsorption energy band structure diagram and (b) chemical adsorption energy band structure diagram.

The existence of the Schottky barrier forms a diffusion layer of Schottky contact between the channel regions. There are three kinds of carrier transport mechanisms at the interface of a metal and 2D material: direct tunneling, Schottky barrier tunneling and electron orbit overlapping. Direct tunneling plays a key role in the MoS_2 contact, followed by Schottky barrier tunneling, and the orbital overlap can be ignored. The carrier transport from the source drain electrode to the channel is equivalent to the direct tunneling through the Van der Waals gap and the Fowler-Nordheim (F-N) tunneling across the Schottky barrier. The key parameters of the tunneling barrier and tunneling effect are the height and width of the Van der Waals gap. The Van der Waals energy gap height of Au and single layer MoS_2 contact $\Phi_{TB} = 7.347\ eV$, width $d = 1.70$ Å. According to Wentzel Kramers Brillouin (WKB) approximation in quantum mechanics [25], the probability of electron tunneling can be expressed as

$$P = exp\left\{-4\pi\left(\frac{2m^*}{h^2}\right)^{\frac{1}{2}}\int_{x1}^{x2}[V(x) - E]^{\frac{1}{2}}\,dx\right\} \tag{3}$$

m^* is electronic effective mass, E is the energy of the electron, $x1, x2$ are the barrier boundary, $V(x)$ is barrier height at x. The Van der Waals gap is approximated as a rectangular barrier, if $x1 = 0, x2 = d$, then $x_1 \le x \le x_2$

$$V(x) = E + \Phi_{TB,eff} \tag{4}$$

By substituting (4) into (3), the equation can be expressed as

$$P = exp\left[-4\pi^2\left(\frac{2m^*}{h^2}\right)^{\frac{1}{2}}\Phi_{TB,eff}^{\frac{1}{2}}d\right] \tag{5}$$

For a single layer of MoS_2, the effective mass of electrons $m^* = m_{effK} = 0.48m_0$ at the bottom of the conduction band. For the ideal tunneling barrier produced by the perfect fit of the surface, $P = 3.44 \times 10^{-5}$ can be obtained by taking the above data into equation (4). The Schottky barrier height of the MoS_2 contact is $\Phi_{SB} = 0.62\ eV$ without considering the non-ideal effects. Because the barrier formed by the Schottky barrier is thinner than the average free path of the electron in MoS_2 monolayers (20 nm), which means that the electron emission theory can reasonably describe the carrier motion, and the collision of electrons in the barrier area can be ignored. Thus, the shape of the barrier is less important than the barrier height. According to the theory of

thermionic emission [26], the current through the Schottky barrier is

$$J = A^* T^2 \exp\left(-\frac{q\Phi_{SB}}{k_0 T}\right)\left[\exp\left(\frac{qV}{k_0 T}\right) - 1\right] \quad (6)$$

where, V is the voltage of metallography to semiconductor, $A^* = qm^* k_0^2/(2\pi^2\hbar^3)$, which is called effective Richardson constant. J_{sT} is a function independent of applied voltage but strongly dependent on temperature $T = 300\ K$, $m^* = 0.48\ m_0$. According to the voltage and current equations of the direct tunneling barrier and Schottky barrier, the current transmission characteristics from D to d and S to s be can deduced as

$$I_{D\to d} = J_{sT}\left\{\exp\left[\frac{q\left(\varphi_D - \varphi_D'\right)}{k_B T}\right] - 1\right\} * P * \Omega \quad (7)$$

$$I_{s\to S} = -J_{sT}\left\{\exp\left[\frac{q\left(\varphi_s - \varphi_s'\right)}{k_B T}\right] - 1\right\} * P * \Omega \quad (8)$$

where Ω is the contact area between the electrode and MoS_2. Because the contact area of the electrode is large and the top contact is adopted, the energy band distribution of different contact positions on the electrode is different, and the Ω is an effective contact area with correction term.

D. ENERGY BAND AND CARRIER CALCULATION OF MoS_2 MATERIAL

Different from the conventional 3D bulky device, the channel thickness of the single layer MoS_2 is 0.65 *nm*. As a result, the change of electric potential perpendicular to the plane direction of the 2D material can be ignored. As the gate voltage changes, the Fermi level shifts vertically and stays flat as shown in FIGURE 7(a). When the gate voltage is positive, the Fermi energy level is close to the conduction band and forms a negative charge in the channel. FIGURE 7(a) shows the discrete energy levels of metal, insulator and MoS_2. When these energy levels are closed together, the Fermi energy levels of metal and semiconductor reach equilibrium due to the potential difference of the insulating oxide layer and space charge layer. The metal work function is larger than MoS_2. When a positive bias voltage is applied to the gate, the potential induces the Fermi energy level shift that will cause the change of the charge density on the semiconductor surface. With 2D transistor approximation and Gauss's Law [27], the charge can be expressed as:

$$\Delta Q = \left(\varepsilon_{TOX} E_{TOX} - \varepsilon_{BOX} E_{BOX}\right) W \Delta x + \left(\varepsilon_{2D} E_x(x) - \varepsilon_{2D} E_x(x + \Delta x)\right) W T_{2D} \quad (9)$$

Among them, ε_{TOX} is the dielectric constant of HfO_2 gate dielectric layer, ε_{BOX} is the dielectric constant of Al_2O_3 substrate insulating layer, T_{2D} is the thickness of single layer MoS_2, E_{TOX} and E_{BOX} are the longitudinal electric field intensity at gate-MoS_2 interface and substrate-MoS_2 interface, respectively, $E_x(x)$ and $E_x(x + \Delta x)$ are the transverse electric field intensity at x and $(x + \Delta x)$ in MoS_2 channel.

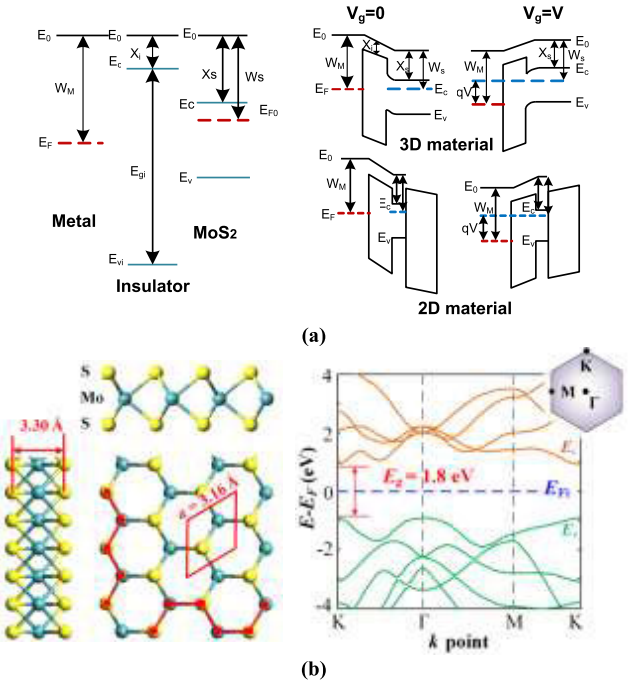


FIGURE 7. (a) MoS_2 energy band structure and energy band structure of device and comparison with 3D material. (b) lattice structures of MoS_2 and the first Brillouin zone of MoS_2 containing the M, K, and Γ points [24].

According to Gauss's Law [27], the relationship among these parameters can be expressed as

$$E_{TOX} = \frac{V_G - \Delta\varphi_t/q - \varphi(x)}{T_{TOX}} \quad (10)$$

$$E_{BOX} = \frac{\varphi(x)}{T_{BOX}} \quad (11)$$

$$E_x(x) - E_x(x + \Delta x) = \frac{d\varphi(x)}{dx}\Delta x \quad (12)$$

where T_{TOX} and T_{BOX} are the thickness of the gate dielectric layer and substrate insulation layer respectively, V_G is gate voltage, $\Delta\Phi_m$ is the work function of metal gate $\Delta\Phi_m = 5.54\ eV$.

From the gradual channel approximation [28], the electric potential does not change along the x direction (i.e. E_x is constant), the equation (9) can be simplified as

$$\frac{\Delta Q}{W\Delta x} = \varepsilon_{TOX}\frac{V_G - \Delta\Phi_m/q - \varphi(x)}{T_{TOX}} - \varepsilon_{BOX}\frac{\varphi(x)}{T_{BOX}} \quad (13)$$

Along with free charge carriers, impurities and defects contribute to the total channel charge, which is mainly caused by process defects, so the channel charge per unit volume

$$\Delta Q_{ch} = -q\left[N_{Dop} + N_{it} + n_{2D}\right] T_{2D} W \Delta x \quad (14)$$

Considering the interface defect as the acceptor, the effective energy E_{it} is located below the conduction band, and the effective trap density is D_{it} that is a delta function of energy, and the number of carriers captured (N_{it}) is given by the

following formula:

$$N_{it} = \int_{-E_0}^{E_0} D_{it} f(E) dE = D_{it}/(1 + \exp(\frac{E_0 - E_{it} - qV_F}{k_B T})) \tag{15}$$

By combining (14) and (15), the equation can be expressed as

$$qT_{2D}(n_{2D} - N_{it}) = \varepsilon_{TOX} \frac{V_G - \frac{\Delta\Phi_m}{q} - \varphi(x)}{T_{TOX}} - \varepsilon_{BOX} \frac{\varphi(x)}{T_{BOX}} \tag{16}$$

For the convenience of calculation, let $\lambda_1 = \frac{1}{qT_{2D}} \frac{\varepsilon_{TOX}}{T_{TOX}}$, $\lambda_2 = \frac{1}{qT_{2D}}(\frac{\varepsilon_{TOX}}{T_{TOX}} + \frac{\varepsilon_{BOX}}{T_{BOX}}))$

$$\begin{aligned} n_{2D} &= N_{it} + \frac{1}{qT_{2D}} \left(\varepsilon_{TOX} \frac{V_G - \frac{\Delta\Phi_m}{q} - \varphi(x)}{T_{TOX}} - \varepsilon_{BOX} \frac{\varphi(x)}{T_{BOX}} \right) \\ &= N_{it} + \lambda_1 (V_G - \Delta\Phi_m/q) - \lambda_2 \varphi(x) \end{aligned} \tag{17}$$

According to the energy band, the carrier density can be calculated. There are two conduction bands of MoS_2 participating in the transmission, one is at the point K in the Brillouin region, the other is in the middle of the point K and Γ in the Brillouin region as shown in FIGURE 7(b). Among them, ΔE_{KQ} is the energy separation between K and Q conduction valley. According to the charge density of the Fermi level, it is calculated as

$$n_{2D} = \int DOS_{2D}(E) \frac{1}{1 + \exp\left(\frac{\varphi - E_F}{k_B T}\right)} dE \tag{18}$$

$DOS_{2D}(E)$ is the 2D density of states corresponding to the lowest band. Compared with the N-type semiconductor [25], the Boltzmann distribution function is used to simplify the expression of charge density

$$n_{2D} = N_{2D} \, exp\left[\frac{\varphi - qV_F}{k_B T}\right] \tag{19}$$

$$N_{2D} = \frac{k_B T g_K m_{effK}}{\pi \hbar} + \frac{k_B T g_Q m_{effQ}}{\pi \hbar} exp\left(-\frac{\Delta E_{KQ}}{k_B T}\right) \tag{20}$$

where Fermi level $E_F = qV_F$, k_B is Boltzmann constant, T is temperature. g_K and g_Q are the degeneracy of K and Q-band Valley respectively, and m_{effK} and m_{effQ} are the effective mass of their respective DOS. For MoS_2, $g_K = 2, g_Q = 6$, $m_{effK} = 0.48\ m_0$ and $m_{effQ} = 0.57\ m_0$, ΔE_{KQ} is the energy gap $(0.11\ eV)$ between K and Q conduction band Valley for single layer MoS_2 as shown in FIGURE 7(b). Then, the bandgap E_g $(1.87\ eV)$ utilized in photoluminescence (PL) in monolayer MoS_2 [26] is adopted for simplicity. The relationship between the Fermi energy level distribution and the electrostatic potential is expressed as

$$V_F = \varphi(x) - \frac{k_B T}{q} ln\left[\frac{1}{N_{2D}} (N_{it} + \lambda_1 (V_G - \Delta\Phi_m/q) - \lambda_2 \varphi(x))\right] \tag{21}$$

E. DRIFT-DIFFUSION CURRENT

According to carrier continuity equation and drift-diffusion law [27], carrier transport can be described as

$$I(x) = qWT_{2D} n_{2D}(x) \mu(x) \frac{dV_F(x)}{dx} \tag{22}$$

where W is the channel width and $\mu(x)$ is the carrier mobility and integration of the current along the channel

$$\begin{aligned} \int_0^L I(x) dx &= -qW\mu_{eff} \int_0^L n_{2D}(x) \frac{dV_F}{dx} dx \\ &= -qW\mu_{eff} \int_{\varphi_s'}^{\varphi_D'} n_{2D}(x) \frac{dV_F}{d\varphi} d\varphi \end{aligned} \tag{23}$$

In the formula, μ_{eff} is the effective mobility of carriers in the channel, and L is the channel length. And $I_{d\to s} = \int_0^L I(x) dx/L$, so the final expression of current is

$$\begin{aligned} I_{d\to s} = \frac{qWT_{2D}\mu_{eff}}{L} \Bigg(\Bigg(N_{it} + \lambda_1 (V_G - \Delta\Phi_m/q) + \frac{k_B T}{q} \lambda_2 \Bigg) \\ \times (\varphi_D' - \varphi_s') - \lambda_2 \frac{(\varphi_D'^2 - \varphi_s'^2)}{2} \Bigg) \end{aligned} \tag{24}$$

Due to Gauss law and thin film transistor approximation, the equation is similar to a 3D transistor. Simultaneous equations and numerical fitting of three parts $\varphi_D = V_D$, $\varphi_s = 0$. The transcendental function can be obtained by combining the above equations

$$I_{DS} = \frac{qW\mu_{eff}}{L} \begin{bmatrix} \left(N_{it} + \lambda_1 \left(V_G - \frac{\Delta\Phi_m}{q}\right) + \frac{k_B T}{q} \lambda_2\right) \\ \times \left(V_D + \frac{2k_B T}{q} ln \frac{PJ_{sT}\Omega}{I_{DS}}\right) \\ -\lambda_2 \left(V_D + \frac{2k_B T}{q} \ln \frac{PJ_{sT}\Omega}{I_{DS}}\right) (V_D - \frac{2k_B T}{q}) \end{bmatrix} \tag{25}$$

For our devices, the process parameters are $T_{BOX} = 1\sim2\ mm (\gg T_{TOX})$, $\varepsilon_{TOX} = 20\varepsilon_0$, $k_B T/q = 0.026\ V$, $\varepsilon_0/q = 5.53 \times 10^7\ V^{-1} \cdot m^{-1}$. The transcendental function is explicated due to the relationship between I_{DS} and V_G. As a result, the transfer characteristic curves under various V_{DS} are plotted. In this article, a custom nonlinear function was defined to fit the equation (25) in OriginLab software. The measurement data is utilized to fit the model and the parameters of the device are W = 90 μm, L = 30 μm, $T_{TOX} = 20\ nm$, $T_{2D} = 0.8\ nm$. For different drain-source voltage V_{DS}, the fitting results are shown in FIGURE 8 (a)-(d). The extraction parameters are follows $\mu_{eff} = 0.9\ cm^2/(V \cdot s)$, $N_{it} = 8.7 \times 10^{26}\ cm^{-3}$. The MPE of the simulation and measurement results are 4.49% which shows the physical compact model and measurement results are in good agreement.

III. SPICE MODEL OF THE MoS_2 TRANSISTOR

The physical model in our paper is derived from the first principle, while the spice models used have fixed templates. The spice model we finally utilized is analogous to the templates for MOSFET, while the parameters in the model, like V_{th}, C_{ox} are defined by the actual device. Finally, the

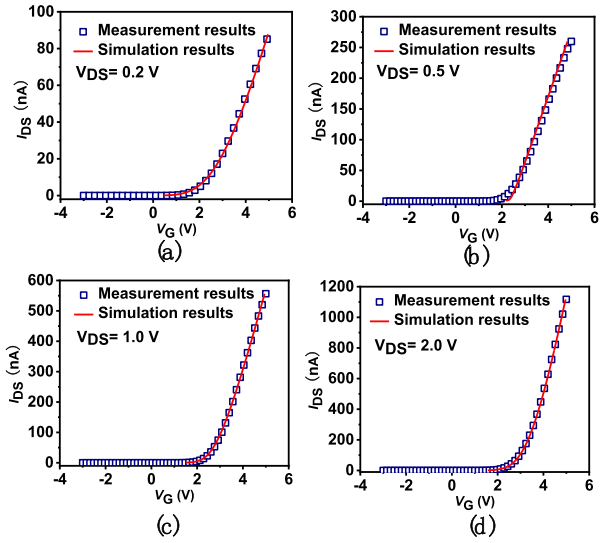


FIGURE 8. **Comparison between the simulation and experimental data for transfer characteristics of MoS_2 FET under different V_{DS} (a) $V_{DS} = 0.2$ *V* (b) $V_{DS} = 0.5$ *V* (c) $V_{DS} = 1.0$ *V* (d) $V_{DS} = 2.0$ *V*.**

results of the measurement are consistent with the modified model, indicating that the model can be utilized for our circuits design. It should be noticed that it is not through the fitting technology to get the formula. Paper [17] shows that the Verilog-A models are verified to support digital circuit design. However, these simplified Verilog-A models can only be utilized for digital circuit design and cannot link the parameters to the physical model and SPICE model [29]–[33]. In this article, accurate different levels of SPICE model linked to the physical model are presented. 2D MoS_2 devices have three main working areas: subthreshold area, linear area and saturation area. The working difference is that the threshold voltage of NMOS is defined as the gate voltage when the surface layer changes from P-type to N-type. In 2D MoS_2, when a positive voltage is applied to the gate, the charges accumulate on the surface layer, forming a conductive channel to improve the conductivity. The public-domain SPICE program has long been available to designers for the purpose of simulating the time-domain and frequency response behavior of silicon integrated circuits. However, there have been no nonproprietary models available for accurate MoS_2 integrated chip simulation.

A. LEVEL-1 SPICE MODELS

Level-1 SPICE model [33] is widely utilized in digital circuit design, the cut-off region refers to the reverse layer that is not formed on the surface of the semiconductor. Thus, there are not enough carriers accumulated in the film to form a conducting channel and the source and drain current $I_{DS} = 0$. When a bias voltage is applied to the gate, a strong inversion layer is formed in the channel. The amount of minority carriers on the surface of the semiconductor is comparable to the number of majority carriers in the semiconductor. Then, when a voltage is applied to the drain, the channel forms an obvious current. At this time, the voltage applied to the gate is defined as the threshold voltage V_{th}.

The linear region refers to the region with $V_{DS} < V_{GS} - V_{th}$, and its current are:

$$I_{DS} = \mu C_{ox} \frac{W_{eff}}{L_{eff}} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) \cdot V_{DS} \cdot (1 + \lambda) V_{DS} \tag{26}$$

The saturation region refers to the region where $V_{DS} > V_{GS} - V_{th}$, and its current is:

$$I_{DS} = \mu C_{ox} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{th})^2 \cdot (1 + \lambda) V_{DS} \tag{27}$$

Among them, V_{th} is the threshold voltage, μ is the channel carrier mobility, C_{ox} refers to the gate oxide capacitance, λ describes the effect of the channel clamping off, defined as $\Delta L/L = \lambda \cdot \Delta V_{DS} = \lambda(V_{DS} - V_{Dsat})$, L_{eff} and W_{eff} are the effective channel length and width. For MoS_2, the structure of the film is an ideal silicon-on-insulator (SOI), and the substrate bias coefficient is zero.

B. LEVEL-3 SPICE MODEL

The level-1 model is not accurate enough to simulate an analog circuit though it can simulate the function of the digital switch circuit. Level-3 SPICE model [33] improves the channel length modulation coefficient and the subthreshold current. Moreover, the influence of channel width and length on the threshold voltage, the change of mobility, the channel length modulation effect caused by channel clipping, current velocity saturation effect are also considered. The threshold voltage V_{th} defined can be expressed as

$$V_{th} = V_{TO} - \gamma \sqrt{\phi} + (\eta - 1)\phi + \gamma \cdot \phi^{\frac{1}{2}} \tag{28}$$

$$\eta = 1 + \delta \cdot \frac{\pi \varepsilon_{si}}{4 C_{ox} \cdot W_{eff}} \tag{29}$$

η, γ is the narrow channel effect factor and short channel effect, δ is the narrow channel width factor to adjust the threshold voltage, ε_{si} is the channel dielectric constant, V_{sb} is the substrate bias voltage and ϕ is the reverse-mode potential. The mobility of carriers on the surface of the transistor will decrease under the influence of the surface electric field. Some empirical parameters are used to describe the carrier mobility drop. In the linear region, the current I_{DS} increases with V_{GS}. In the saturation region, I_{DS} does not follow the square law with the increase of V_{GS}. The saturation voltage V_{sat} is defined as:

$$V_{sat} = \frac{V_{GS} - V_{bi}}{\eta} + \frac{1}{2} \left(\frac{\lambda}{\gamma} \right)^2 \cdot \left\{ 1 - \left[1 + 4 \left(\frac{\eta}{\gamma} \right)^2 \cdot S \right]^{\frac{1}{2}} \right\}$$

$$S = \left(\frac{V_{GS} - V_{bi}}{\eta} + \phi + V_{sb} \right) \tag{30}$$

Considers both bulk charge change effect and V_{bi} bias contrast effect and it can use the slowly varying channel

approximation, so the unified current expression is:

$$I_{DS} = \beta\left[\left(V_{GS} - V_{bi} - \frac{\eta V_{de}}{2}\right)V_{de} - S_1\right]$$
$$S_1 = \frac{2}{3}\gamma F_1\left[(\phi + V_{de} + V_{sb})^{\frac{3}{2}} - \phi^{\frac{3}{2}}\right] \quad (31)$$

Among these

$$V_{de} = \min(V_{DS}, V_{Dsat}) \quad (32)$$
$$\beta = \frac{\mu_s C_{ox} W}{L_{eff}(1 - \lambda V_{DS})} \quad (33)$$
$$F_1 = 1 - \frac{K_1}{L\sqrt{N_A}} \quad (34)$$

In the formula, μ_s is the mobility of carrier surface, F_1 is called short channel factor, and K_1 is the fitting parameter. When the gate voltage V_{GS} is lower than the threshold voltage V_{th}, the channel is in a weak inversion state, and the current flowing through the drain is not equal to zero.

In the subthreshold region, the Level-2 model [34] introduces a fast surface states (N) parameter. When $V_{gs} < V_{on}$, the current can be expressed as

$$I_{DS} = I_{DS}(V_{on}, V_{de}) \cdot \exp\left(\frac{V_{GS} - V_{on}}{F}\right) \quad (35)$$

When $V_{gs} > V_{on}$, the current can be expressed as

$$I_{DS} = I_{DS}(V_{on}, V_{de}) \quad (36)$$

Among these,

$$V_{on} = V_{th} + fast, \quad V_{de} = min(V_{ds}, V_{dsat}) \quad (37)$$

V_{on} refers to the gate voltage applied when switching from weak inversion to strong inversion, and $I_{DS}(V_{on}, V_{de})$ is the current value when $V_{GS} = V_{on}$

$$F = V_t \cdot \left[\eta + \phi^{\frac{1}{2}} \cdot \frac{\partial\gamma}{\partial V_{sb}} + \frac{\gamma}{2 \cdot \phi^{\frac{1}{2}}} + \frac{q \cdot N}{C_{OX}}\right] \quad (38)$$

In order to verify the effectiveness of the SPICE model, the output characteristics of MoS_2 FETs at room temperature are measured, respectively. Compared to the traditional model, Schottky contact is considered to improve the SPICE model.

C. ANALOG CIRCUIT DESIGN FLOW

FIGURE 9 shows the design flow of the analog MoS_2 circuit design. Based on the measurement results and parameter fitting, the accurate physical model and SPICE model can be got. The amplifier is widely utilized in analog systems and a single-stage amplifier is shown in FIGURE 10(a).

According to the type of load, it can be divided into resistance load and transistor load. Firstly, the amplifier based on the resistance load is analyzed. The current flowing through the resistance is: $I_{DS} = (V_{DD} - V_{out})/R_D$. As shown in FIGURE 10(b), the working points (A, B, C, D) of the amplifiers are the intersection of the resistance load line and the output curve of the pull-down transistor. The load line of

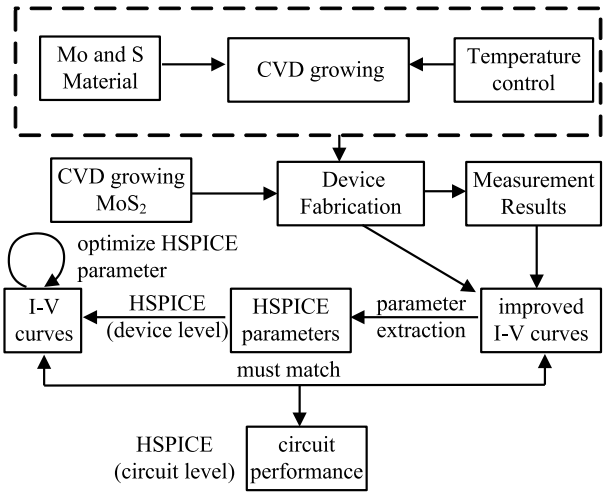


FIGURE 9. Design flow of the analog MoS_2 circuit design.

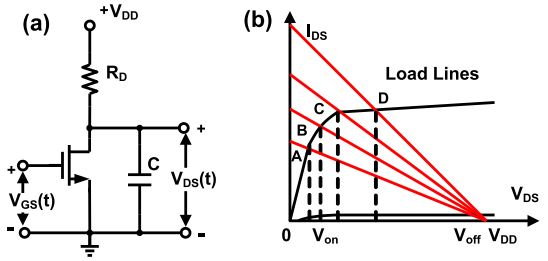


FIGURE 10. (a) Traditional structure of the amplifier. (b) The different resistor load lines of the amplifier and the working points of the amplifiers with different resistors.

different resistances is analyzed to optimize the output voltage range. Smaller the pull-up resistance induce high voltage working point (A, B) that reduces the dynamic output voltage range of the amplifier. As a result, it is essential to select a suitable R_D value, and the working point D is near $V_{DD}/2$ with largest voltage swing and appropriate voltage gain $g_m R_D$.

D. MoS_2 ANALOG CIRCUIT DESIGN

However, the resistor occupies a large area in the integrated circuit. To reduce the area, the transistor is usually used as the load and the current process can only realize N-type transistors. The proposed amplifier structure is shown in FIGURE 11(a)-(b), the M_2 is in the depth subthreshold region and works as a large resistance. With the appropriate size of the load transistor, the working points can be chosen.

An ideal current mirror is a two-port circuit that accepts an input current and produces the output current. The input is a low resistance implemented by a transistor with diode connected. The diode-connected load (30 μm /30 μm) has a high output resistance and its current is constant. As a result, the ideal current mirror circuit can faithfully reproduce the input current regardless of the source and load impedances to which it is connected. In this article, long channel transistor with large output impedance is used as a current source. Based on

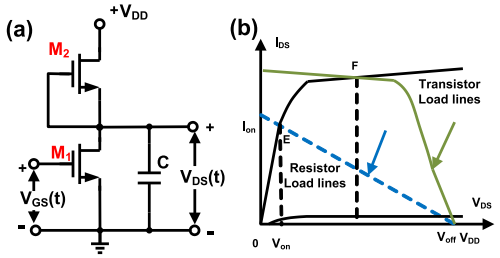


FIGURE 11. (a) The proposed amplifier structure with transistor lines. (b) The different types load lines of the amplifier and the working points of the amplifiers with different resistors.

the current mirror structure, current amplifying circuits can be implemented and are widely utilized in biomedical current stimulation [34]. The stimulation circuits consist of several binary weight current sources to realize different current values.

IV. MEASUREMENT RESULTS

A. DC CHARACTERISTICS

DC characteristics were measured with an Agilent B1500A semiconductor analyzer. As shown in FIGURE 12(a)-(b), the analyzer and the device are connected by four DC probes. The transfer curves of the transistors array are measured to analyze the distribution of the threshold voltage as shown in FIGURE 13(a)-(c). The results show the transistors have good uniform performances.

FIGURE 12. (a) Photo of wafer testing environment. (b) Photo of chip with probe connected.

The Schottky resistance with different voltages is measured as shown in FIGURE 14(a)-(b). The Schottky barrier height Φ_{SB} is highly related to the bias voltage and V_{TG} due to the suppression of hot electron emission (dominated by tunneling operation). Therefore, it is more suitable to extract these resistances to compensate for the I-V curves.

The transistors with the aspect ratio (W/L) of 90 /20 μm and 300 /20 μm are taken as test samples. The source of the transistors is grounded, and a voltage source is connected to the drain. A voltage source V_{GS} is connected between the gate and the source. The I-V characteristics of the transistor are measured and the improved level-3 model is used to extract the empirical parameters of the transistors. The parameters

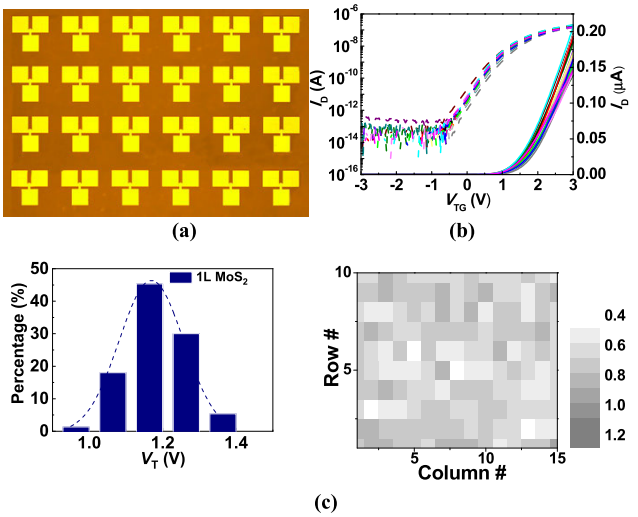


FIGURE 13. (a) The transistors array and (b) transfer curves measurement results of transistor array. (c) The distribution of the threshold voltage with transistor array measurements.

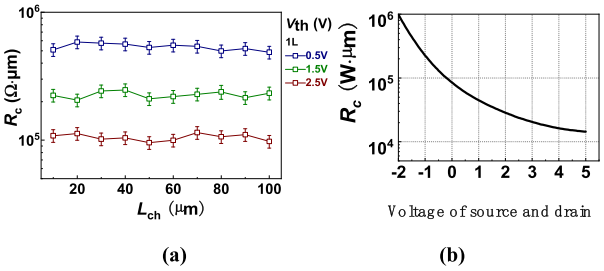


FIGURE 14. (a) The connection resistance of the Schottky contact. (b) The normalized resistance of the Schottky contact with different voltage of the source and drain.

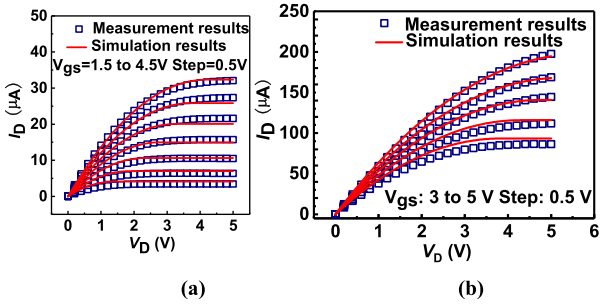


FIGURE 15. (a) Output characteristic curves of the transistors. (b) Output characteristic curves of the transistors when the currents are large.

in the model are obtained by fitting the experimental test data. FIGURE 15(a)-(b) show a good agreement between the measured data and the theoretical prediction based on the model discussed above. The MPE of the simulation and measurement results is 7.00%.

B. THE MEASUREMENT RESULTS OF SINGLE-STAGE AMPLIFIER

Different sizes of the single-stage amplifiers have been implemented and chip micrograph is shown in FIGURE 16.

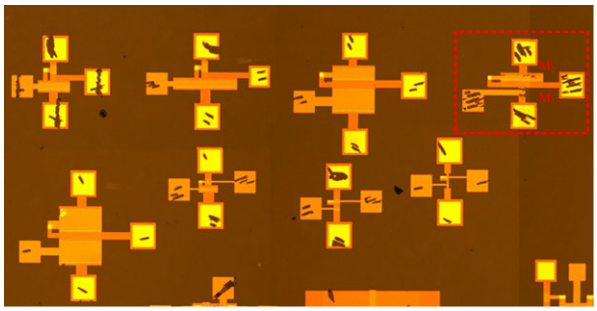


FIGURE 16. The different sizes of the single-stage amplifiers.

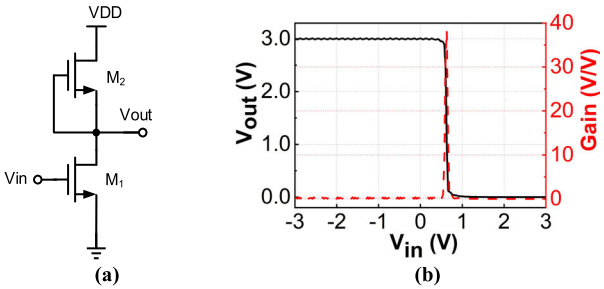


FIGURE 17. (a) The schematic of the signal-stage amplifier. (b) The output curve of the single-stage amplifier and the gain of the amplifier is around 36 (V/V).

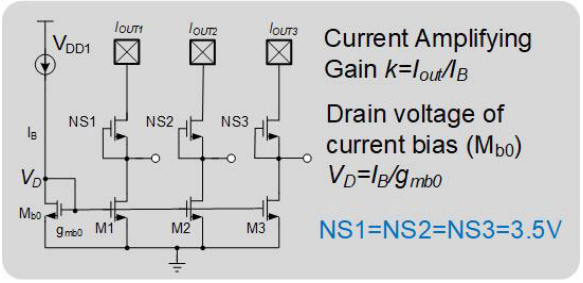


FIGURE 18. The circuit schematic of the current amplifying circuits.

FIGURE 17(a) shows chip micrograph which transistor size (W/L) of M_1 is 200 μm/20 μm and the size (W/L) of M_2 is 30 μm /30 μm. The transfer curve of the amplifier is shown in FIGURE 17(b). The supply voltage is 3 V and the input signal (Vin) is scanned from -3 V to 3 V. The negative input voltage is utilized to check the consistency of the output curves. The black curve is the output voltage measured by the analyzer and its range is from 3 V to 0 V as shown in FIGURE 17(b). The turning point is about 0.6 V which indicts the positive threshold voltage of the transistor. Therefore, the gain of single stage amplifier is around 31 dB. The gain curve is shown as the red dashed curve in FIGURE 17(b).

C. THE MEASUREMENT RESULTS OF CURRENT SIMULATION CIRCUITS

Different sizes of the MoS2 current mirror are shown in FIGURE 18 and both transistors are good current sources, which means that the output is in saturation state. If both

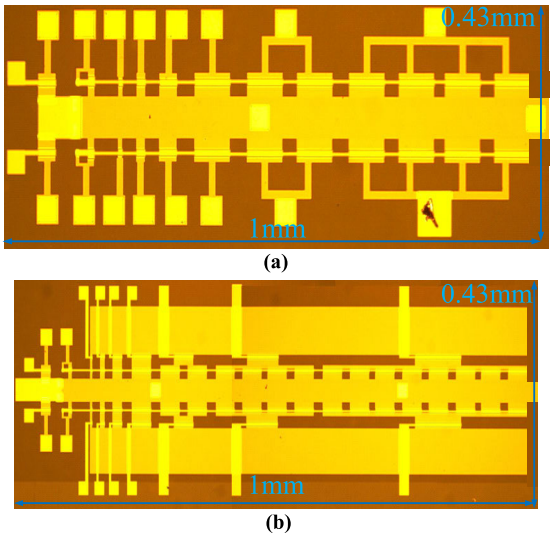
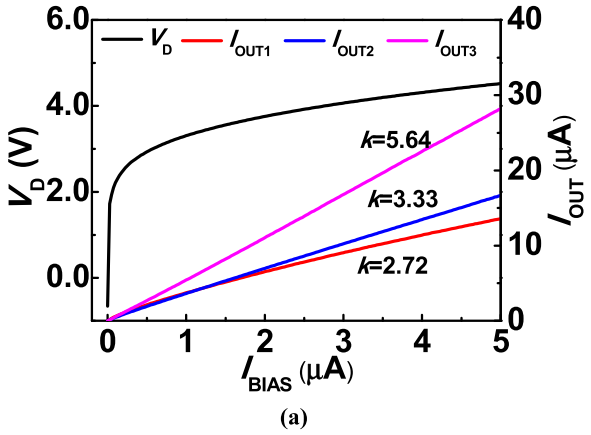


FIGURE 19. (a) The chip photo of the proposed current amplifying circuits for current stimulation. (b) Different layout structures of the proposed chips.



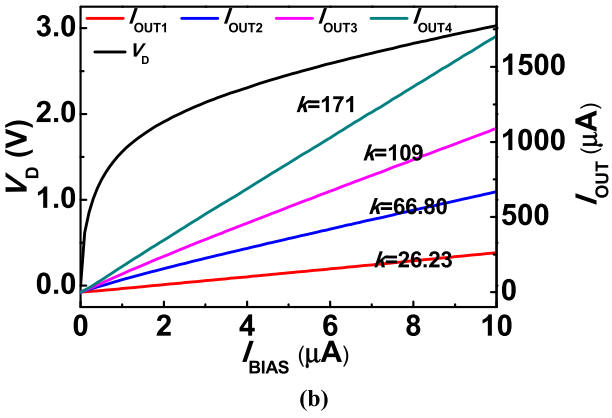


FIGURE 20. (a)-(b) The measurement results of the current gain from 2.72 to 171.

transistors are the same size, the output current source will produce the same current since they both have the same gate-source voltage. In order to show the current amplifying ability of the devices, the binary weight size of the transistors

is realized. Thus, the current sources will produce binary current values. The current can be on and off based on the state of the switch transistors. However, when the finite drain-source impedance is considered and a larger drain-source voltage will also have a larger current. By using long length transistors, the second effect can be reduced.

Two types of devices and layouts are realized as shown in FIGURE 19(a)-(b). With symmetry structure, the foldable with several nanometer thickness current stimulus generator for implantable simulation and measurement results of the current sink array are compared and show good agreement between the simulation and measurement. The measured current can be tuned from 0 μA to 1500 μA and the range can fully cover the implantable, flexible and transparent requirements as shown in FIGURE 20(a)-(b).

V. CONCLUSION

With the end of the Moore era, 2D materials have great potential application to replace rigid silicon in the next generation of electronics and optoelectronics. 2D devices can realize transparent, foldable and lightweight device for implantable and wearable devices. In this work, the MoS_2 enhancement-mode (E-mode) transistor based on CVD grows with accurate physical and SPICE modeling with industrial computer-aided design (CAD) flow is realized to enable complex circuits. Detail physical model and compact SPICE models are utilized to optimize the process and capture the different regions of device performance (subthreshold, linear, saturation). Furthermore, industrial design flow for the design, simulation, and layout of MoS_2-based chips is developed. Thus, the fabrication technology, modeling, and computer-aided design flow for circuits can be co-optimization. For the physical model simulation, the MPE is 4.49%, while for the SPICE model simulation, it is also below 7.00%. It shows that these models own enough accuracy for our analog circuit design. Then, the amplifier and current stimulation circuits are realized with good performance. The measurement shows the great promise of the technology for realizing high performance and complex chip. Finally, our measurements of the realized circuits are exhibited.

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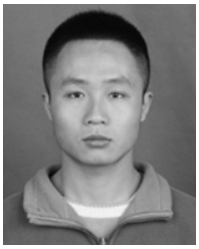

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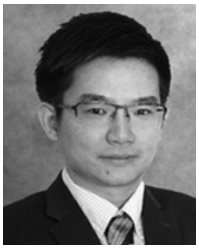

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