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Non-Isolated Fourth-Order Boost DC-DC Converter for Power Management in Low Voltage Low Power DC Grids: Design and Interaction Analysis

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ABSTRACT In this paper, a minimum-phase response fourth-order boost dc-dc converter (FBDC) exhibiting continuous input and output current is proposed. A voltage-mode controller is adopted to this converter to perform bus voltage regulation in a low voltage low power dc distribution system (LVPDS). FBDC supports additional load demand by interconnecting a second power source/battery. A systematic steady-state analysis for FBDC is established and the ripple content and other L-C design expressions are derived. The LVPDS is an integration of solar photovoltaic (PV) source using a conventional dc-dc boost converter (CBDC), and constant power load using a conventional dc-dc buck converter (CBuC). In this LVPDS, the FBDC primarily ensures dc bus voltage regulation, CBDC ensures the maximum power point tracking (MPPT) while CBuC regulates the load voltage. Various transfer function models, formulated through small-signal analysis, are used to address the controller design aspects and interconnected LVPDS stability issues. A generalized small-signal model of LVPDS is also developed to analyze the sub-system interactions arising during the coherent operation of BRC in this multi-converter system. The impact of connecting FBDC, as BRC, with other converters in the LVPDS is also analyzed. The laboratory prototype of a 48 V LVPDS is developed for experimental validation of bus voltage regulation and sub-system interactions. The theoretical and experimental results are found to be in close correlation with each other.

INDEX TERMS Fourth-order dc-dc boost converter, small-signal model, power stage design optimization, particle swarm optimization, low voltage low power dc distribution systems.

NOMENCLATURE

Bus voltage regulating converter	BRC	Low voltage low power dc distribution system	LVPDS
Bus voltage and Bus-side current	v_{bus}, i_{bus}	Loop gain of BRC	$R(s)_B$
Conventional boost converter	CBDC	Minor Loop Gain	MLG
Characteristics Equation LVPDS	CE	Particle Swarm Optimization based Design	PSOD
Control-to-bus volt TF of BRC	$G_{vd(s)B-o}$	Proposed Fourth-Order Boost Converter	FBDC
Continuous input continuous output	CICO	Passive Energy Storage Elements	ESE
Equivalent bus impedance of source and load converter	$Z(s)_{SL}$	Ripple Based Design	RBD
Input voltage/ current of BRC	V_B, I_B	Switching Devices	SD
		Small-signal TF Impedance/admittance	$Z(s) / Y(s)$
		Small-signal TF voltage/current gain	$M(s) / J(s)$
		Transfer Function	TF

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I. INTRODUCTION

Standalone single/multi-source low voltage low power dc distribution systems (LVPDS) involving small scale renewable energy generators (REGs) (such as solar photovoltaic (SPV), wind, fuel cell, and biomass, etc.), energy storage devices (batteries / ultra-capacitors) and loads have evolved as a viable solution not only to meet the power requirements of the secluded areas, still deprived of grid connectivity, but also of urban residential buildings to reduce their dependency on conventional energy sources [1]–[6]. LVPDS is formed by interconnecting several stages of dc-dc converters which process the power and carry out the power management task [3], [4]. The performance of LVPDS depends upon the performance of individual converters and hence selection of converter topologies, for various purposes, is very significant. For safe and reliable operation, standardization agencies have recommended 48 V and 24 V as safe operating voltages for residential consumers [5].

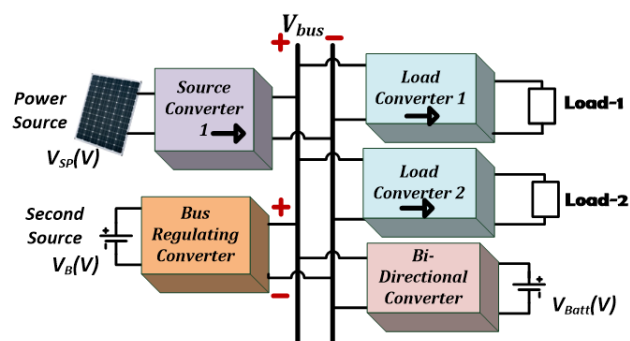


FIGURE 1. The architecture of low voltage low power dc distribution systems.

The generalized architecture of a multi-source LVPDS is shown in Fig. 1, wherein a source converter connects the SPV with the bus and also implements MPPT. The constant power loads are supplied via dc-dc buck converters while the energy storage device(s) are interfaced through bi-directional dc-dc converters [3], [4]. A second power source is interfaced, with the dc bus, using an additional dc-dc converter termed as ‘bus regulating converter’ (BRC). The role of BRC is to meet the additional load demand and also to regulate the bus voltage (V_{bus}) in the presence of fluctuations in the source and load. CBDC is widely used for this purpose but it exhibits (i) non-minimum phase (NMP) behavior due to the presence of right half plane (RHP) zero and (ii) discontinuous bus-side current (i_{bus}). The NMP behavior restricts the dynamic response of the converter by limiting its bandwidth to the frequency of RHP zero. Further, the existence of extra phase lag leads to control difficulties. Its effect is also observed in the start-up response and step change in duty ratio [7]. On the other hand, high current ripples result in more ac losses, thereby reduced efficiency, and induces harmonics and electromagnetic interference (EMI) [7]. The high peak-peak ripples have a larger impact when the working voltages are low. Therefore, the dc-dc converters with enhanced performance are a viable option

for interconnecting power sources within the LVPDS. The desired performance includes continuous input and output current exhibiting lower ripple content, low component count, high power density, faster dynamic response, etc.

Different dc-dc converters, exhibiting improved steady-state performance have been evolved by increasing the number of passive energy storage elements (ESE) and switching devices (SD) [6]–[24]. The performance and voltage gain of these converters depend upon the type of topology, the number of components, and their structural arrangement. Most of the boost topologies have continuous input current, due to the presence of an inductor at the input side, but the nature of load side current (whether continuous/discontinuous) depends on the placement of other circuit components in the converter [8], [9].

A tri-state boost converter having high voltage gain together with low source current ripple was proposed in [10] but its load current is discontinuous and it has six SDs. Boost converters proposed in [11]–[14] had two, four, five, and six switching devices, respectively. Converters having five and six ESEs were analyzed in [15]–[17]. A quasi-Y-source dc-dc converter having high voltage gain together with continuous input current is proposed in [18] but its load side current is discontinuous. Although, the above-discussed higher-order dc-dc boost converters [6]–[18] have a high voltage gain either their input/output current or both input and output currents are discontinuous.

Higher-order dc-dc converters having high voltage gain together with continuous input and output (CICO) current have been reported in [8], [19]–[24]. A group of dc-dc converters exhibiting continuous currents was presented in [8] while a high-gain boost converter exhibiting continuous input and output current is reported in [19] but it has seven energy storage elements and five switching devices.

A KY-Boost converter exhibiting continuous input and output current was proposed in [20] but it has five energy storage elements and three switching devices. A high gain boost converter in [21] exhibits CICO currents but its seven ESEs and five SDs. High gain boost converters proposed in [22], [23] has three SDs and five ESEs.

It is inferred from the above discussion that although increasing the number of ESEs and SD improves the converter performance but it also increases the converter order thereby leading to control complexity. Thus, there is a need to evolve topologies exhibiting improved steady-state and dynamic performance aspects. Particularly, the boost topologies with a minimum-phase response which finds wide utility in the low power dc-distribution systems.

Referring to Fig. 1, when the FBDC is coherently operated with other source and load converters sub-system interactions take place which may have a deteriorating effect on the performance and stability of other converters. However, the severity of the performance deterioration depends upon the converter topology and its design. The instabilities imposed due to load and source converters on LVPDS were discussed in [25], [26], respectively. A systematic approach

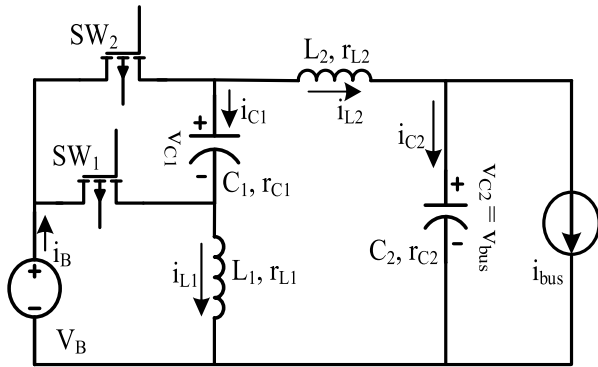


FIGURE 2. Circuit diagram of the proposed converter.

to design the load subsystem for stabilizing an unstable source converter was proposed in [27]. A local impedance-based stability criterion, depending upon the power imbalance conditions, was proposed in [28], [29] for a distributed system. The stability of the bi-directional dc-dc converter was analyzed using local impedance stability criterion in [30], [31].

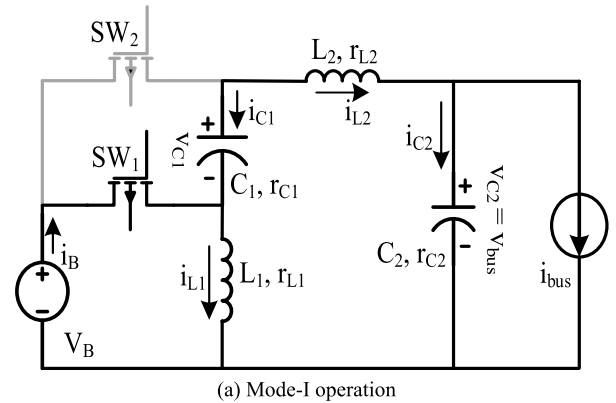
However, the effect of interactions arising due to the interconnection of bus regulating converter on other coherently operating converters needs detailed investigations. Therefore, a generalized small-signal model of the LVPDS is developed and used for analyzing the effect of subsystem interactions arising due to the interfacing of FBDC, as BRC, with other dc-dc converters in the LVPDS.

The main contributions of this paper are summarized as follows: (i) a low component count FBDC converter exhibiting continuous source and load current is proposed and analyzed as BRC in a LVPDS, (ii) a generalized small-signal model of the LVPDS is developed and used for analyzing the effect of subsystem interactions arising due to the interfacing of FBDC with other dc-dc converters in the LVPDS, and (iii) an optimized power stage design methodology is followed for designing FBDC, with the aim, to obtain minimum phase behavior and minimize sub-system interactions.

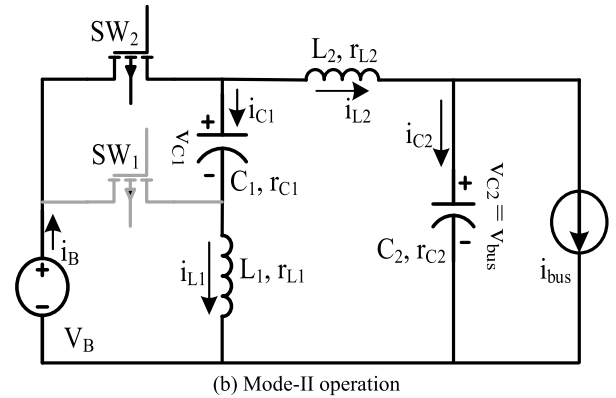
The rest of the paper is organized as follows: Section-II presents a detailed analysis of the power stage of the two-switch fourth-order boost converter. The controller design of FBDC is given in section-III. The architecture of low voltage low power dc distribution system (LVPDS) is discussed in section-IV. The derivation of the generalized small-signal model, considering the source and bus regulating dc-dc converter, is given in section-V. Experimental results are discussed in section-VI while conclusions are given in section-VII.

II. FOURTH-ORDER DC-DC BOOST CONVERTER

The circuit diagram of the proposed fourth-order boost dc-dc BRC is shown in Fig. 2. The salient features of this converter (FBDC) are: (a) exhibits minimum-phase behavior with reference to the control-to-output voltage transfer



(a) Mode-I operation



(b) Mode-II operation

FIGURE 3. Equivalent circuit of proposed converter (FBDC).

function, (b) ensures continuous input current with less ripple content, (c) ensures continuous output current with less ripple content, (d) voltage gain and switching stresses similar to CBDC, (f) low component count, and (h) simpler control structure, as compared to other higher-order dc-dc boost converters. A comparative analysis of the proposed FBDC with other state-of-the-art dc-dc boost converters is presented, in Table-11.

To characterize the proposed converter performance aspects, the continuous-conduction mode (CCM) of operation is analyzed in the following paragraphs. The proposed converter exhibits two modes of operation in one switching cycle. Switch SW_1 modulates with active duty ratio 'D_1' (D_2 = 1 - D_1) while the switch SW_2 operates complementary to it. The equivalent circuit of the converter during each mode is shown in Fig. 3(a)-(b), respectively. For uniformity in analysis, the direction of current in the inductors and capacitors marked for mode-I operation, in the equivalent circuit of Fig. 3(a), are retained for mode-II operation also. The key waveforms showing the nature of the steady-state currents and voltages in various converter components are given in Fig. 4 while the experimental results are given and discussed in section-VI. It is seen from Fig. 4 that both the inductors charges during Mode-I and discharges during Mode-II. On the other hand, the capacitor C_1 discharges during Mode-I and charges during Mode-II operation. The continuous nature of input current (I_B) and output current (I_bus) is also evident from Fig.4.

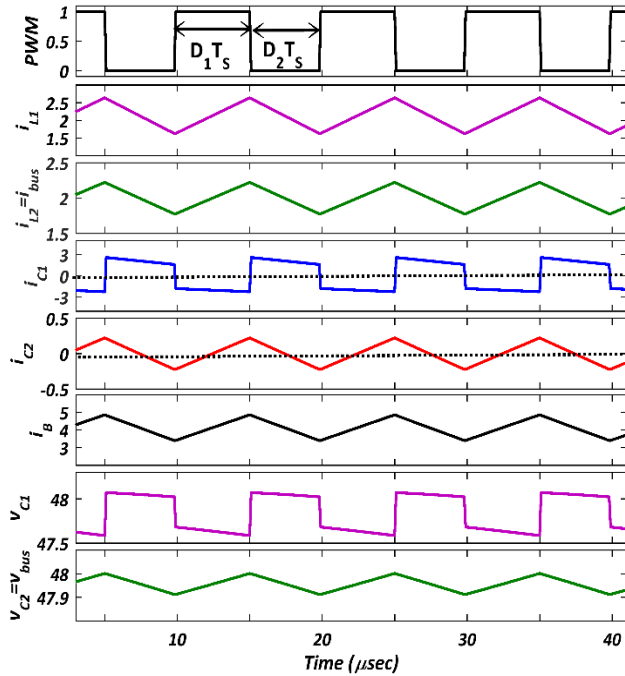


FIGURE 4. Key steady-state waveforms of the proposed converter.

A. STEADY-STATE AND TIME-DOMAIN ANALYSIS

The voltage gain of FBDC is obtained by applying inductor volt-sec balance to inductors L_1 and L_2 , respectively. The corresponding equations are given by (1), where, T_s is the switching time-period. The voltage gains of the converter, given by (2), is obtained by solving (1).

$$V_B D_1 T_s + (V_B - V_{C1}) D_2 T_s = 0$$

$$(V_B - V_{bus} + V_{C1}) D_1 T_s + (V_B - V_{bus}) D_2 T_s = 0 \tag{1}$$

$$V_{bus} = V_B / (1 - D_1) \tag{2}$$

The generalized expressions for the steady-state quantities of ESE and peak-peak ripple in inductor currents and capacitor voltages, given by Table-1 are derived from the instantaneous voltage applied across the inductors and the current flowing through the capacitors, respectively, during different modes of operation. The expressions for the voltage and current stresses across the switches are derived and given in Table 2 for ready reference.

B. SMALL-SIGNAL MODELING

The small-signal models of FBDC are formulated by assuming the dc bus as a current sink. The state-space representation of the converters, exhibiting linear time-invariant response (LTI), during each mode is given by (3).

$$\begin{cases} \dot{x} = [A_m] x + [B_m] u \\ y = [E_m] x + [F_m] u \end{cases} \tag{3}$$

TABLE 1. Expressions for steady-state design.

Design Equations	Steady-State Expressions
$\Delta i_{L1} = \frac{V_B D_1}{L_1 f_s}$	$I_{L1} = I_{bus} D_1 / D_2$ $I_B = I_{bus} / D_2$
$\Delta i_{L2} = \frac{(V_{bus} - V_B) D_2}{L_2 f_s}$	$I_{L2} = I_{bus}$
$\Delta v_{C1} = \frac{V_{bus} D_1}{RC_1 f_s} + \Delta i_{C1} r_{C1}$	$V_{C1} = V_{bus}$
$\Delta v_{C2} = \Delta i_{C2} \left(\frac{1}{8C_2 f_s} + r_{C2} \right)$	$V_{C2} = V_{bus}$
$i_B = i_{L1} + i_{L2}$ $\Delta i_B = \Delta i_{L1} + \Delta i_{L2} = \left\{ \left(\frac{1}{L_1} + \frac{1}{L_2} \right) V_{batt} D_1 T_s \right\}$	
$\Delta i_{L1}, \Delta i_{L2}$ = peak-to-peak ripple in inductor-1 and inductor-2 current Δi_B = peak-to-peak ripple in input current $\Delta v_{C1}, \Delta v_{C2}$ = peak-to-peak ripple in capacitor-1 and capacitor-2 voltage	

TABLE 2. Voltage and current stress on switching devices.

Current Stress on Devices	Voltage Stress on Devices
$I_{batt} + \frac{V_{batt} (L_1 + L_2) D_1}{2L_1 L_2 f_s}$	$\frac{V_{batt}}{(1 - D_1)}$

where $A_{km} \in \mathbb{R}^{N \times N}$, $B_{km} \in \mathbb{R}^{N \times 2}$, $E_{km} \in \mathbb{R}^{2 \times N}$, $F_m \in \mathbb{R}^{2 \times 2}$, state vector $x = [i_{L1} \ i_{L2} \ v_{C1} \ v_{C2}]^T$, input vector $u = [i_{bus} \ v_B]$, and output vector, $y = [v_{bus} \ i_B]^T$. Subscript ‘m = 1, 2’ is for Mode-I and Mode-II, respectively. The state $[A_m]$, input $[B_m]$, output $[E_m]$, and feed-through matrices $[F_m]$ are given by (A1) and (A2) in Appendix-A. The small-signal models, given by (4) and (5), are obtained as discussed in [15]. Here, the quantities with a ‘hat’ represent small-signal perturbations in the respective quantity. \hat{d} represents perturbation in duty ratio D_1 . The key equations to derive these models are given by (A3) and (A4) in Appendix-A.

$$(\Delta)_B = \begin{bmatrix} G_{vd}(s)_{B-o} & G_{id}(s)_{B-o} \end{bmatrix}^T = \begin{bmatrix} \hat{v}_{bus} \\ \hat{i}_{batt} \end{bmatrix} \frac{1}{\hat{d}} \tag{4}$$

$$(\Lambda)_B = \begin{bmatrix} Z(s)_{B-o} & M(s)_{B-o} \\ J(s)_{B-o} & Y(s)_{B-o} \end{bmatrix} = \begin{bmatrix} \hat{v}_{bus} & \hat{v}_{bus} \\ \hat{i}_{bus} & \hat{v}_{batt} \\ \hat{i}_{batt} & \hat{i}_{batt} \\ \hat{i}_{bus} & \hat{v}_{batt} \end{bmatrix} \tag{5}$$

Here, $G_{vd}(s)_{B-o}$ and $G_{id}(s)_{B-o}$ represents the small-signal control-to-bus voltage and control-to-battery current transfer functions (TF), respectively. Small-signal TFs $Z(s)_{B-o}$, $M(s)_{B-o}$, $J(s)_{B-o}$, and $Y(s)_{B-o}$ represents the open-loop grid impedance, audio-susceptibility, reverse audio susceptibility, and input admittance, respectively.

TABLE 3. Coefficients of $G_{vd}(s)_{B-o}$ given by (6).

Coefficient s	Generalized Values in terms of ESE and ESR
a_n	$-C_1C_2L_2V_Br_{C1}$
b_n	$C_1L_2D_2I_{Grid}r_{C1} - C_2L_2V_B$
c_n	$D_2V_B C_1r - V_B C_1r_{C1} + D_2I_{Grid}L_2$
d_n	$D_2V_B - V_B$
a_d	$(D_2 - 1)C_1C_2L_1L_2$
b_d	$(D_2 - 1)C_1C_2L_2r_{C1}$
c_d	$(D_2 - 1)(C_1L_1(D_2 - 1)^2 + C_2L_2 + C_1L_2D_2^2)$
d_d	$C_1r_{C1}(D_2 - 1)^3$
e_d	$(D_2 - 1)^3$

C. CONTROLLABILITY AND OBSERVABILITY OF FBDC

Controllability and observability are important aspects of the closed-loop operation of the dc-dc converters. A converter is controllable if and only if rank ‘N’ of controllability matrix ‘C’ is equal to the order of the converter TF. The controllability matrix ‘C’ for FBDC calculated using the procedure given in [32]-[33] is given by (A5). Here, it is observed that the rank of ‘C’ is 4 which indicates that FBDC is controllable.

A geometric hybrid approach [33], [34] is used to analyze the observability of FBDC. Here, the unobservable subspace, O_1^m of the system is obtained. The converter is completely observable if and only if, $O_1^m = \{0\}$, i.e. all elements of unobservable subspace are zero. The numerical values of unobservable subspaces for FBDC are given in (A6), in Appendix, where it is seen that all elements of O_1^m are zero. Therefore, the converter is completely observable.

D. POWER STAGE DESIGN AND ANALYSIS

The generalized expression of the control-to-bus voltage TF ‘ $G_{vd}(s)_{B-o}$ ’ of FBDC is given by (6) while the coefficients of its numerator and denominator are given in Table 3.

$$G_{vd}(s)_{B-o} = \frac{\hat{v}_{bus}}{\hat{d}} = \frac{(a_n s^3 + b_n s^2 + c_n s + d_n)}{a_d s^4 + b_d s^3 + c_d s^2 + d_d s + e_d} \quad (6)$$

It is observed from (6) and its pole-zero plot, given in Fig. 5, that ‘ $G_{vd}(s)_{B-o}$ ’ has two pairs of complex conjugate poles P_1 and P_2 placed at frequencies f_{P1} and f_{P2} , respectively. It also has a pair of complex-conjugate zeros Z_1 , placed at f_{Z1} , which exists in RHP, and a real zero Z_2 which exists inside the left-hand side plane (LHP). A deeper analysis of the control-to-bus voltage transfer function reveals that the complex-conjugate zero is placed between the poles P_1 and P_2 which may lead to the formation of an up-down glitch in its frequency response (FR) as shown in Fig. 6. The shape of the up-down glitch (i.e. its peak and width) depends on the damping of poles and zeros and the difference between the frequencies at which the P_2 and Z_1 are placed [11]. This up-down glitch not only has a deteriorating effect on the dynamic response and stability of FBDC but also leads to

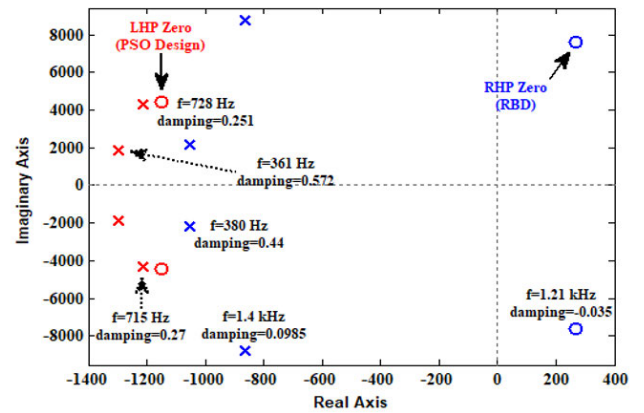


FIGURE 5. Pole-zero map of ‘control-to-bus voltage’ TF during boost mode for RBD and PSO design parameters showing shifting of complex-conjugate zeros from LHP to RHP.

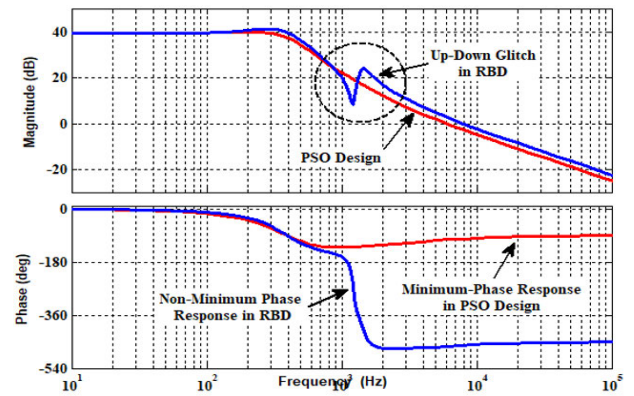


FIGURE 6. Frequency response of ‘control-to-bus voltage’ TF for RBD and PSO design showing up-down glitch and minimum and non-minimum phase behavior.

increased sub-system interactions when interconnected with other converters in LVPDS. The effect of interactions is more dominating in the frequency region where the up-down glitch is formed. Moreover, the presence of RHP zero restricts the control loop bandwidth thereby limiting its dynamic response. It is observed from Table 3 that the location of poles and zeros (magnitude and frequency), in the s-plane, depends upon the converter parameters, their parasitic resistances, and the operating point (i.e. duty ratio). Therefore, an appropriate selection of converter parameters may shift RHP zeros to LHP and also minimize the severity of up-down glitch. However, the manual selection of these parameters is very difficult due to the highly non-linear relation between the contradicting design requirements like placing zeros in LHP, minimizing up-down glitch, simultaneously meeting the steady-state requirements. Therefore, a Particle Swarm Optimization (PSO) based optimized power stage parameter selection procedure described in [11], [35] is followed, in this paper.

A multi-variable constrained optimization problem with the objective function given by (7) is formulated to minimize

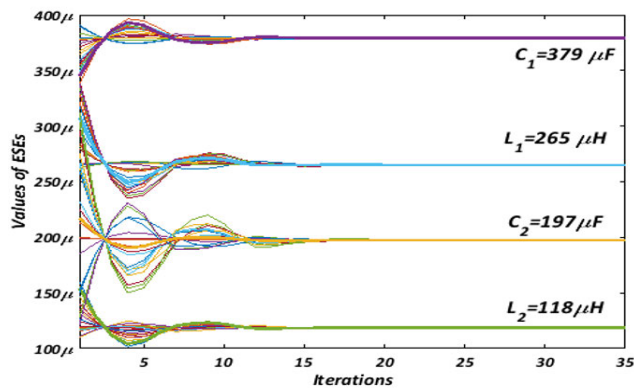


FIGURE 7. Variation of ESEs values against the number of iterations.

TABLE 4. Design specifications and power stage parameters.

	Ripple Based Design Parameters	PSO Design Parameters
$P_B=100$ W	$L_1=200$ μ H, $L_2=250$ μ H	$L_1=265$ μ H, $L_2=118$ μ H
$f_{sw} = 100$ kHz	$C_1=330$ μ F, $C_2= 33$ μ F	$C_1=380$ μ F, $C_2= 200$ μ F
$V_B = 24$ V		
$V_{bus}=48$ V		

the peak and width of up-down glitch subject to the following constraints: (i) peak-to-peak ripples in inductor currents and capacitor voltages are within specified limits, (ii) the poles of $G_{vd}(s)_{B-o}$ are inside LHP, (iii) the zeros of $G_{vd}(s)_{B-o}$ are inside LHP, and (iv) the damping of poles and zeros must be more than the threshold limits. Eq. (7) denotes the objective function of this optimization problem.

$$\text{Minimize } (|G_{vd}(s)_{B-o}| @f_{z1} - |G_{vd}(s)_{B-o}| @f_{p2}) \quad (7)$$

To minimize the above objective function, subject to the constraints, the following parameters are used in the PSO optimization process: (i) number of variables: 4, (ii) particle size: 20, and (iii) number of iterations: 35. The variations in the position of each particle in the parameter space with the number of iterations are shown in Fig. 7.

The values of the power stage design parameters obtained from the PSO design are given in Table 4 while the pole-zero plot for PSO design is shown in Fig. 5. The FR of $G_{vd}(s)_{B-o}$ for PSO designed parameters is shown in Fig. 6 where it is seen that the up-down glitch is not formed in the characterizing transfer-functions. It is also observed from Fig. 5 and the phase plot of Fig. 6 that the optimal selection of converter parameters has led to the shift of complex-conjugate zero of $G_{vd}(s)_{B-o}$ inside LHP which would have otherwise required an additional damping network or magnetic coupling.

The power stage of FBDC is also designed using conventional ripple-based design (RBD) for peak-to-peak ripple in inductor currents ($\Delta i_{L1}, \Delta i_{L2}$) < 20% and capacitor voltages ($\Delta v_{C1}, \Delta v_{C2}$) < 10%. The converter design parameters, obtained by substituting these requirements in the design equations of Table 2, are given in Table 4. The pole-zero

TABLE 5. Transfer function RBD and PSO design.

$G_{vd}(z)_{RBD}$	RBD	$\frac{0.2505(z-0.8592)(z^2-2z+1.005)}{(z^2-1.979z+0.9792)(z^2-1.975z+0.9829)}$
	PSO	$\frac{0.376(z-0.8763)(z^2-1.975z+0.9773)}{(z^2-1.974z+0.9744)(z^2-1.974z+0.9761)}$

map, for these parameters, is plotted in Fig. 5 wherein it is seen that the complex zero ‘Z1’ is placed in RHP. The FR of $G_{vd}(s)_{B-o}$, for RBD parameters, is shown in Fig. 6, wherein the formation of a dominant up-down glitch is seen.

III. DIGITAL CONTROLLER DESIGN

The block diagram representing the dynamics of source current ‘ i_B ’ and dc bus voltage ‘ v_{bus} ’, in terms of small-signal TFs, derived in (4)-(5), is shown in Fig. 8. A single loop voltage-mode control scheme with controller transfer function C_B is also shown in the figure. The closed-loop small-signal TFs, obtained by using the block diagram reduction technique, are given by (8)-(9), as shown at the bottom of the next page. Here, the quantities with subscript { }_{B-o} represents the open-loop TFs while subscript { }_B represents the closed-loop TFs.

$$\text{where, } J'(s)_B = Q(s)_B Z(s)_{B-o}, Y'(s)_B = Q(s)_B M(s)_{B-o}, H(s)_B = 1 + R(s)_B, R(s)_B = C(s)_B G(s)_{B-o}, Q(s)_B = C(s)_B P(s)_{B-o}$$

Here, $R(s)_B$ is the open-loop gain of FBDC which defines its closed-loop stability.

In this section, the digital controller is designed to regulate the dc bus voltage (v_{bus}) using the digital redesign approach wherein the converter model in s-domain is first converted into z-domain and then the digital controller is directly designed using discretized models. To design the controller, the discretized small-signal control-to-bus voltage TF $G_{vd}(z)_{B-o}$ is exported to the single input single output GUI environment of MATLAB. Here, the poles and zeros of the controllers are first placed to achieve absolute stability and then tuned to achieve relative stability as well [11]. The discretized control-to-bus voltage transfer functions, of FBDC, obtained by substituting the RBD and PSO design parameters from Table-4 are given in Table-5. The second-order digital controllers, for RBD and PSO design parameters, along with the obtained relative stability margins are given in Table-6 and Table-7, respectively. Here, it is observed that higher bandwidth is achieved with PSO design (836 Hz as against 382 Hz with RBD) as the up-down glitch is eliminated in this case.

IV. ARCHITECTURE OF LOW VOLTAGE LOW POWER DC DISTRIBUTION SYSTEM (LVPDS)

A detailed scaled-down architecture of LVPDS with distributed control is shown in Fig. 9. The frequency-dependent impedances, admittances, and the notations of voltages and currents of all the converters along with their polarities

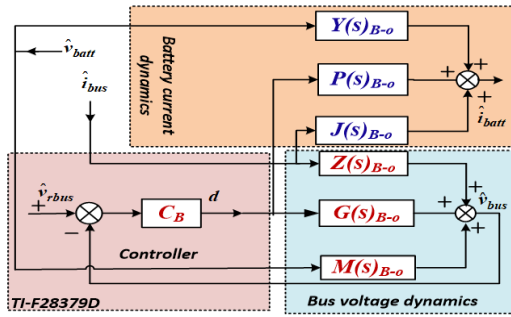


FIGURE 8. Block diagram representing the dynamics of battery current ‘ \hat{i}_{batt} ’ and bus voltage ‘ \hat{v}_{bus} ’ of FBDC with the single-loop voltage-mode control scheme.

TABLE 6. Digital controllers obtained from RBD and PSO design.

$C(z)_{RBD} = \frac{0.01527(z-0.9455)(z-0.931)}{(z-1)(z-0.7135)}$
$C(z)_{PSO} = \frac{0.9235(z-0.99)(z-0.98)}{(z-1)(z-0.04518)}$

TABLE 7. Relative stability margins.

Relative Stability Margins	Design Type	
	RBD	PSO
Phase Margin (PM) in degree	42	82
Gain Margin (GM) in dB	47	9.7
Bandwidth (BW) in Hz	382	836

are also marked. Subscript ‘B’ is used to indicate the TFs of BRC converter while suffix ‘S’ and ‘L’ are used to indicate the TFs of source and load converters in subsequent sections. Description of each converter is described below:

A. SOURCE CONVERTER

The SPV source is connected to the dc bus using the conventional dc-dc boost converter. The main role of the boost converter is to implement MPPT which is implemented using a two-stage controller. Here, Perturb-and-Observe MPPT algorithm is implemented which provides reference voltage ($v_{S,ref}$) for the control loop having a two-pole two-zero digital controller $\{C\}_S$. $\{C\}_S$ regulates the output voltage of SPV at v_{MPP} which is also the input voltage of source converter (v_S). Therefore, the closed-loop dynamics of its source voltage ‘ \hat{v}_S ’

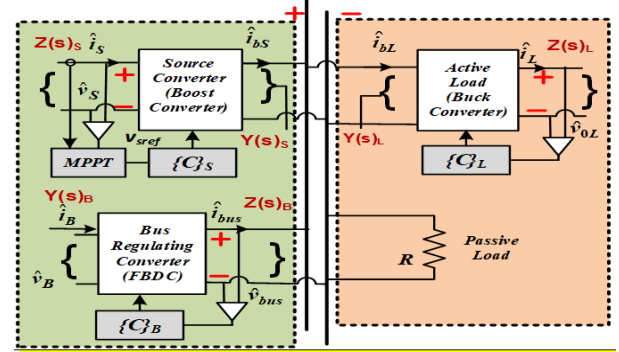


FIGURE 9. Block diagram of LVPDS showing impedance and admittance of source converter, load converter, and BRC.

and bus-side current ‘ \hat{i}_{bus} ’, given by (10), are significant for its interaction and stability analysis.

$$\begin{bmatrix} \hat{v}_S \\ \hat{i}_{bus} \end{bmatrix} = \begin{bmatrix} Z(s)_S & M(s)_S & G(s)_S \\ J(s)_S & Y(s)_S & P(s)_S \end{bmatrix} \begin{bmatrix} \hat{i}_S \\ \hat{v}_{bus} \\ \hat{v}_{rS} \end{bmatrix} \quad (10)$$

here, $Z(s)_S$ and $Y(s)_S$ are the input impedance and output admittance of the source converter, respectively.

B. BUS VOLTAGE REGULATING CONVERTER (BRC)

The FBDC, analyzed in the previous section, is proposed for voltage regulation of the dc bus. BRC connects a second source for supplying additional load demand. The power supplied by the source-2 varies depending upon the maximum power generated by the SPV, state-of-charge (SoC) of the battery, and the load demand. Bus voltage, v_{bus} is regulated by the controller, $\{C\}_B$ of BRC.

C. LOAD CONVERTER

The load connected to the dc bus is a constant power load fed through a conventional buck converter. The main role of this converter is to regulate the load voltage (v_{oL}). A simple voltage mode control is used wherein a two-pole two-zero digital controller $\{C\}_L$ regulates the load voltage. The small-signal closed-loop model of the load side converter is given by (11).

$$\begin{bmatrix} \hat{v}_L \\ \hat{i}_{bL} \end{bmatrix} = \begin{bmatrix} Z(s)_L & M(s)_L & G(s)_L \\ J(s)_L & Y(s)_L & P(s)_L \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{bus} \\ \hat{v}_{rL} \end{bmatrix} \quad (11)$$

$$\begin{bmatrix} \hat{v}_{bus} \\ \hat{i}_{batt} \end{bmatrix} = \begin{bmatrix} Z(s)_B & M(s)_B & G(s)_B \\ J(s)_B & Y(s)_B & P(s)_B \end{bmatrix} \begin{bmatrix} \hat{i}_{bus} \\ \hat{v}_{batt} \\ \hat{v}_{rbus} \end{bmatrix} = [K] \begin{bmatrix} \hat{i}_{bus} \\ \hat{v}_{batt} \\ \hat{v}_{rbus} \end{bmatrix} \quad (8)$$

$$[K] = \begin{bmatrix} \left(\frac{Z(s)_{B-o}}{H(s)_B} \right) & \left(\frac{M(s)_{B-o}}{H(s)_B} \right) & \left(\frac{R(s)_B}{H(s)_B} \right) \\ \left(J(s)_{B-o} - \frac{J'(s)_B}{H(s)_B} \right) & \left(Y(s)_{B-o} - \frac{Y'(s)_B}{H(s)_B} \right) & \left(\frac{Q(s)_B}{H(s)_B} \right) \end{bmatrix} \quad (9)$$

TABLE 8. Converter system design specifications.

Source-side converter: 2 nd order boost converter	
Switching frequency (f_{sw}) = 50 kHz	Ripple Based Design
Source voltage (V_{sp}) = 30 V	$L_1=400 \mu\text{H}$, $C_1=100 \mu\text{F}$
Power (P_{sp}) = 100 W	
Load-side converter: 2 nd order buck converter	
Switching frequency (f_{sw}) = 200 kHz	Ripple Based Design
Load Voltage (V_L) = 24 V	$L_1=400 \mu\text{H}$, $C_1=220 \mu\text{F}$
Load Power (P_L) = 30 W	$R_{load}=20 \Omega$

TABLE 9. Digital controllers for source and load side converters.

$C(z)_S = \frac{0.11(z-0.92)(z-0.9932)}{(z-1)(z-0.04134)}$	$C(z)_L = \frac{1.1559(z-0.9677)(z-0.9461)}{(z-1)(z-0.8348)}$
--	---

D. PASSIVE DC LOADS

The passive dc loads are sometimes directly connected to the dc bus. The power drawn by such loads depends on the bus voltage, v_{bus} . For analysis, all such loads are combined and represented by an equivalent load 'R' as shown in functional block diagram Fig. 9. The design parameters for the source and load side converter are given in Table 8. The second-order controllers used for regulating the output voltage of SPV and load voltage of the load side converter are given in Table 9.

V. FORMULATION OF GENERALIZED SMALL-SIGNAL MODEL FOR SUB-SYSTEM INTERACTION ANALYSIS

In this section, a generalized small-signal model of the LVPDS is developed and used for analyzing the effect of sub-system interactions arising due to the interconnection of BRC with other converters. Although, the model here is derived for LVPDS comprising of two sources and one load converter it can be scaled up for multiple interconnected converters. The small-signal model for LVPDS is formulated from the individual closed-loop small-signal models of the BRC, source converter, and load converter given by (8), (10), and (11), respectively.

The generalized expression of the bus-side current of FBDC, obtained, from Fig. 9, is given by (12).

$$\hat{i}_{bus} = (\hat{i}_{bL} - \hat{i}_{bS} + \frac{\hat{v}_{bus}}{R}) \quad (12)$$

Substituting the expressions of ' \hat{i}_{bS} ' and ' \hat{i}_{bL} ', obtained from (10) and (11), respectively, gives (13) which represents the dynamics of ' \hat{i}_{bus} '. Eq. (13) is then substituted in (8) to obtain the expression for ' \hat{v}_{bus} ' in terms of input quantities (\hat{i}_{bus} , \hat{v}_{batt} and \hat{v}_{rbus}) and is given by (14) which in simplified form is given (15).

$$\hat{i}_{bus} = Y(s)_L \hat{v}_{bus} - J(s)_S \hat{i}_S - Y(s)_S \hat{v}_{bus} - P(s)_S \hat{v}_{rS} \quad (13)$$

$$\begin{aligned} \hat{v}_{bus} (1 - Z(s)_B (Y(s)_L - Y(s)_S)) \\ = M(s)_B \hat{v}_{batt} - Z(s)_B P(s)_S \hat{v}_{rS} \\ - J(s)_S Z(s)_B \hat{i}_S + G(s)_B \hat{v}_{rB} \end{aligned} \quad (14)$$

$$\hat{v}_{bus} = \frac{1}{CE} \left(M(s)_B \hat{v}_{batt} - Z(s)_B P(s)_S \hat{v}_{rS} + Z(s)_B J(s)_S \hat{i}_S + G(s)_B \hat{v}_{rB} \right) \quad (15)$$

' \hat{v}_{bus} ', obtained in (15) is then substituted in (10) to obtain the expression for \hat{v}_S , given by (16), in terms of input quantities (\hat{i}_S and \hat{v}_{batt}) and control quantities (\hat{v}_{rS} and \hat{v}_{rbus}).

$$\hat{v}_S = \frac{1}{CE} \left(\begin{aligned} &M(s)_B M(s)_S \hat{v}_{batt} + (G^1(s)_B - P^1(s)_S) \hat{v}_{rS} \\ &+ Z(s)_B \hat{i}_S + M(s)_B G(s)_B \hat{v}_{rB} \end{aligned} \right) \quad (16)$$

Eq. (15) and (16) together form the small-signal model of LVPDS and is given by (17).

$$\begin{aligned} \begin{bmatrix} \hat{v}_{bus} \\ \hat{v}_S \end{bmatrix} \\ = \frac{1}{CE} \left(\begin{aligned} &\begin{bmatrix} Z(s)_B J(s)_S & M(s)_B \\ Z(s)_B & M(s)_B M(s)_S \end{bmatrix} \begin{bmatrix} \hat{i}_S \\ \hat{v}_{batt} \end{bmatrix} \\ &+ \begin{bmatrix} -Z(s)_B P(s)_S & G(s)_B \\ G^1(s)_B - P^1(s)_S & M(s)_B G(s)_B \end{bmatrix} \begin{bmatrix} \hat{v}_{rS} \\ \hat{v}_{rbus} \end{bmatrix} \end{aligned} \right) \end{aligned} \quad (17)$$

$$\begin{aligned} CE \\ = 1 - (Z(s)_B (Y(s)_L - Y(s)_S)) \end{aligned} \quad (18)$$

$$\begin{aligned} \text{MLG} \\ = 1 - CE = Z(s)_B (Y(s)_L - Y(s)_S) = \frac{Z(s)_B}{Z(s)_S L} \end{aligned} \quad (19)$$

where,

$$Z^1(s)_S = Z(s)_S CE - M(s)_S Z(s)_B,$$

$$G^1(s)_S = G(s)_S CE, \quad P^1(s)_S = P(s)_S Z(s)_B M(s)_S$$

This model is derived, for the case, when the source converter is a current-fed converter and bus is regulated by BRC. Here, the quantities to be regulated are source voltage \hat{v}_S of source converter and bus voltage \hat{v}_{bus} .

The generalized expression of the minor loop gain (MLG), which defines the stability of the interconnected converters is obtained from the characteristic equation 'CE'. CE is given in (18) while the MLG is given by (19). Here, it is observed that the minor loop gains depend on the bus-side impedance/admittance of FBDC, source and load converter $Z(s)_B$, $Y(s)_S$, and $Y(s)_L$, respectively.

A. INTERACTION ANALYSIS OF FBDC WITH OTHER CONVERTERS IN LVPDS

In this section, the sub-system interactions arising due to the interconnection of FBDC with the LVPDS are analyzed using the small-signal model developed in the previous section. The effect of these interactions on other converters operating in LVPDS is also analyzed. From the well-established impedance stability criterion [27], [28], the interactions are minimum and the stability is ensured when (20) is satisfied.

$$\begin{aligned} \sum |Z(s)_B| < \sum |Z(s)_S L| \quad \forall f \\ \text{MLG} = \sum |Z(s)_B| / \sum |Z(s)_S L| < 1 \quad \forall f \end{aligned} \quad (20)$$

MLG and loop gains of the interconnected converters, required for interaction analysis, are obtained using (17)-(19) and plotted in Fig. 10. The FR of the closed-loop bus-side

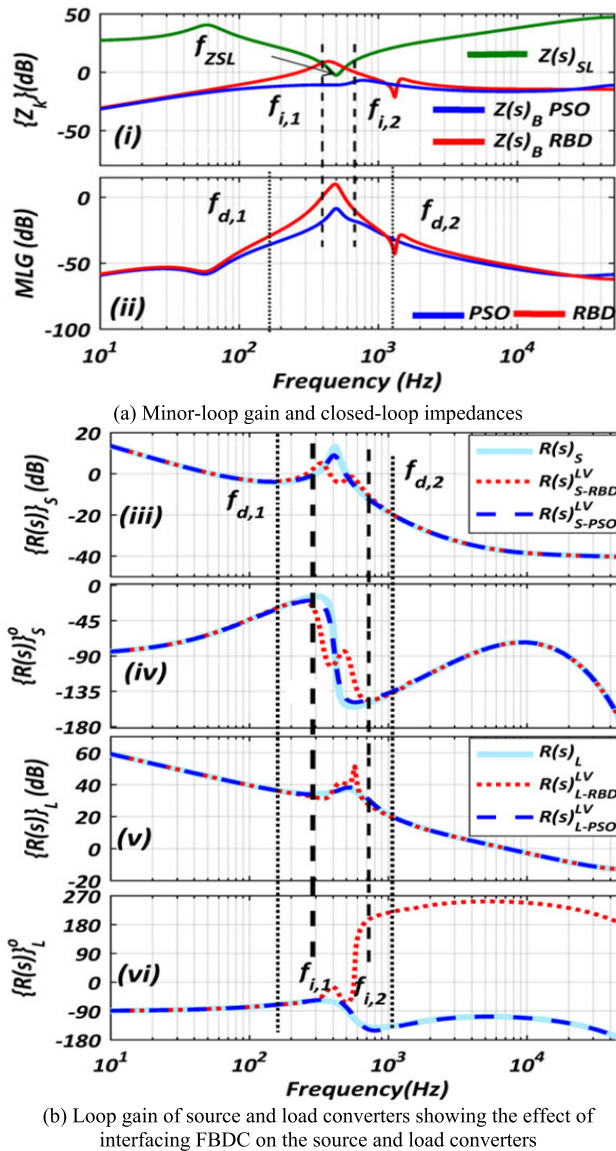


FIGURE 10. Effect of sub-system interactions on the stability of LVPDS, source converter, and load converter.

impedance $Z(s)_{B-RBD}$ and $Z(s)_{B-PSO}$ of FBDC, for RBD and PSO design, respectively are plotted in Fig. 10 (a). These impedances are superimposed with the equivalent bus-side impedance of the source and load converter $Z(s)_{SL}$ in the same figures. Here, it is observed that the FR $Z(s)_{B-RBD}$ intersect with that of $Z(s)_{SL}$ but the FR of $Z(s)_{B-PSO}$ does not intersect with it. This is because the loop gain bandwidth for RBD is 382 Hz which is less than f_{zSL} , the frequency of first resonance in $Z(s)_{SL}$ while the loop gain bandwidth for PSO design is 836 Hz which is greater than f_{zSL} . It is therefore inferred that the sub-system interactions take place when the converter is designed using RBD. This is due to the formation of a dominant up-down glitch. However, interactions are mitigated when designed using PSO. A similar inference is also obtained from the FR of MLG, plotted in Fig. 10 (a-ii), where it is observed that the MLG crosses

the 0 dB line for RBD but it does not cross for PSO design. The FR of loop gain of source converter $R(s)_S$, the interfaced loop gain of source converter for RBD, and PSO design $R(s)_{S-RBD}^{LV}$ and $R(s)_{S-PSO}^{LV}$, respectively, are superimposed in Fig. 10 (b) (iii)-(iv), for RBD and PSO design, respectively. It is observed from Fig. 10 (b-iii) that the FR of $R(s)_{S-RBD}^{LV}$ gets distorted in the frequency range where MLG_{RBD} is greater than 0 dB leading to the formation of an up-down glitch in the magnitude plot. This up-down glitch may induce conditional instability in the source converter. However, it is observed that the FR of $R(s)_{S-PSO}^{LV}$ is identical to $R(s)_S$ indicating that when FBDC is designed using PSO it does not alter the dynamic characteristics of the source converter.

To analyze the effect of sub-system interactions on load converter, the FR of loop gain of load converter $R(s)_L$, the interfaced loop gain of load converter in case of RBD and PSO design $R(s)_{L-RBD}^{LV}$ and $R(s)_{L-PSO}^{LV}$, respectively, are superimposed in Fig. 10 (b) (v)-(vi). It is observed from Fig. 10 (b-v) that the FR of $R(s)_{L-RBD}^{LV}$ gets distorted in the frequency range where MLG_{RBD} is greater than 0 dB. Not only an up-down glitch is formed in $R(s)_{L-RBD}^{LV}$ but the converter behavior also changes from minimum phase to non-minimum phase, as can be seen from its phase plot in Fig. 10 (b-vi). This will not only deteriorate the dynamic performance of the LVPDS but may also destabilize it. However, the FR of $R(s)_{L-PSO}^{LV}$ is identical to $R(s)_L$ which depicts that the interfacing of FBDC with PSO designed parameters do not affect the performance of the load converter.

VI. RESULTS AND DISCUSSIONS

The analytical concepts developed in the previous sections are experimentally verified on the laboratory prototype of the 48V LVPDS. The image of the experimental testbed is shown in Fig. 11. Here, a battery is interfaced via FBDC as a secondary source in an LVPDS to regulate the bus voltage. The zoomed image of a laboratory prototype FBDC, designed using converter parameters given in Table-3 is also shown. The digital control laws are implemented using the Texas Instruments' F28379-D controller. The TerraSAS ETS80 solar array emulator is used to emulate the characteristics of SPV. Initially, the steady-state and dynamic results of FBDC for standalone operation is presented thereafter results for its coherent operation with other converters interfaced in LVPDS, is presented.

A. FBDC AS STANDALONE CONVERTER

The experimentally measured steady-state waveforms of inductor currents (I_{L1} and I_{L2}), input current (I_B), and output voltage of FBDC, ($V_{C2} = V_{bus}$), under nominal operating conditions, are shown in Fig. 12. Here, it is seen that the input current and the output (bus-side) current are continuous and have lower peak-to-peak ripples. The lower ripples reduce the ac losses, which increases the converter efficiency and life of the power source. The variation in the voltage gain of the converter against variation in the duty ratio is plotted in Fig. 13 (a). The variation in the voltage gain of FBDC



FIGURE 11. Experimental prototype of DC-NG: 1. DSO, 2. TerraSAS ETS80, 3. FBDC, 4. Digital Controller, 5. Battery, 6. Source converter, 7. Load converter, 8. Driver and Sensor Circuits.

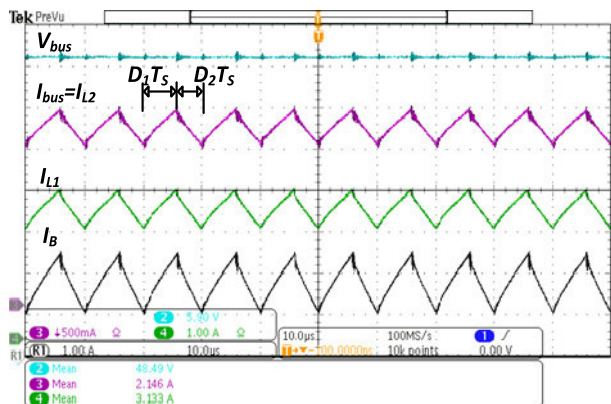
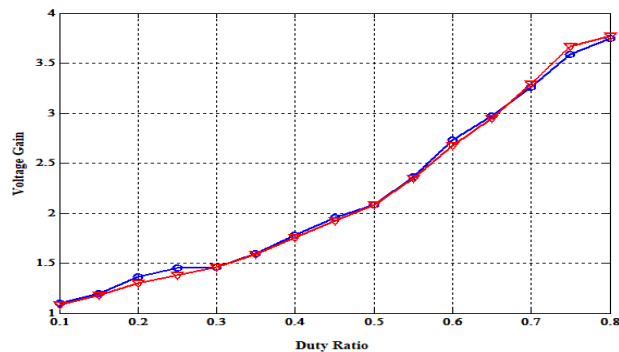


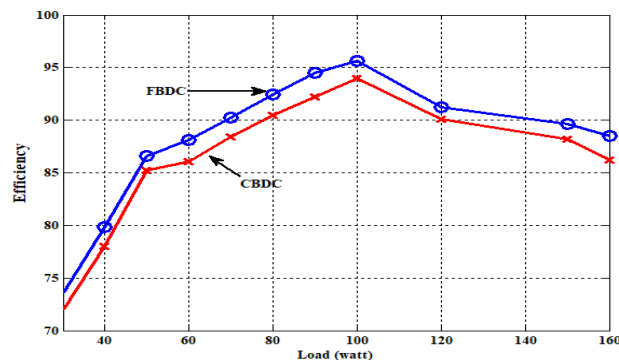
FIGURE 12. Steady-state waveforms of inductor currents (I_{L1} and I_{L2}), input/ battery current (I_B) and capacitive voltage ($V_{C2} = V_{bus}$).

is almost identical to that of CBDC. The experimentally obtained plot of efficiency vs power is plotted and compared with CBDC in Fig. 13 (b) which shows that even though FBDC has four energy storage elements its efficiency is almost comparable with CBDC.

The dynamic response of the converter for step-change in the load current I_{bus} from 1.5 A to 2.5 A, i.e. 66.67% change, is shown in Fig. 14. Here, it is observed that the second source supplies the additional current which increases from 3.1 A to 5.2 A. It is also seen that the bus voltage is regulated at 48 V. The experimental results to demonstrate that FBDC exhibits improved dynamic performance, for parameters designed using PSO, are given in Fig. 15. Here, the dynamic response of FBDC designed using RBD and PSO design is compared. For comparison purposes, the experimentally obtained data points, for both cases, are exported to Matlab for data handling. It can be seen in Fig. 15 (a) that although the bus voltage is regulated for both the design parameters, regulation time is quite less for PSO design as compared to RBD. Moreover, higher undershoot is observed for RBD design. This is because the loop gain bandwidth and phase margin for RBD design is less than that of PSO design. The dynamic response for the step decreases in bus current is shown in Fig. 15(b). Here, it is seen that although the converter, with RBD parameters, tries to regulate the bus voltage the response is not stable.



(a) voltage gain comparison with CBDC



(b) efficiency comparison with CBDC

FIGURE 13. Performance comparison of FBDC with CBDC [9].

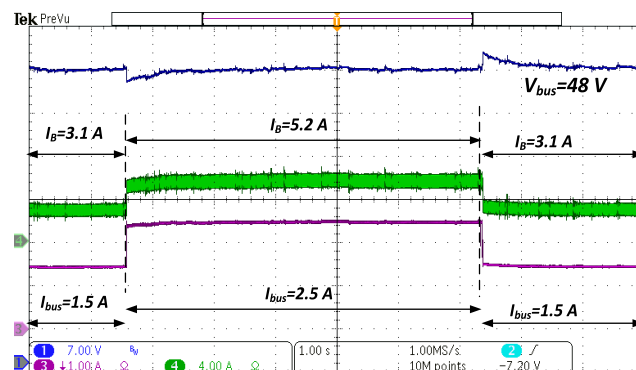
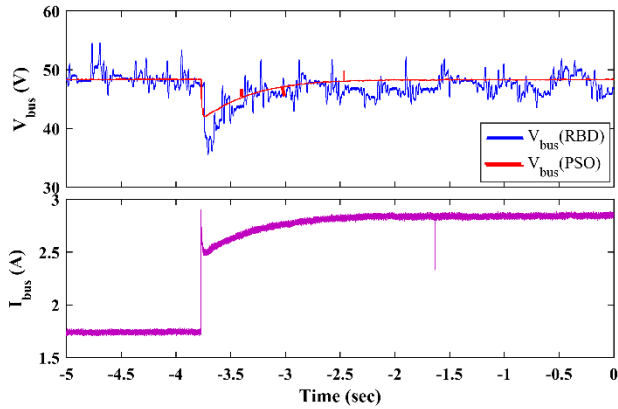


FIGURE 14. Dynamic response for step-change in ' I_{bus} '.

Fig. 16 shows the comparison of the dynamic response of the proposed FBDC with other dc-dc boost converters exhibiting continuous input and continuous output current. In this figure dynamic performance of CICO-1 [21], CICO-2 [23], and CICO [24] are compared with the proposed converter. The dynamic response is plotted for step-change in load current I_{bus} from 2 A to 3.2 A. Here, it is observed that the proposed converter exhibits a better response with minimum undershoot as compared to other converters.

B. FBDC FOR DC BUS VOLTAGE REGULATION IN LVPDS

As described in previous sections, FBDC regulates the bus voltage, the load side converter regulates the load voltage, and the source converter ensures MPPT.



(a) Step increase in bus current ' i_{bus} '
 (b) Step decrease in bus current ' i_{bus} '

FIGURE 15. Comparison of dynamic response for RBD and PSO design.

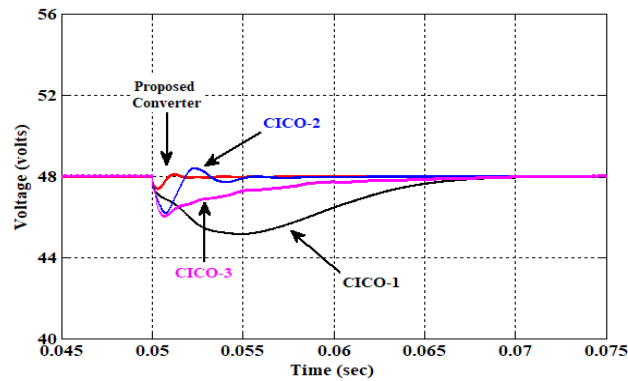


FIGURE 16. Dynamic performance comparison of dc-dc boost converters exhibiting continuous input continuous output (CICO) current for a step change in load current from 2 A to 3.2 A.

Depending upon the local weather conditions when the solar PV power is less than the load power; the source converter and FBDC get connected in parallel to supply the load. The 180 Wp solar panel is connected to provide power to an active load rated at 24 V, 30 W and variable passive load that varies between 30 to 190 W. As the power supplied by SPV and loads are intermittent, the FBDC regulates the dc bus voltage simultaneously supplying additional load demand. The solar panel power generation data at different insolation levels are given in Table-10. The screenshots of the solar array emulator interface software showing MPPT at different

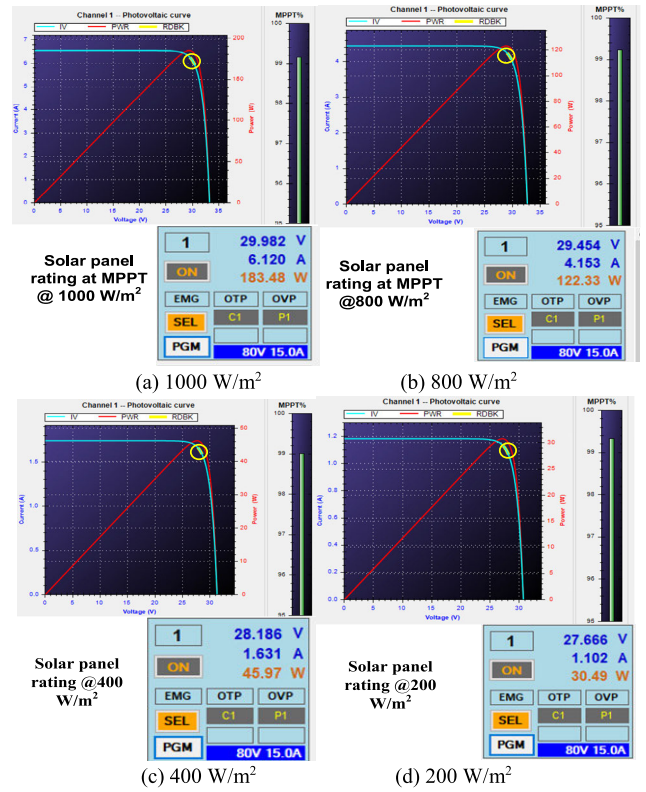


FIGURE 17. Screenshots of solar array emulator showing MPPT.

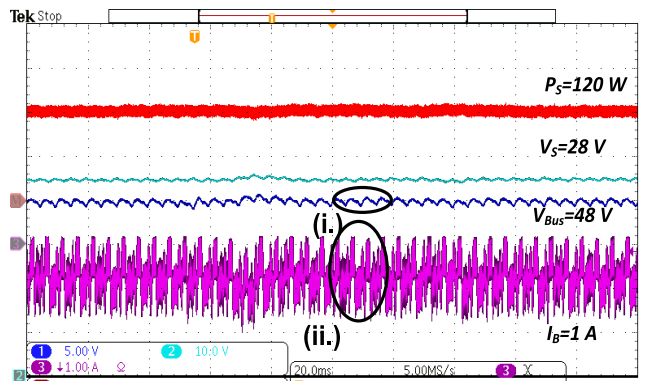
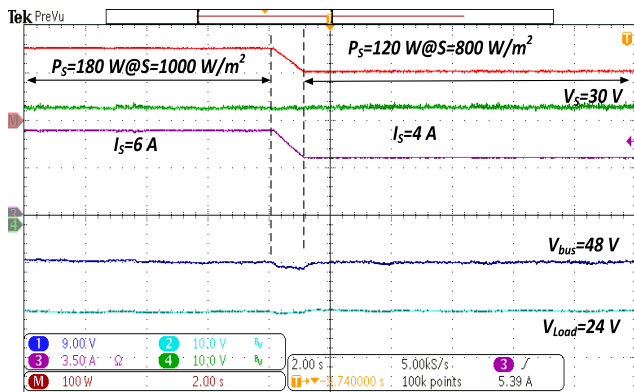


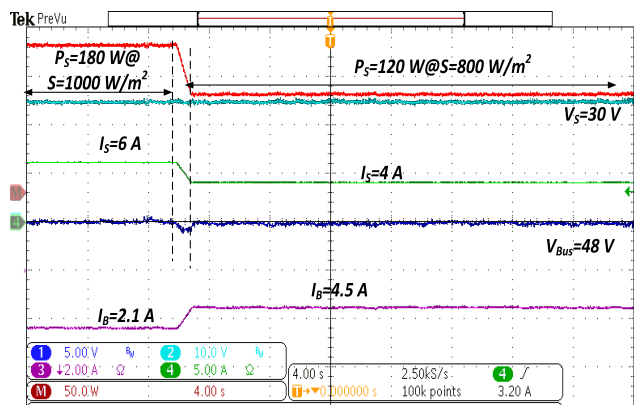
FIGURE 18. Dynamic response of LVPDS when connected to RBD designed FBDC.

irradiance levels are shown in Fig. 17. The corresponding voltage, current, and power are also shown in the figures. In case, the battery is fully charged and the power generated by SPV and second power source is greater than the load demand then the source converter is controlled to operate at OFF MPPT point in-order to ensure power balance within the LVPDS.

Figure 18 shows the performance of LVPDS, when FBDC designed using RBD is connected as BRC. As the impedance $Z(s)_B$ of the FBDC overlaps with the impedance $Z(s)_{SL}$ of source and load converter sub-system interactions take place and affect the performance of the other interconnected converters, as shown in Fig. 10. The sub-system interaction causes low-frequency but high magnitude oscillations in the



(a) Step change in irradiance to show voltage regulation



(b) Step change in irradiance to show power balance

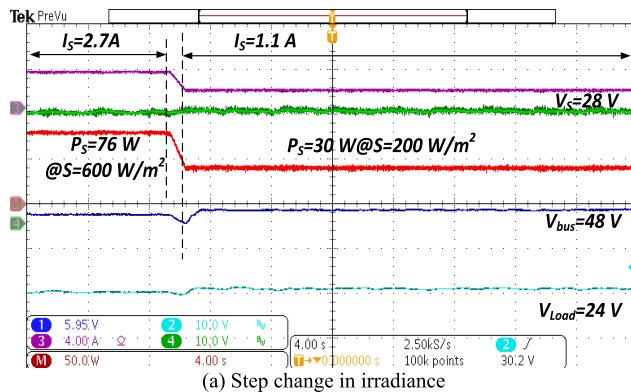
FIGURE 19. Dynamic response of LVPDS for higher irradiation levels.

TABLE 10. Specifications of solar array emulator.

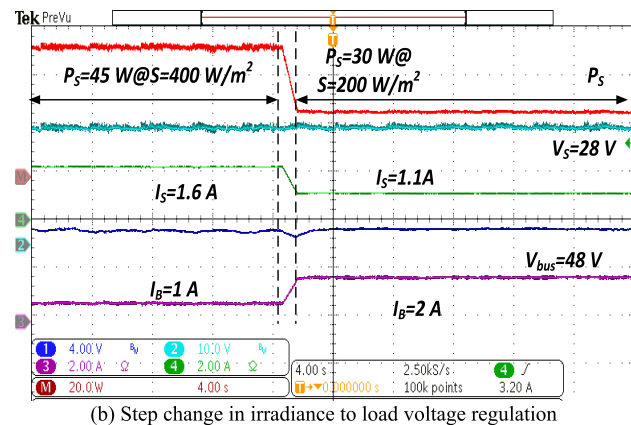
Irradiation (W/m ²)	P _S (Watt)	V _S (Volt)	I _S (Amp)
1000	183	29.98	6.12
600	122	29.45	4.15
400	45.97	28.19	1.63
200	30.49	27.67	1.1

SPV voltage, bus voltage, and input current of FBDC. These as shown in regions (i) and (ii) of Fig. 18. It is therefore inferred that the formation of up-down glitch with RBD parameters results in sub-system interactions which deteriorates the performance of LVPDS.

The experimental results for the coherent operation of converters in LVPDS are shown in Fig. 19 to 21. While carrying out the experiments, FBDC with parameters designed using PSO is used. The experimental results for variation in solar irradiation (S) from S = 1000 W/m² to 800 W/m² are shown in Fig. 19 (a) where it is observed that even though the SPV power is reduced the power balance is maintained in the LVPDS. FBDC regulates the bus voltage while the load converter regulates the load voltage at 48 V and 24 V, respectively. In this case, a 190 W passive load is introduced for validating the operation of FBDC at higher irradiation levels. It is observed from Fig. 19 (b) that when the SPV generation is decreased from 180 W to 120 W, the input current drawn by FBDC is increased from 2.1 A to 4.5 A



(a) Step change in irradiance



(b) Step change in irradiance to load voltage regulation

FIGURE 20. Dynamic response of LVPDS for lower irradiation levels.

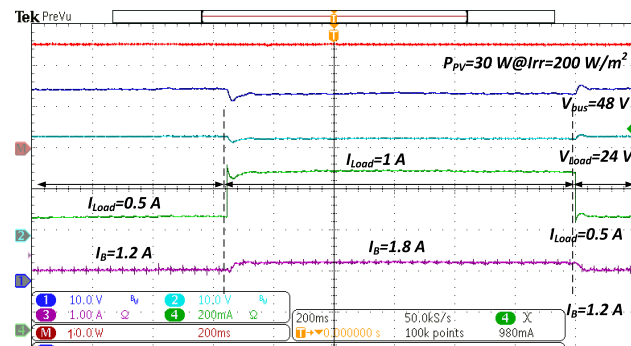


FIGURE 21. Dynamic response of LVPDS for step load change showing source, load and bus voltage regulation.

to compensate for the decrease in power and to maintain the power balance in the LVPDS. The experimental results for the coherent operation of the converters during low irradianations are shown in Fig. 20.

A 40 W passive load is connected to the bus. Fig. 20 (a) shows the effect of gradual variation in solar irradiation from S = 600 W/m² to S = 200 W/m². The source converter tracks the maximum power as it changes from P_S = 76 W to P_S = 30 W with SPV current (I_S) changed from 2.7 A to 1.1 A and SPV voltage regulated at V_S = 28 V. The load converter regulates load voltage at V_{Load} = 24 V and FBDC regulates the bus voltage at V_{bus} = 48 V. Although, the slight steady-state error is observed in V_{bus} but it is well within acceptable limits of low voltage dc grids.

The experimental results for change in irradiation from $S = 400 \text{ W/m}^2$ to $S = 200 \text{ W/m}^2$ are shown in Fig. 20(b). During a decrease in solar irradiance, it is observed that the BRC converter regulates the bus voltage and compensates for additional load demand by an increase in its input current from 0.5 A to 2 A. Meanwhile, the load voltage is regulated at 24 V with a constant load current. The experimental results for the increase in load current from 0.5 A to 1 A at constant solar power are shown in Fig. 21. It is observed here that the FBDC input current increases from 1.2 A to 1.8 A. Here, it is seen that the bus voltage and the load voltage are regulated to their respective reference values while the battery current increases to meet the increased load demand.

VII. CONCLUSION

In this paper, a low component count fourth-order boost converter, which exhibits continuous input and output current, was proposed for bus voltage regulation of LVPDS. The small-signal analysis of the converter revealed the formation of an up-down glitch in the converter models. The impact of glitch was minimized by optimal selection of the values of energy storage elements. Also, it was demonstrated that the optimal parameter selection shifted the RHP zero to LHP simultaneously mitigating the impact of up-down glitch in the converter models. This not only improved the dynamic performance and stability of the FBDC but also minimized the sub-system interactions within the LVPDS. A generalized small-signal model of LVPDS was derived and used to analyze the effect of sub-system interactions arising due to interconnection of FBDC with other coherently operating converters in the LVPDS. It was shown, through frequency response analysis, that RBD design parameters resulted in sub-system interactions which was reflected in the form of sustained oscillations in the experimentally obtained

time-domain results for standalone and coherent operation. The power management feature of the LVPDS was demonstrated experimentally wherein it was shown that FBDC regulates the dc bus voltage simultaneously supplying the extra load demand when the SPV generation decreases. The analytical predictions were found to be in close agreement with the experimental results.

APPENDIX

A. STATE, INPUT AND OUTPUT MATRICES FOR STATE-SPACE MODEL

The state $[A_k]$, input $[B_k]$, output $[E_k]$, and feed-through matrices $[F_k]$, for FBDC, are given in this appendix. The equations for obtaining the small-signal models in ‘s’ domain are also given.

$$\begin{aligned}
 A_1 &= \begin{bmatrix} -\frac{R_p}{L_1} & 0 & \frac{-1}{L_1} & \frac{1}{L_1} \\ 0 & \frac{-r_{L2}}{L_2} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{-1}{C_2} & 0 & 0 & 0 \end{bmatrix}, \\
 A_2 &= \begin{bmatrix} \frac{-(r_{L1} + r_{C1})}{L_1} & 0 & \frac{-1}{L_1} & 0 \\ 0 & \frac{-(r_{L2} + r_{C2})}{L_2} & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 \end{bmatrix} \tag{A1}
 \end{aligned}$$

TABLE 11. Comparative analysis of the proposed converter with other state-of-the-art non-isolated higher-order boost dc-dc converters reported in literature.

	Topology-1 [13]	Topology-2 [18]	Topology-3 [4]	Topology-4 [21]	Topology-5 [19]	Topology-6 [22]	Proposed converter
Source current	Continuous	Continuous	Discontinuous	Continuous	Continuous	Continuous	Continuous
Output current	Discontinuous	Discontinuous	Continuous	Continuous	Continuous	Continuous	Continuous
Nos. of switching devices	5	5	3	5	5	3	2
Nos. of inductors / capacitors	2	5	2	2	1	2	2
	2	4	1	5	2	3	2
Coupled Inductors	No	Yes	No	No	No	No	No
Voltage Gain	$\frac{1}{D(1-D)}$	$\frac{1}{1-K^I}$	$\frac{1}{(1-D)}$	$\frac{(2+D)}{(1-D)}$	$\frac{(2-D)}{(2-2D)}$	$\frac{(1+D)}{(1-D)}$	$\frac{1}{(1-D)}$
$K^I = \frac{N_3 + N_1}{N_3 - N_2}$							

$$\begin{aligned}
 B_1 = B_2 &= \begin{bmatrix} \frac{r_{C1}}{L_1} & 0 & \frac{-1}{C_1} & 0 \\ \frac{1}{L_1} & \frac{1}{L_2} & 0 & 0 \end{bmatrix}^T, \\
 E_1 = E_2 &= \begin{bmatrix} r_{C1} & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \end{bmatrix}, \\
 F_1 = F_2 &= \begin{bmatrix} -r_{C1} & 0 \\ 0 & 0 \end{bmatrix}
 \end{aligned} \tag{A2}$$

$$(\Delta_k)_B = E(sI - A)^{-1}\Psi_k + \Gamma_k \tag{A3}$$

$$(\Lambda_k)_B = E(sI - A)^{-1}B \tag{A4}$$

where, $A = (A_1D_1 + A_2D_2)$, $\Psi = (A_1 - A_2)X_{ss} + (B_1 - B_2)U$, $\Gamma = (E_1 - E_2)X_{ss} + (F_1 - F_2)U$, $B = (B_1D_1 + B_2D_2)$, $X_{ss} = -(A_1D_1 + A_2D_2)^{-1}(B_1D_1 + B_2D_2)U$, X_{ss} and U are the steady-state values of state variables and input, respectively while $R_p = r_{L1} + r_{L2} + r_{C1} + r_{C2}$.

B. CONTROLLABILITY AND OBSERVABILITY MATRIX

$$C = [C_1 \ C_2 \ C_3 \ C_4] \tag{A5}$$

where

$$\begin{aligned}
 C_1 &= \begin{bmatrix} -0.0775 \\ 0.1177 \\ -0.1875 \\ 0.2206 \end{bmatrix} \times 10^{15} & C_2 &= \begin{bmatrix} -0.4704 \\ 0.8257 \\ -0.1028 \\ 0.4693 \end{bmatrix} \times 10^{26} \\
 C_3 &= \begin{bmatrix} -0.128 \\ 0.3217 \\ -0.019 \\ 0.0166 \end{bmatrix} \times 10^{38} & C_4 &= \begin{bmatrix} -0.1839 \\ 0.8498 \\ 0.1285 \\ -0.5719 \end{bmatrix} \times 10^{49} \\
 O_1^1 &= \begin{bmatrix} E_{11} \\ E_{11}A_1 \\ E_{11}A_1^{N-1} \end{bmatrix} & O_2^2 &= \begin{bmatrix} E_{21} \\ E_{21}A_2 \\ E_{21}A_2^{N-1} \end{bmatrix}
 \end{aligned} \tag{A6}$$

The unobservable subspace of the system is defined as given by (16).

$$O_1^2 = O_1^1 \cap (e^{-A_1D_1T_s} O_2^2) \tag{A7}$$

$$\begin{aligned}
 O_1^1 &= \begin{bmatrix} 0.2 & 0 & 1 & 0 \\ 1.92e^3 & -0.07e^3 & -0.75e^3 & -0.75e^3 \\ -1.26e^7 & -0.056e^7 & -0.725e^7 & 0.725e^7 \\ -1.01e^{10} & 0.597e^{10} & 4.77e^{10} & -4.77e^{10} \end{bmatrix}, \\
 O_2^2 &= \begin{bmatrix} -1.021 & 0.7768 & 2.2913 & 0.4168 \\ -1.041 & 0.7921 & 2.336 & 0.425 \\ -1.041 & 0.7921 & 2.336 & 0.425 \\ -1.041 & 0.7921 & 2.336 & 0.425 \end{bmatrix} \times 10^{10}, \\
 O_1^2 &= \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}
 \end{aligned} \tag{A8}$$

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