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Fault Tolerant Control of Five-Level Inverter Based on Redundancy Space Vector Optimization and Topology Reconfiguration

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ABSTRACT Compared with two-level and three-level inverters, five-level inverters have more redundant space vectors to implement flexible control strategy. A fault tolerance method for open circuit fault of power tube in Neutral Point Clamped (NPC) five level inverter is proposed. The open circuit fault of inverter is divided into type I and type II in this paper. Redundant space vector optimization and topological reconfiguration fault tolerance strategies are used for type I and type II failures, respectively. The basic vector of the synthetic reference vector U_{ref} is reoptimize according to the redundant vector, and get a new control strategy after the decision. This method enables the inverter to achieve fault-tolerant operation without modifying hardware or adding bridge arms. The output performance of the inverter after fault is guaranteed and the cost of fault tolerance is greatly reduced. The feasibility and effectiveness of the proposed fault-tolerant method are verified through experiments.

INDEX TERMS Five level inverter, fault tolerance, redundancy space vector optimization, topology reconfiguration.

I. INTRODUCTION

The reliability of the inverter is one of the important factors for the stable operation of the photovoltaic system [1]. Multi-level converter has the advantages of less harmonic content of output voltage, lower switching loss, and lower stress, and it is considered to be the best choice for medium-high voltage and high power occasions [2]. One of the viable topologies is the 24-switch five-level NPC inverter [3]. However, the multi-level inverter will increase the possibility of fault due to the increase of power switching devices, which will reduce the reliability of the system. It will bring huge economic losses or catastrophic accidents once the multi-level inverter fails [4]. Therefore, it is of great significance to improve the reliability of multilevel inverter systems.

One of the important methods to improve system reliability is fault-tolerant technology. The premise of fault tolerance is fault diagnosis. The fault diagnosis method of the inverter has been extensively studied [5]–[7]. At present, fault-tolerant technologies for inverter failure are mainly divided into software level solutions without additional hardware and hardware solutions [8]. On the fault tolerance method of the software level. The fault tolerance of ANPC inverter can be realized through a simple change in the reference waveform [9]. The fault-tolerant method based on redundant space vector strategy is applied to NPC inverter power transistor short-circuit fault [10]. When the software level fault tolerance strategy can not meet the requirements of the system, topology reconfiguration technology is adopted [28]. The fault types of inverter are divided into two categories in [11]. Different fault tolerance strategies are adopted for different fault types.

Hardware-level fault-tolerant scheme is a kind of inverter fault-tolerant technology that has been studied more. This scheme can add switching devices [12], bridge arms [13], the entire system [14] or auxiliary module [28]. A five-level inverter topology consisting of two-level and single-phase five-level inverters was proposed in [12]. The inverter topology can realize fault-tolerant control of partial faults by changing the switch combination. The four-switch

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three-phase inverter (FSTPI) and eight-switch three-phase inverter (ESTPI) fault reconfiguration topology are given in [15]–[18] respectively. It makes the fault phase of the inverter to output "O" level forcibly.The DC voltage utilization rate of FSTPI and ESTPI is half of the inverter. The method of adding extra bridge arm was widely used in fault tolerance of inverter [19]–[21]. The essence of the method is to use the fourth bridge arm to replace the faulty bridge arm, but it increases the cost of the system undoubtedly. [22] gives a back-to-back six-bridge arm fault-tolerant converter topology circuit. When the fault is detected, the converter is reconstructed to make the converter work in the five-bridge arm model. The full-bridge fault-tolerant inverter topology is adopted in [23]–[25], but this topology can only achieve single-phase current excitation during open circuit faults, which has certain limitations.

According to the advantages and disadvantages of software level and hardware level fault-tolerant methods, a fault-tolerant method based on redundancy space vector optimization and topology reconstruction strategy is proposed. The fault tolerance of the inverter is improved by adding a few switching devices.

The inverter can be divided into cascaded H-bridge, NPC inverter and flying capacitor [26]. The faults of the inverter are mostly open circuit and short circuit faults of the power switch tube. Normally, the short circuit fault will be turned into an open circuit fault by the hardware protection circuit [27].The possibility of a single-tube failure of the inverter is greater than that of multiple simultaneous failures. The main object of this paper is the single-tube open-circuit fault tolerant control of NPC five level inverter. The structure of the article is as follows:

Sectiont II introduces the working principle of the NPC five-level inverter, and the failure analysis was given in Section III. The sectiont IV and sectiont V introduce the inverter fault-tolerant strategy based on redundant vector and topology reconfiguration respectively. The effectiveness is validated by the experimental results in Section VI. Finally, the conclusions are given in Part VII.

II. WORKING PRINCIPLE AND FAULT ANALYSIS OF FIVE-LEVEL INVERTER

The topology of a A-phase NPC five-level inverter is shown in Fig. 1. The topological structure includes a DC voltage source U_{dc} and four capacitors $C_1 \sim C_4$. And there are eight power switch tubes $S_{x1} \sim S_{x8}$, eight freewheeling diodes $D_{x1} \sim D_{x8}$ and twelve clamp diodes in each phase, where x = a,b,c. Four power switch tubes are in the on state at the same time only, and the remaining four are in the off state. Define the direction in which the load current flows from the inverter into the load as a positive direction, and define S_a, S_b, and S_c as the switching status of each phase.

1) When S_{a1}, S_{a2}, S_{a3}, S_{a4} are turned on: As shown in Fig. 2 (a), if $i_a > 0$, the current ia flows from point P_2 through S_{a1}, S_{a2}, S_{a3}, S_{a4} to the load; when $i_a < 0$, the current i_a flows into point P_2 via D_{a4}, D_{a3}, D_{a2}, D_{a1}. At this time, the output voltage $u_{ao} = U_{dc}/2$, and the switching state $S_a = 2$.
2) When S_{a2}, S_{a3}, S_{a4}, S_{a5} are turned on: As shown in Fig. 2 (b), if $i_a > 0$, the current i_a flows into the load from P_1 through S_{a2}, S_{a3}, S_{a4}; when $i_a < 0$, the current i_a flows into P_1 through S_{a5} and clamping diode. And the output voltage $u_{ao} = U_{dc}/4$, and the switching state $S_a = 1$.
3) When S_{a3}, S_{a4}, S_{a5}, S_{a6} are turned on: As shown in Fig. 2 (c), if $i_a > 0$, the current i_a flows into the load from point O through S_{a3} and S_{a4}; when $i_a < 0$, the current ia flows into point O through S_{a5} and S_{a6}. The output voltage $u_{ao} = 0$, and the switching state $S_a = 0$.
4) When S_{a4}, S_{a5}, S_{a6}, S_{a7} are turned on: As shown in Fig. 2 (d), if $i_a > 0$, the current i_a flows into the load from point N_1 through S_{a4}; when $i_a < 0$, the current i_a flows into point N_1 through S_{a5}, S_{a6}, S_{a7}. And the output voltage $u_{ao} = -U_{dc}/4$, and the switching state $S_a = -1$.
5) When S_{a5}, S_{a6}, S_{a7}, S_{a8} are turned on: As shown in Fig. 2 (e), if $i_a > 0$, the current i_a flows from N_2 through D_{a8}, D_{a7}, D_{a6}, D_{a5}; when $i_a < 0$, the current ia flows into N_2 through S_{a5}, S_{a6}, S_{a7}, S_{a8}. At this time, the output voltage $u_{ao} = -U_{dc}/2$, and the switching state $S_a = -2$.

The relationship between the inverter's switching state and output voltage is shown in Table 1.

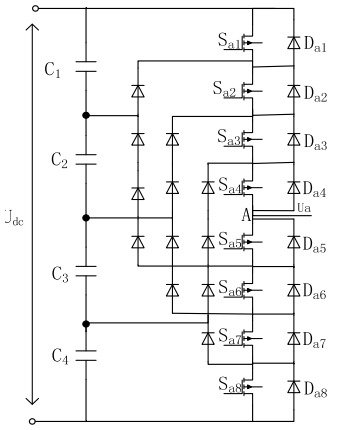

FIGURE 1. Topological structure of A-phase NPC five-level inverter.

TABLE 1. Relationship between switch state and inverter output voltage.

S_a	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	The output voltage
2	1	1	1	1	0	0	0	0	$U_{dc}/2$
1	*0*	1	1	1	1	0	0	0	$U_{dc}/4$
0	*0*	0	1	1	1	1	0	0	0
-1	*0*	0	0	1	1	1	1	0	$-U_{dc}/4$
-2	0	0	0	0	1	1	1	1	$-U_{dc}/2$

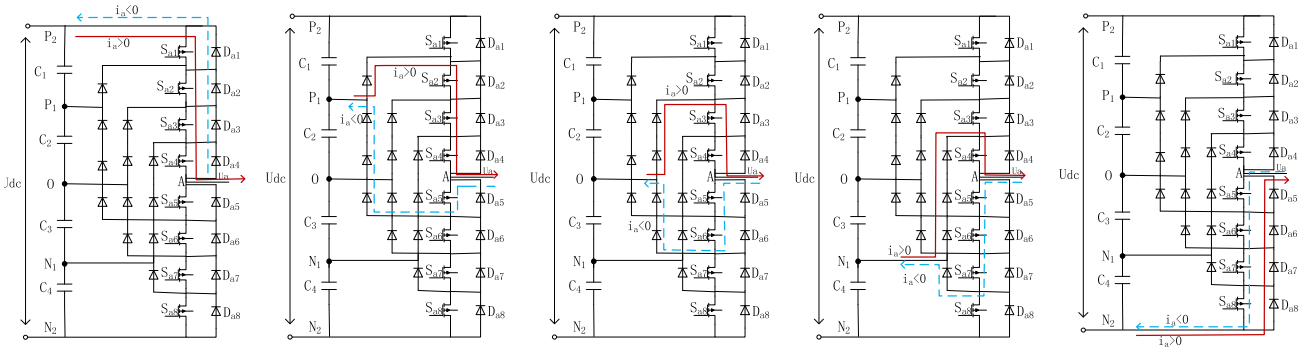

FIGURE 2. The working principle of the A-phase bridge arm of the five-level inver.

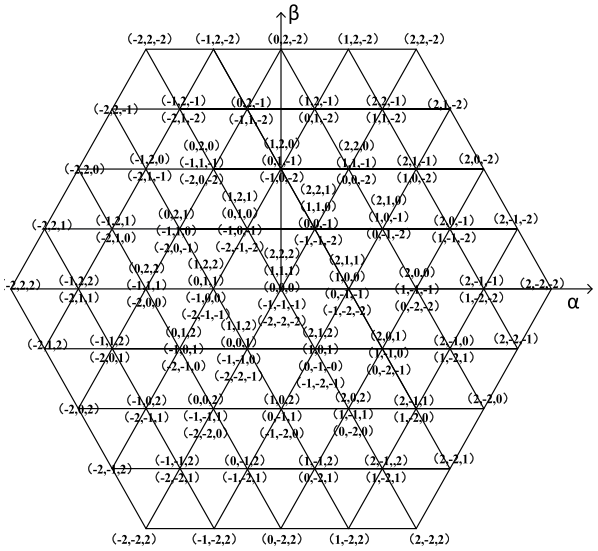

FIGURE 3. Space vector diagram of NPC five-level inverter.

Five kinds of output voltages $U_{dc}/2$, $U_{dc}/4$, 0, $-U_{dc}/4$, $-U_{dc}/2$ can be obtained for each phase of the five level inverter, which are represented by "2", "1", "0", "1" and "2" respectively. The three-phase five-level inverter can obtain $5^3 = 125$ voltage state combinations.

From table 1, it can be concluded that:

$$U_x = S_x U_{dc}/\mathbf{4} \quad x = a, b, c \tag{1}$$

The synthesizing vectors U_{out} can be expressed as follows:

$$U_{out} = \frac{\mathbf{1}}{\mathbf{6}} U_{dc}(S_a + S_b e^{j\frac{2}{3}\pi} + S_c e^{-j\frac{2}{3}\pi}) \tag{2}$$

The space vector distribution of five level inverter is shown in Fig. 3.

III. OPEN CIRCUIT FAILURE ANALYSIS

This article only analyzes the open-circuit faults of S_{a1}, S_{a2}, S_{a3}, and S_{a4} due to the symmetry of the five-level inverter.

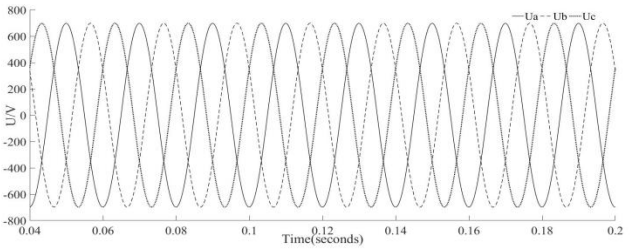

FIGURE 4. Three-phase output voltage of NPC five-level inverter under normal operation.

A. NORMAL SITUATION

The inverter can obtain all the space voltage vectors in Fig. 3 through the SVPWM control strategy when it works normally. And the output voltage of the inverter is shown in Fig. 4.

B. OPEN CIRCUIT FAILURE OF S_{a1}

When S_{a1} has an open circuit fault, the working state in Fig. 2 (a) is invalid, which making the A-phase unable to obtain the state "2". Therefore, the inverter will lose all space vectors of A-phase containing the level state "2". The output voltage and space vector distribution of the three-phase inverter during S_{a1} open circuit fault are shown in Fig. 5 (a) and (b) respectively.

Among them, valid vectors are in the red area, and invalid vectors are crossed out. The following is similar.

C. OPEN CIRCUIT FAILURE OF S_{a2}

When S_{a2} is open-circuited, the working states (a) and (b) in Fig. 2 are invalid, and the level states "2" and "1" are lost in A-phase. Therefore, the inverter loses the space vector of A-phase including "2" and "1". Fig. 6 (a) and (b) show the distribution of the output voltage and space vector of the three-phase inverter after the open circuit fault of S_{a2}.

D. OPEN CIRCUIT FAILURE OF S_{a3}

When S_{a3} has an open circuit fault, the working states (a), (b), and (c) in Fig. 2 cannot be achieved, and A-phase loses the level states "2", "1", and "0". Then, the space

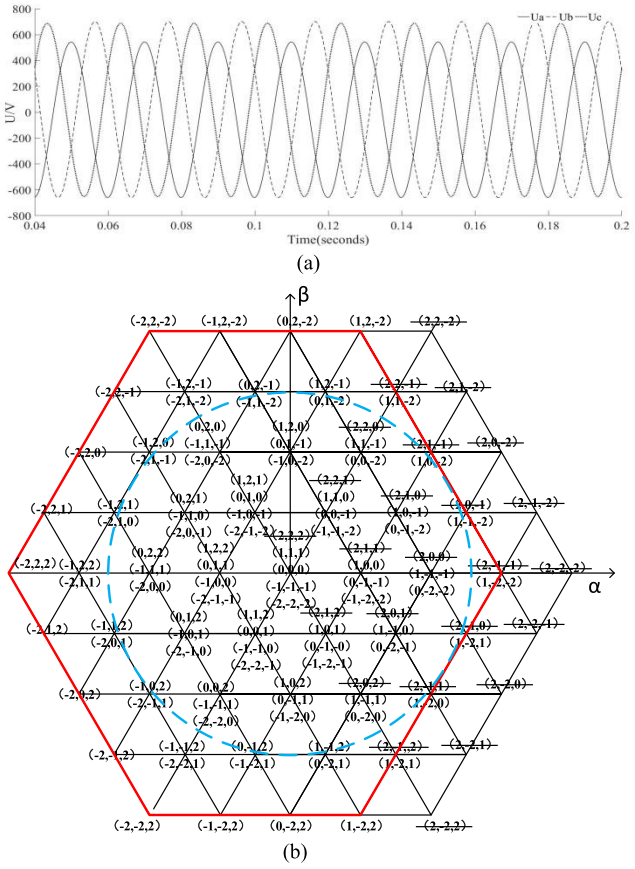

FIGURE 5. S_{a1} open circuit failure (a) The three-phase output voltage of inverter. (b)Space vector distribution.

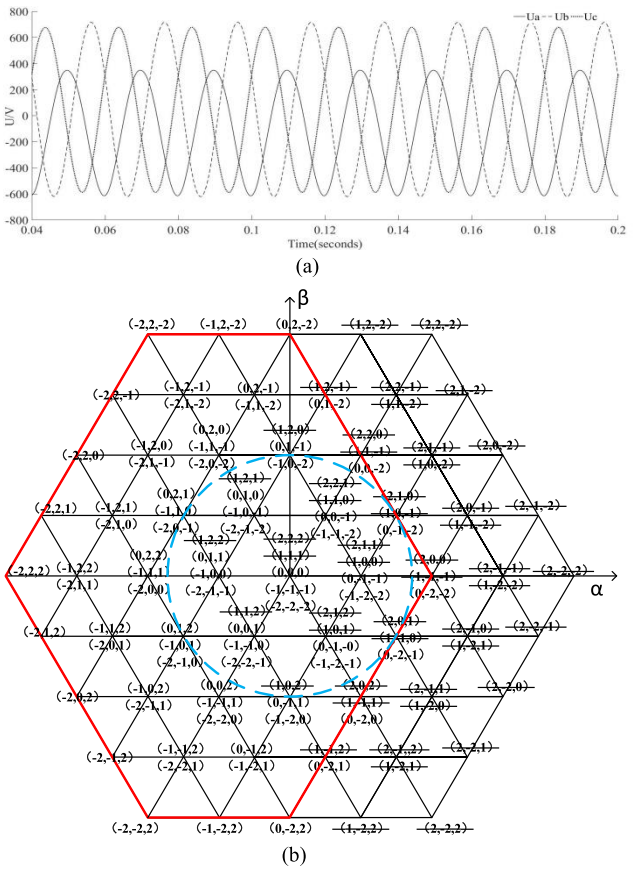

FIGURE 6. S_{a2} open circuit failure (a) The three-phase output voltage of inverter. (b)Space vector distribution.

vectors of A-phase including "2", "1", and "0" are lost. Fig. 7 (a) and (b) show the output voltage and space vector distribution of the three-phase inverter after S_{a3} has an open circuit fault.

E. OPEN CIRCUIT FAILURE OF S_{a4}

When an open circuit fault occurs in S_{a4}, the working states of (a), (b), (c), and (d) in Fig. 2 fail, A-phase loses level states "2", "1", "0", and "−1". Therefore, the space vectors of A-phase including "2", "1", "0", and "−1" are all lost. Fig. 8 (a) and (b) show the of the output voltage and space vector distribution of the three-phase inverter after the open circuit fault of S_{a4}.

When S_{a1}, S_{a2}, S_{a3} has open-circuit failure, the basic vectors used to synthesize the reference vectors can be re-optimized using the redundant space vector strategy, and obtain a circular undistorted rotation vector with the origin as the center by adjusted the SVPWM modulation strategy. But the output voltage amplitude needs to be reduced to ensure the fault-tolerant operation of the inverter. When an open circuit fault occurs in S_{a4}, the space vector distribution is shown in Fig. 8 (b), and all voltage space vectors on the right side of the β axis in the α-β plane are lost. Therefore, an undistorted circular rotating voltage vector cannot be generated. In response to this situation, the topology of the inverter can be reconfigured, and fault-tolerant control can be achieved by changing the topology of the inverter.

TABLE 2. Fault classification.

Faulty device	Lost level status	Fault tolerance	Fault type
S_{a1}	2	√	
S_{a2}	*2*、*1*	√	Type I
S_{a3}	*2*、*1*、*0*	√	
S_{a4}	*2*、*1*、*0*、*-1*	×	Type II

So, it's divided into two types, which are defined as type I fault and type II fault, as shown in Table 2.

IV. FAULT TOLERANCE BASED ON REDUNDANCY SPACE VECTOR

After the type I fault occurs, the redundancy space vector strategy can ensure the inverter derating and stable operation. The derated operation degree of the inverter is different when an open circuit fault occurs in different power tubes.

The fault-tolerant control of open-circuit faults in S_{a1}, S_{a2}, and S_{a3} will be analyzed respectively in this section.

A. OPEN CIRCUIT FAILURE OF S_{a1}

In the SVPWM modulation mode, the maximum undistorted circular rotating voltage vector that the inverter can output

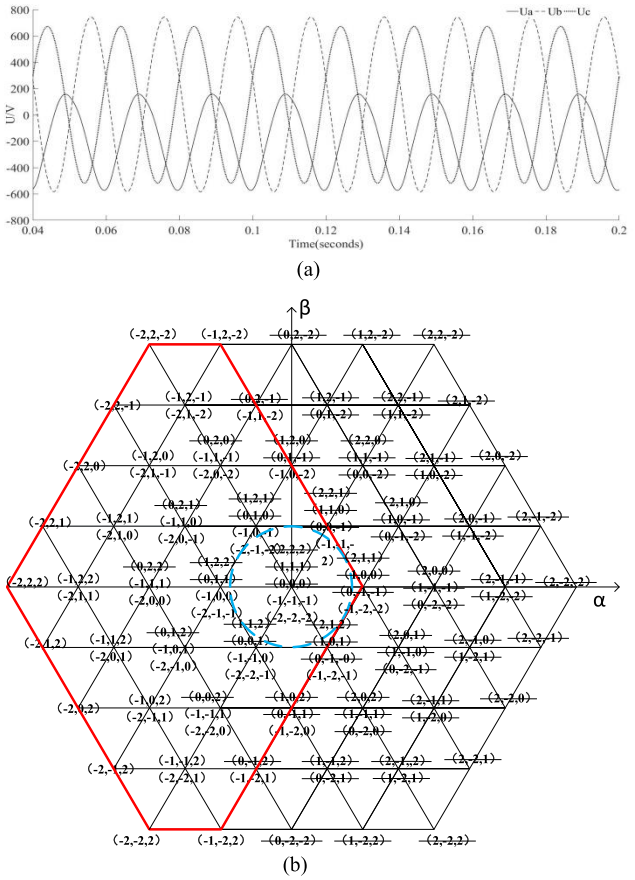

FIGURE 7. S_{a3} open circuit failure (a) The three-phase output voltage of inverter. (b) Space vector distribution.

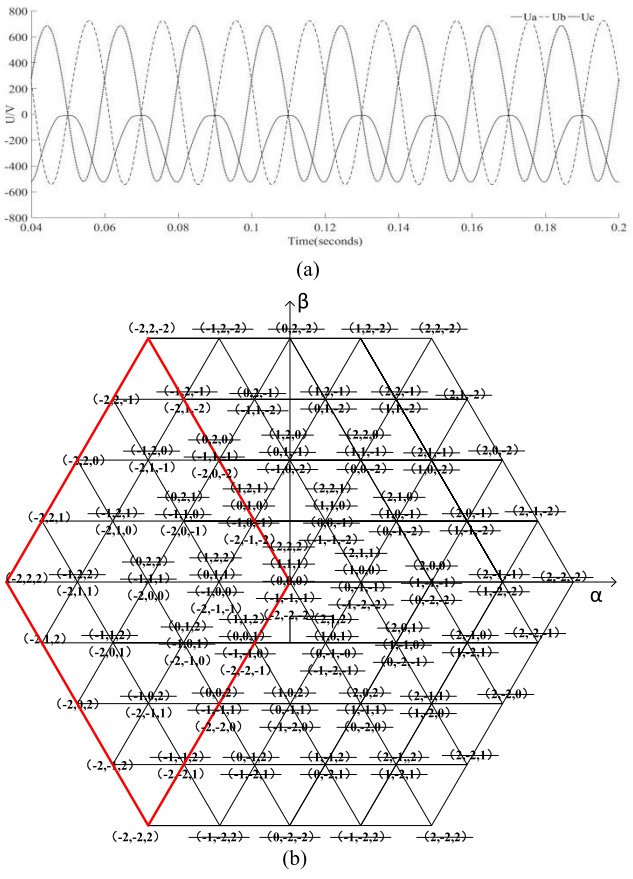

FIGURE 8. S_{a4} open circuit failure (a) The three-phase output voltage of inverter. (b) Space vector distribution.

during normal operation is the inscribed circle of the largest regular hexagon in Fig. 3, and its amplitude is $(\sqrt{3}/2) \times (2U_{dc}/3) = U_{dc}/\sqrt{3}$. It means that the maximum phase voltage amplitude of the five level inverter is $U_{dc}/\sqrt{3}$. When the open circuit of S_{a1} fails, the five-level inverter can output the maximum undistorted circular rotating voltage vector as the circle in Fig. 5(b), and its amplitude is $\sqrt{3}U_{dc}/4$. Therefore, the inverter system need derating to make it run stably.

1) INTERVAL JUDGMENT

Since the space vector is equally divided into six sectors, the sector where it is located can be judged according to the angle θ of the reference vector U_{ref}. For example, when $0 \le \theta < 60°$, U_{ref} is in sector I; when $60 \le \theta < 120°$, U_{ref} is in sector II, and so on. Taking sector I as an example, there are 16 small sections, and a small triangle is a section. After S_{a1} has an open circuit fault, there are only nine effective sections in each large sector: (1) ∼ (9), as shown in Fig. 9.

Let $U_d = 2U_{dc}/3$, U_{dc} is the DC bus voltage. The purpose is to keep the reference voltage U_{ref} always in the effective space area, which avoids raising the DC bus voltage during the fault tolerance process.

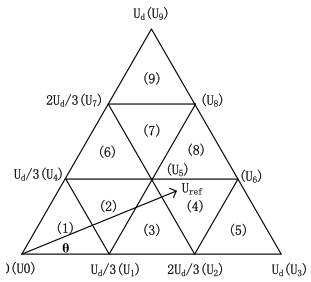

FIGURE 9. Sector I (S_{a1} open circuit fault).

2) SYNTHESIS OF REFERENCE VECTOR U_{REF}

According to the divided sections, three space vectors for synthesizing the reference vector U_{ref} are determined. In order to simplify the calculation, the 60° coordinate system (g_h coordinate system) is used to calculate the time of each vector synthesis. The reference vector U_{ref} is transformed into:

$$\begin{cases} V_g = V_\alpha - V_\beta/\sqrt{3} \\ V_h = 2V_\beta/\sqrt{3} \end{cases} \tag{3}$$

Take the reference vector U_{ref} falling in the section (7) of sector I as an example to calculate the action time of the correlation vector. According to the principle of volt-second

TABLE 3. The action time of the space vector of the sector I (S_{a1} open circuit fault).

I(1)	$T_1=3T_sV_g/U_d$	$T_4=3T_sV_h/U_d$	$T_0=T_s-T_1-T_4$
I(2)	$T_1=T_s(U_d-3V_h)/U_d$	$T_4=T_s(U_d-3V_g)/U_d$	$T_5=T_s-T_1-T_4$
I(3)	$T_1=T_s(2U_d-3V_h-3V_g)/U_d$	$T_2=T_s(3V_g-U_d)/U_d$	$T_5=T_s-T_1-T_2$
I(4)	$T_2=T_s(U_d-3V_h)/U_d$	$T_5=T_s(2U_d-3V_g)/U_d$	$T_6=T_s-T_2-T_5$
I(5)	$T_3=T_s(3V_g-2U_d)/U_d$	$T_6=3T_sV_h/U_d$	$T_2=T_s-T_3-T_6$
I(6)	$T_4=T_s(2U_d-3V_h-3V_g)/U_d$	$T_7=T_s(3V_h-U_d)/U_d$	$T_5=T_s-T_4-T_7$
I(7)	$T_8=T_s(3V_g+3V_g-2U_d)/U_d$	$T_7=T_s(U_d-3V_g)/U_d$	$T_6=T_s-T_7-T_8$
I(8)	$T_8=T_s(3V_h-U_d)/U_d$	$T_6=T_s(3V_g-U_d)/U_d$	$T_5=T_s-T_6-T_8$
I(9)	$T_9=T_s(3V_h-2U_d)/U_d$	$T_8=3T_sV_g/U_d$	$T_7=T_s-T_8-T_9$

balance, the equation is established in the g_h coordinate system using the parallelogram rule:

$$\begin{cases} T_sV_g = U_dT_5/3 + U_dT_8/3 \\ T_sV_h = U_dT_5/3 + 2U_dT_7/3 + 2U_dT_8/3 \\ T_s = T_5 + T_7 + T_8 \end{cases} \tag{4}$$

Solution:

$$\begin{cases} T_7 = T_s(U_d - 3V_g)/U_d \\ T_8 = T_s(3V_h + 3V_g - 2U_d)/U_d \\ T_6 = T_s - T_7 - T_8 \end{cases} \tag{5}$$

Similarly, the correlation vector synthesis time between other sections in sector I can be calculated, as shown in Table 3.

3) DETERMINE THE SWITCHING SEQUENCE

In the process of space voltage vector modulation, the principle of reducing the number of switching of the switching device should be followed, and it is ensured that only the switching state of one phase is changed when the space vector is switched. The seven-segment vector synthesis method is adopted when the inverter works normally. For example, in the section (5) of sector I, the vector sequence is (2,0,-1)-(2,-1,-1)-(1,-1,-1)-(1,-1,-2)-(1,-1,-1)-(2,-1,-1)-(2,0,-1). After the open circuit fault of S_{a1}, all the space vectors starting with "2" are lost, the way of vector synthesis mode should be changed. The seven-segment vector synthesis method can be used because of the existence of redundant vectors. Table 4 shows the switching sequence among the nine sections in sector I.

After the vector action sequence is determined, the pulse distribution method is similar to the normal operation of the five-level inverter, so it will not be described here.

B. OPEN CIRCUIT FAILURE OF S_{a2}

When an open circuit fault occurs in S_{a2}, all the space vectors containing "1" and "2" in A-Phase are lost. At this time, the five-level inverter can output the maximum undistorted circular rotating voltage vector as the circle in Fig. 6 (b), and its amplitude is $U_{dc}/2\sqrt{3}$. According to the above analysis

TABLE 4. Vector acting order of sector I. (S_{a1} open circuit fault).

Section	Vector action sequence
I(1)	(1,1,0)-(1,0,0)-(0,0,0)-(0,0,-1)-(0,0,0)-(1,0,0)-(1,1,0)
I(2)	(1,1,0)-(1,0,0)-(1,0,-1)-(0,0,-1)-(1,0,-1)-(1,0,0)-(1,1,0)
I(3)	(1,0,0)-(1,0,-1)-(1,-1,-1)-(0,-1,-1)-(1,-1,-1)-(1,0,-1)-(1,0,0)
I(4)	(1,0,-1)-(1,-1,-1)-(1,-1,-2)-(0,-1,-2)-(1,-1,-2)-(1,-1,-1)-(1,0,-1)
I(5)	(1,-1,-1)-(1,-1,-2)-(1,-2,-2)-(0,-2,-2)-(1,-2,-2)-(1,-1,-2)-(1,-1,-1)
I(6)	(1,1,0)-(1,1,-1)-(1,0,-1)-(0,0,-1)-(1,0,-1)-(1,1,-1)-(1,1,0)
I(7)	(1,1,-1)-(1,0,-1)-(1,0,-2)-(0,0,-2)-(1,0,-2)-(1,0,-1)-(1,1,-1)
I(8)	(1,0,-1)-(1,0,-2)-(1,-1,-2)-(0,-1,-2)-(1,-1,-2)-(1,0,-2)-(1,0,-1)
I(9)	(1,1,-1)-(1,1,-2)-(1,0,-2)-(0,0,-2)-(1,0,-2)-(1,1,-2)-(1,1,-1)

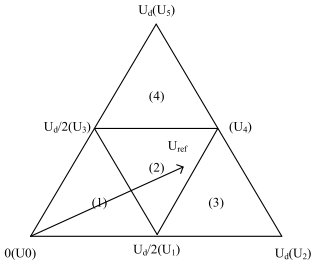

FIGURE 10. Sector I (S_{a2} open circuit fault).

TABLE 5. The action time of the space vector of the sector I (S_{a2} open circuit fault).

I(1)	$T_1=2T_sV_g/U_d$	$T_3=2T_sV_h/U_d$	$T_0=T_s-T_1-T_3$
I(2)	$T_1=T_s(U_d-2V_h)/U_d$	$T_3=T_s(U_d-2V_g)/U_d$	$T_4=T_s-T_1-T_3$
I(3)	$T_1=T_s(2U_d-2V_h-2V_g)/U_d$	$T_2=T_s(2V_g-U_d)/U_d$	$T_4=T_s-T_1-T_2$
I(4)	$T_3=T_s(2U_d-2V_h-2V_g)/U_d$	$T_5=T_s(2V_h-U_d)/U_d$	$T_4=T_s-T_3-T_5$

TABLE 6. Vector action sequence of sector I (S_{a2} open circuit fault).

Section	Vector action sequence
I(1)	(0,0,-1)-(0,-1,-1)-(-1,-1,-1)-(-1,-1,-2)-(-1,-1,-1)-(0,-1,-1)-(0,0,-1)
I(2)	(0,0,-1)-(0,-1,-1)-(0,-1,-2)-(-1,-1,-2)-(0,-1,-2)-(0,-1,-1)-(0,0,-1)
I(3)	(0,-1,-1)-(0,-1,-2)-(0,-2,-2)-(-1,-2,-2)-(0,-2,-2)-(0,-1,-2)-(0,-1,-1)
I(4)	(0,0,-1)-(0,0,-2)-(0,-1,-2)-(-1,-1,-2)-(0,-1,-2)-(0,0,-2)-(0,0,-1)

method, the interval of the reference vector U_{ref} and the action time of each space vector of the synthesized reference vector can be determined, as shown in Fig. 10 and Table 5, respectively.

After the open circuit fault of S_{a2}, there are still some redundant vectors, even if most of the vectors on the right side of the β axis are lost, such as $(0, 0, -1)$ $(-1, -1, -2)$ and $(0, -1, -1)$ $(-1, -2, -2)$. Therefore, a seven-segment vector synthesis method can also be adopted, as shown in Table 6.

C. OPEN CIRCUIT FAILURE OF S_{a3}

When an open circuit fault occurs in S_{a3}, all space vectors beginning with "0", "1", and "2" are lost. The maximum undistorted circular rotating voltage vector after this fault

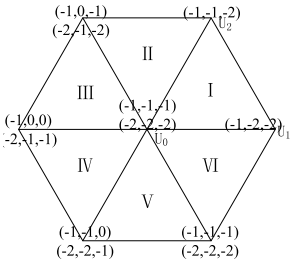

FIGURE 11. Vector distribution diagram (S_{a3} open circuit fault).

TABLE 7. Vector action sequence (S_{a3} open circuit fault).

I	(-1,-1,-1)-(-1,-1,-2)-(-1,-2,-2)-(-2,-2,-2)-(-1,-2,-2)-(-1,-1,-2)-(-1,-1,-1)
II	(-1,-1,-1)-(-1,-1,-2)-(-2,-1,-2)-(-2,-2,-2)-(-2,-1,-2)-(-1,-1,-2)-(-1,-1,-1)
III	(-1,-1,-1)-(-2,-1,-1)-(-2,-1,-2)-(-2,-2,-2)-(-2,-1,-2)-(-2,-1,-1)-(-1,-1,-1)
IV	(-1,-1,-1)-(-2,-1,-1)-(-2,-2,-1)-(-2,-2,-2)-(-2,-2,-1)-(-2,-1,-1)-(-1,-1,-1)
V	(-1,-1,-1)-(-1,-2,-1)-(-2,-2,-1)-(-2,-2,-2)-(-2,-2,-1)-(-1,-2,-1)-(-1,-1,-1)
VI	(-1,-1,-1)-(-1,-2,-1)-(-1,-2,-2)-(-2,-2,-2)-(-1,-2,-2)-(-1,-2,-1)-(-1,-1,-1)

occurs is 1/4 of the normal operation, and the amplitude is $U_{dc}/4\sqrt{3}$. The effective voltage vector distribution in the fault tolerance process is similar to that of the two-level inverter, as shown in Fig. 11.

The position of U_{ref} can be determined by the angle θ. Taking sector I as an example, the basic vector action time of the synthesized U_{ref} is:

$$\begin{cases} T_1 = T_s V_g / U_d \\ T_2 = T_s V_h / U_d \\ T_0 = T_s - T_1 - T_2 \end{cases} \tag{6}$$

After the S_{a3} fault, there are still two zero vectors, so a seven-segment vector synthesis method can be used, as shown in Table 7.

When a type I fault occurs, the inverter can output an undistorted circular rotating voltage vector because of the existence of redundant space vector. Therefore, the vector redundancy fault-tolerant strategy for type I faults will make the inverter get a stable output, but it needs to be derated.

V. FAULT TOLERANCE METHOD BASED ON TOPOLOGY RECONFIGRUATION

The space vector on the right side of the β axis are completely lost when the S_{a4} open circuit fault. Compared with the redundancy space vector strategy, the topology reconfigruation strategy is more suitable for type II failure. The topology of the A-phase five-level fault-tolerant inverter is shown in Fig. 12. The inverter can obtain reliable operating performance by connecting the faulty phase load directly to the DC bus midpoint.

A-Phase is forced to obtain the state ''O'' with the help of a bidirectional switch. The inverter can get $1*5^2 = 25$ groups of different space vectors, but only 19 of them

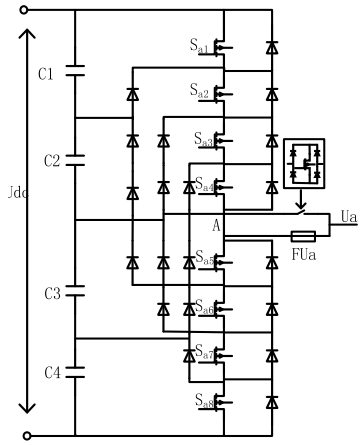

FIGURE 12. Topology of five-level A-phasefault-tolerant inverter.

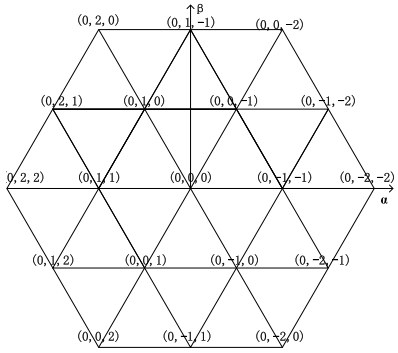

FIGURE 13. Vector distribution diagram of five-level fault-tolerant inverter.

TABLE 8. Five-segment vector action sequence (S_{a4} open circuit fault).

Section	Vector action sequence
I(1)	(0,0,0)-(0,0,-1)-(0,-1,-1)-(0,0,-1)-(0,0,0)
I(2)	(0,0,-1)-(0,-1,-1)-(0,-1,-2)-(0,-1,-1)-(0,0,-1)
I(3)	(0,-1,-1)-(0,-1,-2)-(0,-2,-2)-(0,-1,-2)-(0,-1,-1)
I(4)	(0,0,-1)-(0,0,-2)-(0,-1,-2)-(0,0,-2)-(0,0,-1)

are vaild. Fig. 13 shows the effective vector distribution after S_{a4} failure.

Fig. 13 is the same as the vector distribution diagram when S_{a2} fails, except for the space vectors. Therefore, the interval time of U_{ref} and the action time of the space vector are consistent with the analysis of S_{a2} failure. It is worth noting that the five-segment vector synthesis method is adopted because there is no redundant vector. Table 8 is the vector action sequence of sector I.

To compare the proposed fault-tolerant method with the techniques for the others inverters, Table 9 has been provided. Both software and hardware solutions have been included in this comparison.

According to Table 9, the software level solution does not need to add additional devices, but can only solve part of the fault. The hardware level method increases the fault tolerance cost, but the fault tolerance effect is better. The method

TABLE 9. Comparison of fault-tolerant methods.

Comparative features	Method			
	[9]	[20]	[28]	Proposed method
Number of DC voltage sources	1	1	6	1
Number of reserved switches	0	6	6	3
The fourth leg	No	Yes	No	No
Fault tolerant for all single tube failures	No	Yes	Yes	Yes
THD	3.34%	—	3.05%	0.15%

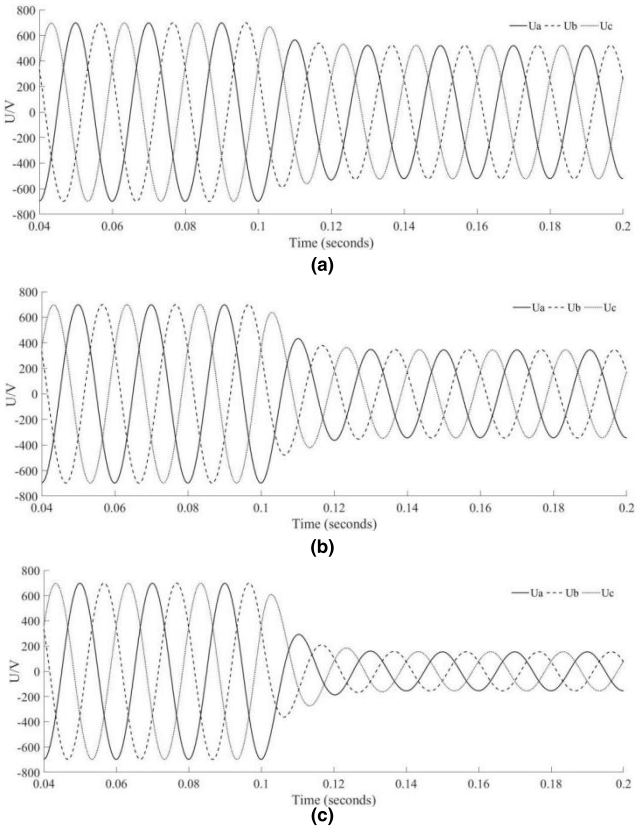

FIGURE 14. (a) S_{a1} open circuit fault output waveform after fault tolerance (b) S_{a2} open circuit fault output waveform after fault tolerance (c) S_{a3} open circuit fault output waveform after fault tolerance.

proposed in this paper realizes the single switch fault-tolerant control of inverter by adding few switches.

VI. EXPERIMENTAL RESULTS

A Matlab / Simulink simulation model of NPC five-level inverter was built to verify the inverter fault-tolerance method mentioned in this paper. Taking the open-circuit fault of the A-phase bridge arm power tube as an example, the fault-tolerant performance of the inverter after Type I fault and Type II fault is verified respectively. The main parameters of the simulation are set as follows: DC voltage = 1000V, reference voltage = 548.5V, load resistance = 20Ω and load inductance = 10mH. Uniformly set an open circuit fault to the inverter at 0.1 seconds.

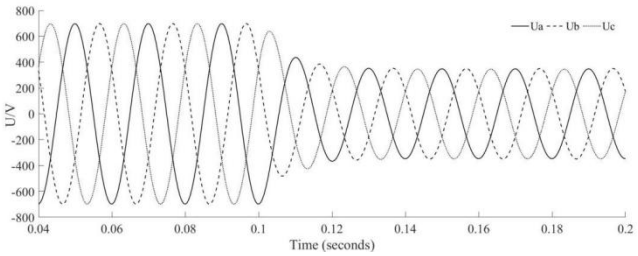

FIGURE 15. S_{a4} open circuit fault output waveform after fault tolerance.

TABLE 10. The THD of the inverter's output voltage waveform after fault tolerance.

Normal Situation(THD)	After fault tolerance (THD)			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
0.02%	0.04%	0.10%	0.21%	0.15%

Take the switching devices S_{a1}, S_{a2} and S_{a3} as examples to verify the operating characteristics of the fault-tolerant inverter after Type I fault. The phase voltage waveform of three-phase load after type I fault tolerance is shown in Fig. 14. Although the amplitude of the three-phase voltage output by the inverter has decreased after fault tolerance, the three phases are still balanced, which can ensure stable and continuous operation of the system.

Take the switching device S_{a4} as an example to verify the operating characteristics of the fault-tolerant inverter after type II fault. The output waveforms of the three-phase voltage of the inverter before and after the S_{a4} fault are shown in Fig. 15. Although the amplitude of the output waveform has decreased after the fault tolerance, the waveform still maintains a good sine degree and can maintain the stable operation of the system.

The total harmonic distortion (THD) of the inverter's output voltage waveform after fault tolerance are shown in Table 10.

From the above analysis, the topology reconfiguration strategy can be used to tolerate the S_{a3} open circuit fault to obtain better output performance.

VII. CONCLUSION

A fault tolerance method has been proposed, which based on redundancy space vector optimization and topology reconfiguration under single-tube open circuit fault for NPC five-level inverter. The fault types of NPC five-level inverter are divided into type I and type II according to the voltage space vector distribution after the fault occurs. The strategy of redundancy space vector optimization was adopted to Type I. The basic vector of the synthetic reference vector U_{ref} is re-optimize according to the redundancy vector, and get a new SVPWM control strategy to the failure circuit. The maximum output voltage of inverter would be reduced to 3/4 of the ordinary voltage of inverter. Once a type II fault occurs, the fault phase is forced to output the level state "O" with the help of a fuse

and a bidirectional switch, and the magnitude of the output voltage is reduced to half of the ordinary voltage. By contrast most of fault tolerance methods of multi-level inverter, it is no need to add redundant bridge arms by the method of this paper proposed.

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