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Design of Double-Gate Tri-Active Layer Channel Based IGZO Thin-Film Transistor for Improved Performance of Ultra-Low-Power RFID Rectifier

SHASHI K. DARGAR, (Senior Member, IEEE), AND VIRANJAY M. SRIVASTAVA, (Senior Member, IEEE)
Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban 4041, South Africa
Corresponding author: Shashi K. Dargar (drshashikant.dargar@ieee.org)

ABSTRACT In a Radio Frequency Identification (RFID) circuit, the rectifier plays a vital role since it converts the received RF energy from a distant transmitter (reader) to power the entire RF circuit of the passive tag. The thin-film transistors have the potential to affect the rectifier circuit performance using the channel structural modification in the device to accomplish better gate-control for low-power operations. In this paper, the authors have presented a novel design of a double-gate amorphous In-Ga-Zn-O (IGZO) based thin-film transistor with a tri-active layer channel structure. Further, the experimental characterization of the device has been implemented using the SPICE model to analyze the device performance in the rectifier circuits. The simulation reports the competitive results with an improved rectifier performance using the proposed structure. The performance of ultra-low-power rectifier topologies has been compared with the conventional rectifier circuit. Among others, the differential rectifier circuit arrangement has a high power conversion efficiency of *20.06%* for low input *0.45* V−*0.61* V, whereas Self-V_{TH}-Cancellation (SVC) configuration optimum power consumption is 0.14 μW. The promising results suggest the device deployment in the passive RFID tags and implantable devices in ultra-low-power integrated circuits.

INDEX TERMS Amorphous IGZO, active layer channel, RFID, thin-film transistors, VLSI.

I. INTRODUCTION

In recent times, Radio Frequency Identification (RFID) systems are increasing much progressively due to the technological advancements in device designs. The RFIDs are a driving technology that utilizes a communication interface between RFID identifiers (tags) and a reader. The modern systems such as product in-out management, library book management, supply-chain management, and other analogous industries are using RFIDs for item-level tracking and monitoring in several applications areas such as transport, hospitals, commerce, airlines, and cloth-trading and many more [1]. Despite being the fact that the RFIDs have great potential in a variety of upcoming applications, though a limitation of the high manufacturing cost is associated with the RFID tags. Alternatively, non-silicon materials such as an oxide or organic material in Thin-Film Transistors (TFTs) has drawn significant attention in the last decade for the production of low-cost, flexible, transparent RFID tags [2]–[4]. The RFID tags using organic thin-film transistors have been capable of realizing wireless operations up to a few kHz. However, attaining a satisfactory operational speed and maintaining low-power consumption in the organic-TFTs remained challenging thus far. In contrast, the oxide-TFTs have been quite promising for making transparent RFID tags and appeared as a prominent application other than the active matrix displays [5]. Primarily, due to the advantages such as ease of fabrication processing, good transparency, high mobility, and low leakage current, the amorphous In-Ga-Zn-O (α-IGZO) material was preferred over the other oxide-TFTs and well-recognized for the transparent RFIDs [6]–[8]. In particular, since the RFID tag operates quite distant from the reader, the received RF signal is attenuated due to travel distance, and often a very low voltage is induced across the tag antenna [9], [10]. Therefore, the rectifier, as a subsequent circuit in the passive RFID tag, should have a small turn-on voltage. The conventional circuit based on the Schottky diode stands incompatible owing to the limitation of fabrication technology and processing costs [11].

In this paper, the authors have proposed a Double-Gate (DG) amorphous IGZO thin-film transistor that contains a Tri-Active Layer (TAL) channel structure obtained from

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the experimental characterization of multi-stack layers and implemented using LEVEL3 SPICE to analyze the performance in various RFID rectifier circuits at the operating frequency of 13.56-MHz. The paper is organized as follows: Section II details the device model and foundation of layer structure for our design. The detail of the simulation and characteristics of the DG-TAL IGZO TFT are described in Section III. Section IV presents the circuit implementation derived from the device characteristics and the results of the rectifier circuit simulation for the comparison of performance. Finally, conclusions drawn from the obtained results are presented in Section V.

II. DEVICE MODEL AND STRUCTURE DESIGN

The electrical behavior of an amorphous IGZO-TFT is substantially affected by the amount of Indium (*In*) and Gallium (*Ga*) present in the channel layer. Also, the density of states (DOS), which signifies the number of states neighboring to some specific energy level, is usually the governing parameters for determining the device performance [12]. In an α-IGZO structure, g_{ta}, g_{td}, and g_{gd} are the acceptor-like conduction band-tail, the donor-like valence band-tail, and the donor shallow-gap states, respectively, affect the device behavior. Precisely, the metal cation s-bands disorder is the reason for g_{ta} that causes the 5s orbitals of the Indium (*In*) in its Conduction Band Minimum (CBM). Consequently, increasing the *In* content leads to an increase of the g_{ta} as well. Furthermore, both the g_{td} and g_{gd} parameters have a profound effect on the existing Oxygen Vacancy (OV). The effective carrier concentration of fixed material can be determined from the Fermi-Dirac statistics.

As the subgap DOS of α-IGZO are well defined using exponent distribution of band-tail (g_{ta}, g_{td}), and Gaussian-distributed OV states (g_{ga}, g_{gd}), it implies that the acceptor-like states are modeled from the linear superposition of g_{ta} and g_{ga} [13], [14], which can be given as:

$$g_A(\mathrm{E}) = n_{ta} \times \exp\left[\frac{E - E_C}{w_{ta}}\right] + n_{ga} \times \exp\left[-\left(\frac{E_{ga} - E}{w_{ga}}\right)^2\right] \quad (1)$$

where n_{ta}, E, E_c, and w_{ta} are the edge intercept density, state energy, edge energy, and characteristic slope (decay energy) of the conduction band, respectively, and n_{ga}, E_{ga} & w_{ga} are the total DOS, the peak energy, and the standard deviation of states, respectively. Similarly, the donor-like Gaussian function can be described by the equation as given in (2).

$$g_{gd}(\mathrm{E}) = n_{gd} \times \exp\left[-\left(\frac{E - E_{gd}}{w_{gd}}\right)^2\right] \quad (2)$$

where n_{gd} is the total DOS, E_{gd} is the peak energy, and w_{gd} is the characteristic decay energy of the valence band. Furthermore, in *a*-IGZO drift carrier mobility, μ_d depends largely on charge mobile carrier density Q_{CB} [15].

However, it is hard to determine the drift mobility as the Q_{CB} diminishes due to the gate-induced total charge density and the subgap traps, Qs. Instead, Qs can be merely calculated using $[\mathrm{Q}, (V_G - V_x)] \approx C_G(V_G - V_T - V_x)$, where C_G, V_x, and V_T are the gate capacitance per unit area, the potential in the channel at a distance x from the source, and the potential difference between the gate and the channel, respectively. Henceforth, renormalizing the subgap traps in the mobility term in the bias-dependent field-effect mobility, $\mu_{FE}(V_G)$, can be written as:

$$\mu_{FE}(V_G) = \frac{\mu_d[Q, (V_G - V_x)]}{Q_{CB}(V_G - V_T)} \quad (3)$$

and,

$$Q_{CB} = C_G k_\mu (V_G - V_T)^{1+\beta} \quad (4)$$

where $k\mu$ is a constant, which includes n_{t0}. Substituting (4) for Q_{CB} in (3) with the power index β according to Leroux [16], by $2[(w_{ta}/k_B T)-1)]$, the bias dependent mobility $\mu_{FE}(V_G)$ including trap density of states and carrier mobility from Rensselaer Polytechnic Institute (RPI) TFT model [17], is given by:

$$\mu_{FE,\,RPI}(V_G) = \mu_d k_\mu (V_G - V_T)^\beta \quad (5)$$

The effective gate voltage in the channel changes as a function of x with the voltage difference dV between x and $x+dx$ is $I_D(V_G, V_D)dx \times [\mu_{FE}. \mathrm{WC_G}(V_G - V_T - V_x)(V_G - V_x)]^{-1}$, therefore, I_D in the linear region (i.e., $V_D < V_G - V_T$) can be determined from the following equation [18]:

$$I_D(V_G, V_D)_{lin} = \frac{W}{L} C_G \int \mu_{FE}(V_G - V)(V_G - V_T - V)dV \quad (6)$$

The equation (6) can also provide I_D in the saturation region ($V_G - V_T \leq V_D$) if the integral is limited up to the pinch-off voltage by $Vp = V_G - V_T$ conditions.

The Gallium (*Ga*) ion caters much tighter bonding with the oxygen ions owing to the equitably high ionic potential than to the Indium (*In*) and Zinc (*Zn*) ions; therefore, *Ga* content suppresses the creation of OV, and results in both the g_{td} and g_{gd} to decrease with the increase in *Ga* amount. When an increased *In* content is preferred, the mobility increases, but unfortunately, the off-current and the sub-threshold swing raises [12], [19]. On the contrary, increasing *Ga* can result in the reduced off-current and steeper sub-threshold swing, however, at the cost of a decrease in the device mobility. Therefore, to adopt as a compromise for achieving improved electrical performance of the device and to overcome arised-inconsistencies, the double-active layer structures have been proposed. Fig. 1 shows the effect on the subband gap states of the DOS model due to the bulk-IGZO and gate-insulator interface. In Fig 1, the peak density n_{ta} and slope w_{ta} describe the acceptor band-tail states (TA) and the peak density n_{ga}, the characteristic decay energy w_{ga}, and the peak energy E_{ga} represent the Gaussian deep-level acceptor (GA) states. Similarly, referring to the same illustration, the Gaussian

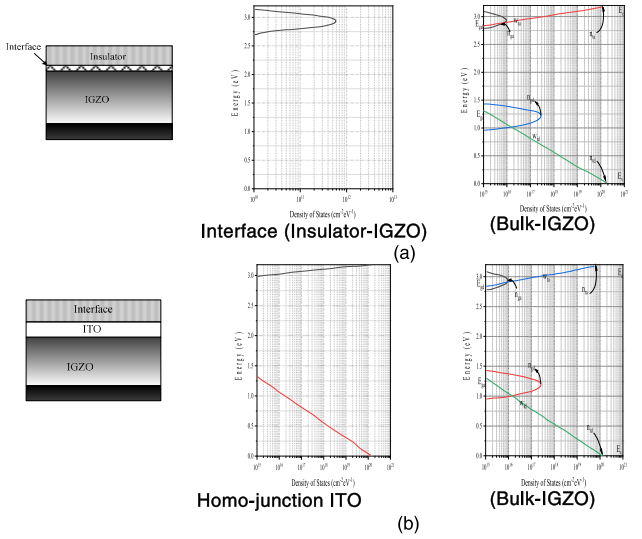

FIGURE 1. Amorphous-IGZO DOS model (a) single-IGZO/insulator (b) proposed for IGZO/ITO interface.

distributed donor states (GD) are designated by $n_{\rm gd}$, w_{gd}, and the $E_{\rm gd}$, while the donor band-tail (TD) states are defined by the peak density n_{td}, and the Urbach energy (slope) w_{td}.

Subsequently, we have conducted an experimental trial of variation in thickness in the adjoining layers, which compose the active layer of the IGZO-TFT channel. Since the mobility in multi-component oxide material depends on the overlapping of the s-orbitals, the *In* can be more effectively rationalized for achieving higher mobility compared to *Ga* [20].

According to the reported literature up till now, the Electron Band Mobility (EBM) obtainable from the α-IGZO device lies between 10 to 20 $\rm cm^2V^{-1}s^{-1}$ [21]–[24]. At the same time, an α-IZO combination has been reported mobility of the order of 59 $\rm cm^2V^{-1}s^{-1}$ [25]. Therefore, in order to achieve high mobility, incorporating α-IGZO (*In*:*Ga*:*Zn*; 1:0:1 atomic-ratio) with for EBM to 50 $\rm cm^2V^{-1}s^{-1}$ and an adjoining α-IGZO with (*In*:*Ga*:*Zn* = 1:1:1 atomic ratio) can be is set to 15 $cm^2V^{-1}s^{-1}$ in dual active layer has been proposed previously. The electron affinity ($\chi_{\alpha-IGZO}$) of the device can be estimated from the linear relationship among the three fundamental compounds that constitute the material, as given by:

$$\chi_{(\alpha-\rm IGZO)} = \rm A\chi_{(In_2O_3)} + B\chi_{(Ga_2O_3)} + C\chi_{(ZnO)} \qquad (7)$$

where A, B, and C correspond to the mol % of In_2O_3, Ga_2O_3, and ZnO, i.e., 4.45 eV, 3.19 eV, and 4.5 eV, respectively, adapted from [26]. In the proposed the layer1 considered to contains negligible *Ga* contents (*In*:*Ga*:*Zn* = 1:0:1), then A, B, and C are 0.33, 0, and 0.67, respectively) and $\chi_{(\alpha-\rm IGZO)}$ of layer1 is 4.48 eV. Similarly, for the layer2, *In*:*Ga*:*Zn* = 1:1:1 (A, B and C are 0.25, 0.25, and 0.5, respectively), and $\chi_{\alpha-IGZO}$ of the layer2 is 4.16 eV.

It is evident from Table 1 that at $x = 30$ nm (TFT channel has only high mobility layer1) at which poor sub-threshold is obtained due to higher mobility, DOS of the tail, and

TABLE 1. α-IGZO TFT electrical characteristics at different x along the channel.

	At different x of α-IGZO layer1						(Tri-active layer)
Symbol (Unit)	0 nm	15 nm	23 nm	25 nm	27 nm	30 nm	23nm/ 4nm/ 3nm
V_{TH} (V)	1.18	-0.41	-2.62	-1.52	-3.22	1.85	-4.24
I_{ON} ($\mu A/\mu m$)	1.70	2.096	1.167	1.034	0.855	0.285	9.23
I_{OFF} ($nA/\mu m$)	1.3E-2	3.3E-3	8.2E-6	3.9E-7	1E-9	2.1E-7	4.9E-8
SS ($mV/Dec.$)	0.290	0.275	0.283	0.164	0.190	0.663	0.198

donor-like states of layer1 in comparison to the layer2. In contrast, the device has a low I_{ON} with a fairly upright performance in the subthreshold region with $x = 0$ nm where the TFT channel is only of layer2, i.e., *In*:*Ga*:*Zn* = 1:1:1). In between these two values of x, the sub-threshold performances are reasonably good. It happens because the high mobility material serves as a front-channel to increase the drain current in the on-state of the device. Whereas the low mobility material the backchannel, reasons to reduce the drain current in the off conditions. Then, with the variation of threshold voltage, it is observed that bringing $x = 5$ nm layer1, the threshold voltage is abruptly changed from 1.18 V to –0.41 V. On the contrary, SS and the ratio ION/IOFF exhibited the same tendency on x, where the electrical performance increases when x varies from 0 to 15 nm, then decreases when x changes from 15 to 30 nm. Therefore, it has been noticed that the relative position of the interface (between layer1 and layer2) and the main charge conducting active layer adjoining the gate insulator is vital in determining the device parameters. Further studies have been carried out on the influence of gate voltage on the distribution of carriers. Similar trends have been realized with each simulation of the device when $x = 10$, 23, and 27 nm were considered.

It is noteworthy that the device performance is governed by the location of the active layer interface. Thereby, amending a layer thickness in a multi-layer structure can bring a shift to the position of the interface, and that, results in the difference in the device performance parameters, as listed in Table 1.

Fig. 2 compares the distribution of carrier concentration along the channel for different x (thickness of layer1). The TFT channel consisting of layers, as shown in Fig. 2 (a)-(c), have been simulated in each run with variation in sublayer thickness for a cumulative thickness of 30 nm. It could be inferred that the structure in which the layer interface is located adjacent to the conductive channel between layer1 and layer2 affects the low turn-on voltage. Such occurrence is due to a large number of carriers pre-exist in the primary conductive channel due to positive gate bias. In addition, electrical performance in negative gate bias is also commendable as the carriers get unperturbed, passing through the

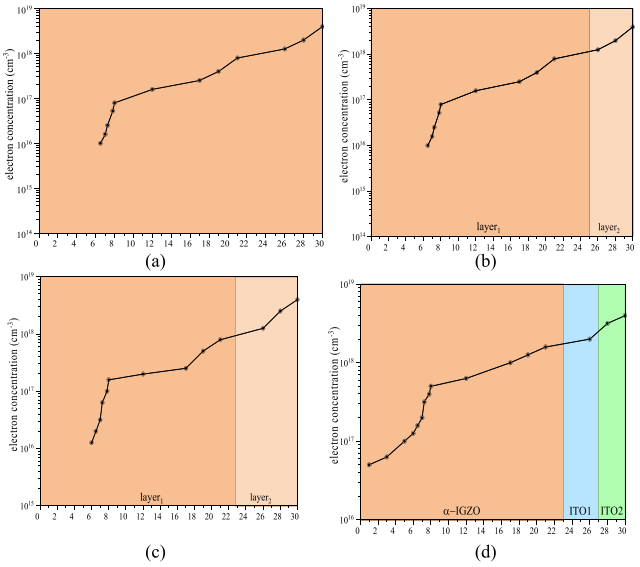

FIGURE 2. Distribution of carrier concentration along the channel (x=30 nm) at $V_G = 5V$ in (a) single-active layer (b) double-active layer with $layer_1$/ $layer_2 = 25$ nm/5 nm (c) double-active layer with $layer_1$/ $layer_2 = 23$ nm/7 nm, and (d) tri-active layer.

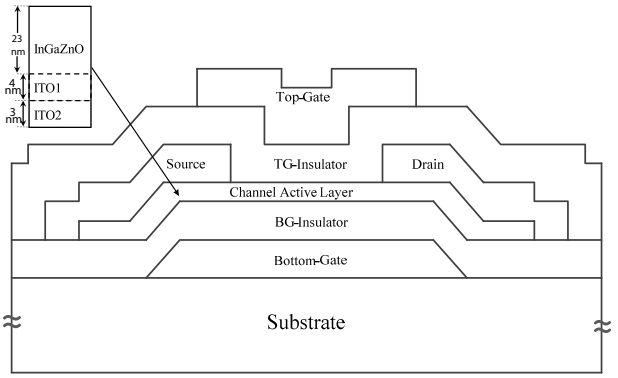

FIGURE 3. Proposed schematic of the Double-Gate Tri-Active Layer (DG-TAL) channel IGZO TFT.

interface between layer1 and layer2. With an applied negative gate bias, the carriers at the most can only accumulate in the regions near the moderately lower resistive interface between layer1 and layer2, and therefore, it results in low electrical performance, i.e., high turn-off current.

Fundamentally, the bilayer/DAL TFTs, the high-mobility semiconductor is complemented with low carrier concentration amorphous oxide semiconductor to achieve higher mobility and stability that in comparison to the single active layer channel structure because both the front and back channels inhibit high charge trap density and carrier concentrations [27], [28]. Subsequently, several other DAL combinations such as ITO–IGZO, IZO–IGZO, IZO–ZTO, and IZO–AIZTO exist. However, ITO–IGZO combination attained more focus due to minimal interface trap density (d_{it}), the existence of smoother surface in both layers, and the homo-junction formation by ITO and α-IGZO [19]. Moreover, based on the solid-state energy scale [29], the oxygen anion-derived valence band makes almost equal ionization potential and the same bandgap for both the ITO and α-IGZO thin films.

III. DEVICE SIMULATION

As shown in Fig. 3, a TFT device has been designed in a double-gate structure incorporating the tri-layer channel from our experiment of layer variation results. An active layer serves as the channel containing α-IGZO and Tin-doped Indium Oxide (ITO) of *30* μm channel-length. The channel layer is formed of sublayers, including *23* nm thick α-IGZO, *4* nm of an ITO layer-1 (ITO-1), and *3* nm of ITO layer-2 (ITO-2), making the total thickness of the active layer as *30* nm. The ITO sublayers are distinct in terms of the concentration of order 3.63×10^{14}cm^{-3}. The thicker ITO with high doping results in better gate control, and high doping provides greater control on the device characteristics.

The third ITO comparatively thin layer of the channel affects the charge trapping at a lower concentration to enhance the channel mobility in the structure. The symmetric-gate structure is considered; therefore, the SiO_2 gate-insulator of *130* nm thickness was used in the device structure for each of the bottom- and top-gate. The gate and S/D ohmic contacts of Molybdenum were assigned, and both thermionic emission and tunneling current were considered in this work. As revealed from the experiment of layer thickness variation TFT, the Tri-Active Layer channel structure has been incorporated. The simulation and DOS model parameters of our proposed TFT are listed in Table 2. The device model is based on the Rensselaer Polytechnic Institute amorphous IGZO (RPI- α-IGZO) model [32]. The device simulation parameters have been adapted from the author's previous findings [33], [34] for this work, and the compact model outlines have been applied in the Keysight Advance Design System (ADS 2015.01).

Fig. 4 illustrates the electron concentration and current density dispersal in the channel along the length of our proposed device, as obtained from the structure simulation at $V_{G(\text{top gate})} = 0$ V and $V_{G(\text{bottomgate})} = 20\ V$, and $V_D = 0.1$. The increased V_{BG} inculcates carriers to tempt the channel conductivity. The resulting characteristics are promising with the typical transistor theory. The electrical parameters of a TFT that describe the performance of the device include field-effect mobility μ_{FE}), current-ratio (I_{ON}/I_{OFF}), the threshold voltage (V_{TH}), and subthreshold voltage swing (SS) are derived from the device I-V characteristics of the device. In the double-gate structure, it is anticipated that the V_{TH} is affected by the top gate (TG) bias. Consequently, it is imperative to see if the influence of TG voltage V_{TG} on the electrical characteristics of the device. The obtained characteristics of the device are shown in Fig. 5, where Fig. 5 (a) is the corresponding transfer-characteristics of double-gate α-IGZO TAL TFT, and the drain current-voltage relationship at different biasing conditions of the bottom-gate is shown in Fig. 5 (b). The electrical parameters of the

TABLE 2. Key simulation parameters of α-IGZO TAL TFT.

Parameter (Symbol)	Value			Unit
	α-IGZO layer$_1$	*α-IGZO* layer$_2$	ITO layer$_3$	
Bandgap (E_g)	3.25	3.05	3.25	eV
Electron effective mass (m_e)	0.34 [30]	0.34 [30]	0.30 [31]	-
Electron band-mobility (μ_n)	50	15	35	$cm^2V^{-1}s^{-1}$
Electron affinity (χ)	4.48	4.16	4.16	eV
Hole band-mobility (μ_p)	0.1	0.1	_	$cm^2V^{-1}s^{-1}$
Peak density, donor band-tail states (n_{td})	2×10^{20}	1.55×10^{20}	1.55×10^{20}	cm^{-3}/eV
Peak density, acceptor band-tail states (n_{ta})	2×10^{20}	1.55×10^{20}	2.20×10^{20}	cm^{-3}/eV
Urbach energy donor-tail (w_{td})	0.11	0.11	0.11	eV
Urbach energy donor-tail (w_{ta})	0.030	0.030	0.018	eV
Gaussian donor Decay energy (w_{gd})	0.1	0.1	_	eV
mean energy OV states (E_{gd})	2.95	2.95	_	eV
Gaussian donor peak density (n_{gd})	3×10^{17}	1.6×10^{16}	_	cm^{-3}/eV
Interface-trap density (d_{it})	6×10^{11}	6×10^{11}	$\sim10^{10}$	cm^{-3}/eV
Gaussian acceptor peak density (n_{ga})	3.2×10^{17}	3.2×10^{17}	_	cm^{-3}/eV
Gaussian donor Decay energy (w_{ga})	0.1	0.1	_	eV

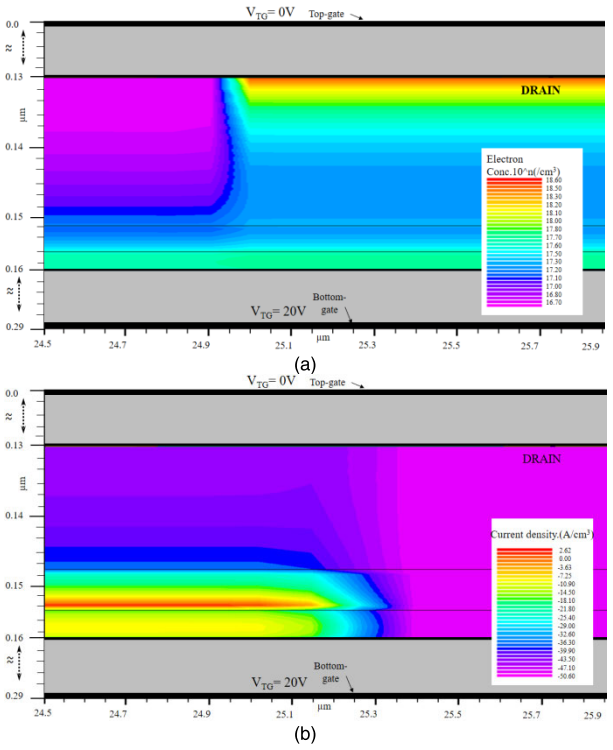

FIGURE 4. Double-Gate Tri-Active Layer (DG-TAL) channel IGZO TFT structure simulation along with the channel length (a) distribution of electron concentration, and (b) current density.

TABLE 3. Comparison of device parameters of double-gate TAL IGZO TFT.

Parame (Unit)	Proposed device with Gate and S/D Overlap length 2 µm			Proposed device with Gate and S/D Offset length 1.5 µm			Gate and S/D Offset and overlap length 0 µm in Coplanar Structure DAL TFT [36]		
	TG	BG	DG	TG	BG	DG	TG	BG	DG
V_{TH} (V)	0.80	0.55	0.27	-0.64	0.79	0.49	0.42	0.54	0.55
I_{ON} (µA/µm)	9.2	6.13	2.9	9.23	0.45	3.1	0.63	1.3	2.0
I_{OFF} (nA/µm)	3E-6	2E-6	3E-4	5E-5	1E-5	2E-8	< 1E-4	< 1E-4	< 1E-4
SS (V/decade	0.297	0.162	0.107	0.283	0.171	0.199	0.286	0.153	0.100
μ_{FE} (cm^2/V-s)	12.79	13.82	16.08	4.21	9.11	6.07	11.52	12.8	13.08

device μ_{FE}, V_{TH}, and SS are 38.2 $cm^2V^{-1}s^{-1}$, −4.83 V, and 0.198 V/decade, respectively, for an effective channel width and length of 180 μm and 30 μm, respectively. However, for circuit designing, the negative V_{TH} value of the TFT is unfavorable. It can be observed that the transfer curves undergo a parallel shift in response to V_{TG} without any changes of SS and I_{OFF}. Our results have been compared with those obtained for DG α-IGZO TFTs. In particular, the magnitude of V_{TH} shift is smaller, and SS and I_{OFF} are increasing for V_{TG} values greater than 0 V in the α-IGZO TFT [35], [36].

It has been speculated that the difference lies due to the nonexistence of the hole in the active layer. At the same time, the band bending takes place at the bottom interface due to applied results in electron accumulation.

Therefore, in response to V_{TG} less than 0 V, V_{TH} could be predicted in shifting towards a positive direction. If the hole is possibly accumulated in α-IGZO, then it would occur at the top interface. Furthermore, the hole accumulation layer could change I_{OFF} and SS by generating undesired leakage current.

The double gate α-IGZO TFTs does not exhibit such variation of I_{OFF} and SS. A similar observation was already made for DG a-IGZO TFTs [35], [34]. Table 3 gives the comparison of device simulation and electrical performance parameters with the coplanar structure of α-IGZO TFT. The gate on the top of α-IGZO TFT channel modulates the V_{TH} by positive biasing, which raises the fermi-level of α-IGZO and adjusts the threshold voltage for a smooth turn-on. Conversely, the negative back gate bias low down the fermi-level of α-IGZO and makes it difficult to turn the TFT on [37]–[40].

To realize binning, the model parameters for the device channel length ($L \leq 30$ μm) and ($L \geq 30$ μm) have been determined, considering a continuity at $L = 30$ μm. Subsequently, the reference dimension of the channel length L_{REF} and channel width W_{REF} of the device are 30 μm and 180 μm, respectively. The the zero-bias threshold voltage V_{TO} of the standard RPI-aTFT model has been amended using the following model fitting equations.

$$V_{TO} = P_{vr} \times 0.35\text{V} \times (1 + L_{Ref}/L)^{L/L_{Ref}} - 0.15\text{V};$$

where P_{vr} is the process variation factor, the SPICE

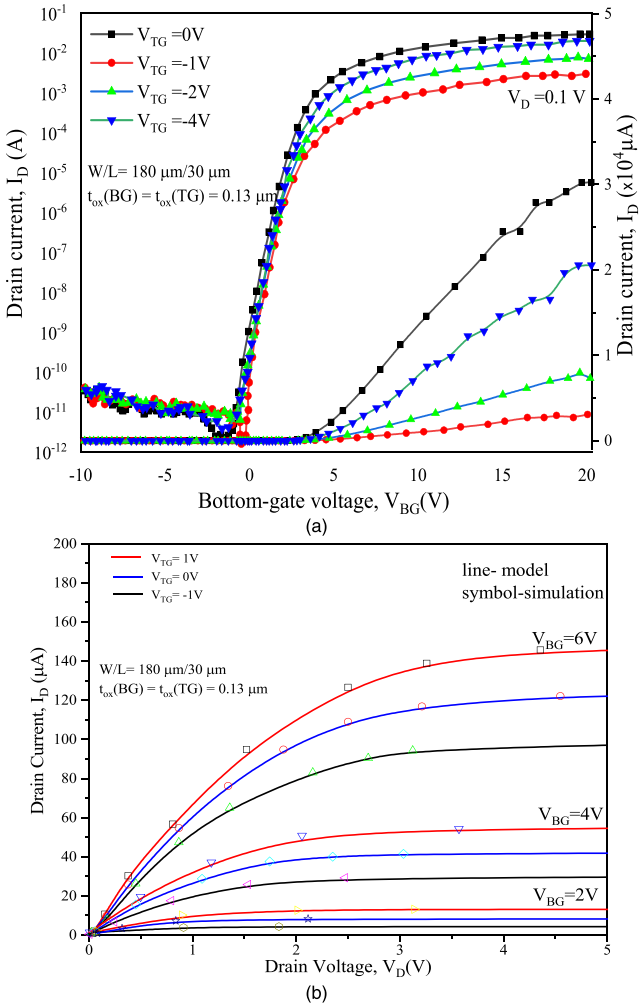

FIGURE 5. Double-gate TAL IGZO TFT (a) Transfer characteristics ($I_D - V_G$) at the various top-gate voltage and $V_D = 0.1$ V; and (b) Drain-characteristics (I_D–V_D) at V_{BG} 2V, 4V, and 6 V, respectively.

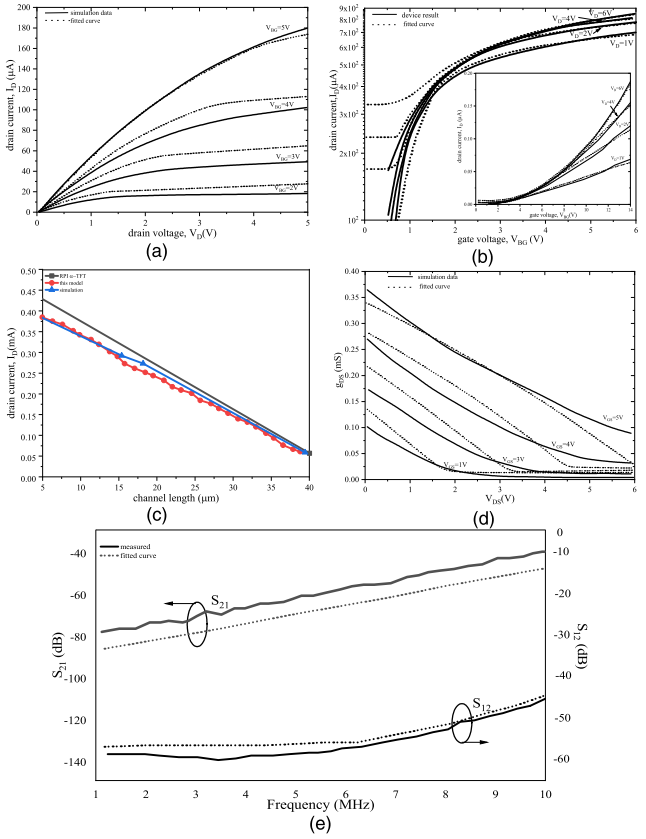

FIGURE 6. Device characteristics and fitted parameters with the compact model (W/L = 180/30μm). (a) $I_D - V_D$ at various V_{BG} (b) $I_D - V_G$ at various V_D (c) drain current at various channel length (d) gds–V_{DS} characteristics (e) s-parameters of the typical sample of a single TFT DUT) and (Eta = 12).

LEVEL3 MOSFET model template is chosen for TFT modeling as the static feedback parameter eta [41]. The model is suitable for describing the short-channel effects yet also applicable in TFT devices. The relevant process and device of the model parameters listed in Table 4 are fitted to both dc and ac results of the TFT for the shorter channel lengths. For the dc characteristics, output and transfer characteristics have been obtained on TFT samples of two different sizes: $W/L =$ 180/60 and 180/30 μm and fitted with the average of four device samples to interpret the scalability of the drain current. The value of mobility (Uo) in Table 4 is selected using close approximation with the measured dc characteristics and the value of η (eta) [41]. Fig. 6 shows the short-channel device characteristics and fitted curves with the compact model eta = 12). As shown in Fig. 6(a), all the curves are not well fitted. In particular, the curves with gate bias 5 V and 2 V are closely fitted when the eta is changed to 16 and 8, respectively. Fig. 6 (c) shows ~14% difference of drain current, which is tolerable with the dc characteristics and relevant to analog circuit design; however, the absolute accuracy is a tradeoff compared to the more critical parameters, such as g_{DS} and g_m. It was found that at eta = 12, the transconductance slope g_{DS}, as shown in Fig. 6(d) has been accurately optimized in the saturation region with gate bias 3V. For fitting the ac characteristics, the S-parameter measurements are carried out on TFT devices ($W = 180$ and $L = 30$ μm) that showed dc characteristics closest to the average of four samples used for dc fitting. A comparison between the ac measurement results and fitted curves are shown in Fig. 6(e). The small-signal parameters of the model are derived from s-parameter measurements using the method described in [42]. The aggregate value of the source and drain overlap capacitance is ~2.35 pF. Therefore, the overlap capacitances C_{GSO} and C_{GDO} in per meter and per side can be assigned as $((2.35/2)e - 12/30e - 6 = 39.2$ nF/m. To account a conventional CMOS, SiO_2 gate oxide material has been assumed in the realized model. In the case of different materials, the physical thickness of 130 nm can be scaled with the ratio of dielectric permittivity to replace an effective oxide thickness.

IV. IMPLEMENTATION AND CIRCUIT ANALYSIS

The RFID tags are the distinct microelectronic passive chip that receives power from the radio frequency Transmitter (or reader), and a rectifier for supplying DC voltage is the pri-

TABLE 4. Extracted small-signal circuit values at V_{GS}5V, V_{DS}6V).

Circuit parameter (Unit)	Value
Capacitance, C_{GS} (F)	0.58×10^{-13}
Capacitance, C_{GD} (F)	0.44×10^{-13}
Capacitance, C_{DS} (F)	0.54×10^{-14}
Delay, τ (s)	68×10^{-12}
Resistance, R_{DS} (Ω)	35.2×10^{3}
Resistance, R_i (Ω)	280
Transconductance, g_{mo} (S)	0.20×10^{-3}

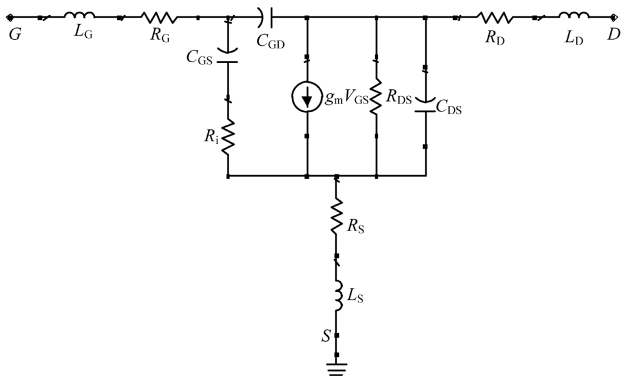

FIGURE 7. The small-signal model of the simulated device.

mary element of the RFID communication system [43], [44]. The input RF signal received from the antenna of the identifier is fed to the rectifier that transforms the incident input RF signal into Direct Current (DC). The RFID devices are usually being ordered in four leading communication bands, i.e., the frequency range of 135 kHz, band at 13.56 MHz, a band at 900 MHz, and a band at 2.4 GHz [45], [46]. Although amorphous silicon-based TFTs can operate even at low-frequency 135 kHz as well, however, due to impaired mobility, they are restrained in RFID applications. The oxide-TFTs based TFTs are capable of operating in the 13.56 MHz band [46]. Moreover, a double-gate device provides the degree of freedom for the threshold voltage tuning using the alternative gate [47], which brings an advantage in designing of high gain and low-power analog circuits. The model of the α-IGZO TFT using small-signal analysis is shown in Fig. 7. The fundamental model components have been escalated, and the extracted values are listed in Table 4. The g_{mo} parameter represents a maximum value of transconductance, and C_{GS}, C_{GD}, and C_{DS} are the capacitances between gate-source, gate-drain, and drain-source terminals, respectively. R_{DS} and R_i are the output drain-source and circuit internal resistance, respectively. The model predicts the frequency response and the performance of the scaled device [48].

TABLE 5. Circuit model device parameters.

Name	Value	Units	
TOX	1.30E-07	m	Gate oxide-thickness
LD	2.95E-03	m	Channel length reduction
WD	1.80E-04	m	Channel width reduction
UO	17.26	$cm^2V^{-1}s^{-1}$	Low field mobility at no bias
VTO	4.62	V	threshold voltage of long channel device (at zero substrate bias)
THETA	-0.208	1/V	Gate-field mobility reduction parameter
RS, RD	28.06	ohm	Lumped resistances
DELTA	2.27	–	Narrow channel effect on V_{TH}
XJ	1.84E-07	m	Drain/Source junction depth
ETA	12	–	Barrier lowering coefficient
KAPPA	6.92E+02	1/V	Channel length modulation effect
NFS	3.00E+11	cm^{-2}	Surface state density
CGSO	3.92E-08	F/m	Gate-Source capacitance
CGDO	3.92E-08	F/m	Gate-Drain capacitance
CGBO	5.75E-10	F/m	Gate-body capacitance
XQC	0.40	–	Charge partitioning parameter
PB	0.95	V	Junction built-in potential, PB = (KT/q)ln (NSUB/ni) + 0.56

The modeling parameters were extracted from the TFT measured data by fitting the AC and DC characteristics for a good agreement, and the well-scalable TFT gate-length (l_G) values have been considered [49]. The computed device model parameter values are listed in Table 5, which were then exported to the ADS circuit simulator. More accurate and faster compact models tailored to the simulation of TFT devices of various semiconducting materials based on physics are available, which is available in a number of circuit simulators. The physics-based parameters as well as empirical parameters are suitable to model effects observed in amorphous TFTs. Consequently, it can be fitted to a-IGZO TFT devices more accurately than other TFT models and then the proposed SPICE Level 3 MOSFET model. Besides being these few shortcomings of convergence and speed, the Level3 spice has the advantage that among the options available in the public domain for unlicensed use, the proposed approach has not been obsolete and capable of providing approximation of results for early detection of desired outcomes.

In particular, a high Power Conversion efficiency (PCE) and low-power consumption of the logic circuit are the desired figure of merit in an RFID tag.

The PCE of a rectifier, i.e., the power ratio of output dc to the RF input, depends on the device characteristics, the circuit arrangement, input range of the RF signal, and the output load.

A switching transistor with adequately low resistance can act as similar to a Schottky device in large-signal

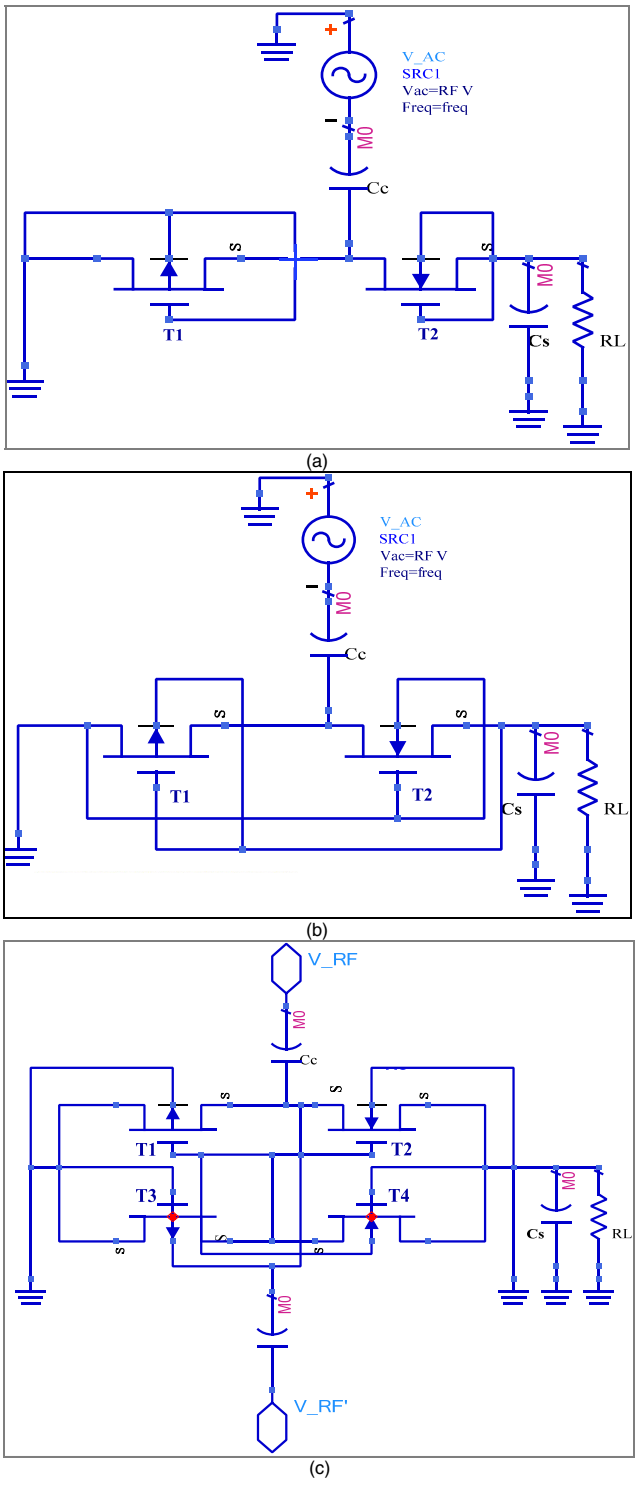

FIGURE 8. Proposed rectifiers configurations using DG-TALα-IGZO TFTs (a) Simple Rectifier (b) Self-V_{TH}-Cancellation (SVC) (c) Differential arrangement.

TABLE 6. Comparison of proposed results with existing rectifiers.

Reference	Frequency	Power	PCE
Low power double-gate PEALD ZnO TFT rectifier [51]	4 Hz	<150 nW.	Small 200-mV p-p PCE by 0.2–4.7%
3TDGMOSFET [47]	Wp/Wn = 2, f = 100 MHz.	0.01–36 µw for SVC, 0.01–14 µw for conventional and 0.5–515 µw for differential rectifier	DC output power increase by 296 pw–4.1 µw and PCE change by 1.2–2.2%.
diode-connected MOS [53]	900-MHz	−15 dBm to −4 dBm	PCE 30%, and the maximum output voltage is 5.5 V
Pt/In-Ga-Zn-O Schottky Diodes [54]	125 kHz - 134 kHz,	-	output voltage amplitude of 0.87 V for 2 V supply voltage.
This work	13.56 MHz	power consumption is 0.14 µW (SVC) configuration	power conversion efficiency of 20.06% for low input 0.45 V−0.61 V.

rectifiers [50]. Therefore, the gain of the PCE is achievable at the low-threshold voltage of the device. However, the threshold voltage cannot be dropped significantly since the sub-threshold leakage current increases with a lower threshold that, on the contrary, limits the PCE of the rectifiers. For the comparison of the performance of our device in the RFID rectifier circuit, we have simulated rectifier topologies aiming at the ultra-low-power applications, as illustrated in Fig. 8. A simple diode-connected MOS rectifier circuit arrangement is shown in Fig. 8(a). In this arrangement, when V_{RF} is high, T2 operates in the linear region with very low on-resistance; accordingly, V_L across R_L reaches up as high as V_p. On the other hand, when V_{RF} goes low, the resultant V_G is reduced by the factor $V_{RL} - V_{in}$. The absolute value goes $V_{GD1} < V_{TH1}$, and consequently, T1 switches to cut off. Fig. 8(b) shows Self-V_{TH}-Cancellation (SVC) circuit rectifier that is quite similar to the simple rectifier, except it utilizes the connection enhancements using complementary-MOS arrangement to increase the output DC voltage [52]. The circuit parameters are as follows $C_C = C_S = 10$ pf and $R_L = 10$ kΩ. The differential arrangement is an active V_{TH} cancellation circuit to minimize in a forward-bias by a cross-coupling circuit formation, as depicted in Fig. 8(c).

Fig. 9 illustrates the comparison of the key performance parameters results as a function of RF input in terms of the frequency response, PCE, power consumption, and the output DC voltage, respectively, as obtained from the circuit simulation. Fig. 9(a) shows the plot that compares the frequency operation obtained from the simulation of a rectifier and the one by solving the parameters of small-signal model circuits. The relationship between PCE and input voltage is

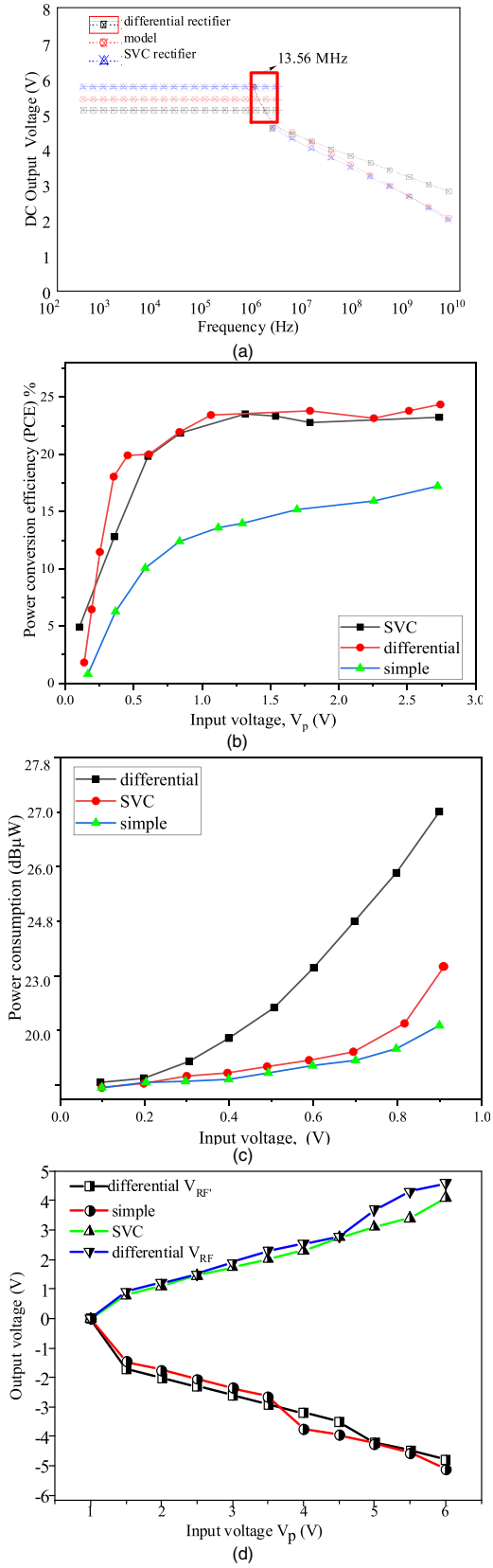

FIGURE 9. Performance comparison of DG-TAL α-IGZO TFT rectifier circuits topologies as a function of RF input voltage (a) DC output voltage versus frequency (b) power conversion efficiency (c) power consumption (d) output DC voltage.

plotted in Fig. 9(b) for all the three circuit topologies with the sinusoid RF input of 13.56 MHz and the output load is 10 kΩ. According to the results, the considerable high conversion efficiency is achieved by the α-IGZO TFT based circuits, specifically at low-level RF input amplitudes in comparison to the results of power consumed by the simple diode rectifier. Later, for the sufficiently high level of the signal values, a good agreement has also been obtained. Fig. 9(c) corresponds to the power consumed by the circuit for rectification.

In general, the differential arrangement has high power consumption, probably due to the power dissipated in the number of components than to the simple diode rectifier circuit. However, for the conversion of low RF input peak values up to 0.2V(V_p), the power consumption is comparable to other topologies and significant for ultra-low power operations. The comparison of output DC voltage output by the various rectifier topologies inline to the variation in input levels is shown in Fig. 9(d). Table 6 shows the comparison of proposed rectifier performance with the existing RFID rectifier topologies.

V. CONCLUSION

In this research work, the authors have proposed a design of a double-gate amorphous In-Ga-Zn-O thin-film transistor in a novel tri-active layer channel structure and then successfully implemented the device performance to realize the rectifier circuits for an RFID tag. The extracted electrical parameters of the device have displayed significant performance, such as high mobility (μ_{FE}) $\sim$ 38.2 $cm^2V^{-1}s^{-1}$, a low threshold voltage (V_{TH}) $-$ 4.83 V, steeper subthreshold swing 0.198 V/decade, and high I_{ON}/I_{OFF} $\sim$ 10^8 respectively. In conclusion, the proposed device in the double-gate structure is capable of better gate control and switching. This device design of TFT has been found suitable for the RFID frequency 13.56 MHz. The device characteristics have been successfully implemented for the simulation of rectifier circuit configurations in ADS. In the comparison of RFID rectifiers performance, the differential arrangement circuit delivers the utmost power conversion efficiency and the least power consumption for weak RF input values.

The achieved Power Conversion Efficiency (PCE) for the same RF input voltage level is ranging from *22–39%* for differential arrangement, *4–21%* for self-V_{TH}-cancellation rectifier circuit, and *0.2–9%* for the simple rectifier. The power for the differential, SVC, and the simple rectifier circuits are $\sim$0.024 μW to 0.44 μW, 0.01–14 μW, and 0.5–515 μW, respectively. The promising results of the novel device deployment open up newer prospects of improvement in the ultra-low-power RFID rectifiers.

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SHASHI K. DARGAR (Senior Member, IEEE) received the bachelor's degree in electronics and communication engineering, the master's degree in digital communication, and the Ph.D. degree in microelectronics, in 2005, 2013, and 2017, respectively. He is currently a Postdoctoral Fellow with the Department of Electronic Engineering, University of KwaZulu-Natal, Durban, South Africa. He has been contributing to the research and academics for a period of 12 years. He has authored 30 scientific research articles in reputed journals and conferences. His research interests include microelectronics, thin-film device design, VLSI, wireless communication, and microwave and communication engineering. He is a Life Member of the IEEE HKN-Mu Eta Chapter.

VIRANJAY M. SRIVASTAVA (Senior Member, IEEE) received the bachelor's degree in electronics and instrumentation engineering, the master's degree in VLSI design, and the Ph.D. degree in RF microelectronics and VLSI design, in 2002, 2008, and 2012, respectively. He has worked for the fabrication of devices and development of circuit design. He is currently an Associate Professor with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa. He has more than 17 years of teaching and research experience in VLSI design, RFIC design, and analog IC design. He has supervised various bachelor's, master's, and Ph.D. research. He has authored/coauthored more than 220 scientific contributions, including articles in international refereed journals, chapters in book, and conferences. He is a Senior Member of SAIEE. He is also a member of IET, the IEEE-HKN, and IITPSA.