IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 4, 2020, accepted October 17, 2020, date of publication October 26, 2020, date of current version November 18, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3033718

An FPGA Kalman-MPPT Implementation Adapted in SST-Based Dual Active Bridge Converters for DC Microgrids Systems

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This work was supported in part by the CONACYT-FONCICYT under Grant 266438, and in part by the UK Research and Innovation (UKRI) Department.

ABSTRACT The design of digital hardware controllers for the integration of renewable energy sources in DC microgrids is a research topic of interest. In this paper, a Kalman filter-based maximum power point tracking algorithm is implemented in an FPGA and adapted in a dual active bridge (DAB) converter topology for DC microgrids. This approach uses the Hardware/Software (HW/SW) co-design paradigm in combination with a pipelined piecewise polynomial approximation design of the Kalman-maximum power point tracking (MPPT) algorithm instead of traditional lookup table (LUT)-based methods. Experimental results reveal a good integration of the Kalman-MPPT design with the DAB-based converter, particularly during irradiation and temperature variations due to changes in weather conditions, as well as a good-balanced hardware design in complexity and area-time performance compared to other state-of-art FPGA designs.

INDEX TERMS DC-DC power converters, power generation, field programmable gate arrays.

I. INTRODUCTION

DC microgrid is an attractive technology for electrical grid systems because of its natural interface with renewable energy sources, electric loads, energy storage systems and galvanic isolation. It can supply more effectively and efficiently the renewable energy sources to power electronic loads by choosing a suitable voltage level and thereby avoiding conversion stages [1].

Recent studies show an increase in research works on the development of digital controllers for direct current (DC) microgrids systems [2]–[10]. Implementations on different technology fields, such as, vehicle to grid (V2G) [2], [8], power management distribution from PVs [3], [4], hybrid AC/DC microgrids [5]–[7], [10] have been proposed with different converter configurations. Its power capacity is very variable and uncertain when solar photovoltaic (PV) arrays are integrated due to its dependency on weather conditions. To solve this problem, the digital implementation of maximum power point tracking (MPPT) algorithms is necessary for extracting the maximum power from a PV array under different conditions [11]–[14]. In this regard, the parallel programming, fast processing capabilities, decreasing cots and the HW/SW co-design features of the field programmable gate array (FPGA) looks like an attractive option for the digital control implementation [15]–[21]. For example, a time-area performance analysis in FPGAS of an adaptive perturb and observe (P&O) maximum power point tracking controller for photovoltaic application is presented in [15]. Also, the FPGA-based stability analysis of the P&O

The associate editor coordinating the review of this manuscript and approving it for publication was Yuh-Shyan Hwang.

method is performed by [16] and under partial shading conditions in [17]. Despite these HW design analysis, a drawback of P&O is that, at steady state, the operating point oscillates around the maximum power point with an unstable behavior.

In the design, it is desired a trade-off between the resource implementation area, the tracking speed and the oscillations that occur around the maximum power point (MPP). Alternative implementation approaches are fuzzy logic controller (FLC) [21], [22], evolutionary algorithms (EAs) [23], bio-inspired algorithms [24], modified sine-cosine [25], partial swarm optimization (PSO) [26]–[28], intelligent fuzzy particle swarm optimization (ANFIS-PSO) [29], ANFIS with artificial bee colony (ANFIS-ABC) [30], ANFIS-FLOWER pollination optimization algorithm [31], Lyapunov function-based controller [32], gravitational search algorithm with particle swarm optimization (GAS-PSO) [33], PSO with artificial bee colony (PSO-ABC) [34] and neural network (NN) [12], to effectively deal with the non-linear characteristics of I-V curves. However, they require complex and extensive computations, which means a large area and complex FPGA implementation [35]–[38]. In particular, FPGA implementations of arithmetic operations require specific methods, such as in [35] for a complex divider, a piecewise polynomial approximation technique for a matrix inversion architecture [36], an adaptive segmentation methodology for evaluation functions [37] or an approximation technique as presented in [38]. In this sense, the Kalman-MPPT design with a parallel FPGA implementation represents a good fit to estimate non-measurable signals with a fast convergence and a well-balance in area-time performance. In comparison with traditional implementations, such as the perturb & observe (P&O) that is widely used in industry, Kalman filter has a faster tracking response [48], [49]. The filtering capabilities of the Kalman filter allow using more inexpensive sensors for the implementation of DC microgrids [47]. Figure 1 shows the conceptualization of the Kalman-MPPT adapted to the DAB converter for DC microgrids.

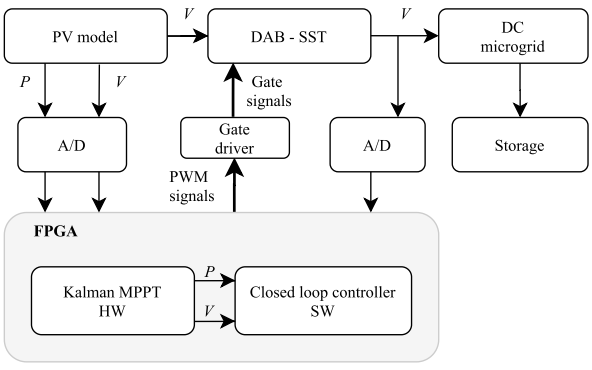

FIGURE 1. Conceptualization of the Kalman-MPPT and DAB controller for DC microgrids.

In this paper, an FPGA-based Kalman-MPPT architecture is implemented and adapted into a DAB-based converter for DC microgrids applications. In the design, the pipelined implementation with piecewise polynomial approximation (PPA) is developed. This hardware digital core is then connected as a coprocessor unit in the hardware/software (HW/SW) codesign paradigm. The main contributions of this work are:

- A low-cost and well-balanced area-time design of a full-custom Kalman-MPPT core with 55dB signal quantization to noise ratio (SQNR) for 24-bit resolution in an FPGA.
- Pipelined HW logic design implemented by using a PPA-based technique instead of lookup table (LUT)-based methods.
- A small-area Kalman-MPPT design that occupies less hardware resources than designs with intellectual property (IP) arithmetic blocks architectures.
- A system on a chip integration of the Kalman-MPPT logic-core with the HW/SW co-design technique in a flexible and rapid prototyping.

Although, there are studies of MPPT architectures and complex algorithms for DC microgrids in current iterature, many of these works avoid the implementation of arithmetic operations, such as matrix inversion, square roots, number divisions, among others, by using intellectual property (IP) cores, or removing this important arithmetic blocks from design; however, this restriction leads to losing algorithm precision and problems for converging to the correct results [19], [39], [45], [46], [50]. The use of Kalman-MPPT adapted to a DAB-based converter represents a reliable option to route renewable energy from homes and businesses with low-cost sensors and galvanic isolation to accommodate different voltage levels into the DC microgrid.

The rest of the paper is organized as follows: Section 2 reviews the background of Kalman-MPPT for SST-based DC microgrids. Section 3 presents a parallel Kalman-MPPT architecture and its integration in an HW/SW co-design. Section 4 analyzes the implementation results, and then, compares the hardware performance with the state-of-art designs on FPGAs. Section 5 shows a discussion of the performance analysis, and finally, Section 6 presents the concluding remarks.

II. KALMAN-MPPT IN DC MICROGRIDS

In this section, it is presented the analysis of the Kalman-MPPT algorithm for DC microgrids. As shown in Figure 1, the Kalman-MPPT implementation is conceptualized as a coprocessor unit following the HW/SW co-design technique. In order to implement and adapt the Kalman-MPPT design, the DAB mathematical model is described.

A. KALMAN-MPPT MODEL

The Kalman-MPPT is modelled to maximize the power capacity extracted from PV arrays. Considering that PV arrays have variations in the measurements of irradiance and temperature levels due to environmental fluctuations,

the Kalman filter can estimate the optimal voltage and power value to avoid loses in the MPPT accuracy.

The following model is used:

$$x_{k+1} = x_k + M\frac{\Delta P}{\Delta V}, \tag{1}$$
$$y_k = x_k + w_k, \tag{2}$$

where x_{k+1} is the updated value by the MPPT, M is the step size corrector, $\frac{\Delta P}{\Delta V}$ the slope of the P-V curve, w measurement noise. The general representation form in state space is the following:

$$x_{k+1} = Ax_k + Bu_k,$$
$$y_k = Cx_k + w_k, \tag{3}$$

with $A = 1, B = M, C = 1$ the main Kalman model parameters. Here, the Kalman filter approach is applied, and consists in proposing an estimated model of the system, as follows:

$$\hat{x}_{k+1} = \hat{x}_k + M\frac{\Delta P}{\Delta V} + K_k(y_k - C\hat{x}_k), \tag{4}$$

where K_k is the gain of the Kalman-MPPT that reduce the error between the output y_k and the estimated output of $\hat{y} = C\hat{x}_k$.

The gain is updated to predict the forward estimated state and the covariance error. These estimates operate as a correction mechanism that reduces the error as follows:

$$K_k = Z_k C^T (CZ_k C^T + R)^{-1}, \tag{5}$$
$$Z_{k+1} = (I - K_k C)Z_k. \tag{6}$$

With the correction mechanism, the reference voltage and power for DAB-SST operation are generated, obtaining the maximum value of the P-V curve.

B. DAB-SST MODEL

The DAB-SST model is analyzed in this subsection. Remark that the DAB-SST topology provides galvanic isolation and voltage adaption. It can operate at frequencies of kHz, and thus, a considerable reduction in component size is achieved [40], [41]. The schematic of a DAB-SST converter is presented in Figure 2.

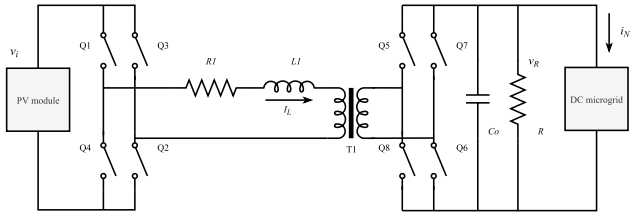

FIGURE 2. Conceptualization of the Kalman-MPPT and DAB-SST controller for DC microgrid.

As illustrated in Figure 2, the DAB-SST converter is composed of a high-frequency transformer with a Np/Ns ratio of $1:1$, two H-bridges of high-voltage power MOSFETs Qi, $i = 1, 2, \ldots$, the leakage inductance of the transforme r$L1$ and Resistance $R1$, DC output capacitor Co and the output resistor R.

Table 1 presents the parameters used in the DAB-SST converter.

TABLE 1. DAB-SST parameters used in the experiment.

$R = 1/20$	$C_o = 0.0002$
$R1 = 30$	$L1 = 0.0005$
$k_{I1} = 1$	$k_{v1} = 100$
$k_{I2} = 1$	$k_{v2} = 10$

Now, let us consider the matrix representation of the DAB-SST state-space model as follows:

$$\dot{x} = Ax + Bu, \tag{7}$$

where,

$$A = \begin{bmatrix} -\frac{1}{RC_0} & -\frac{4\sin(d\pi)}{\pi C_0} & -\frac{4\cos(d\pi)}{\pi C_0} \\ \frac{2\sin(d\pi)}{\pi L1} & -\frac{R1}{L1} & w_s \\ \frac{2\cos(d\pi)}{\pi L1} & -w_s & -\frac{R1}{L1} \end{bmatrix}, \tag{8}$$

$$B = \begin{bmatrix} 0 & -\frac{1}{C_0} \\ 0 & 0 \\ -\frac{2}{\pi L1} & 0 \end{bmatrix}, \tag{9}$$

$$x = \begin{bmatrix} v_R & \text{REAL}(I_L) & \text{IMAG}(I_L) \end{bmatrix}^{\mathrm{T}}, \quad \text{and} \tag{10}$$

$$u = \begin{bmatrix} v_i & i_N \end{bmatrix}^{\mathrm{T}}. \tag{11}$$

The state equation of (7) represents the dynamic behaviour of the DAB-DC-DC converter. Each H-bridge of the DAB simultaneously turn-on and turn-off the diagonal switches. However, these activations can cause DC offsets in both inductor current and transformer magnetic flux density in transient states. Therefore, a controller unit is necessary for phase shift modulation to control each H-bridge [1].

C. DAB-SST CONTROL

In order to control the power capacity of the DC microgrid, the flow of energy between the PV source and the DAB-SST must be controlled. A controller is proposed to stabilize the system and to achieve a good steady-state and dynamic response.

A testbench was employed with Xilinx Project Navigator and MATLAB/Simulink environment. The PWM signals (feedback controller) are generated to gate drivers and turn on/off the MOSFETs, using the reference signals addressed by the Kalman filter, as well as, DAB-SST output voltage and current measurements.

In this regard, the system introduced in (7) is rewritten as:

$$\dot{x}_1 = f_1(x) + b_1 u_1,$$
$$\dot{x}_2 = f_2(x), \tag{12}$$
$$\dot{x}_3 = f_3(x) + b_2 u_2,$$

where

$$f_1(x) = -\frac{1}{RC_0}x_1 - \frac{4\sin(d\pi)}{\pi C_0}x_2 - \frac{4\cos(d\pi)}{\pi C_0}x_3,$$
$$f_2(x) = \frac{2\sin(d\pi)}{\pi L1}x_1 - \frac{R1}{L1}x_2 + w_s x_3,$$
$$f_3(x) = \frac{2\cos(d\pi)}{\pi L1}x_1 - w_s x_2 - \frac{R1}{L1}x_3,$$
$$b_1 = -\frac{1}{C_0},$$
$$b_2 = -\frac{2}{\pi L1}.$$

The controller for the DAB-SST system is now represented as:

$$u_2 = i_N = C_o[f_1(x) + k_{v1}e_v + k_{v2}\int (e_v)\,dt], \quad (13)$$
$$u_1 = v_i = \frac{\pi L_t}{2}[f_3(x) + k_{I1}e_I + k_{I2}\int (e_I)\,dt], \quad (14)$$

with $(k_{i,j})$, the adjustment parameters, e_i the error, between the reference and the state variable, $(i = v, I)$ and $(j = 1, 2)$, respectively.

III. KALMAN-MPPT ARCHITECTURE

HW/SW co-design is conducted for complex algorithm implementations in a system on a chip (SoCs), which integrates the synergy of hardware and software intending to optimize design constraints such as performance and power of the implementation [42], [43]. The Xilinx Zynq Processing System consists of a SoC style integrated processing system (PS) and a programmable logic (PL) unit, providing an extensible and flexible SoC solution on a single chip [42].

In this study, the Kalman-MPPT is implemented with hardware PL unit and the dual-core ARM PS is used for the DAB-converter control as illustrated in Figure 3. The PL core is connected to the CPU dual-core ARM through the AXI bus.

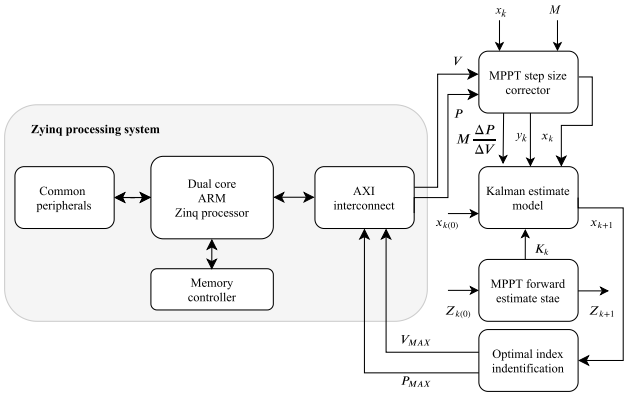

FIGURE 3. HW/SW co-design approach.

The strategy of the HW Kalman-MPPT unit consists of a well-balanced design in time and area. Piecewise polynomial approximation (PPA) technique is used for the complex operations of the Kalman-MPPT algorithm according to the block diagram of Figure 4.

The first stage of the design flow is the MPPT model. The dynamic variations of the PV array generate the output voltage and power for the corresponding level of temperature and irradiance. Remark that these variations are due to environmental fluctuations, which affect the behaviour of the SST-DAB converter. The slope of the PV curve is calculated with the reciprocal operation $\frac{\Delta P}{\Delta V}$ and a step size corrector M that is applied as one degree of freedom of the design. The updated MPPT value x_{k+1} is generated according to (1).

In the Kalman forward estimate operation, the functions $K_k = Z_k C^T (C Z_k C^T + R)^{-1}$ and $Z_{k+1} = (1 - K_k C) Z_k$ of (5) and (6) are implemented. These modules work together as a correction mechanism of the Kalman-MPPT algorithm. Finally, the integration of MPPT model with a Kalman Forward Estimate stage provide the reference voltage for the DAB converter.

The hardware architecture is employed considering the precision of 24 bits fixed-point operations, 4-bits integer and 20-bits decimal (i.e., for signed numbers in a two-complement format) and the clock frequency of 100 MHz.

A. MPPT STEP SIZE CORRECTOR

Figure 5 illustrates the parallel design of the MPPT step size corrector module. Two independent memory buffers receive and subtract the input data of the power and voltage from the PV panel. The reciprocal operation (divisor module) is implemented via the PPA technique as previously implemented in [36]. This FPGA implementation is different than other designs in the open literature; which avoid the implementation of computer arithmetic blocks.

For the divisor module design, the following methodology is applied: a) a non-uniform segmentation is defined to achieve the PPA technique. The segmentation is applied dividing the function domain in $m + 1$ segments located in power of two; i.e., $0, 1/2^{(m)}, \cdots, 1/2^3, 1/2^2, 1/2, 1$ [36], [37]. After that, a widely known range reduction strategy is applied, i.e., for a given function $f(x)$, with $a \leq x < b$, it is transformed into a new function $H(z) = W(f(x))$ for $0 \leq z < 1$; b) after defining the limits of segments of the PPA technique, this is necessary to evaluate the architecture performance via a bit-width optimization in order to identify the required number of bits of each fixed-point operand in the data-path. The last step will guarantee the desired SQNR. Therefore, after fixed-point and SQNR analysis, the divisor module architecture was configured with the following configuration parameters: a 24-bit data-path, 2-degree polynomials, and $m + 1 = 2^3 + 1 = 9$ non-uniform segments, which results in an SQNR equal to 55.6 dB for the divisor module. It is possible to improve the reached SQNR, however, this implies to consider the following: a) a higher number of segments in order to obtain a better representation of the approximated division function; b) an increment in the word length. Both cases convey to an increment in the used area resources in the designed architecture; i.e., memory

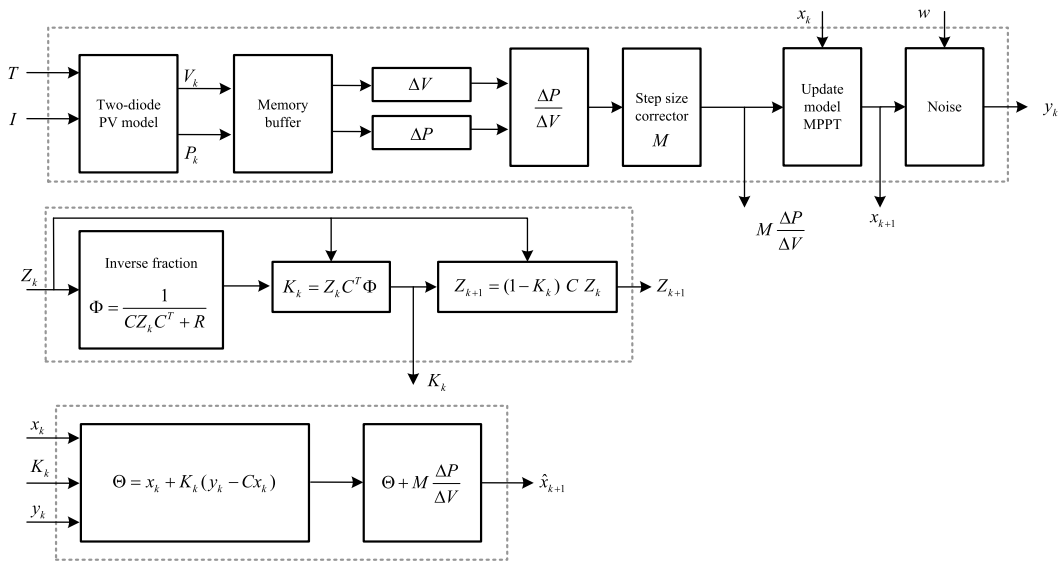

FIGURE 4. Block diagram of Kalman-MPPT architecture.

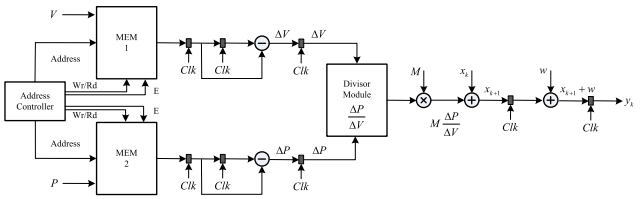

FIGURE 5. MPPT step size corrector module architecture.

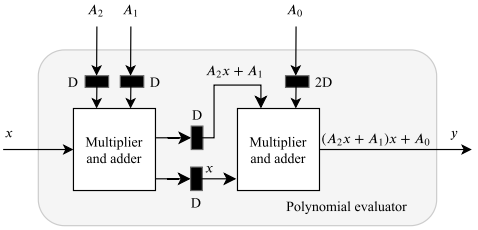

FIGURE 7. Polynomial evaluator architecture.

ROMs for allocating the polynomial coefficients, and an increase in the design data-path.

Figure 6 illustrates the general architecture of the divisor module to compute $\frac{1}{\Delta V}$; after that, it is multiplied by M and ΔP for obtaining $M\frac{\Delta P}{\Delta V}$.

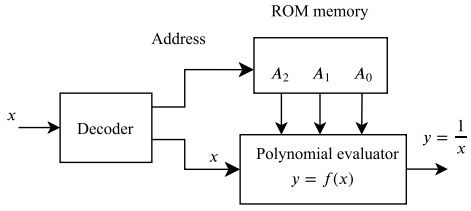

FIGURE 6. General architecture that uses a PPA technique with hierarchical segmentation method.

The PPA-based reciprocal architecture is addressed with a serial of multiply-accumulate operations. The resulting implementation is composed of a buffer memory block, which stores the coefficients of the 9 segments of the division curve labelled as ROM A0, A1 and A2; a decoder, or coefficient detector, used to identify the interval where the input value belongs; and the fixed-point arithmetic operations of the 2-degree, which evaluates the input value (considering a range reduction of [0, 1)) with the polynomial coefficients.

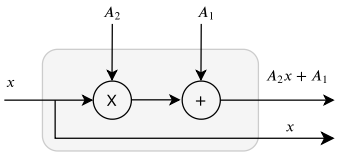

FIGURE 8. Multiplier and adder (MAC) architecture.

Figure 7 shows the 2-degree polynomial evaluator architecture and the multiply-accumulate (MAC) architecture is presented in Figure 8. The general architecture computes the division operation in only one cycle after an initial latency. Notice that, this is a full-custom architecture based on FPGA in contrast to CORDIC, IP cores, or DSP sequential implementations.

B. MPPT FORWARD ESTIMATE STATE

This stage implements an estimator that acts as a correction mechanism. The first step implements the inverse function $\Phi = (CZ_kC^T + R)^{-1}$, and then, the matrix-vector operations are carried out updating the value of Z_{k+1}. Due to the variables, C and R are scalar values, the inverse function is approximated with PPA-cells as another reciprocal function $\Phi = \frac{1}{CZ_kC^T + R}$.

This hardware architecture of the MPPT forward estimate state is shown in Figure 9 and it is implemented considering the parameters: word-length precision of 24 bits fixed-point operations for signed numbers in two-complement format, 9 segments and 2-degree polynomials.

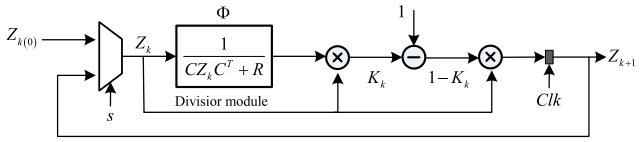

FIGURE 9. MPPT forward estimate state.

The Kalman estimate model consists in the adaptation of the MPPT and Kalman algorithms. The PPA-cells of the reciprocal functions and the arithmetic operations of the MPPT model are integrated into this architecture. This design improves the FPGA area resources results of previous studies reported in [19]–[21], [50] incorporating in the design PPA-cells and guarantying an accurate fixed-point evaluation by measuring the SQNR.

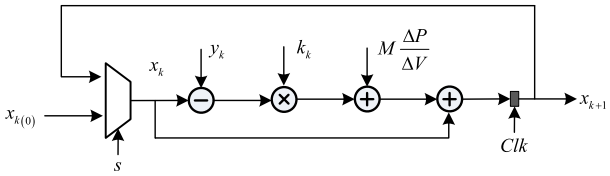

FIGURE 10. Kalman estimate model conceptualization.

Figure 10 shows the hardware implementation of the Kalman estimate modules with fixed-point operations of 24 bits and signed numbers in two-complement format. Finally, the index detector module generates the reference voltage and power values for the DAB converter controller.

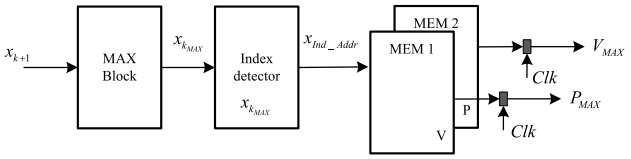

FIGURE 11. Optimal index identification.

IV. IMPLEMENTATION RESULTS

In this section, the results of the system and hardware level implementation of the Kalman-MPPT adapted in an SST-based DAB Converter are reported. In order to demonstrate the performance of the system, four test-case scenarios are conducted to analyze the Kalman-MPPT accuracy for DC microgrid applications. The area-time analysis of the HW core is also analyzed with the Xilinx Zybo Z7-10, which tightly integrates a dual-core ARM cortex-A9 processor with Xilinx-7 XC7Z010-1CLG400C FPGA Logic.

The test-case scenarios are designed to analyze the response of the Kalman-MPPT implementation with uncertain perturbations considered under controlled lab conditions and the integration for DC microgrids applications. In this sense, different irradiance and temperature levels were introduced in the implemented system via the use of an emulated PV array based on the two-diode model [44].

The test-case scenarios are implemented with the ARM Cortex-A9 processor and the Kalman-MPPT logic core in a HW/SW codesign. The Vivado Integrated Development Environment (IDE) and the Xilinx Zybo Z7-10 platform enable the validation of the co-design with experimental data used in the test-cases.

Figure 12 illustrates the test-case validation using the HW/SW codesign approach using off-line experimental data with the Vivado IDE environment, the hardware in the loop tool and the Xilinx Zybo Z7-10 platform. The temperature and irradiance radiation measurements were taken from the University of Quintana Roo meteorological station (DAVIS model Vantage PRO2) in Mexico.

A. TEST-SCENARIO 1: FIXED TEMPERATURE - VARIABLE IRRADIANCE

The first test-case scenario considers the fixed-point toolbox of Matlab-Simulink to transfer the evaluation data to the FPGA. A set of variations on irradiance levels that generate output voltage and power values on a PV array based on Multi-crystalline Kyocera KG200GT PV modules are emulated with a fixed temperature value of 25° C.

Figure 13 shows a comparative analysis of the response of the Kalman-MPPT implementation for solar irradiance variations. The output voltage and power of the Kalman-MPPT HW unit is compared with the response of the P&O method.

From the analysis of Figure 13, one can deduce that a reduction in irradiance levels reduce the PV current; therefore, the captured power is proportionally reduced, and consequently, the voltage for maximum power collection is also modified. However, it is worth to mention that Kalman-MPPT has a better response than P&O, as well as, a good convergence of the DAB closed-loop controller.

B. TEST-SCENARIO 2: FIXED IRRADIANCE - VARIABLE TEMPERATURE

The second test-case scenario considers the emulation of a data set of output voltage and power of the same Kyocera KG200GT PV array using a fixed irradiance of 1000 W/m^2 and variations on temperature levels.

Figure 14 shows the input temperature variations and the comparative results of the output voltage and power of the system without MPPT, the output of the HW Kalman-MPPT core compared with the P&O method and the DAB converter.

As presented in Figure 14, an increase in temperature levels causes a change in the voltage and power of the PV array. The Kalman-MPPT shows a better response than the system without Kalman and the P&O. Also, the closed-loop controller implementation had a good convergence at the output DAB converter. Notice that temperature changes have more impact in the system than irradiance variations.

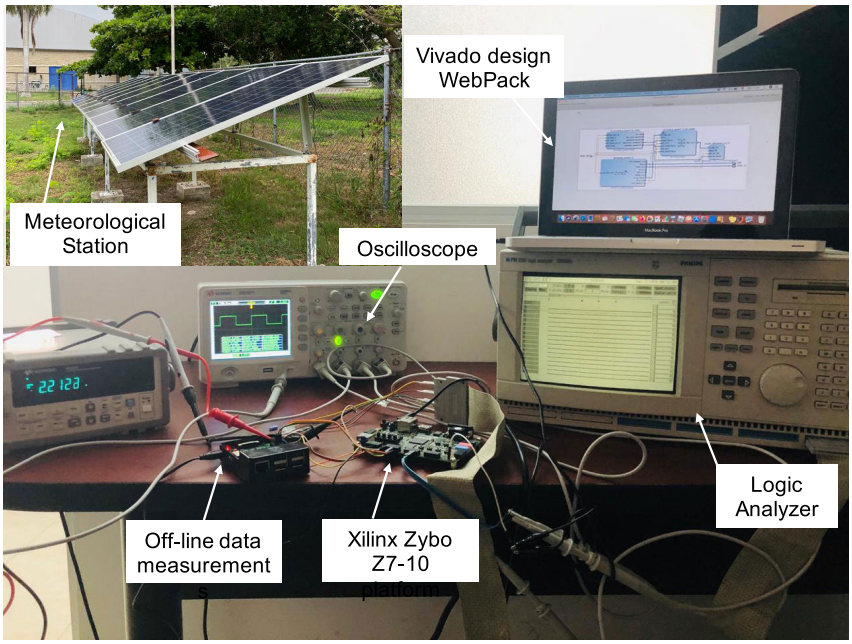

FIGURE 12. HW/SW codesign with the Kalman-MPPT as the coprocessor PL unit.

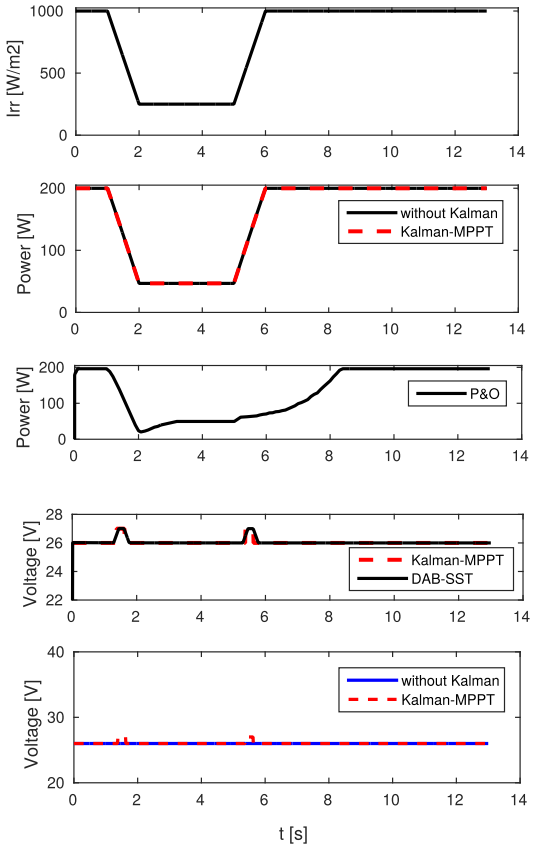

FIGURE 13. Results of Kalman-MPPT implementation for extreme irradiance disturbances.

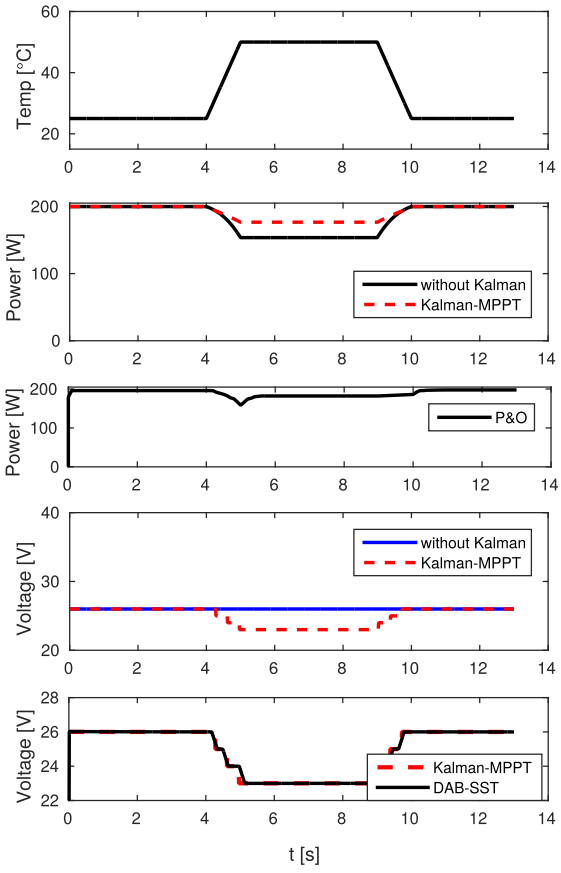

FIGURE 14. Results of Kalman-MPPT implementation for temperature variations.

C. TEST-SCENARIO 3: IRRADIANCE AND TEMPERATURE VARIATIONS

The third test-case scenario considers variations of irradiance and temperature levels at the same time. The data set is emulated achieving output voltage and power disturbances in the PV array. The input temperature and irradiance variations are illustrated in Figure 15. Also, the FPGA-based output

voltage and power of the Kalman-MPPT core, the system output without MPPT and the output DAB-SST converter are reported.

Despite extreme variations in temperature and irradiance, the Kalman-MPPT shows a better performance in comparison of the without Kalman system and P&O method as illustrated in Figure 15. Also, the closed-loop controller demonstrates a good integration with the DAB converter.

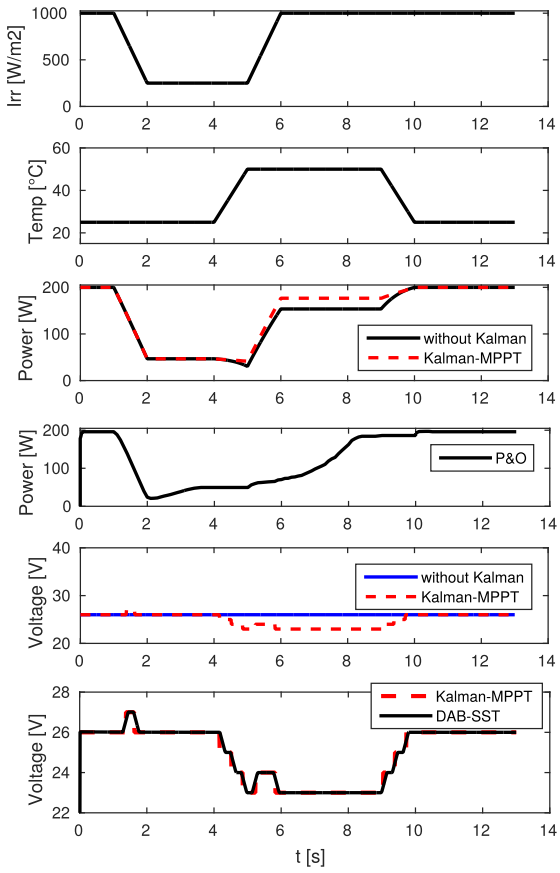

FIGURE 15. FPGA-based Kalman-MPPT results for temperature and irradiance variations.

D. TEST-SCENARIO 4: MEASUREMENTS OF IRRADIANCE AND TEMPERATURE VARIATION OF A WEATHER STATION

The last test-case scenario uses the temperature and irradiance radiation measurements of the meteorological station. The voltage and power measurements were applied off-line for this test. Figure 16 shows the output response with and without Kalman-MPPT.

The Kalman-MPPT implementation has been successfully adapted via the HW/SW co-design technique. The test-case scenarios demonstrate the performance achieved with our presented approach and the SST-based DAB converter.

E. ARCHITECTURE PERFORMANCE ANALYSIS

The results and performance of the Kalman-MPPT architecture integrated with the DAB-SST converter using the

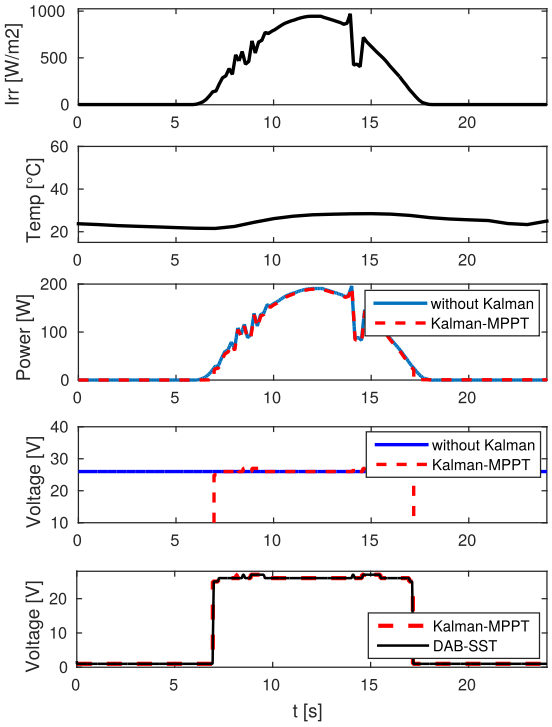

FIGURE 16. FPGA-based Kalman-MPPT results for temperature and irradiance measurements in University of Quintana Roo, Mexico.

HW/SW co-design are presented. The design is implemented using Verilog-HDL and synthesized with the Vivado design suite HL WebPack tool.

TABLE 2. Area performance analysis of Kalman-MPPT core.

Kalman MPPT	FPGA XC7Z010-1CLG400C HW word-lenght (bits)		
	24	28	32
Area resources			
Clock. freq. (MHz)	100	70	68.8
Slice registers	780	891	995
Slice LUTs	567	684	734
DSPs	18	36	36
Accuracy			
SQNR (dBs)	51.4	54	56

Table 2 summarizes the HW implementation results on the Xilinx Zybo Programmable System-on-Chip, which integrates a dual-core ARM Cortex-A9 processor and the FPGA-target XC7Z010-1CLG400C. The table analyzes the accuracy and area trade-off of the proposed architecture in terms of hardware resources and SQNR for different architecture's number of bits. The Optimize Instantiated Primitives Synthesis (balanced mode) option is used in the Xilinx synthesis tool. The analysis of Table 2 iindicates a well-balanced design of the Kalman-MPPT core for 24 bits and 55dB of SQNR. Note the hardware resource scalability analysis for

TABLE 3. Performance comparative analysis of the FPGA-based Kalman-MPPT core with state-of-art implementations.

FPGA analysis	[19] Kalman-MPPT	[21] Fuzzy-MPPT	[18] Reduced-EKalman	[50] Unscented-Kalman	Our design Kalman-MPPT
	Sign-function	*SysGen*	*Pipeline-design*	*IP-core*	*PPA*
Word-length (bits)	42	12	22	floating-point	24
Maximum frequency (MHz)	53	50	12.5	100	98.8
Latency (ns)	–	–	–	–	970
Slice Registers	20,770	12	5,996	7,688	780
Slice LUTs	15,773	1,336	20,823	5,764	567
DSP48	51	–	5	35	18

28- and 32-bits architectures with an increase in the accuracy of ≈4dB.

The time processing result is the following. The total execution time for Kalman-MPPT operation is equal to 1.75μs with a latency of 970 ns.

Table 3 shows a comparative analysis of our proposed design with other similar state-of-art FPGA designs. Note the design technique used in each reference for the complex analysis of the arithmetic operations. For example, reference [19] based its Kalman model design on the *sign* function. [21] uses IP-core functions of Xilinx-Matlab/Simulink and [20] implements a pipelined technique. However, the presented results demonstrate that the PPA technique achieved fewer hardware resources than the other state-of-art implementations.

To test our design, the Kalman-MPPT is adapted to a DAB-SST converter using the HW/SW co-design technique. In the experiment, the Kalman-MPPT is employed as hardware coprocessor and the Cortex-A9 ARM processor is used for the DAB-SST closed-loop controller. This reduces computational resources and space area enabling a low cost FPGA implementation. The whole co-design is implemented in the Xilinx Zybo platform.

Finally, the time analysis of the co-design is presented in (15), as follows:

$$t_{co-design} = t_{AXI} + t_{Kalman-MPPT} + t_{DAB-SST}, \qquad (15)$$

where $t_{co-design}$ is the total time for the Kalman-MPPT adapted in the DAB-SST, t_{AXI} is the intercommunication time between the ARM and FPGA device, $t_{Kalman-MPPT}$ is the processing time of the Kalman-MPPT using PPA technique, and $t_{DAB-SST}$ is the processing time of the sequential closed-loop controller in the dual-core ARM processor of the DAB-SST control.

The resulting performance for the implementation is t_{AXI} equal to 0.337 ms, $t_{Kalman-MPPT} = 1.75\mu$s, and $t_{DAB-SST} =$ 3.57 ms. Therefore, the total time of the co-design implementation is 3.9087 ms.

The presented results demonstrate a well-balanced HW design implementation of the Kalman-MPPT integrated in the DAB-SST converter. The comparative analysis presented in the test-case scenarios show better tracking responses than the reference P&O method with a low-cost and low-area FPGA implementation.

V. DISCUSSION

Hardware implementation of complex arithmetic operations is expensive in FPGA resources. The current literature review in introduction section and the Kalman-MPPT model presented in Section 2.1 show the complexity of the arithmetic operations. Particularly, the reciprocal operations in (4) and (5) are essential for the Kalman-MPPT, however, the implementation is computationally costly demanding a lot of FPGA resources. The integration of PPA and HW/SW co-design techniques are used as described in this study for efficient incorporation of PV renewable energy arrays with DAB-SST converters. The HW design methodology described in Section 3.1 includes a bit-width optimization strategy to identify the required number of bits of the fixed-point design. Notice that for a well-balanced area-accuracy design, it is necessary to apply a non-uniform hierarchical segmentation to the PPA design. Also, floating-point implementations, such as most of the IP-cores, require a long execution time and large area resources than full-custom specific fixed-point architectures.

As can be seen in the comparative area performance analysis of Table 3, our proposed Kalman-MPPT design has fewer hardware resources than the FPGA implementations of [18], [19], [21], [50]. The number of Slice registers, Slice LUTs and DSP48 FPGA elements used in the reference works in the comparative table suggest the selection of expensive FPGA or DSP devices. In this paper, our proposed architecture offers a low-cost, rapid prototyping and a well-balanced FPGA design with fewer hardware resource instead of traditional implementations with digital controllers, such as the 1202-dSPace [51]. This design is suitable to be implemented in a low-cost QMTECH Xilinx FPGA Spartan6 XC6SLX16 Spartan-6 of less than 20 USD. The Kalman-MPPT logic unit represents an interesting solution for DC microgrids. The FPGA-based rapid prototyping with the HW/SW co-design is a low-cost and low-area solution but with a high-accuracy performance, in comparison of other state-of-art implementations.

VI. CONCLUSION

DC microgrid systems are considered a key technology for the implementation of future electric power distribution systems. In this study, an FPGA Kalman-MPPT implementation

was implemented and adapted into a DAB-SST converter. The proposal uses the HW/SW codesign, integrating the Kalman-MPPT logic core and a closed-loop PID controller in the dual-core ARM processor on the Xilinx Zybo platform.

The Kalman-MPPT logic core was implemented using a hardware architecture that requires the reciprocal operation computed by a non-uniform piecewise polynomial approximation. The results show that the hardware resources are significantly reduced in comparison with state-of-art FPGA implementations. The HW synthesis reveals an achieved SQNR of 52 dB with 24 bits word-length, with 780 Slice registers, 567 Slice LUTs and 18 DSP48 hardware resources. The proposed logic core implementation can be used as a coprocessor unit in a HW/SW codesign paradigm for many DC microgrid applications.

Finally, the Kalman-MPPT implementation integrated with a DAB converter can improve the actual electric distribution system in many countries, representing an important approach to route efficiently renewable energy in DC microgrids.

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