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From MTJ Device to Hybrid CMOS/MTJ Circuits: A Review

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ABSTRACT Spintronics is one of the growing research areas which has the capability to overcome the issues of static power dissipation and volatility suffered by the complementary metal-oxide-semiconductor (CMOS) industry. Magnetic tunnel junction (MTJ), one of the prominent spintronic devices, is not only used to develop the fully non-volatile-logic (NV-L) but combines magnetism and electronics to develop next-generation NV-memory (NV-M) and hybrid CMOS/MTJ circuits. To be specific towards hybrid CMOS/MTJ circuits, the fabrication of first hybrid full-adder in 2009, fabrication of MTJ based 240-tile NV-field programmable gate array (NV-FPGA) chip in 2013, fabrication of a 3000-6-input-LUTs based NV-FPGA chip in 2015, fabrication of MTJ based NV-logic-in-memory-large scale integration (NV-LIM-LSI) in 2017 and recently the fabrication of a full hybrid magnetic/CMOS System on Chip (SoC) under EU GREAT Project in 2019 has strengthened the belief and motivated the researcher to be continued in this domain. This review article aims to provide the complete design flow of hybrid CMOS/MTJ circuits developed using one of the fab compatible MTJ spintronic devices and its integration with conventional CMOS logic. The broad coverage of the article is MTJ construction, its switching mechanisms, a brief history of various compact models, reliability issues, and the concept of logic-in-memory (LIM) architecture. Finally, the article concludes with the challenges and future prospects of hybrid CMOS/MTJ circuits, which will motivate people in academia to cultivate research in this domain and industry to realize the prototype for a wide range of potential applications.

INDEX TERMS MTJ, spintronic, CMOS/MTJ, LIM, iMTJ, pMTJ.

I. INTRODUCTION

As the technology node shrinks below 45 nm, power dissipation and performance become two major concerns for the next generation computing system [1]. The expected gate length in the future is reported to be ≈5 nm by International Technology Roadmap for Semiconductors (ITRS, 2013) [2]; because of that, the off-leakage current will be too high for the entire chip. There are various techniques to reduce the power at the circuit level, in which double gate-metal oxide semiconductor field-effect transistor (DG-MOSFET), fin-field effect transistor (fin-FET), and Si-nanowire MOSFET are the most promising one [3]. Carbon nanotube field-effect transistor (CNTFET) is another feasible nano-device similar in structure and successor of complementary metal-oxide-semiconductor (CMOS) technology. It has higher performance, transconductance, and lower power consumption than conventional CMOS technology. Many logics have been developed using these methods [4], but all the logic discussed above suffer volatility issues. Similar concern related to power dissipation was also reported in a recent report by the semiconductor industry association [5] by stating that if we follow the same way of computing by bit '0' and '1' (which need absolute minimum energy suggested by Landauer [6] in IBM Lab in 1961), we will not have the capability to power all the machines around the globe by 2040. To overcome, industries are looking for some alternate way of energy-efficient computing technique that will replace the classical computers (limited by minimum energy to perform one operation) with quantum computers. Spintronics is one of the emerging areas that have the potential to change the future of electronics beyond CMOS technology [7]–[10]. It is one of the growing technology which can reduce the heat dissipation of integrated circuit (IC) significantly. In charge based device

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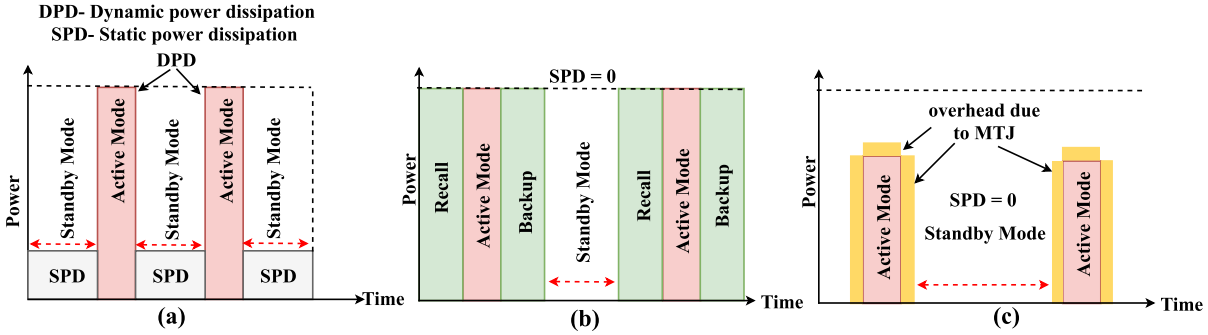


FIGURE 1. (a) An example of conventional CMOS-IC or SRAM cache dissipating both dynamic and static power without power gating. (b) By applying power gating, SPD = 0 in standby mode, but two additional operations data "Backup" and "Recall" are added before "switching-off" and "switching-on" the power, respectively. Switching-off the power is not allowed in CMOS logic due to their volatile nature. Further, this strategy also increases the delay due to the time spent in storing and recalling it before "switch-off" to "switch-on". (c) In hybrid CMOS/MTJ circuits, as the power is switched off, data is being stored in MTJ and is readily available for logic operation as soon as the power is switched on. DPD and delay are significantly reduced, and almost zero SPD is noted in standby mode. A small overhead due to MTJ can be observed. Reproduced using refs. [28]–[30].

to switch from logic '0' to logic '1', the magnitude of the charge must be changed in the active region of the device due to which current flows from drain (D) to source (S). It is not possible with charge-based electronics to reduce the power (or heat) dissipation significantly because the charge is a scalar quantity, and the presence or absence of charge gives logic '1' or logic '0' respectively. Spin, unlike charge, is a pseudovector quantity which has a fixed magnitude of $\hbar/2$ with a variable polarization, where $\hbar$ is the reduced Planck's constant. If an electron is placed in a magnetic field, it can have many states, but for encoding digital information, only two states, '1' and '0' are needed. These states can be achieved with a polarization parallel (P) and antiparallel (AP) to the magnetic field, which can encode logic '1' and logic '0' respectively. In that case, switching is accomplished by flipping the polarization of spin without any change in the flow of current, as that is the case in hybrid spintronics. This may result in significant energy savings. However, there is still some energy dissipated in flipping the spin, but it will be of the order of $g\mu_B B$, where g is the Lande factor, μ_B is the Bohr magneton, and B is the magnetic field required to keep the spin polarization bi-stable. The term $g\mu_B B$, can be reduced by lowering B, but it may cause more random bit flips. However, bit-flip errors can be handled by error-correcting codes up to a certain extent [11], [12].

Spin logics are the emerging ones, which improves battery life by consuming less power from portable devices to large data centers [13] and are non-volatile (NV) in nature. MTJ nanopillar is an important spintronic device used for logic and memory applications, which combines magnetism and electronics and promises high read/write speed, nonvolatility, infinite endurance, etc. [8], [10], [14]. It is a promising candidate to develop NV memory and hybrid logic (CMOS and MTJ) [15]–[17] due to its quality of low power consumption, less area, faster speed, and easy integration at the top of CMOS [18]–[20]. MTJs developed using CoFeB(top electrode)/MgO(barrier)/CoFeB(bottom electrode) structure has a wide range of applications, especially in magnetic random access memory (MRAM) due to its high tunnel magnetoresistance (TMR) and the reasonable range of resistance area (RA) product. Much research is continuously progressing on the use of MTJ to develop the NV-STT (spin-transfer torque)-MRAM memory to become the universal memory technology [21]–[27]. Power gating is also one of the techniques used in CMOS technology to reduce the static power dissipation when the circuit is not used for a longer period. Fig. 1 (a) represents the power dissipated either in conventional CMOS-IC or static random access memory (SRAM)-cache. Here, dynamic power dissipation (DPD) is in active mode, and static power dissipation (SPD) is in standby mode without power gating [28]–[30].

A part of the static power can be reduced by applying the power gating technique, but it requires two operations, data ''Backup'' and data ''Recall'' (Fig. 1 (b)). Due to the volatile nature of CMOS circuits, directly ''switching-off'' the power in CMOS circuits is strictly prohibited. This arrangement needs temporarily storing the data somewhere during backup and recalling it again while wake-up, which introduces a significant delay. In contrast, hybrid CMOS/MTJ circuit developed using LIM, the power can be easily removed (or the power is switched off) in an idle state, and there is no static power dissipation in standby mode [31], [32]. However, due to the physical property of MTJ, there is a small overhead in dissipated power (Fig. 1 (c)). It can be noticed that, as soon as the power is switched off/on, the backup and recall operations are not performed in a hybrid circuit, so no external memory is required. Due to the NV nature of the MTJ, stored data will be immediately available for logic operations [29], [30]. As a result, the hybrid CMOS/MTJ circuits developed using LIM structure not only improve the performance and power dissipation but also are reliable due to the large radiation hardening capability of the circuit [33], [34]. However, due to stochastic variation, MTJ suffers switching errors and may lead to a malfunction in hybrid

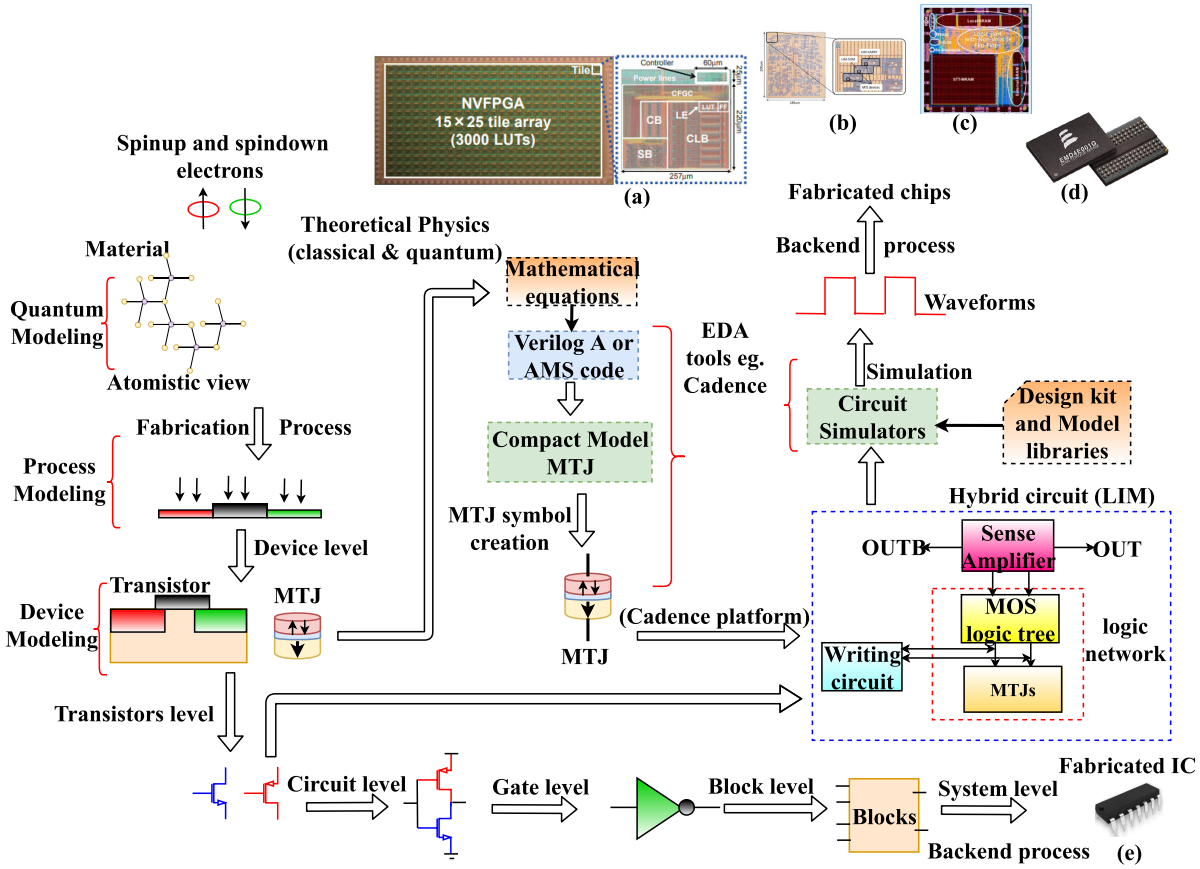


FIGURE 2. Design cycle from material (the atomistic view) to the system level with various abstraction levels and the simulation framework has been shown. An industry-standard EDA tool, e.g., Cadence platform, can be used for both front-end and back-end parts of the design flow. Verilog-A/AMS language is used for developing the physics-based compact model, which is further used to integrate MTJ symbols with MOS logics to develop the hybrid LIM structures. Process design kit and model library will be used in the Analog design environment (ADE) of the Cadence tool for circuit simulation. Figs. (a), (b), (c), (d), and (e) represent the fabricated test chips for hybrid CMOS/MTJ circuits and CMOS only circuits, respectively. (a) Die photo of NV-FPGA test chip with 3000-6-input-lookup table (LUT), fabricated using 90 nm CMOS/75 nm pMTJ technologies [37]. (b) Micrograph of fabricated processing elements (LIM carry, LIM sum, and MTJ devices) [38]. (c) First, SoC of its kind developed and taped out at Israel-based Tower Jazz in 2018, under the EU GREAT project by SPINTECH (Spintronics IC Design team) with other project partners. Both Analog and digital blocks are embedded on the same die using hybrid CMOS/MTJ circuits and are known as multifunctional standard stack (MSS) [39], [40]. (d) 1 Gb STT-MRAM (ST-DDR4) manufactured by Everspin (EMD4E001G) [41]. (e) A simple DIP-IC, 74HC04 hex inverter CMOS IC [42].

CMOS/MTJ circuits [35], [36]. Thus, hybrid CMOS/MTJ circuits have enormous potential to overcome the issues raised in CMOS technology. Fig. 2 shows the framework of the design cycle/or the steps involved from the atomistic view of material used in MTJ, front end view of the design, equivalent backend process, and finally, the end product in terms of various fabricated ICs. Figs. 2 (a, b, c, d) and (e) are the recently fabricated ICs of hybrid CMOS/MTJ circuits [37]–[41] and general-purpose dual-in-package (DIP) IC of the inverter [42], respectively.

The organization of the paper is as follows: After a brief introduction, we start with the section "Background," which consists of the subsections "MTJ construction," "Interpretation of TMR," and "Interpretation of Magnetic Anisotropy". In the "MTJ construction" subsection, the use of ferromagnetic (FM) materials is discussed by the Energy level (E-K) diagram using the Stoner-Wohlfarth (S-W) model. TMR ratio, an essential characteristic of MTJ, is discussed while developing the hybrid circuits. Magnetic anisotropy (MA), an inherent property of the MTJ, is explored to understand the difference between perpendicular magnetic anisotropy (PMA) and in-plane magnetic anisotropy (IPA). In section "MTJ Switching mechanisms," various switching mechanisms are discussed. Due to its commercialization point of view, the STT switching mechanism has been explored broadly based on theoretical and experimental results. The basic Landau–Lifshitz–Gilbert (LLG) equation, which covers the magnetization dynamics of the free layer (FL), is revisited. Further, the Landau–Lifshitz–Gilbert-Slonczewski (LLGS) equation was modified by Slonczewski (due to spin-polarized electrons in the LLG equation) is discussed. "A brief history of MTJ device modeling" is presented in the next section. These models work as a reference for the circuit design engineer. To build the hybrid CMOS/MTJ circuits, a compact model of the MTJ is needed, which can be further integrated with MOS

transistors (Fig. 2) using any electronic design automation (EDA) tools. This study will help the reader be familiar and updated with various MTJ models reported in the literature from time to time. We have also discussed the shortcomings of various model timely reported in the literature. Section ''Reliability of hybrid CMOS/MTJ circuits'' explores the reliability of MTJ and the hybrid CMOS/MTJ circuit. We start with a traditional bathtub curve to explain the failure rate of a CMOS IC. A thorough MTJ model, which includes all the reliability issues, is still missing in the literature. Time-dependent dielectric breakdown (TDDB), one of the important reliability issues, has been discussed using both intrinsic and extrinsic breakdown mechanisms. Further, the pinhole growth extrinsic mechanism is reviewed using the energy band diagram. ''Hybrid CMOS/MTJ circuits'' is the most important section, where we discussed the way to design the hybrid circuits using MOS transistors and MTJs. The idea of logic-in-memory (LIM) is preferred over traditional von-Neumann architecture, which suffers the large interconnect delay between logic and memory block. The three main components of the LIM structure, i.e., the read circuit, write circuit, and logic network, are explained. Finally, ''Summary and outlook'' of the review article are presented. To understand the effect of various pulses used in voltage-controlled magnetic anisotropy (VCMA) switching mechanism, we simulated the VCMA-MTJ model, and the results are analyzed in Appendix A. Appendix B representing the design, working, and simulation of three basic LIM hybrid circuits of two input NV-NAND/AND, NV-NOR/OR and NV-XNOR/XOR using STT-PMA-MTJ model have also been appended for convenience.

As the field of spintronics itself is in the growing stage, this review cannot be the final word for the hybrid CMOS/MTJ circuit. Instead, it is a comprehensive reference for those who like to explore more in this research area. Due to the broad coverage of this article, it not only binds the researcher of the various interdisciplinary area but also can be used as a tutorial by the early-stage researcher to start their research at the circuit level. However, on the other side, due to its broad coverage and fast-growing stage worldwide, some research publications may be inevitably missed.

II. BACKGROUND

This section recollects and highlights the necessary information of MTJ to build the background for developing the hybrid circuits. Here, we explore the MTJ construction, type of material used in MTJ and their energy band (E-K) diagram, Interpretation of tunneling effect, and the types of MA.

A. MTJ CONSTRUCTION

MTJ is a multilayer structure comprising of an ultra-thin insulating layer (also known as a barrier layer) sandwiched between two FM layers. In one of the FM layers, the magnetic orientation is fixed and is called a fixed/reference layer (RL), while another FM layer has a magnetic orientation, which can be either P or AP to the RL and is called FL. The magnetic orientation of FL can be altered by the application of an external magnetic field or application of suitable current/voltage in a particular direction. The process of switching the relative magnetization of the FL from P to AP state or vice versa is called MTJ writing/switching, which offers hysteresis behavior. When the magnetic orientation of the FL and RL are parallel, then the resistance offered by the device for the flow of read current is less, and it is denoted by parallel resistance (RP). Whereas, if the magnetic orientation of the FL is opposite to that of the RL, the device offers more resistance to the flow of read current, and therefore it is in the high resistance state and denoted by antiparallel resistance (RAP). Figs. 3 (a, b, c, d) represents the in-plane MTJ (iMTJ), perpendicular MTJ (pMTJ), typical R-H curve of pMTJ [43], and energy band diagram of pMTJ [44], respectively. Further explanations are done using pMTJ device. Here, pMTJ is assumed to be coded as '1' and '0' for RP and RAP states, respectively. So, the resistance variation of these two states of the device can be represented by the TMR ratio using Eq. 1 [7], [8],

$$TMR = \frac{R_{AP} - R_P}{R_P} = \frac{G_P - G_{AP}}{G_{AP}} \tag{1}$$

Here G_{AP} and G_P are the conductance in AP and P state, respectively. Tunneling between FM films was first observed by Jullière in 1975 using Fe/Ge/Co multilayer [45]. Due to the limitation of the experiment, less attention was paid, and there was no significant high TMR reported during the next 20 years [46]. Initially, TMR was first reported at room temperature by Moodera *et al.* and Miyazaki *et al.* in 1995 individually using the AlOx barrier [47], [48], which opened a path not only for NV-memories (NV-Ms) but also for the development of NV hybrid CMOS/MTJ circuits. The size, shape, thickness, and the material used in the barrier and the stacking layers while developing the MTJ decides its TMR ratio. A high TMR is one of the key parameters to design the NV hybrid circuits and NV-M.

Large TMR, around the range of 50% to 200%, is sufficient to differentiate the voltage difference between the logic states '0' and '1' for hybrid circuits and can be used for various applications. Recently high TMR ratio is obtained by fabricating both iMTJ and pMTJ for the optimal thickness of 1.6 nm of FL [49]. Both the crystalline MgO and amorphous AlOx insulating barrier based MTJ have been reported in the literature. The maximum value of TMR is achieved by 80% by using the AlOx barrier at room temperature using CoFeB material as FL and RL [46], [50]. Fig. 4 represents the TMR ratio plotted at room temperature for various MTJ structures developed using both AlOx and MgO barrier [47], [49], [50], [52]–[69]. Significant growth in TMR for MgO-based MTJ is observed during the year 2001 to 2008. It can also be noticed that MgO-based MTJ leads to higher TMR as compared to the AlOx barrier [51]–[53]. It is due to the crystalline structure of the MgO barrier enabling coherent tunneling over the AlOx amorphous barrier. Further, at low temperature, in MgO-based MTJ, a gradual increase

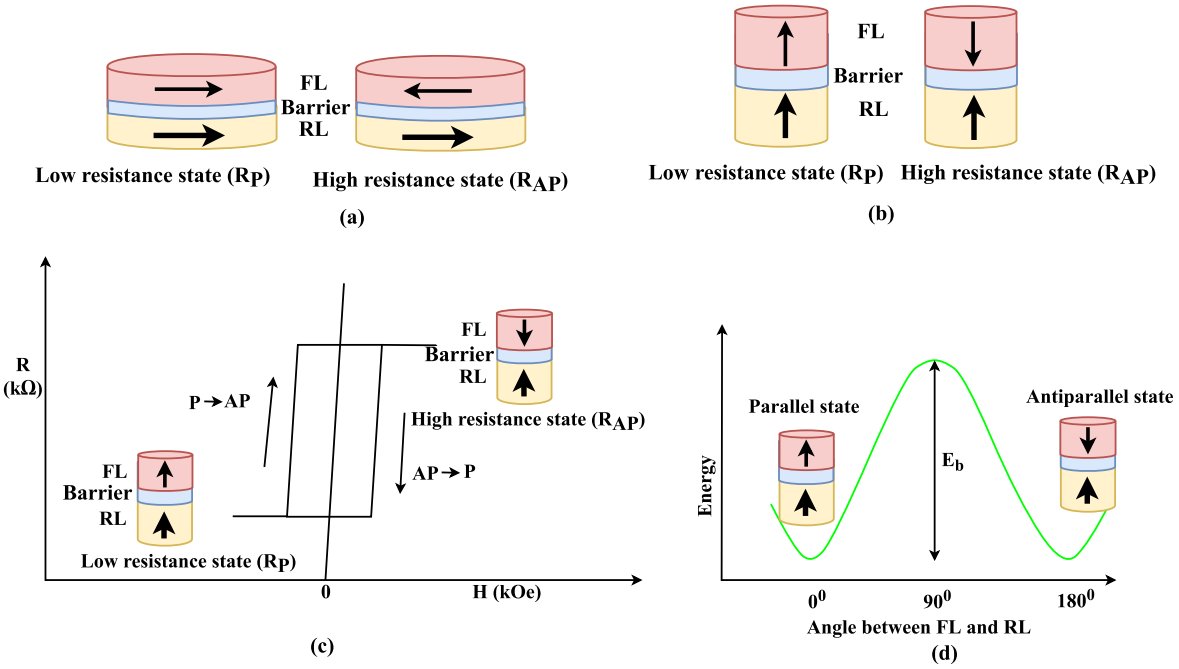


FIGURE 3. (a), (b) Front view of MTJ switching from P state to AP state, and vice versa for iMTJ and pMTJ, respectively. (c) R-H curve, here R_P represents the low resistance state, while R_{AP} represents the high resistance state due to the TMR effect of pMTJ [43]. (d) An energy barrier separates p and AP states of pMTJ (E_b). The barrier height decides the stability of stable states of pMTJ [44].

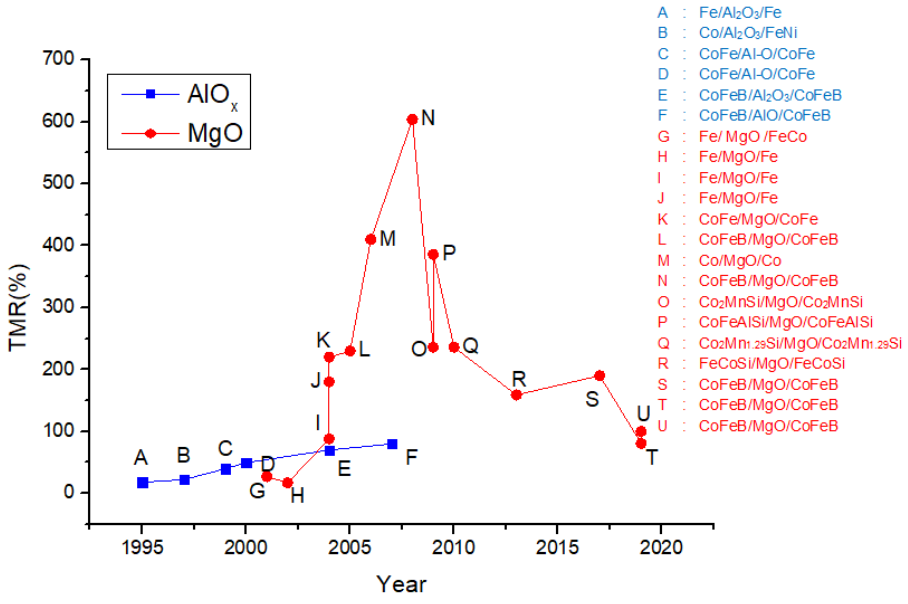


FIGURE 4. TMR ratio plotted for the refs. [47], [49], [50], [52]–[69] at room temperature for various MTJ structures developed using both AlOx and MgO barrier with a different FL and RL. Initially, the MTJ was reported using the AlOx barrier [47], [50], [57]–[60], and the highest TMR ratio was reported 80% during the year 2007 [50]. Significant growth can be observed in the TMR ratio of MgO-based MTJ using Refs. [52], [53], [56], [61]–[65] compared to AlOx during the year 2001 to 2008. Refs. [49], [68] are the recent development of MTJ with MgO barrier on a flexible substrate, which has opened the way to its use for future flexible spintronic devices.

in TMR was observed. It was reported 1135 % at 4.2K by Ishikawa *et al.* [54] and Yamamoto *et al.* [55] while 1144% at 5K temperature by Ikeda *et al.* [56]. To understand the charge particle behavior in metal, first, we set up the relation between energy and density of states of metal. The spin polarization is calculated theoretically by the given relation [8], [70], [71],

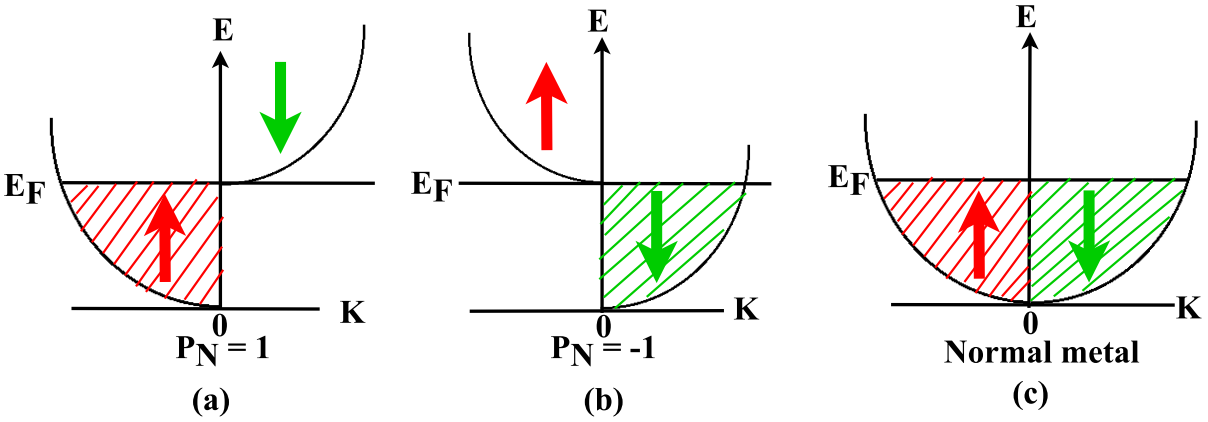


FIGURE 5. Energy level (E-K) diagram using S-W model, (a) if $N_{\downarrow} = 0$, $P_N = 1$ means the material is 100% up spin-polarized. (b) While for $N_{\uparrow} = 0$ the material is 100% down spin-polarized. (c) In normal metal both $N_{\uparrow}$ and $N_{\downarrow}$ are equal [8].

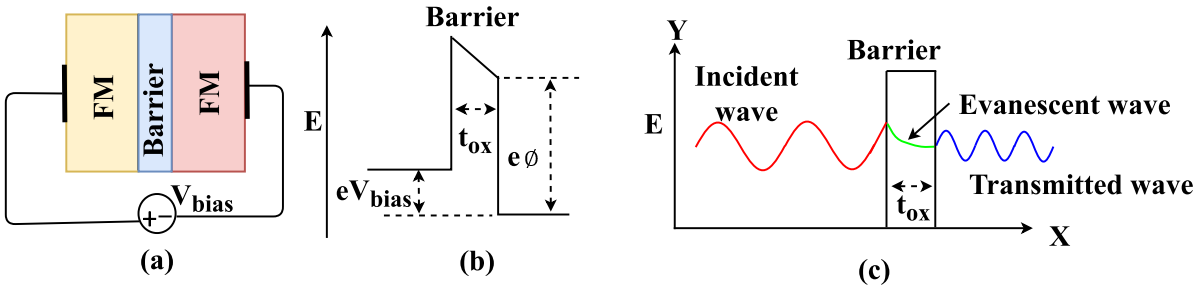


FIGURE 6. (a) Schematic of MTJ with applied voltage V_{bias}, (b) its energy band diagram (c), and the tunneling of the electrons due to its wave nature. Assume the electrons are traveling to the x-axis, which is represented by an incident electrons wave, and if the barrier height is greater than the energy of the electrons, electrons will tunnel into the barrier. Electrons wave become evanescent inside the barrier, and its amplitude exponentially decays into the barrier [72].

as shown in Eq. (2),

$$P_N = \frac{N_{\uparrow} - N_{\downarrow}}{N_{\uparrow} + N_{\downarrow}} \tag{2}$$

Here $N_{\uparrow}$ and $N_{\downarrow}$ are the up and down spins, respectively. When $N_{\downarrow} = 0$, $P_N = 1$ (Fig. 5 (a) means the only majority up spins are there, and the spin polarization is 100%, but it is difficult to achieve for spintronic devices during realization. Such materials are known as FM half metals or heusler alloys. If $N_{\uparrow} = 0$; $P_N = -1$ (Fig. 5 (b)) and for $N_{\downarrow} = N_{\uparrow}$; $P_N = 0$ (Fig. 5 (c)), only for paramagnetic or normal metal. When the number of up spins and down spins are not equal, the magnetism can influence electrical transport. This idea helped the researcher to choose FM material over normal metal for the formation of the top and bottom layers of MTJ.

The ratio of P and AP resistance can be written in terms of spin polarization of FM layers as [7],

$$\frac{R_P}{R_{AP}} = \frac{1 - P_1P_2}{1 + P_1P_2}, \quad \text{here} \begin{cases} R_P = \dfrac{2}{1 + P_1P_2} \\ R_{AP} = \dfrac{2}{1 - P_1P_2} \end{cases} \tag{3}$$

P_1 and P_2 are the spin polarizations of two FM layers, which can be calculated using Eq. 2. Further, the TMR effect strongly depends on spin polarization and can be obtained using Eqs. 1 and 3 by the Julliere's model [7], [45],

$$TMR = \frac{2P_1P_2}{1 - P_1P_2}. \tag{4}$$

TMR is a quantum mechanical effect and is a consequence of spin-dependent tunneling. Fig. 6(a) shows the applied V_{bias} across the two terminal of the MTJ, and Fig. 6(b) represents the corresponding energy band diagram [72]. The electrons tunneling phenomena are due to the wave nature of the electrons and has been shown in Fig. 6 (c). If the barrier is thin enough, evanescent wave amplitude does not vanish perfectly; rather, it re-emerges with residual amplitude and forms the transmitted wave. Consequently, the transmitted wave with a decrease in amplitude propagates along the x-axis. The electrical conductance of the junction can be represented by the electrons wave function in the evanescent state of the tunneling electrons in the barrier. The tunneling electrons across the barrier has an exponential dependency on barrier thickness (t_{ox}) (Fig.6 (b)). A direct relation of the tunneling current density with t_{ox}, V_{bias}, and average tunnel barrier height (Ø) is theoretically reported by Simmons in 1963 [73].

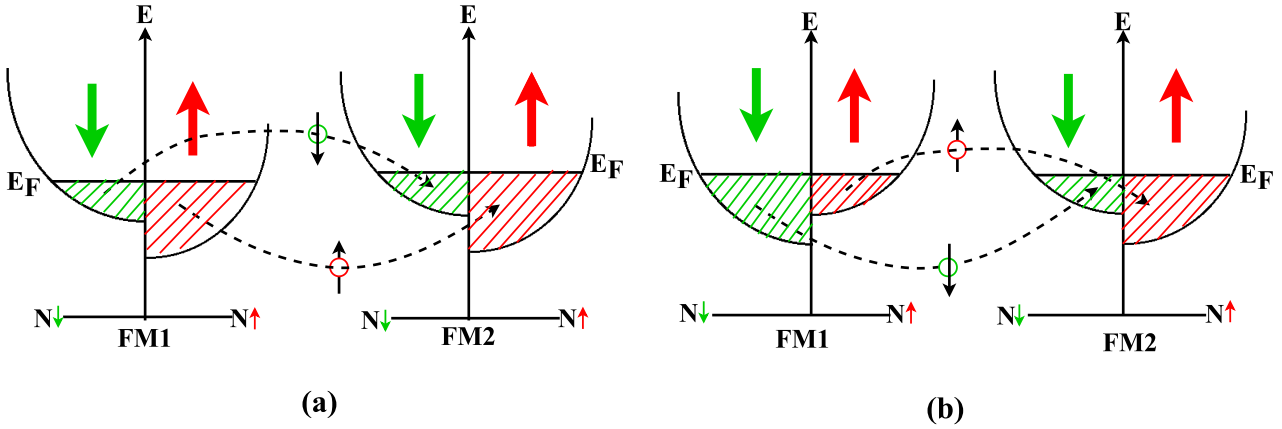


FIGURE 7. Interpretation of TMR effect pictured as in ref. [17]. (a) Represents the tunneling of electrons in P state from FM1 to FM2 layer while (b) represents the tunneling of electrons in AP state from FM1 to FM2 layer. For convenience, the barrier has not been shown in both figures.

B. INTERPRETATION OF TMR

Electrons with different spin can tunnel from one ferromagnetic layer (FM1) to another ferromagnetic layer (FM2) through the barrier layer (or non-conducting thin insulating layer) provided there is the availability of states with the same spin orientation.The expression of parallel conductance (G_P) in P state is,

$$G_P = N_{\downarrow}.N_{\downarrow} + N_{\uparrow}.N_{\uparrow} \tag{5}$$

Here the first term of Eq. 5 is obtained by minority down spin ($N_{\downarrow}$) electrons in FM1 layer and minority down spin ($N_{\downarrow}$) electrons in FM2 layer, while the second term is obtained from majority up spin ($N_{\uparrow}$) electrons in FM1 layer and majority up spin ($N_{\uparrow}$) electrons in the FM2 layer. It can be observed that in the P state (Fig. 7 (a) the majority spin up ($N_{\uparrow}$) electrons and the minority spin down ($N_{\downarrow}$) electrons from FM1 can easily tunnel to the FM2 layer with majority spin up ($N_{\uparrow}$) and minority spin down ($N_{\downarrow}$) electrons. It will cause high conductance or low resistance. Whereas in AP state majority spin down ($N_{\downarrow}$) electrons and minority spin up ($N_{\uparrow}$) electrons of FM1 tunnel across the barrier with difficulty to fill minority spin down ($N_{\downarrow}$) and majority spin up ($N_{\uparrow}$) electrons of the FM2 layer. It will cause the low conductance or large resistance. Similarly, the expression of antiparallel conductance (G_{AP}) in AP state can be written as,

$$G_{AP} = N_{\downarrow}.N_{\uparrow} + N_{\uparrow}.N_{\downarrow}. \tag{6}$$

Here the first term of Eq. 6 is obtained by majority spin down ($N_{\downarrow}$) electrons in FM1 layer and majority spin up ($N_{\uparrow}$) electrons in FM2 layer, while the second term is obtained from minority spin up ($N_{\uparrow}$) electrons in FM1 layer and minority spin ($N_{\downarrow}$) down electrons in the FM2 layer (Fig. 7 (b)). Thus in the R_P state, electrons will experience a low resistance compared to the R_{AP} state. Hence, it can be concluded from Fig. 7 that the TMR effect strongly depends on the spin polarization. Further spin conductance ratio (SCR) can be calculated from Eqs. 5 and 6 [7], [8],

$$SCR = \frac{G_P - G_{AP}}{G_P + G_{AP}}. \tag{7}$$

The conductance of the junctions in the parallel and antiparallel configurations can be represented by $G_P = \frac{1}{R_p}$ and $G_{AP} = \frac{1}{R_{Ap}}$. Similarly, Junction magnetoresistance ratio (JMR) is another useful quantity and can be written as Eq. 8 [7], [8], [45],

$$JMR = \frac{G_P - G_{AP}}{G_P} = \frac{R_{Ap} - R_p}{R_{Ap}}. \tag{8}$$

It can be observed from the above equations that TMR, JMR, and SCR represent three different magnetoresistance ratios to characterize the difference between R_p and R_{Ap} resistance.

C. INTERPRETATION OF MA

It is the directional dependence of the magnetic properties of magnetic materials. Principally, In the absence of the applied magnetic field, the magnetic moment of magnetically anisotropic materials will tend to align along easy-axis while a magnetic isotropic material has no preferred direction for its magnetic moment. Easy-axis is the preferred direction along which the magnetic material can be magnetized. Depending on the direction of the easy-axis, MA can be classified into IPA or PMA. MTJ with IPA and PMA is also known as iMTJ and pMTJ, respectively. The following Figs. 8 (a, b) distinguish between easy-axis and hard-axis of FL of ellipsoidal shape iMTJ. We chose the single domain approximation in which the magnetization is kept uniform inside the FM layer by transferring the magnetic poles inside the surface, as shown in Figs. 8 (a, b). The magnitude of the demagnetization field and energy required for easy and hard-axis can also be calculated for Figs. 8 (a, b). It can be observed that in Fig. 8 b, the demagnetizing field and energy is large for the hard-axis as compared to the easy-axis due to large geometry dependent demagnetization factor along the y-axis as compared to the x-axis ($N_{dem_y} > N_{dem_x}$). The ellipsoidal

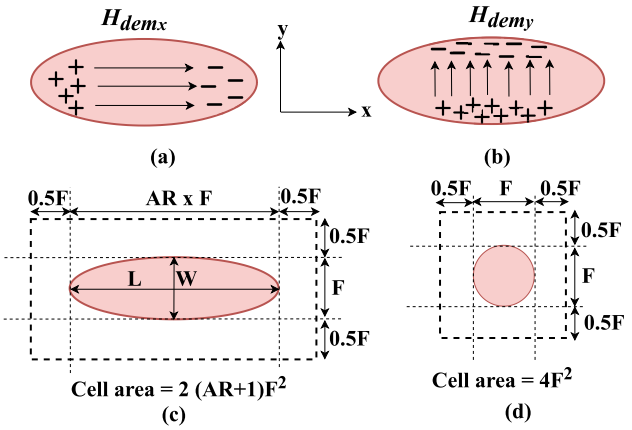


FIGURE 8. Top view of the FL of iMTJ, (a) the magnetization (shown by arrow) is along the longer x-axis named in-plane easy-axis. The poles are separated along the smaller surface, hence the demagnetizing field ($H_{dem_x} = 4\pi N_{dem_x} M_s$) in the x-direction is smaller compared to the demagnetizing field ($H_{dem_y} = 4\pi N_{dem_y} M_s$) in the y-direction (b) The magnetization (shown by arrow) is oriented along the short axis of the ellipse, since $N_{dem_y} > N_{dem_x}$, the demagnetizing field and energy are maximized hence named as in-plane hard-axis in the y-direction. Further, the demagnetization energy [9] can be calculated by, $E_{dem} = \frac{1}{2}\int_V \vec{M_S}.\vec{H}_{dem}dV$. (c) Cell area calculation using the top view of iMTJ and (d) pMTJ, it can be noticed that pMTJ is more compact than iMTJ.

shape is preferred not only due to patterning issues but also helps to reduce the pinning centers for the magnetization. The pattern and the material used to develop the FL should be such that it could store the NV magnetization state for certain years while developing the memory or hybrid circuits. Anisotropy is also one of the prerequisites for hysteresis in the FM layer, and it should be kept high for long time data storage. Since the FL direction needs to be switched to write '0' and '1' states, so for effective magnetization switching, anisotropy should not be too high. An ellipsoidal shape iMTJ results in a minimum cell area of $2\,(AR+1)\,F^2$, Where AR (=L/W; here L is in the x-axis, and W is along the y-axis) is the aspect ratio of the ellipse, and F is the minimum feature size for the technology node (Fig. 8 c). In general, the minimum size transistor can be in the order of $(6-8)F^2$, so the size of the MTJ should be chosen for no additional area penalty by selecting the aspect ratio and feature size appropriately. Further, for high-density memory and the hybrid CMOS/MTJ circuit, if the area is critical, a more compact circular shape pMTJ with an area of $4F^2$ is preferred (Fig. 8 (d)). Moreover, the MTJ with PMA has higher TMR and performs better in terms of thermal stability, critical current, and access speed compared to MTJ with IPA [26]. Anisotropy nature of a nanomagnet (or thin-film) is distinctly different than that of the bulk magnet, i.e., in thin films, PMA is seen, whereas, in the bulk magnet, parallel MA (or IPA) is inherent. Anisotropy associated with the shape of the thin film nanomagnet is also known as shape anisotropy [9].

PMA is further classified into interfacial PMA (iPMA) and crystalline PMA (cPMA). iPMA has been observed in CoFeB whose thickness is less than the critical thickness (t_c), while cPMA was observed in CoPt and FePd, whose crystalline anisotropy is very high [74], [75]. Mathematically the effective perpendicular anisotropy field [76] is given by,

$$H_{K_{\perp}eff} = H_{K_{\perp}} - H_{dem_z} = \frac{2K_{\perp}}{M_s} - 4\pi N_{dem_z} M_s. \quad (9)$$

Here, $H_{K_{\perp}}$ is the perpendicular anisotropy field and H_{dem_z} is the demagnetization field. H_{dem_z} in the z-direction tends to make the magnetization perpendicular to the plane. $K_{\perp}$ is the perpendicular anisotropy field, N_{dem_z} is the geometry dependent demagnetization factor in z-direction and M_s is the saturation magnetization. For iPMA, $K_{\perp}$ can be replaced as $\frac{K_i}{t_f}\left(=\frac{2\pi M_s^2 t_c}{t_f}\right)$; here K_i is the interfacial anisotropy energy density and t_f is the thickness of FL. Recent experiments have revealed that in the stacking of CoFeB/MgO/CoFeB, iPMA can be modulated by applying the external voltage and is known as the VCMA effect [77]–[82]. The linear relationship between K_i and the applied bias voltage (V_{app}) has been verified experimentally [79]–[84],

$$K_i\left(V_{app}\right) = K_i\left(V_{app}=0\right) - \frac{\xi V_{app}}{t_{ox}}. \quad (10)$$

Here $K_i\left(V_{app}\right)$ is the voltage-dependent interfacial anisotropy energy density, $K_i\left(V_{app}=0\right)$ is the interfacial anisotropy energy density at $V_{app} = 0$, ξ is the VCMA coefficient depending on the type of material stack to find the corresponding change in K_i by V_{app} and the thickness of the oxide layer (t_{ox}). The change in iPMA modulates the energy barrier of the FL while switching. For cPMA $K_{\perp}$ can be replaced by K_u, which is known as the crystal anisotropy energy density.

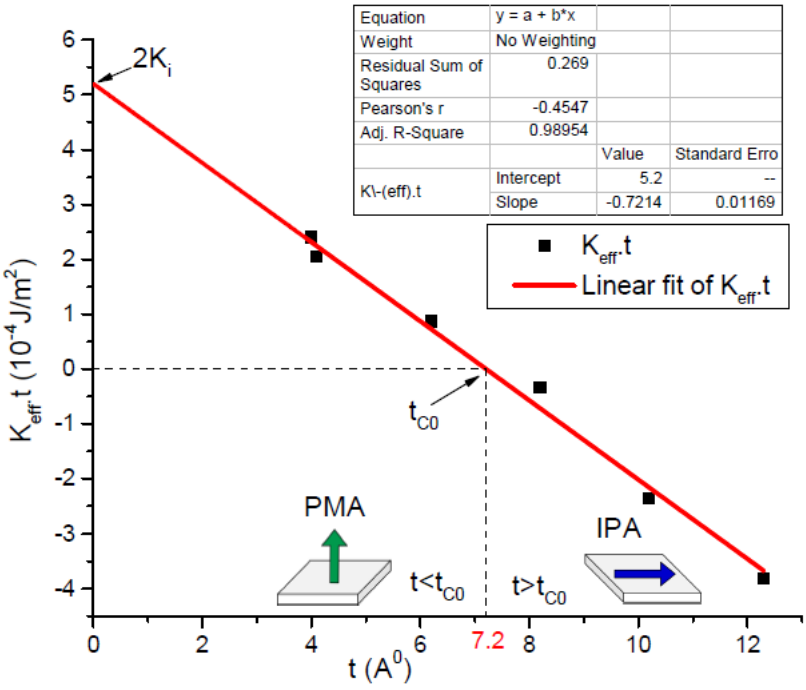
To understand the MA in MTJ for multilayer, we first revisited the previously reported work by Draaisma *et al.* in 1987 [85]. In multilayer structures, magnetic anisotropy energy (MAE), K_{eff} (J/m^3) arises from two components; volume contribution K_v (J/m^3) and surface (or interface) contribution K_i(J/m^2), which is given by the Eq. (11) [85],

$$K_{eff} = K_v + \frac{2K_i}{t}. \quad (11)$$

This relationship presents the weighted average of MAE of inner volume atoms and interface atoms. Here K_v contains contributions from the shape, magneto-crystalline, and magneto-elastic anisotropy [86], and t is the thickness of the magnetic layer. Factor 2 is included in Eq. 11 due to the same interface contribution on both sides. Fig. 9 shows a typical example of the Pd/Co multilayer consists of an ultrathin layer of Co (2-12 A^0) [85]. Fig. 9 (a) is the experimental data obtained by Pd/Co multilayer [85], and Fig. 9 (b) is the corresponding graphical technique to find K_i and K_v from the plot of ($K_{eff}.t$) versus t. Once K_i and K_v are obtained from the plot, K_{eff} can be calculated using Eq. 11. This basic idea is still followed in the literature to find the K_{eff} [49]. PMA and IPA can be easily distinguished using Fig. 9 (b). In bulk materials, anisotropy is dominated by the volume component of the equation, whereas in thin films, the interface term is dominant; because the thickness becomes very small. K_{eff} represents the preferred direction of magnetization in the

t	K_{eff}
4	0.6
4.1	0. 5
6.2	0.14
8.2	-0.04
10.2	-0.23
12.3	-0.31

(a)



(b)

FIGURE 9. MAE in the stack of Pd/Co multilayer using an ultrathin layer of Co. (a) Experimental data reproduced from ref. [85] (b) The graph is plotted using the origin software between ($K_{eff}.t$) versus t. The intercept along the y-axis gives $2K_i$, from which $K_i = 0.26 \times 10^{-3} J/m^2$ while the slope of the plot gives $K_v = -0.72 \times 10^6 J/m^3$. The positive K_{eff} indicates the preferred direction is perpendicular while negative K_{eff} indicates that the preferred direction is parallel to the in-plane magnetization. The critical thickness ($t_{Co} = \frac{-2K_i}{K_v} = 7.2$Å) indicates zero intercepts and K_i is a positive quantity favoring perpendicular magnetization.

multilayer structure (Fig.9). A positive K_{eff} leads to PMA in a multilayer structure (thin-films) whereas negative K_{eff} leads to IPA. The negative slope indicates K_v, and intercept at zero thickness indicates K_i. So below a particular thickness, called critical thickness (t_{Co}), K_i is more dominant than K_v. Hence in thin-film structures, PMA is seen predominantly due to minimal thickness. The critical thickness can be obtained from Eq. 11 by substituting K_{eff} to zero [86], [87],

$$t_{Co} = \frac{-2K_i}{K_v}. \tag{12}$$

III. MTJ SWITCHING MECHANISMS

Changing MTJ resistance either from R_{AP} to R_P or vice versa can be achieved by switching the magnetic orientation of the FL. MTJ switching process is also known as writing or storing the data in MTJ. There are many ways of switching the magnetization direction of the FL of MTJ, and we listed a few of them and discussed their potential for practical application.

A. FIELD-INDUCED MAGNETIZATION SWITCHING (FIMS)

FIMS mechanism was employed in the first-generation iMTJs developed using an aluminum oxide-based insulating barrier [88]. In FIMS, the magnetization of the FL is switched by an externally induced magnetic field produced by the current-carrying conductors placed close to the MTJ device. MTJ is placed in between the two orthogonal current lines called digit line (DL) and bit line (BL). Bit line current (I_b) with the assistance of digit line current (I_d) is used to change the magnetic orientation of MTJ (Fig. 10(a)) [89]. The current polarity of Ib decides the state of the MTJ (P or AP). Based on this mechanism, Freescale launched the first commercial 4-Mbit MRAM-MR2A16A in 2006 [90]. But, this method has several disadvantages, such as; FIMS occupies a large area per cell and refrain from achieving the high density. FIMS mechanism needs a large current (write current ~10 mA), which increases the total power consumption. In addition to that, as the separation between the adjacent cells reduces, the magnetic field interference is induced between the cells causes write error. MTJ situated close to the selected MTJ will be influenced by the external magnetic field generated by BL and DL. This tends to change the logic stored in the adjacent unselected MTJ. It is called the half selectivity disturbance. Later, Engel *et al.* proposed a toggling switching method to overcome the half selectivity issue [91].

B. THERMALLY ASSISTED SWITCHING (TAS)

The limitations of the FIMS, power consumption, and write selectivity are mitigated in the TAS mechanism [88], [92]. Antiferromagnetic layers are added above the FL and below

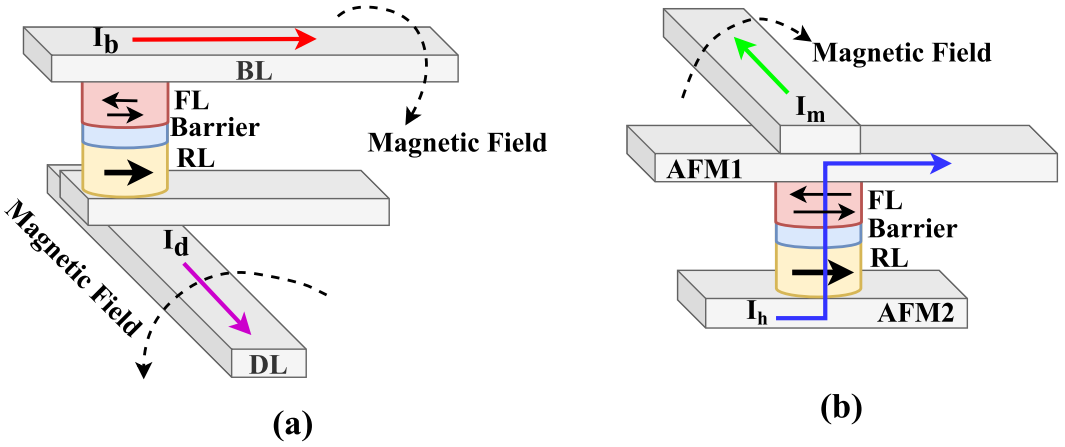


FIGURE 10. (a) A picture to understand the FIMS switching mechanism in iMTJ [89], situated between DL and BL, respectively. (b) A picture to understand the TAS [89] switching mechanism in iMTJ, which is present between two antiferromagnetic layers named AFM1 and AFM2.

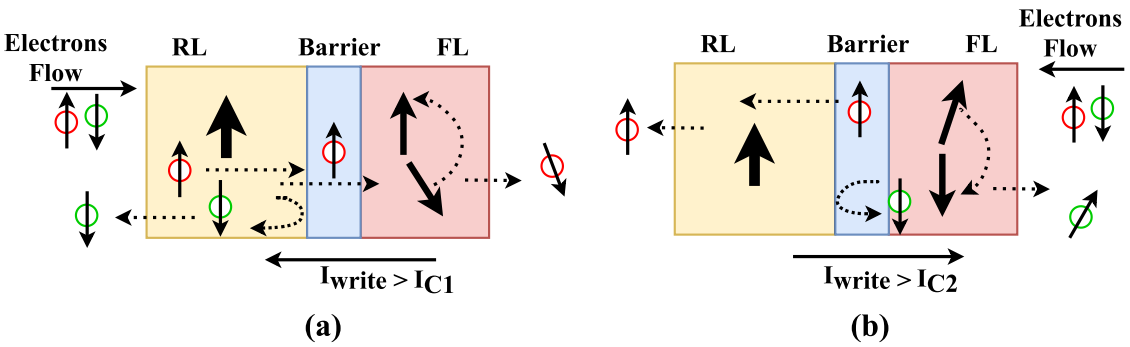


FIGURE 11. Schematic illustration of the STT switching mechanism. (a) In AP to P switching, when $I_{write} > I_{C1}$ flows from FL to RL, resistance state changes from R_{AP} to R_P, (b) on the contrary, in P to AP switching, when $I_{write} > I_{C2}$ flows from RL to FL, resistance state changes from R_P to R_{AP} [24], [99].

the RL, named AFM1 and AFM2, respectively [93]. The blocking temperature of AFM2 is higher than that of AFM1. In this technique, the iMTJ cell that needs to be written is elevated to a higher temperature by the application of heating current (I_h). When the temperature exceeds the blocking temperature of the FL, then an external magnetic field is induced by the magnetization current (I_m) to switch the magnetic orientation of FL (Fig. 10(b)) [94]. The writing process in TAS is faster than FIMS due to the use of higher temperatures, but the limitation of this technique is lower density in limited area or scalability.

C. STT

STT was theoretically predicted by Slonczewski [95] and Berger [96] independently in 1996. Later it was experimentally observed in deep submicron-sized low resistance $CoFeB/Al_2O_3/CoFeB$ MTJ structure in 2004 [97]. STT, current-induced magnetization switching (CIMS) approach showed significant improvement in speed and power dissipation compared to field-induced switching. In STT, a spin-polarized current is employed in the MTJ device to switch the magnetic orientation of FL. MTJ cells can also be switched from AP to P state or vice versa by passing a write conduction current as well [98], [99]. In the case of conduction current, conduction electrons will be polarised to the magnetization direction of the FM layer and imbalance spin population. $I_{write}(= I_{AP\rightarrow P})$ passing from FL to RL should be higher than critical current (I_{C1}) to switch the magnetization from AP to P state (Fig. 11 (a)). In a similar manner, I_{write} $(= I_{P\rightarrow AP})$ passing from RL to FL should be higher than critical current (I_{C2}) to switch the magnetization from P to AP state (Fig. 11 (b)). Electrons flowing from RL to FL are spin-polarized, i.e., these electrons are aligned in the magnetization direction of the RL. The majority up spin electrons tunnel through the barrier without losing their polarization and reach in FL, where they transfer their spin angular momentum to the magnetization of the FL by applying a large STT. When sufficient large current $I_{AP\rightarrow P} > I_{C1}$ is applied, the magnetic orientation of FL aligns toward RL. While the minority down spin electrons are reflected back at the barrier interface and exerts insufficient torque, which is unable to switch the magnetization of RL. Synthetic antiferromagnetic (SAF) layer, known as the exchange layer (not shown here in Fig. 11), is used below the RL in pMTJ to

fix the magnetization of RL. When conduction electrons flow from FL to RL, they first enter into FL and get polarised in the magnetization direction of FL. Majority spin-up electrons will tunnel the barrier and cross the RL without affecting the magnetization of RL, while minority spin-down electrons are reflected at the barrier interface and exert torque in FL. This starts to change the direction of FL and when the current condition, $I_{P\rightarrow AP} > I_{C2}$ is met, significant torque aligns the magnetization direction of FL to AP direction. It has been reported around 50% large write current is needed in the case of P to AP switching. It has been proved that the critical current required for switching out of the P to AP state is more than AP to P state i.e. $I_{C2} > I_{C1}$. Thus there is a strong asymmetry in switching conditions of pMTJ due to different spin polarization efficiency factors for P and AP state, which further depends on spin polarization and the angle between FL and RL. The average critical current density$J_{C0}(= \frac{|J_{C1}|+|J_{C2}|}{2}$; here J_{C1} and J_{C2} are the critical current densities for switching the AP to P and P to AP states respectively) and average critical current $I_{C0}\left(= \frac{|I_{C1}|+|I_{C2}|}{2}\right)$ are used for comparison purposes. For MgO based MTJ, J_{C0} is reported $\sim 2.2 \times 10^6$ A/cm^2, i.e., one-third of that in AlOx based MTJ [98]. Further, by changing the structure of MTJ, J_{C0} can be reduced. For dual barrier, MgO based MTJ cell J_{C0} is reported as 1.1×10^6 A/cm^2 [98].

The magnetization dynamics of the FL layer can be explained by the Landau–Lifshitz–Gilbert (LLG) equation [100]–[102]. In general, the LLG equation is the basis for computational micromagnetics and holds almost all the physical features of strong ferromagnets,

$$\frac{\partial \vec{M}}{\partial t} = \underbrace{-\mu_0 \gamma \vec{M} \times \vec{H}_{eff}}_{\text{Precession}} + \underbrace{\frac{\alpha}{M_s}\left(\vec{M} \times \frac{\partial \vec{M}}{\partial t}\right)}_{\text{Damping}}. \quad (13)$$

Here, the first term describes the precession of the magnetization ($\vec{M}$) of FL around the effective magnetic field ($\vec{H}_{eff}$). It is always perpendicular to both $\vec{M}$ and $\vec{H}_{eff}$. Here, γ is the gyromagnetic ratio and μ_0 is the magnetic permeability of the free space, the term $\gamma_0 = \mu_0\gamma$ which is equivalent to $2.211 \times 10^5 mA^{-1}sec^{-1}$ for a free electron. The effective magnetic field is the sum of various fields,

$$\vec{H}_{eff} = \vec{H}_{ext} + \vec{H}_{an} + \vec{H}_{dem} + \vec{H}_{amp} \quad (14)$$

Here $\vec{H}_{ext}$ is the applied external magnetic field, $\vec{H}_{an}$ is the magnetocrystalline anisotropy that exists due to crystal structure, $\vec{H}_{dem}$ is the demagnetization field and $\vec{H}_{amp}$ is the Amperian field generated by the injected current passing through the MTJ. Further, the material's magnetic anisotropy can contribute to easy-axis (or in-plane axis), perpendicular axis, and planar fields. The second term in the LLG equation is the damping term (Eq. 13), which reduces the precession angle (θ) and align the magnetization in the direction of $\vec{H}_{eff}$. Here α is the damping constant, determines the rate at which energy dissipation occurs. Slonczewski added the additional term in the above equation due to spin polarised electrons and is known as the LLGS equation [103], [104]. STT due to coupling of spin polarised electrons can be represented by additional term in the equation as below,

$$\frac{\partial \vec{M}}{\partial t} = -\gamma_0 \vec{M} \times \vec{H}_{eff} + \frac{\alpha}{M_s}\vec{M} \times \frac{\partial \vec{M}}{\partial t} + \underbrace{\vec{T}_{CIP} + \vec{T}_{CPP}}_{\text{Torque}}. \quad (15)$$

Here the two additional term at last in the LLGS equation is due to STT and are related to the current in-plane ($\vec{T}_{CIP}$) and current perpendicular to plane ($\vec{T}_{CPP}$) geometry. $\vec{T}_{CPP}$ occurs in multilayer structure while $\vec{T}_{CIP}$ finds in single materials in which spatial magnetization gradients occur. For pMTJ, $\vec{T}_{CIP} \approx 0$ and $\vec{T}_{CPP}$ can be represented by,

$$\vec{T}_{CPP} = \omega(\theta)\frac{\sigma J}{M_S^2}\vec{M} \times \left(\vec{p} \times \vec{M}\right). \quad (16)$$

Here, $\omega(\theta)$ is the angular dependency of STT on the angle θ between FL and RL magnetization, $\vec{p}$ is along the direction of RL stack and the spin transfer efficiency ($\sigma = P\frac{g\mu_B}{e}\frac{1}{d}$; here P is the spin polarization, d is the thickness of the film, g is the spin polarization efficiency factor and μ_B is the Bohr magneton). Further, the saturation magnetization M_S can be defined as total magnetization per unit volume when all spins are aligned. STT can lead to negative damping, depending on the direction of applied current density (J) and $\vec{p}$.

Much research on STT induced magnetization dynamics has been reported from time to time [102], [105]–[109]. Magnetization dynamics of both iMTJ and pMTJ can be easily understand using the LLGS equation. Assume that the applied current is such that the STT is opposite to DT, as shown in Fig. 12 (a), and MTJ is switching from P to AP state. Based on the analytical and numerical calculations, the current-driven magnetization represented by Fig. 12 can be explained as following [98], [110], [111],

(i) If the initial magnetization $\vec{M}$ of the FL is tilted instantaneously from its position as shown in Fig 12 (b), then in the absence of STT and DT term it will precess in a circle due to FT term produced by the $\vec{H}_{eff}$ in $\hat{z}$ direction.

(ii) If the applied current is small, i.e., J < J_{C0}, the magnetization of the FL spiral back to the magnetization direction of the RL (here, we assume both FL and RL are pointing in the same direction $\hat{z}$ initially). It is similar to the situation in which even if the current is '0' and we perturb the $\vec{M}$ away from $\vec{H}_{eff}$, it will come back to $\hat{z}$ along the spiral path with gradually decreasing the precession angle. It is due to the damped motion in which the DT component is higher than the STT term. Due to damped motion, the precession angle reduces, and the STT is insufficient to inverse the initial magnetization (Fig. 12 (c)).

(iii) If the applied current J = $J_{C0,}$ the STT term becomes higher than the DT term, precession angle increases initially, and achieves a steady state of dynamic equilibrium (Fig. 12 (d)). The magnetization of the FL spirals away from the RL and precessing continuously at some

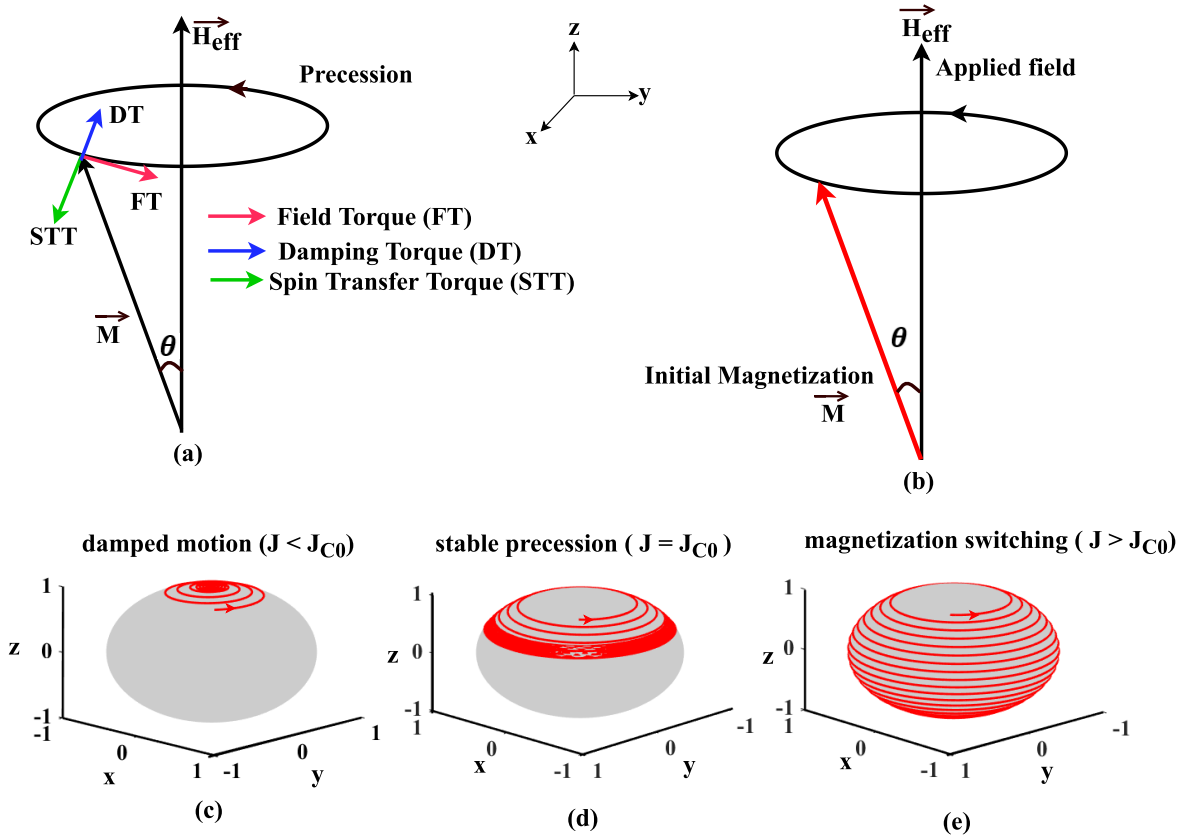


FIGURE 12. Schematic illustration of LLG equation with field torque (FT), Gilbert damping torque (DT), and spin-transfer torque (STT) terms pictured as in ref. [102] (a) Here, FT is generated due $\vec{H}_{eff}$, DT is exactly opposite to STT. (b) Magnetic configurations showing the applied field and $\vec{M}$ of the FL for figs. c, d, and e. (c) For ($J < J_{C0}$), $\vec{M}$ spirals back to the applied field due to damped motion [102]. (d) As current is increased, $\vec{M}$ spirals to the applied field and a steady-state is reached ($J=J_{C0}$) between the DT and STT due to which $\vec{M}$ precesses along $\hat{z}$ with a constant precessing angle [102]. (e) When $J > J_{C0}$, due to large current, magnetization reversal of the FL takes place, in which $\vec{M}$ switches AP to the applied magnetic field [102].

fixed average angle in response to the applied current. In this case, the energy gained from STT during each precession cycle is balanced by the energy lost in the DT term.

(iv) In other scenarios, if the applied current exceeds critical current, i.e., $J > J_{C0}$, the STT term continuously increasing and becomes significant than the DT term. The ever increasing precession angle becomes large enough to 180^0, and the magnetization of the FL switch opposite to the RL, meaning $\vec{M}$ is reversed to $\vec{H}_{eff}$ (Fig. 12 (e)).

A similar explanation can be made for AP to P state switching. The above explanation is made by neglecting the MA, but it is still valid for the sample with material anisotropies [102]. Further, the switching speed of the MTJ depends on the duration and amplitude of the applied current pulse used in the STT mechanism [112]. Three different switching regimes were reported based on the range of the width of the applied current pulse (Fig. 13) [98]. To understand the effect of current pulse width (τ) in these switching regimes, we reinvestigated the switching current density equations reported by Raychowdhury *et al.* [113]. Eqs. 17, 18, and 19 represent the switching current densities for Precessional switching (PS) regime, Thermal activation (TA) regime, and Dynamic reversal (DR) regime respectively [113], [114],

$$J_{c,PS}(\tau) = J_{c0} + \frac{C ln\left(\frac{\pi}{2\theta}\right)}{\tau} \quad \text{for } (\tau < 3ns), \tag{17}$$

$$J_{c,TA}(\tau) = J_{c0}\left(1 - \frac{k_B T}{E_b} \ln\left(\frac{\tau}{\tau_0}\right)\right) \quad \text{for } (\tau > 10ns), \tag{18}$$

$$J_{c,DR}(\tau) = \frac{J_{c,TA}(\tau) + J_{c,PS}(\tau)\exp(-A(\tau - \tau_c))}{1 + \exp(-A(\tau - \tau_c))} \quad \text{for } (3\,ns < \tau < 10\,ns). \tag{19}$$

Here, $J_{c,PS}(\tau)$, $J_{c,TA}(\tau)$ and $J_{c,DR}(\tau)$ are the switching current densities for PS, TA, and DR regimes, respectively. k_B is the Boltzmann constant, T is the temperature, E_b is the thermal energy barrier, J_{c0} is the critical current density, τ is the write time, Δ is the stability factor ($\Delta = \frac{E_b}{k_B T}$ should be greater than 60 for NV applications), θ is the angle between FL and RL and τ_0 is the inverse of attempt frequency. Here A (>0), C and τ_c are the fitting parameters. The following analysis can be made from Eqs. 17, 18, and 19,

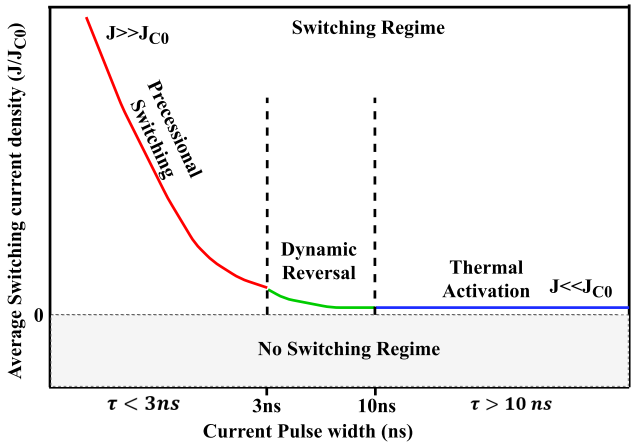


FIGURE 13. A plot between the average switching current density vs. applied current pulse width from ref. [98]. Three regions; PS with red color ($\tau < 3ns$), DR with green color ($3ns < \tau < 10ns$), and TA region with blue color ($\tau > 10ns$) are shown using ref. [113]. The two regimes ($J > J_{C0}$) and ($J < J_{C0}$) have been well studied, but the DR region with the least information have shown a great potential for practical realization of NV memory [111], [115], [116].

(i) If the applied current density $J > J_{C0}$, PS contributes to magnetization reversal. The write pulse needed for this switching regime is $\tau < 3ns$ (Eq. 17). Katine *et al.* reported the switching time 5-20ns at room temperature [112].

(ii) If the current density $J < J_{C0}$, the magnetization reversal is still possible by the thermal activation (Eq. 18). The write current pulse needed in this region is ($\tau > 10ns$), but the switching speed will be low. Thus there is a trade-off between the switching speed and current density.

The two regimes $J > J_{C0}$ and $J < J_{C0}$, have been well studied, but the in-between region, i.e., the DR region, is difficult to model [115]. Unlike the other two regimes, there is no explicit formula for dynamic reversal. However, the DR region combines both PS and TA switching in the nanosecond regime, as represented by Eq. 19. It is a very small region ($3ns < \tau < 10ns$) used for practical application. The operating speed in this region corresponds to the realization of STT-MRAM [116].

STT switching mechanism easily adopts the scaling trends; hence high density can be achieved. The STT-MTJ cell area is significantly lesser than that of FIMS and TAS cells. Moreover, the magnitude of the switching current can be reduced, which results in low power consumption. The expression for average critical current for pMTJ is given by Eq. 20 [117],

$$I_{C0} = \alpha \frac{\gamma e}{\mu_B g} M_S . H_K V. \tag{20}$$

Here α is the damping constant, γ the gyromagnetic constant, e is the magnitude of electron charge, μ_B is the Bohr magneton, V is the volume of the FL, and g is the spin polarization efficiency factor, also known as Lande factor. Further, g is determined by the spin polarization (P) and the angle between FL and RL magnetization directions. Switching delay or average switching time (AST) of pMTJ is given by Eq. 21 [118], [119],

$$\langle \tau \rangle = \left[\frac{C + \ln\left(\pi^2 \xi / 4\right)}{2} \right] \frac{em(1 + P_{ref} P_{free})}{\mu_B P_{ref} (I_{write} - I_{C0})}. \tag{21}$$

Here C is the Euler's constant, ξ is the activation energy, μ_B is the Bohr magneton, e is the magnitude of the electron charge, m is the magnetic moment of FL, and P_{ref}, P_{free} are the tunneling spin polarizations of the RL and FL. It is clear from Eq. 21 that the pMTJ switching speed depends on I_{write} and I_{C0}. Increasing the I_{write} and decreasing the I_{C0} both will contribute to bring down the switching delay, which elicits the methods to optimize the trade-off between area and speed of STT-pMTJ [120]. Another important factor in STT-pMTJ is thermal stability, which is defined by Eq. 22 [117],

$$\Delta = \frac{E_b}{k_B T} = \frac{K_{eff} V}{k_B T}. \tag{22}$$

Here, E_b denotes energy barrier similar to in Eq. 18, K_{eff} is the effective MAE constant and is given by $K_{eff} = E_b/V$, T is the absolute temperature and k_B is the Boltzmann constant. From Eqs. 20 and 22 it is clear that I_{C0} and Δ are directly proportional to the device dimension, hence as technology scales down, K_{eff} should be changed to a higher value to maintain 10-year retention against thermal fluctuations [121]. iMTJ devices have an elliptical shape (Fig. 8 (c)) whereas pMTJ is circular (Fig. 8 (d)); hence pMTJ devices are easy to manufacture compared to iMTJ devices. Further to cancel the demagnetization field, I_{C0} in pMTJ is lower than iMTJ. Due to less I_{C0} and less area compared to iMTJ, pMTJ devices are considered prominent candidates not only to be used in high-density NV memory devices but also in hybrid circuits [15], [24], [99].

D. SHE

There are various Hall effects, but we would like to distinguish among the normal Hall effect (NHE), anomalous Hall effect (AHE), and pure spin Hall effect (PSHE) [7].

1) NHE

It was discovered by Edwin Hall in 1879 [122] and is widely used today to find the carrier concentration or types of polarity (whether n-type or p-type) of semiconductor material. Consider a solid conductor (or semiconductor bar) is placed in a z-direction magnetic field of flux density $B_z (= \vec{B}.\vec{a_z})$ (Fig. 14 (a)). Assume the electric filed ($\vec{E}$) is applied in the –y-direction (i.e., the direction of the charge current), so from theory, electrons are assumed to move in the y-direction. Meanwhile, scattering causes a frictional force which opposes the force due to $\vec{E}$. Under the steady-state, when the two forces balance, the electrons move with constant velocity in the y-direction, and this velocity is known as drift velocity ($\vec{v}_{drift}$). This model is known as the Drude model of electrical conduction [123]. Due to the presence of both $\vec{E}$ and $\vec{B}$, the electrons will experience a Lorentz

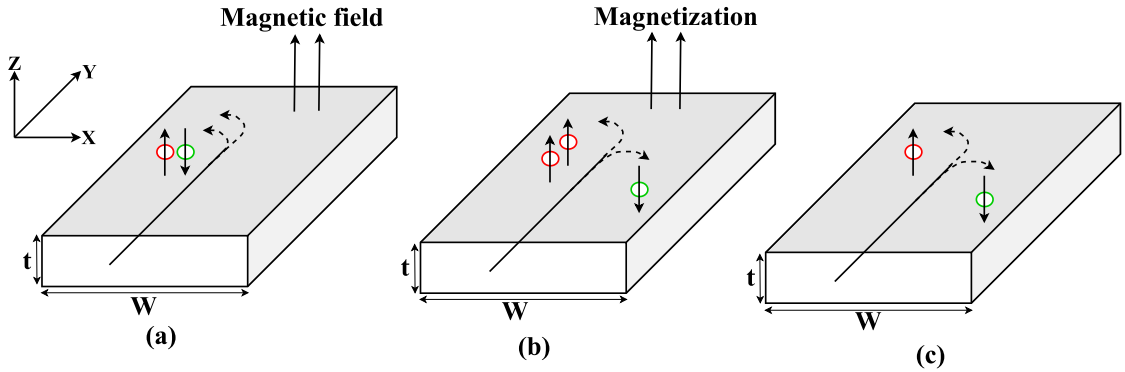


FIGURE 14. (a) A semiconductor bar showing NHE caused by the $\vec{E}$ applied along –y-axis and magnetic field of flux density ($\vec{B}$) applied in the z-direction. Due to the charge accumulation, Hall voltage is generated, but there is no accumulation of spins due to the equal number of up and down spins. (b) FM bar showing AHE in which the Hall voltage depends on the magnetization. It is observed that due to the spin-dependent scattering (or deflection) of the charge carrier, spins start accumulating at the lateral edges, and the Hall voltage is generated. (c) A heavy nonmagnetic metal bar with strong spin-orbit interaction is used to generate pure spin current (I_s). In PSHE, due to the accumulation of an equal number of up and down spins at the opposite edges of the bar, the Hall current gets cancel, and hence no Hall voltage develops. Notably, no magnetic field or magnetization is needed in PSHE. Reproduced from refs. [7] and [124].

force, $\vec{F} = -e[\vec{E} + (\vec{v}_{drift} \times \vec{B})]$ which pushes them in either $-\overrightarrow{a_x}$ or $\overrightarrow{a_x}$ direction based on the direction of the applied magnetic field in $\overrightarrow{a_z}$ and $-\overrightarrow{a_z}$ respectively. If the sample has boundaries, then the electrons will start piling, as shown in Fig. 14 (a), causing a charge imbalance in both the lateral edges. This charge imbalance will cause an x-directed $\vec{E}$ and the associated potential difference is known as Hall voltage (V_H). The sign of the V_H depends on the polarity of the charge carriers, i.e., whether they are electrons or holes. The magnitude of the V_H can be given by [7], [123],

$$V_H = \frac{I_y B_z}{nte} \tag{23}$$

Here $I_y(= ntWv_y(-e))$, v_y is the drift velocity component in the y-direction, tW is the cross-sectional area, n is the charge carrier density, and $(-e)$ is the negative charge on the electron. The magnitude of V_H is directly proportional to B_z and inversely proportional to n.

2) AHE

The origin of the AHE has been a controversial topic for a long time and investigated experimentally and theoretically from time to time [124]. It is of two types, intrinsic and extrinsic AHE [7]. The scope of this article is to discuss the origin of extrinsic AHE only. In FM material, there are the majority and minority spin electrons, as discussed above, using the energy band diagram (Fig. 7). It is clear from the band diagram that the band structure of FM material is spin-dependent. Due to magnetization ($\vec{M}$), the majority up spins are polarized in the z-direction, and minority down spins are polarized in –z-direction, which causes more electrons to scatter, and they start accumulating towards one edge of the FM bar as compared to other.

The Hall voltage is developed due to the charge imbalance between these two edges (Fig. 14 (b)). Since spin is the intrinsic property of the electron, the intrinsic imbalance of the spin produces two asymmetric spin hall currents along the direction perpendicular to the electric field (here up current is in –x-direction and down current is in the x-direction, refer Fig. 14 (b)). It is known as the extrinsic anomalous Hall effect (EAHE). The V_H is proportional to the spin polarization (i.e., the magnetization). AHE directly depends on the magnetization of the material and is often much larger than the NHE. In AHE, even in the absence of a magnetic field, if the material is magnetized, then also it can generate the V_H [124]–[126].

3) PSHE

SHE originates from the coupling of the charge and spin current (I_s) due to spin-orbit interaction and was reported in 1971 by Dyakonov and Perel [127], [128]. The term ''Spin Hall Effect'' was first introduced by Hirsch in 1999 [129]. Even in the absence of the magnetic field, it can be observed that a charge current passing through the two-dimensional electron gas (2-DEG) sample induces spin accumulation at the lateral boundaries due to the strong Rashba spin-orbit interaction [130]–[132]. Spin polarization on the boundary depends on the magnitude of the applied current, and the direction of polarized spins switched if the applied current direction is reversed. The spin up charge and spin down charge generates two types of Hall currents, which cancel each other and no V_H is developed (Fig. 14 (c)). Spin-dependent scattering keeps generating both types of I_s, as long as the spin-orbit interaction is non-vanishing even in the absence of a magnetic field. However, a spin imbalance forms just like in the case of AHE. The origin of the spin-orbit torque (SOT) generated by spin-orbit interaction is still under debate. Rashba spin-orbit interaction [130], [131], SHE [133], [134] and combination of both are the possible mechanisms for SOT [135]. To understand SHE, let us assume a heavy metal (Tantalum (Ta) or platinum (Pt)) is

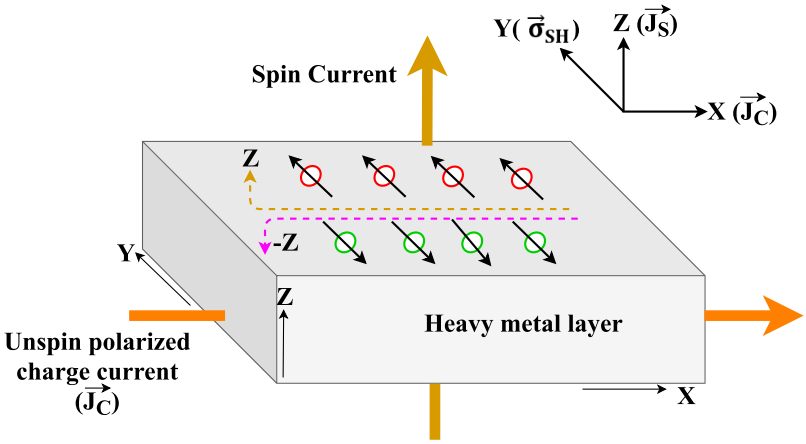


FIGURE 15. The charge current (or conduction current) flowing in x-direction through the heavy metal bar produces the accumulation of up spins polarised in the y-direction, down spins polarised in –y-direction towards z and –z-axis, respectively. It can be observed that I_S is always normal to the charge current and the direction of spin polarization (here ± y-axis) of electrons. The direction of I_S is given by the Eq. 24 [89].

TABLE 1. Comparison among various Hall effects using [7].

Ordinary Hall effect	Anomalous Hall effect	Pure spin Hall effect
Magnetic field or $\vec{B}$ is required	$\vec{M}$ is needed	No magnetic field
Accumulation of charge, no spin accumulation	Accumulation of spins	Accumulation of spins
V_H developed	V_H developed	No V_H developed

placed, as shown in Fig. 15, in which the charge current is flowing through the x-axis. It produces an accumulation of spins on the lateral surfaces due to strong spin-orbit interaction [129], which produces the I_s normal to the direction of charge current and electron spin vector. The direction of the I_s can be given by the following relation [127], [136],

$$\vec{J}_s = \eta_{SH}\vec{J}_c \times \vec{\sigma}_{SH}, \tag{24}$$

here $\vec{J}_s$ is the spin current density vector, $\vec{J}_c$ conduction current density vector and $\vec{\sigma}_{SH}$ is the electron spin vector. η_{SH} is the spin Hall angle and $\frac{\hbar|\vec{J}_s|}{4\pi e}$ is the magnitude of spin current density. $\vec{J}_s$ generated along the z-axis is dissipationless [7], so $\vec{J}_s.\vec{E} = 0$. Here $\vec{E}$ is the electric field in x-direction. It is clear from Fig. 15 that the SHE effect can be used to generate pure I_s and is also known as PSHE. This idea is further used in three terminals SHE device for switching the magnetization of FL. Table 1 summarizes the comparison among various Hall effects.

CMOS/MTJ hybrid circuits developed using a two-terminal MTJ device based on the STT switching mechanism suffers from reliability issues. It is because of the accidental writing that occurs during the reading process. Since STT-MTJ is a two-terminal device, MTJ reading and writing paths are the same. A low magnitude current is needed as read current, whereas a higher magnitude current (above the critical current) is used as write current. But due to low TMR and thermal noise, there is a high probability of writing the STT-MTJ during the reading process [99], [137]. A three-terminal MTJ device that works on SHE based switching mechanism is shown in Figs. 16 (a, b) [137]. The heavy nonmagnetic metal layer of Tantalum ($\beta - Ta$)/Platinum (Pt) with a large spin-orbit coupling parameter is stacked below the FL. In the three-terminal SHE-MTJ device, the write and read operation path are different; hence in principle, read disturb faults (i.e., accidental writing while reading) do not occur (Fig. 16 (c)). Although there is an increase in the area, it improves the MTJ in various aspects [138]. It has also been observed that by reducing the thickness of the Ta layer, the switching current can be reduced by one order of magnitude compared to the STT switching mechanism. When the charge current passes through the stripe of the heavy metal layer, electrons with different spins are scattered in such a way that up spin electrons collect at one edge and down spin electrons on another edge. Due to spin-orbit coupling, the charge current passing horizontally induces perpendicular I_s, which generates SOT in FL of iMTJ to switch its magnetization [134], [139]. A significant amount of the charge current is needed to change the magnetization of the FL. The direction of charge current also decides the direction of induced I_s. But for pMTJ device, an external magnetic field ($\vec{H}_{app}$) is required [140] because the direction of electron spin and the anisotropy axis are not collinear (Fig. 16 (b)). This issue can be resolved by passing the STT write current instead of $\vec{H}_{app}$ and is known as the SHE-assisted STT switching mechanism [141], which has been discussed broadly in the next subsection. A simple way of generating the $\vec{H}_{app}$ is by just attaching a permanent magnet to the device. But attaching a permanent magnet

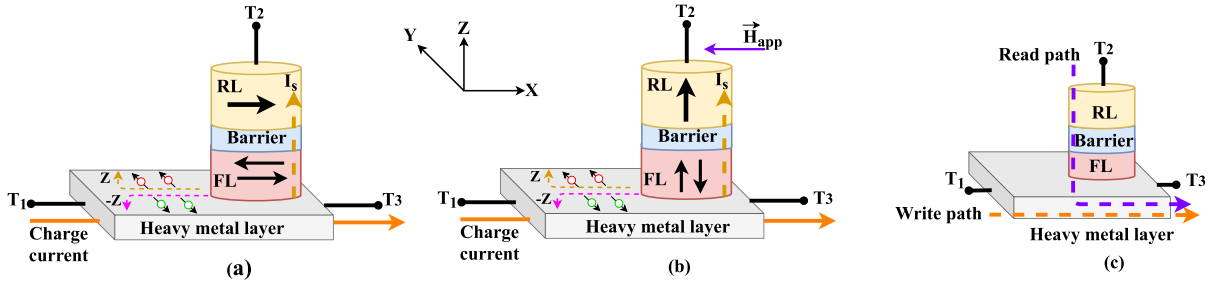


FIGURE 16. Magnetization switching of FL using SHE. (a) In iMTJ the sufficient I_S (z-direction) is able to switch the magnetization of FL [134], [139], (b) while in pMTJ, $\vec{H}_{app}$ is needed through terminal T_2 to T_3 in addition to I_S [140]. (c) SHE-MTJ structure with terminals T_1, T_2, and T_3 highlighting separate write (T_1 to T_3) and read path (T_2 to T_3) [9], [140].

seems undesirable for practical reasons. A magnetic field reduces the energy barrier between the stable magnetization, which can directly affect the thermal stability of the device. But in all the cases $\vec{H}_{app}$ required for switching will increase the complexity of hybrid CMOS/MTJ circuits.

Few studies claimed the perpendicular magnetization switching of MTJ by strong SOT in the absence of $\vec{H}_{app}$ [142]–[146]. $\vec{H}_{app}$ can be eliminated by doing the engineering in the device structure. Yu *et al.* reported a heterostructure device, $Ta/CO_{20}Fe_{60}B_{20}/TaO_x$ (fabricated the layers from bottom to top order such as nonmagnetic heavy metal/ferromagnetic (FM)/ insulator) by introducing a lateral structural asymmetry. When an in-plane current flows in these structures, the thickness of the insulator layer, which reduces from one end, gives rise to a new field-like SOT component [142]. Similarly, You *et al.* fabricated a heterostructure stack of Ta/CoFeB/MgO in which the CoFeB (FM) layer is reduced to one end to tilt the MA slightly from the perpendicular direction of the film [143]. Tilting the MA from a perpendicular direction emulates the effect of a magnetic field, which can affect the thermal stability. From the design of the hybrid CMOS/MTJ circuit perspective, both the structures are undesirable from a technological point of view. First, it needs the complex fabrication process, which can accurately control the continuous variation of the insulator or FM layer to develop the tapered structures. Another concern is the scaling of these tapered structures limits their use for hybrid circuits. Further, Kazemi *et al.* proposed a theoretical device comprising of Pt/Co/AlOx layers respectively and named it as all-spin orbit perpendicularly magnetized (ALPE) device [144]. Compared to the above-discussed devices, they did not use any tapered structure, and the materials used by them were similar to the conventional spin-orbit device. ALPE device enhances the switching energy-time product by two orders of magnitude as compared with STT switching based perpendicular magnetized devices.

E. SHE-ASSISTED STT SWITCHING MECHANISM

In pMTJs, torque at the start of the event is zero as both magnetic orientations of FL and RL are collinear because of their stable states. Reversal of the magnetic orientation of FL depends on the random fluctuations in order to disturb this

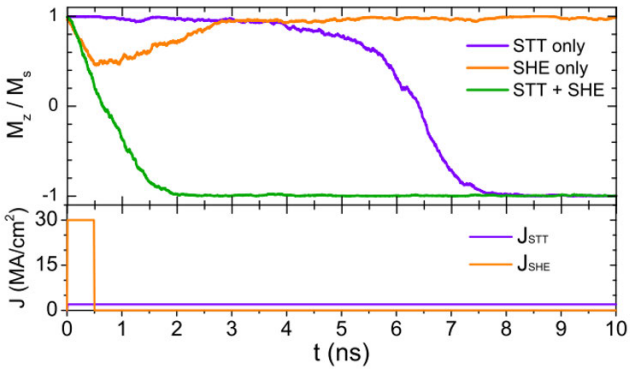


FIGURE 17. Magnetization trajectories reported by Brink *et al.* in STT, SHE, and STT+SHE switching mechanisms with applied current pulses of $\vec{J}_{STT}$, $\vec{J}_{SHE}$ and $\vec{J}_{STT} + \vec{J}_{SHE}$ respectively. Reproduced from ref. [141], with the permission of AIP Publishing.

initial alignment, which can take several nanoseconds [147]. This delay is called incubation delay, and it not only slows down the MTJ switching significantly but also contributes to the reliability issues [141]. In order to compensate for this, the strength of the switching current can be increased, but it will lead to more power dissipation in the writing circuit. Further, increasing the switching current increases the risk of dielectric breakdown in MTJ devices. SHE-assisted STT switching mechanism (STT + SHE) is experimentally demonstrated by various groups to overcome the incubation delay [133], [134], [141]. This method needs two switching currents ($\vec{J}_{STT}$ for STT and $\vec{J}_{SHE}$ for SHE) to switch the state of the FL. Van den Brink *et al.* studied the magnetization reversal process under device properties, current density, and applied pulse time. Following points can be noticed from their particular simulation (Fig. 17) [141],

i. The incubation delay is highest, and the switching delay is 8ns for conventional STT switching mechanism using $\vec{J}_{STT} = 2\ MA/cm^2$.
ii. For SHE switching mechanism using $\vec{J}_{SHE} = 30\ MA/cm^2$ with a pulse duration of 0.5 ns, an immediate and significant effect on magnetization is observed.
iii. For SHE-assisted STT switching mechanism, by combining $\vec{J}_{STT}$ and $\vec{J}_{SHE}$, switching delay is 2ns with complete elimination of incubation delay.

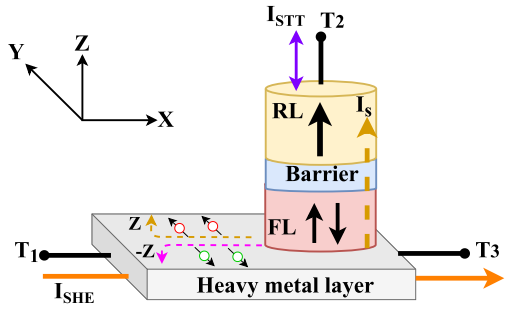


FIGURE 18. 3D view of pMTJ switched by SHE-assisted STT switching mechanism. FL and a heavy metal layer are in contact with each other. Assume the pMTJ is in AP state (RL pointing in the z-axis, FL is in –z-axis). Passing the I_{SHE} current along the x-direction through terminal T_1 to T_3 of heavy metal layer generates I_s to z-direction with spin-polarized along the y-axis (red color). When $I_s$enters the FL layer, it rotates the magnetization direction of the FL layer to the y-axis; simultaneously, an additional I_{STT} current is passed from terminal $T_2$to T_3 through MTJ. The electrons spin-polarized by RL in the z-direction tunnel through the barrier apply torque in FL and rotate the FL layer's magnetization from y to the z-axis [148].

To keep the continuity of this section, we have revisited the discussion on SHE from the previous section. SHE is one of the mechanisms which is used to switch the state of iMTJ by injecting I_{SHE} in hall material. But an $\vec{H}_{app}$ is required in pMTJ to switch the state of MTJ (Fig. 16 (b)). In SHE-assisted STT switching, this $\vec{H}_{app}$ is eliminated by passing STT current (I_{STT}) pulse [148]. To understand SHE-assisted STT switching, assume the pMTJ is in AP state (Fig. 18). When I_{SHE} passes through the heavy metal along the x-direction, spin up current (I_s) is generated along the z-axis. I_s is always normal to I_{SHE} and the direction of its spin polarization that is along the y-axis [134]. When I_s enters into FL, due to spin-orbit coupling it exerts a torque called SOT, which shifts the initial magnetization direction of the FL from $-z$-axis (Fig. 18) to the x-y plane in the y-direction. At this moment, I_{STT} is applied along with the T_2-T_3 terminal, which generates z-direction spin-polarized electrons. These spin-polarized electrons tunnel through the barrier and push the magnetization direction of the FL from the y-axis to be changed in z-direction. A similar explanation can be used to switch from P state to AP state.

F. VCMA

VCMA is the recent development that is used to switch the state of the MTJ by applying the voltage across its terminals [149], [150]. Charge starts accumulating or depleting at the metal barrier interface based on the electric field generated by the applied bias voltage (V_{app}). It modifies the spin-orbit interaction at the interface and changes the MA. The reduced MA enables the capability of magnetization switching of MTJ with low power dissipation [151]. It motivated the researcher to develop hybrid circuits [152], [153] and NV memory [154], [155] using this mechanism. The first experiment to observe the properties of FM materials by applying the electric field was observed by Ohno *et al.* in 2000 [156]. Further experiments were carried out using electric field switching of pMTJ by stacking of various FM layers. The switching characteristics were observed with the thickness variation of the barrier and the effect of anisotropy [80], [81], [157], [158]. Assume the two stable magnetization states in pMTJ are separated by an energy barrier (E_b) (Fig. 3d). Here, E_b determines the thermal stability of pMTJ and is a function of V_{app} (Fig. 19 (a), which can be positioned accordingly, as shown in Fig. 19 (b). It can be represented mathematically using Eq. 25 [159],

$$E_b\left(V_{app}\right) \approx \left[K_i\left(V_{app}\right) - 2\pi M_s^2\left(N_{demz} - N_{demx,y}\right) t_f\right] A. \tag{25}$$

Here notations are similar as used in the subsection "Interpretation of magnetic anisotropy". $N_{demx,y}$ is the geometry dependent demagnetization factor in in-plane direction and N_{demz} is along the perpendicular direction. A is the area of the FL in pMTJ. Thermal stability (Δ), an important factor, determines the data retention capability is directly related to the reliability of the pMTJ and can be obtained from Eq. 22 [159],

$$\begin{aligned}\Delta &= \frac{E_b}{k_B T} = \frac{M_s H_{K_{\perp}eff} V}{2k_B T} \\ &= \frac{\left[K_i\left(V_{app}\right) - 2\pi M_s^2\left(N_{demz} - N_{demx,y}\right) t_f\right] A}{k_B T}.\end{aligned} \tag{26}$$

Now assuming $N_{demx} = N_{demy}$ for circular shape pMTJ (Fig. 8 (d)) and if FL is much thinner than the lateral dimension of the pMTJ, then $N_{demx} = N_{demy} = 0, N_{demz} = 1$ [159] and Eq. 26 can be approximated as,

$$\Delta = \frac{\left[K_i\left(V_{app}\right) - 2\pi M_s^2 t_f\right] A}{k_B T}. \tag{27}$$

Substituting $K_i\left(V_{app}\right)$ from Eq. 10 to Eq. 27, we have [82],

$$\begin{aligned}\Delta\left(V_{app}\right) &= \frac{[K_i\left(V_{app} = 0\right) - \frac{\xi V_{app}}{t_{ox}} - 2\pi M_s^2 t_f]A}{k_B T} \\ &= \Delta\left(0\right) - \frac{\xi V_{app} A}{k_B T t_{ox}}.\end{aligned} \tag{28}$$

Here $\Delta\left(0\right)$ is the thermal stability factor under zero bias voltage, k_B is the Boltzmann constant, and T is temperature. At the critical point, the energy barrier vanishes ($\Delta\left(V_{app}\right) = 0$) and critical voltage ($V_{crit}$) can be obtained by setting Eq. 28 to zero [160],

$$V_{crit} = \frac{\Delta\left(0\right) k_B T t_{ox}}{\xi A}. \tag{29}$$

VCMA assisted switching can be obtained using a precessional and thermally activated regime for both iMTJ and pMTJ [161]–[163], but we have restricted our discussion to pMTJ only. When a positive voltage is applied across the terminals, as shown in Fig. 19 (a), $K_i\left(V_{app}\right)$ will be reduced (refer Eq. 10), which lowers the E_b. When it is equal to or greater than V_{crit}, the barrier disappears completely, and a new minimum will form in the in-plane direction. In this case, the magnetization of the FL becomes unstable and

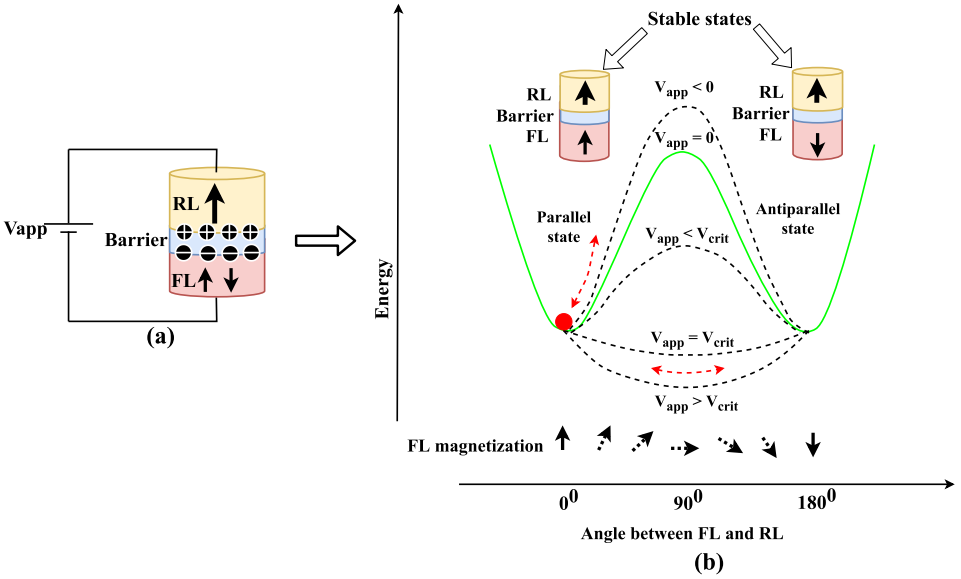


FIGURE 19. (a) A cross-sectional view of the VCMA assisted pMTJ device. (b) VCMA induced switching mechanism showing the energy barrier diagram for various scenarios of the applied voltages using ref. [160]. E_b between two stable states is eliminated by high positive voltage ($V_{app} \geq V_{crit}$), E_b is lowered by comparatively low positive voltage ($0 < V_{app} < V_{crit}$), E_b is enhanced by negative voltage ($V_{app} < 0$). Reproduced from ref. [160].

precessionally oscillates between P and AP states. When the magnetization is precessing to the in-plane direction, MTJ switching can be obtained by the proper timing of the magnetic dynamics. If $0 < V_{app} < V_{crit}$, then barrier is lowered but not completely eliminated as in precessional switching.

Due to thermal activation, the position of the barrier may vary, but it will not be significant enough to switch the magnetization alone. When the barrier is lowered down, an additional magnetic field or charge current is required to overdrive it, while in case of precessional switching, precise control of voltage pulse duration is needed. In general, the timing of the write pulse should be at half of the precession cycle; otherwise, a full precession cycle returns to no change in the magnetization of the initial state. It is similar to the toggling scheme in which after each write pulse, the state of magnetization keeps changing, and we don't know the final state of magnetization. Hence before writing the information, it is needed to read the state whether the state is P or AP, and then the write pulse is applied to change the magnetization. Precessional switching is faster than thermally activated switching [160] and can achieve a Ghz rate with a limited voltage pulse [159]. While for negative applied voltage ($V_{app} < 0$), E_b increases, which makes the FL difficult to switch [159]. The requirement of pulses (voltage or current) used in various techniques of VCMA assisted switching strategies have been discussed in Appendix A.

MTJ writing can be effectively accomplished either by using STT, SHE, or by the combination of both as discussed. In STT and SHE switching mechanisms, dynamic power and the delay for the writing process is relatively larger compared to the volatile CMOS based flip-flops and needs improvements to avoid degradation in the performance [152]. Recent experiments revealed a significant improvement in dynamic power dissipation and the write delay of MTJ using VCMA assisted switching mechanism [160], [164]. Various switching strategies like precessional VCMA, precessional VCMA-assisted STT, thermally activated VCMA-assisted STT, and precessional VCMA-assisted SHE switching mechanisms, etc. have been reported. But among all, precessional VCMA-assisted STT has proved to be more efficient [76], [152], [160] in performance and energy-efficient operations.

IV. A BRIEF HISTORY OF MTJ DEVICE MODELING

Modeling of spintronic devices has been growing rapidly in the last decades and an emerging area of research. Slonczewski proposed his idea of magnetic hysteresis in the confidential research memorandum of IBM in 1956, which was published later in 2009 [165]. The reported work proclaimed its use in developing NV memory array and a variety of NV logic functions. Several research groups had developed three dimensional, continuous-time models for magnetization dynamics [166]–[168], but these models are proprietary, and the papers do not reveal which languages or simulator tools were used. Early modeling work to support spintronic elements and circuits has mostly consisted of a quasi-static Simulation Program with Integrated Circuit Emphasis (SPICE) models, which uses electrically equivalent circuits and behaves like the magnetoresistive junction. Some models are state-driven, such that when certain physics-based conditions are met, a magnetization change takes place. Das and Black reported Hewlett Simulation Program with

Integrated Circuit Emphasis (HSPICE) models for a spin-valve made of voltage-controlled resistors, current sources, and voltage sources. It was the first generalized circuit macromodel for a pinned spin-dependent tunneling devices. This model accurately represents the nonlinear and hysteresis behavior of the spin valve and verified by simulating the memory circuits [169]. The same group also reported the first universal circuit macromodel for giant magnetoresistance (GMR) in 2000. The model was flexible and relatively simple, behaving accurately the nonlinear and hysteresis behavior of GMR [170]. MTJ macromodel, applicable to an HSPICE circuit simulator, was developed by Lee *et al.* [171]. It was realized as a five-terminal subcircuit that reproduced the characteristics of an MTJ; hysteresis, asteroid curves with thermal variation, and the resistance–voltage curve [171]. Modeling of MTJ has been grown rapidly since then, and there are various other models reported in the last decades [120], [172]–[180]. In 2007, the SPINTEC library reported C compiled MTJ model (but models were not published), which was verified using the Cadence Spectre simulator. Hybrid CMOS/MTJ circuits were developed using this model [92]. Harms *et al.* reported the SPICE macromodel of MTJ using the STT mechanism [181]. The model was characterized by hysteresis bias voltage dependence of the resistance and the critical switching current versus the critical switching time. The model was designed to work over a wide range of operating conditions. Further MTJ based D flip-flop was developed for model verification, but the model had wide applications too.

HSPICE/SPICE is an industry-standard simulator, but the biggest advantage of Verilog-A/AMS (Analog and mixed-signal) and VHDL (Very high-speed integration circuits hardware description language)-AMS over SPICE model is its flexibility, improved readability, modularity, integration of the model in any design flow, etc. These languages provide high compatibility with different dimensions of CMOS design kit using the Cadence tool. The physics-based mathematical model of spintronic devices can be developed using these languages, and if there are any improvement reports in the literature, the model can be updated just by adding or deleting some terms in the equations [182]. Using these ideas, many MTJ models have been reported timely. Kammerer *et al.* reported a compact MTJ model using VHDL-AMS language. This model was developed based on the S-W model and claimed to be the first compact model, which includes the vectorial aspect of the magnetic field [183]. Madec *et al.* developed a continuous 3D model using the VHDL-AMS language in which the magnetization switching takes place using the STT mechanism [184]. Later, Faber *et al.* developed the dynamic STT-MTJ model by including the switching probability and thermal effects. The code was written using Verilog-A language and implemented on the Cadence Virtuoso platform [185]. A new VHDL-AMS MTJ model description has been reported by Madec *et al.* in June 2010, but the code was not published [186]. The two important advantages of the model are that it includes all the first-order effects and uses physical parameters instead of fitting parameters. A 3D continuous-time model using Verilog-A for STT-MTJ has been reported by Linda E in her Ph.D. thesis for the use of industry-standard simulation tools [187].

Zhao *et al.* developed an electrical static macromodel of CoFeB/MgO/CoFeB MTJ structure using Verilog-A language, which has a good TMR ratio and switching performance [188]. Later the static, dynamic, and stochastic behaviors are integrated into the physical model. Many experimental parameters are directly included to improve the agreement of simulation with experimental measurements [120]. Despite the excellent potential in an STT-MTJ, the device performance is limited by considerable reliability issues such as process variations, stochastic switching, temperature fluctuation, and TDDB. TDDB is a mechanism to determine the MTJ lifetime and depends on the polarity of applied voltage, thickness variations, and other process induced damages [189]. pMTJ having an oxide barrier of size less than 1 nm designed to transmit a high-density spin-polarized current (>1 MA/cm^2) can cause dielectric breakdown due to self-heating, which can generate a functional error in the hybrid CMOS/MTJ circuits [117], [190]. Wang *et al.* proposed a compact model of MTJ by incorporating the phenomena of dielectric breakdown of the MgO barrier with STT stochastic behavior in which technical variations and temperature evaluation are integrated [36]. In this model, they could not include the effect of the current pulse width on the dielectric breakdown. Further, they reported an updated SPICE compact model by considering the temperature variation and its effect on performance in 2015 [191]. An MTJ SPICE compact model, including the TDDB mechanism, has been developed in 2016 [192]. It has been observed that this TDBB behavior is asymmetric for both up and down currents [193]. In a hybrid CMOS/MTJ design, the resistance of the MTJ should be comparable with the resistance of the transistor over which the MTJ has been fabricated. To get a lower resistance, the thickness of the MgO tunnel barrier of the MTJ should reduce but meanwhile, it should be capable of bearing the high current needed for the STT mechanism, which generates considerable potential across the MTJ [192]. Several experiments have been performed to understand this behavior [194]–[196]. Thus, a timely, updated, thorough MTJ model is required. Field and voltage dependence, Ramped voltage breakdown, time-to-failure, temperature evaluations, area scaling, technical variation, and TDDB probability, etc. should be included in the model to design the reliability-aware hybrid circuits.

V. RELIABILITY OF HYBRID CMOS/MTJ CIRCUITS

This section explores the reliability issues of hybrid circuits. Reliability aware device simulation is an integral part of the design process which decides the success of the system. Reliability aware simulators are needed, which can simulate the stochastic behavior of MTJ. While at the device level, a compact physics-based MTJ model is required, which can

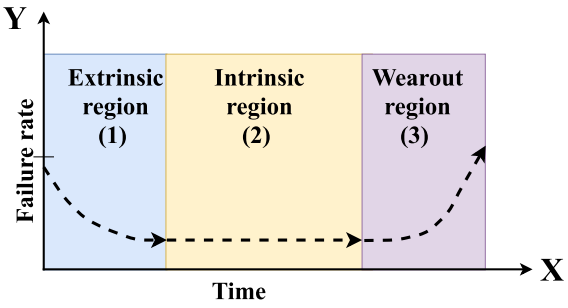


FIGURE 20. Traditional failure rate bathtub curve used for reliability analysis. Arrow indicates the direction of failure rate in all the regions with time (axes are not in scale) [197].

cover the magnetization dynamics, stochastic behavior, and reliability issues. These mechanisms are modeled throughout the complete design process so that the device can work up to its specified time duration without any distortion. The failure rate of hybrid circuits can be explained using the traditional bathtub curve (Fig. 20) used for reliability engineering [197]. It gives the type of failures once the product reaches the customer. The curve has three distinct regions depending on the variation of failure rate with time [197]–[199].

(i) Extrinsic region (region 1)- also known as early life or infant mortality period. At time t = 0; when the customer first starts using it, the high failure rate can be noticed. It is due to the manufacturing defects which could not be identified during the test.

(ii) Intrinsic region (region 2)- most of the circuits are designed to operate in this region. Here, one of the reasons can be thermal over-stress since the device is used for a longer duration. In this region, the failure percentage is low and constant over a long period of time.

(iii) Wear out (region 3)- this is the last phase of the circuit lifetime, where the circuit fails due to aging effects on the device. The change of the device characteristics is due to electrical stress.

Scaling the device [200] impacts the device reliability significantly. Scaling the device reduces the aspect ratio, which may cause an error in the photolithography process, resulting in a defective fabricated device. Further scaling the device dimension may also have a degrading effect on shrinking the gate dielectric of the MOSFET or MTJ barrier layer. A thin barrier layer will suffer from a higher leakage current as compared to a thicker one under the same bias voltage. Once the device is manufactured and has been used in a circuit for a longer time, there are still chances of changing the device characteristics due to electrical stress, and in the worst case, it can cause failures. This effect is called the aging effect. A framework in the simulator must be included which can cover hot carrier degradation (HCD), both positive and negative bias temperature instability (P/NBTI), TDDB and Electro-migration (EM), etc. [201]–[203]. The exact information of all these models is needed to accurately predict the reliability either at the device level or circuit level. Among all, TDDB is one of the most common reliability issues responsible for IC failure and has been extensively reported in the literature [204]–[224]. We have broadly reviewed the TDDB mechanism in hybrid CMOS/MTJ circuits.

A. TDDB MECHANISM

The breakdown is a physical process (or transition phase) in which the dielectric turns to be conductive rather than insulating under the applied electric field [225]. Various models have been developed to explain the lifetime of MOSFET and MTJ due to the reduction of an oxide layer, e.g., E-model, 1/E-model, Exponential $E^{1/2}$-Model, and Power-law voltage V^N-Model [195], [225]– [228]. All these models are either electric field-based models [204]–[223], current-based models [224], [229]–[231], or combination of both current and electric field-based models [216], [232]. As various switching mechanisms are used to change the state of MTJ either by applying the I_s, external magnetic field, or by the combination of both (refer section 3). In either of the case, a large electric field is developed across the two terminals of MTJ, which forms the conductive path between FL to RL or vice versa through the barrier layer. This process could be accelerated as the thickness of the oxide layer reduces and becomes a major concern during scaling. In particular, as the oxide layer reduces, TDDB lifetime becomes a serious concern for pMTJ than iMTJ [193]. There is a lot of controversy for the E vs. 1/E model due to the range of the applied electric field [214]. To distinguish clearly, the data must be collected over a wide range of fields. TDDB in MTJ can be modeled using two different mechanisms; intrinsic and extrinsic breakdown mechanism, also known as E and 1/E-model, respectively [189].

1) INTRINSIC BREAKDOWN MECHANISM

In this mechanism, due to the large electric field-induced by the I_s, microscopic ohmic shorts are formed, and a rapid decrease in the electrical resistance leads to dielectric breakdown [227]. Low field (10 MV/cm) time-to-failure (TF), E-model for thin SiO_2 film is given by the relation [214],

$$\ln(TF) \propto [\left(\frac{H_0}{K_B T}\right) - \gamma E_{ox}]. \tag{30}$$

Here, H_0 is the activation energy, K_B is the Boltzmann constant, T is the temperature, γ is the field acceleration parameter and E_{ox} is the oxide field. Eq. 30 gives the mechanism, which is also known as a thermochemical model [207], [233], [234]. For the thermochemical model, they considered the dielectric as a collection of the dipole. They represented the free energy of activation using the above equation as a series expansion of E. Further, McPherson *et al.* reported the molecular origin of the thermochemical model [235], [236] in 1997. Thermochemical model predicts that $\gamma \propto \frac{1}{T}$, which in turn leads to a linear decrease in activation energy with applied electric field [214]. There are many TDDB models which considered temperature-independent γ and a field independent activation energy. The conditions

(or equations) for a very high electric field cannot be applied for low field conditions without changing the physics of failure; otherwise, a very large scale integration (VLSI) circuits will have a strong implication. Now we will try to set the relation between RA product and breakdown voltage. The RA product of the MTJ barrier is exponentially dependent on the thickness (t_{ox}) of the device and has been well established [53]. The relation can be written as [196],

$$RA = Bexp(\alpha t_{ox}) \quad \text{or} \quad \ln(RA) = \ln(B) + \alpha t_{ox}; \tag{31}$$

Here α (unit of the inverse of length) and B are the constant. Dimitrov *et al.* [196] categorized their observation on the MgO barrier by the hard and soft breakdown. The soft breakdown is not intrinsic and happens in a small part of the device. It is due to tunnel junction imperfection, while the hard breakdown is due to the applied electric field when it reaches a critical value. For hard breakdown, when the applied electric field reaches the critical value (E_c) then the breakdown voltage ($V_{breakdown}$) $= E_c t_{ox}$ [196]. Thus eq. 31 can be rewritten as [196],

$$\ln(RA) = \ln(B) + \alpha \frac{V_{breakdown}}{E_c}. \tag{32}$$

It is clear from the above equation that ln (RA) linearly varies with $V_{breakdown}$ for the P and AP configuration of MTJ. Dimitrov *et al.* reported a minimal change (between 0.03 and 0.05 V) in the breakdown voltage by changing the polarity of the device from P to AP. Khan [226] also reported similar values for CoFeB/MgO/CoFeB MTJ by changing the polarity of the voltage bias, but this much small voltage was not suitable for any practical applications [194].

2) EXTRINSIC BREAKDOWN MECHANISM

When large I_s is passed through the ultrathin MgO barrier layer-based CoFeB/MgO/CoFeB MTJ, the pre-existing pinholes formed by the diffusion of boron in the oxide layer start growing due to the localized heating, which leads to the dielectric breakdown. Breakdown in the thinner barrier is dominated by extrinsic mechanisms as compared to intrinsic mechanisms [227], [237], [238]. Extrinsic breakdown can be improved by reducing the roughness of the bottom electrode [227]. It is a current-driven process in which time-to-failure follows 1/E dependency due to the Fowler-Nordheim conduction with the oxide field (E_{ox}) [224], [229], [231]. The model suggests that TDDB data can be selected in microsecond time and then be safely extrapolated back to a 10-year lifetime without the failure of physics. The model is troublesome to explain at E $=$ 0 due to singularity. Since at E $=$ 0, dielectric will not be degraded, and the model will fail to include the thermal (or diffusion) processes of material, cause to fail the second law of thermodynamic ($S \geq 0$). In 1963, Simmons derived a theoretical model which is widely used to find J_{jun} flowing between a similar electrode of metal separated by a thin insulating barrier [73]. It can be observed from Eq. (33) that J_{jun} depends on average barrier height ($\emptyset$), bias voltage (V_{bias}) and barrier thickness (t_{ox}). Here e, $\hbar$, and m_e are the electron charge, reduced Planck's constant and electron mass, respectively.

$$J_{jun} = \frac{e}{4\pi^2 \hbar t_{ox}} \left\{ \left(\emptyset - \frac{eV_{bias}}{2} \right) \times \exp\left[-2t_{ox} \sqrt{\frac{2m_e}{\hbar^2} \left(\emptyset - \frac{eV_{bias}}{2} \right)} \right] - \left(\emptyset + \frac{eV_{bias}}{2} \right) \exp\left[-2t_{ox} \sqrt{\frac{2m_e}{\hbar^2} \left(\emptyset + \frac{eV_{bias}}{2} \right)} \right] \right\} \tag{33}$$

J_{jun} can be easily obtained theoretically from Eq. 33 by substituting the V_{bias}, $\emptyset$, t_{ox}, e, $\hbar$, and m_e. Experimentally, the J-V curve can be easily plotted by varying the V_{bias} applied on MTJ (Fig. 6(a)). Using the curve fitting, one can find $\emptyset$ and t_{ox} simultaneously [238]. Oliver *et al.* discussed the extrinsic mechanism by modeling the MTJ with a pinhole in the barrier as a tunnel magnetoresistor (with resistance R1) in parallel with an ohmic resistor (with resistance R2) [189], [227]. According to Kirchhoff's law, the total bias current (I_{bias}) passing through the MTJ can be represented as the sum of the current passing through the two parallel resistors, residual junction current (I_{res_jun}) and pinhole current ($I_{pinhole}$) (Fig. 21 (a, b)).

$$I_{bias} = I_{res\_jun} + I_{pinhole} \tag{34}$$

The current passing through the residual junction can be calculated using Eq. (33),

$$I_{res\_jun} = J_{jun} \times A_{res\_jun} = J_{jun} \times (A_{initial} - A_{pinhole}). \tag{35}$$

Here, $A_{initial}$ is the total initial junction area before the formation of the pinhole. $A_{pinhole}$ is the area of the pinhole and A_{res_jun} is the remaining area of the junction excluding the pinhole area (or known as residue MgO barrier). Once I_{res_jun} is calculated from the Eq. 35, $I_{pinhole}$ can be calculated from Eq. 34 (since $I_{pinhole} = I_{bias} - I_{res\_jun}$). Once $I_{pinhole}$ is obtained, the current density inside the pinhole is calculated as,

$$J_{pinhole} = \frac{I_{pinhole}}{A_{pinhole}}. \tag{36}$$

Oliver *et al.* reported a resistance model to calculate the effective RA product of MTJ as [239],

$$RA_{effective} = \frac{A_{initial}}{\left(\frac{A_{initial} - A_{pinhole}}{RA_{res\_jun}} \right) + \left(\frac{A_{pinhole}}{RA_{pinhole}} \right)}. \tag{37}$$

Here, RA_{res_jun} is the resistance area product before the breakdown, and $RA_{pinhole}$ is the resistance area product when TMR goes to zero. Now the relation of the pinhole area can be written as [189],

$$A_{pinhole} = \frac{A_{initial} \times RA_{pinhole}}{RA_{effective}} \left(\frac{RA_{res\_jun} - RA_{effective}}{RA_{res\_jun} - RA_{pinhole}} \right). \tag{38}$$

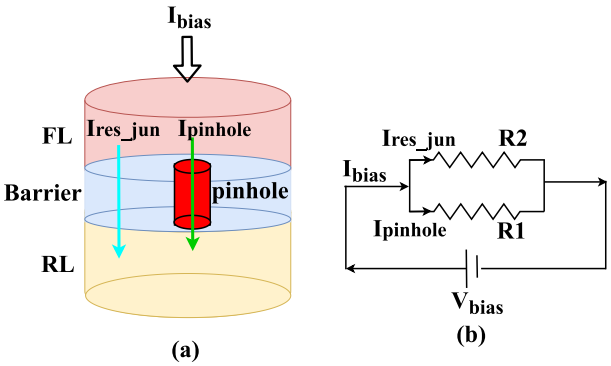


FIGURE 21. (a) Schematic representation of pinhole growth based extrinsic mechanism in CoFeB/MgO/CoFeB pMTJ [227]. (b) I_{bias} is the total current passing through the MTJ, which is equal to the sum of the currents $I_{pinhole}$ and I_{res_jun}.

When pinholes are present, there will be competition between the tunneling current passing through the undamaged part of the junction and the spin-independent current shunted through the pinhole [239],

$$\frac{TMR_{effective}}{TMR_{res\_jun}} = \left(\frac{RA_{effective} - RA_{pinhole}}{RA_{res\_jun} - RA_{pinhole}}\right). \quad (39)$$

Here effective TMR ($TMR_{effective}$) simply follows the $RA_{effective}$, and TMR_{res_jun} is the TMR of the device before breakdown. Recently Lv *et al.* investigated CIMS in pMTJ fabricated with the following parameters; ultrathin (≈50 nm) MgO barrier, TMR = 123.9 %, RA product of 7 $\Omega\mu m^2$ with $J_{C0} = 1.4 \times 10^{10}\ A/m^2$ and 300 nm junction diameter. They reported that breakdown in pMTJ is dominated by the extrinsic mechanism [238], as discussed by the Eqs. (34-39) [189], [239].

TDDB MECHANISM OF PINHOLE GROWTH USING ENERGY BAND DIAGRAM

The breakdown process in MTJ is characterized by increasing the bias current (I_{bias}). It has been experimentally demonstrated that below a certain bias current pinhole area is zero. As the I_{bias} increases, the pinhole area increases linearly and saturates after a critical bias current, which indicates the junction has been completely occupied by the pinhole area [189], [227], [238], [239]. The mechanism of pinhole growth can be divided into three phases,

(i) Initially, when $V_{bias} = 0$, there is no degradation in the barrier height (Fig. 22). In phase 1, by applying I_{bias} the linear increase of voltage indicates the resistance is constant, and there is no degradation in the junction (here $I_{pinhole}$ current = 0).

(ii) In phase 2, As I_{bias} increases significantly, the breakdown happens at a particular voltage, and this voltage is known as breakdown voltage ($V_{breakdown}$). $eV_{breakdown} > Ø$ is the condition of the breakdown, where $V_{breakdown}$ strongly depends on the barrier height Ø (Fig. 23 (a)). With increasing I_{bias} the voltage stabilizes and keeps constant for a large current range can be denoted as stable bias voltage ($V_{b,stable}$). It has been experimentally verified by Lv *et al.* [238] that $V_{b,stable}$ is always smaller than $V_{breakdown}$, which indicates that the initial breakdown is an unsteady state and moves the system to come to a steady-state (Fig. 23 (b)).

(iii) In phase 3, after the complete breakdown of the junction (or barrier), the device performance is completely determined by the metallic pinhole formed inside the barriers. During the pinhole growth, I_{res_jun} decreases, while $I_{pinhole}$ increases (refer Eq. 34), since the pinhole current density is constant and the only way to bypass the additional current is to increase in pinhole area. Once the pinhole expands to the entire junction region, then all the current passes through the pinhole resulting in an ohmic behavior of the device.

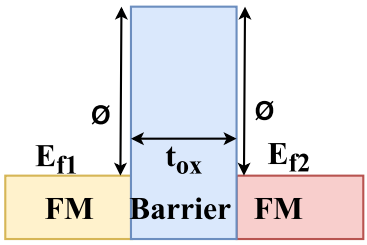


FIGURE 22. Energy band diagram, when no bias voltage is applied. Here Ø is the average barrier height, and E_{f1}, E_{f2} is the fermi levels of FM layers separated by the barrier.

From the above discussion, it can be concluded that the barrier height plays a vital role in barrier breakdown and can be used as a reference value to improve the breakdown performance. A more optimize and efficient method to measure the stability of MTJ under high applied bias reported by Lv *et al.* is to compare the barrier height rather than measuring the statistical barrier height since the latter will permanently damage the samples [238].

VI. HYBRID CMOS/MTJ CIRCUITS

There are various spintronic devices like spin-valve [240], MTJ [81], [241]–[245], ferroelectric tunnel junction (FTJ) [246]–[248], domain wall [249]–[256], Skyrmion [257]–[260] and all spin logic (ASL) devices [261]–[268], etc. have been reported in the literature. We are restricting ourselves towards the design and development of hybrid CMOS/MTJ circuits only, and the discussion on other hybrid circuits are out of scope for this article. In hybrid CMOS/MTJ circuits, MTJ is used due to its important feature of logic computation and nonvolatility, i.e., storing the data for a longer duration even if the power is switched off. Alternatively, it consumes zero static power and has an instant ON-OFF feature, makes it one of the promising candidates for developing the revolutionary STT-MRAM memory as well [24], [41], [43], [98], [116]. The von-Neumann concept was developed in 1940 when the first electronic computers were built [269]–[273]. In traditional von-Neumann architecture, the logic and memory blocks are kept separated, and the communication between them is set up by global

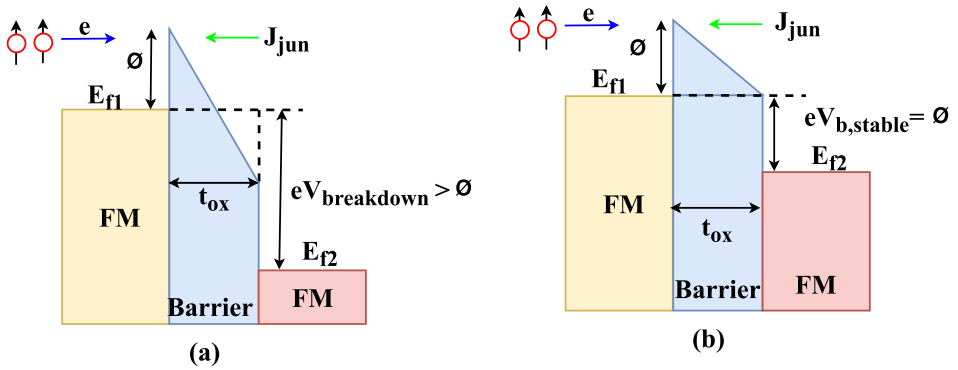


FIGURE 23. (a) Schematic representation of the unsteady state of MTJ pictured as in ref. [238]. It is clear that the breakdown to happen, $V_{breakdown}$ must be greater than $\left(\frac{\emptyset}{e}\right)$. Higher barrier height needs a larger barrier breakdown voltage. J_{jun} is the direction of tunneling current density (green arrow) while electrons are moving in the opposite direction (blue arrow) (b) Represents the steady-state of the MTJ during the breakdown, here $V_{b,stable}$ is equal to $\left(\frac{\emptyset}{e}\right)$. Reproduced from ref. [238].

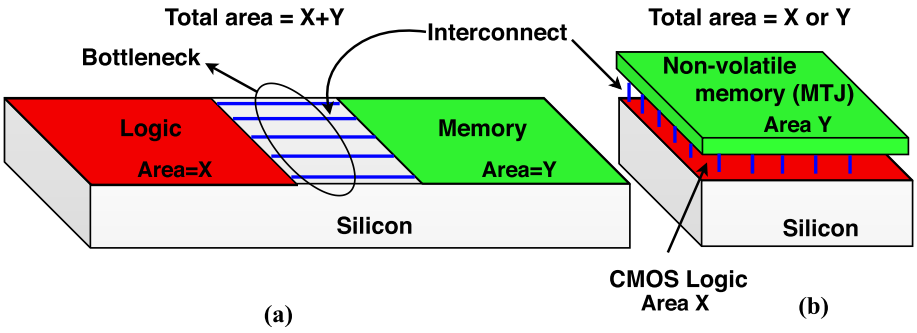


FIGURE 24. (a) Von-Neumann architecture showing the logic and memory block placed separately over the silicon layer. The area occupied by the logic and memory block is X+Y, and the interconnect facilitates communication between them [29]. (b) In general, LIM structure developed using logic, and MTJ blocks reduce the total area to be either X or Y and the global wire interconnect length, which resolves the data transfer bottleneck between memory and logic block [29].

interconnects (Fig. 24 (a)). The major problem of this architecture is the limitation of data transfer bandwidth between these blocks and the large area occupied by them. Another issue is the static power dissipation of the logic block, which increases tremendously in deep sub-micron technology due to scaling. Global interconnects used for signals and clock are also used to drive the large circuits (or higher load) and consumes considerable power. The idea of LIM was initially proposed by Kautz in 1969 [274], and around a year later, an approach for LIM computer was reported by Stone in 1970 [275]. LIM offers the solution by placing the memory block at the top of CMOS logic (Fig. 24 (b)). The use of MTJ spintronic devices in the LIM structure provides nonvolatility, which means if a particular block is not used or it is in an idle state, the power of the block can be switched off completely. There will be almost zero static power dissipation in standby mode. As soon as the block restarts functioning, the data can be recovered instantaneously, so this approach is suitable for ''instant on'' and ''normally off'' system [30]. Another important feature is the easy integration or 3D-stacking of the MTJ at the top of CMOS using 3D metal layers stacking, which reduces the latency and increase the integration density.

Fig. 25 (a) illustrating the separation of a processor (shown by core1 and core2) and memory blocks (shown by memory 1 and memory 2) using von-Neumann architecture. In the growing phase of LIM, the logic blocks were placed near to memory in a 2D plane or by 3D stacking of more memory block above the logic block without reducing the memory access [23], [276]–[279]. This approach is known as logic-near-memory (LNM) (Fig. 25(b)) and seems to be very similar to LIM. LNM can reduce communication bottleneck between logic and memory [280]. Still, the only difference is that in LIM structure, the innovative computing architecture reduces the global routing and data transfer time between memory and logic block (or reduces the number of access from memory blocks) by the integration of MTJ with CMOS logic (Fig. 25 (c, d)). Various similar kinds of technology are reported in the literature and have been named differently [281]–[283]. Other than that, attempts

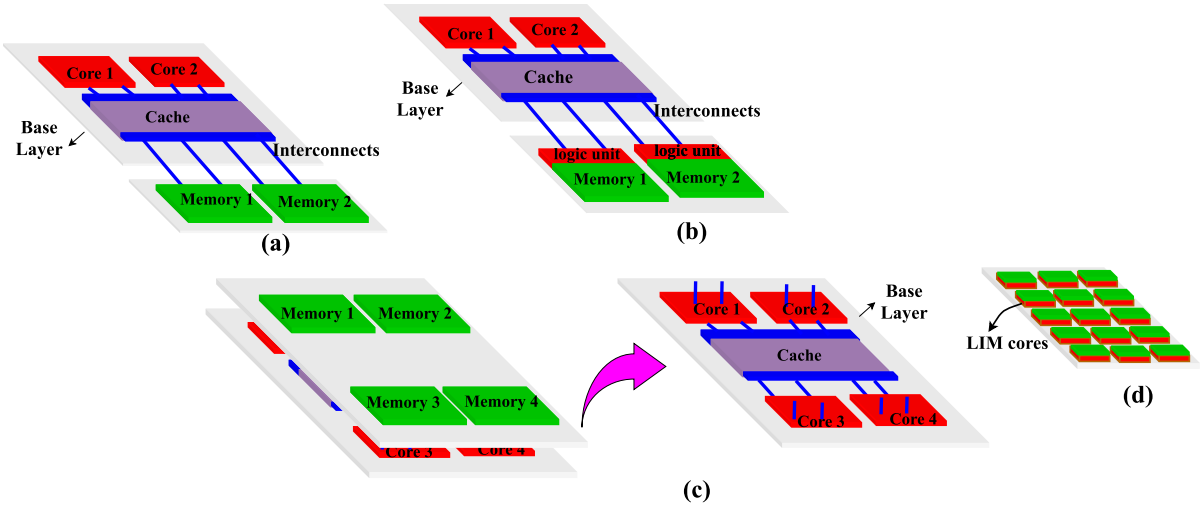


FIGURE 25. (a) A conventional von-Neumann architecture, where core1 and core2 are kept separately to memory 1 and memory 2. (b) An initial phase of LIM, where the logic units are added to memory 1 and memory 2 similar to LNM. (c) Another representation of LNM showing 3D stacking of memory blocks above the cores, where the base layer has been separated for visibility of cores. (d) LIM structure in which LIM cores are distributed all around the die, here the memory and logic are on the same die with the smallest grain. Reproduced using the refs. [276] and [281].

are being made to develop novel spintronic based reconfigurable logic-memory devices [284]–[287]. An innovative multilayer magnetic device Ta/CoFeB/MgO, which combines logic and memory operations, was proposed by Luo *et al.* in 2017. It utilizes both the AHE and negative differential resistance (NDR) phenomenon to perform the various reconfigurable logic operations. It can work at a high speed of GHz range with low energy consumption and expected to break the bottleneck of conventional von-Neumann architecture [285]. At the time of writing this article Pu *et al.* reported the new magnetic logic-memory device by coupling the AHE in magnetic material and insulator-to-metal (ITM) transition in Vanadium dioxide (VO2). Their device showed an improvement in switching speed (switching time of $1 \sim 10$ *ns*) with high reliability and a low magnetic field (<20 mT) [286]. Recently, Rectified-tunnel magnetoresistance (R-TMR) is another novel device fabricated by integrating PMA double interface MTJ and Schottky diode for in-memory computing (IMC). This work is expected to promote more practical applications of R-TMR based spintronic devices for IMC [287]. Other than that, few unconventional spintronics paradigms, e.g., reservoir computing, probabilistic computing, and memcomputing, etc. are also emerging [288].

Fig. 26 represents the schematic of the hybrid circuits based on LIM architecture [31], [99], [289], [290]. Three main components of this architecture are,

(i) *Read circuit*- Sense amplifier is a read circuitry which is used to read the data stored in the pair of MTJ. In general, the pair of MTJ is in opposite nature means either AP-P state or vice versa. Hence an MTJ can be modeled as a nonlinear resistor [29], [291]. Reading operation is possible only due to the inherent property of the MTJ, i.e., AP resistance is always larger than the P resistance.

A wide variety of sense amplifiers, for e.g., dynamic current-mode sense amplifier [290], SRAM based sense amplifier [292], and a precharge sense amplifier (PCSA) [293], have been reported in the literature. The basic idea behind all the current-mode sense amplifiers is to measure the difference of the current passing through two branches in which the pair of MTJ is connected in parallel. A significant amount of the difference of current in both the branches are needed to read the signal without distortion. I_L current in left branch and I_R current in the right branch directly depends on the sum of the total resistance of nMOS logic trees and MTJs associated with each path. As the resistance difference of the MTJ is directly related to the TMR ratio, higher TMR is always needed for the faithful operation of hybrid CMOS/MTJ circuits. This characteristic helps to integrate MTJ with the current-mode sense amplifier [294] that detects the MTJ state and amplify the output to state the proper logic. PCSA consists of seven MOS transistors and is capable of reading the state of a pair of MTJ in very less time $\approx$200 *ps*. Specifically, the sensing reliability ($\sim 10^{-5}$), sensing speed ($\sim$124 ps/bit), and sensing power consumption ($\sim$1 fJ/bit) were calculated by performing the simulation using a 90nm ST microelectronics design kit [293]. As the technology node is scaled down or below 40 nm, the sensing reliability becomes worse and further affects the hybrid circuits. It is due to the reduced power supply (V_{DD}) and a large number of process variations. Later a highly reliable process tolerant sensing circuit with a significant read sensing margin was reported by Kang *et al.* for deep submicron technology using the STT-MTJ model [295]. Further, the same group developed a separated precharge sensing amplifier (SPCSA), which improved the sensing reliability by 100 times of PCSA while retaining the other advantages like low power and higher speed [296]. But it still suffers from the sensing margin

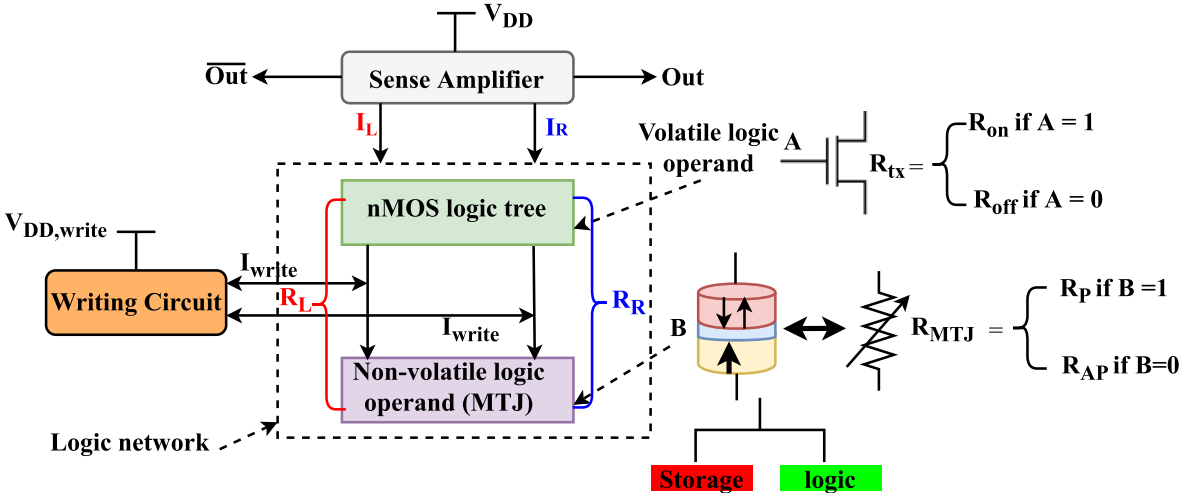


FIGURE 26. Generic LIM architecture to develop the hybrid CMOS/MTJ circuits. Here nMOS logic tree block contains nMOS transistor while the NV logic block contains MTJs. A writing circuit block generates enough I_{write} to write the data in MTJs. R_L and R_R is the sum of total resistance due to the resistance of the nMOS transistor and the MTJs in the left and right branch, respectively. MTJ is used for both storage and logic implementation purposes. Here, A and B are assumed two logical operands of the function. Reproduced using the refs. [276] and [281].

issue affected by the process variation and can produce the sensing error. Recently Zhang *et al.* proposed the reliability enhanced PCSA (RESPCSA) to achieve a large sensing margin. The results were compared with SPCSA for 150% TMR, 10% process variation, 40 nm technology library, and using the same STT-MTJ model. They reported zero sensing error rate with a slight increase in the number of transistors, sensing energy per bit, and sensing delay, respectively [297]. Among all, the PCSA based sense amplifier became quite popular and widely used to develop the various hybrid CMOS/MTJ circuits.

(ii) *Write circuit-* It is used to write the values in pair of MTJ. A pair of MTJ is needed to store the one-bit value, which is read later by various types of sense amplifier, as discussed above. Various write circuits have been developed to write the data values in pair of MTJ. Again the circuitry was different based on the type of switching mechanism used in MTJ [298]–[301].

A brief explanation of read/write operations of basic hybrid circuits have been discussed in Appendix B. For STT switching to take place, the average critical current (I_{C0}) required to be in the range of $I_{C0} < 50\mu A$ for 28nm technology [302]. 4T and 8T writing circuits have been reported in the literature [99], [302] according to the requirement of bidirectional write current (I_{write}). 4T write circuit is the simplest, while 8T write circuit generates the larger I_{write} and the smallest delay. All the hybrid circuit suffers the long writing delay, an obstacle to operating with higher clock frequency operation. From a circuit perspective,

- Increase in supply voltage ($V_{DD,write}$) of the writing circuit increases the write current, which decreases the write delay but impacts the power dissipation, since $P \propto V^2_{DD,write}$. However, $V_{DD,write}$ is always kept at higher voltage compared to supply voltage of sense amplifier (V_{DD}) (refer to Fig. 26).
- As all the write circuits are build using nMOS and pMOS transistors, so the magnitude of I_{write} is inversely proportional to the width (W) of the transistors [303]. Hence an increase in W increases I_{write} and improve the writing delay at the cost of area overhead.

An appropriate novel write circuit needs to be developed, which produces large I_{write}, less power dissipation with improved writing delay, and minimum area.

(iii) *Logic network-* It plays a significant role in implementing the logic function. Any function can be implemented using the volatile nMOS logic tree and non-volatile MTJs. All the input variables of the functions are given as input to the nMOS transistors and MTJs. Due to its inherent nature of nonvolatility and the different resistance value for both P and AP states, an MTJ is used for input logic variable and also store the data for a longer period even if the power is switched off. The nMOS transistor is switched ON (if $V_{gs} > V_t$) for A $= 1$, and its ON resistance, $R_{on} \approx K\Omega$. The nMOS transistor is switched OFF ($V_{gs} < V_t$) for A $= 0$, and its OFF resistance, $R_{off} \approx G\Omega$. While the state of the MTJ is represented by R_P or R_{AP} corresponds to logic operand B $= 1$ or 0, respectively (Fig. 26). In general, ON resistance of the NMOS is less than P state resistance of the MTJ; $R_{on} < R_p$. While OFF resistance of the NMOS is more than the AP state resistance of MTJ; $R_{off} > R_{AP}$. The actual value of R_p and R_{AP} depends upon TMR of the MTJ represented by Eq. 1.

Let us assume that the total resistance (resistance due to nMOS logic and MTJ) and the current flowing in the left side

and right side path is R_L, I_L and R_R, I_R respectively. The two outputs (Out and $\overline{Out}$) give the true and complementary value simultaneously based on the current flowing in the left and right paths. If the total resistance in the left path is more than the right path i.e. $R_L > R_R$ (or $I_L < I_R$) the right side path is faster than the left side path pulling Out node quickly to the logic '0' and $\overline{Out}$ to logic '1'. Similarly, if $R_L < R_R$ (or $I_L > I_R$) the left side path is faster than the right side path, will pull the $\overline{Out}$ node quickly to the logic '0' and Out to logic '1'.

Various hybrid CMOS/MTJ circuits are realized using this approach, a few of them are NV-NAND/AND, NV-NOR/OR and NV-XNOR/XOR [241], [304], magnetic flip-flops [305], [306], magnetic look up table [92], [307], magnetic full adder [31], [289], [302], [308]–[311], magnetic decoder [312], magnetic true random number generator [313]–[315], magnetic arithmetic logic unit (ALU) [316], [317] and magnetic cryptographic circuits [318] etc.. Due to high magnetic sensitivity of MTJ, hybrid circuits are further used in developing the magnetic sensors [14], [319], [320], NV-FPGA circuit [92], [321]–[330], NV-ternary content addressable memory (TCAM) memory [331]–[338], NV random access logic LSI unit [38], [339], ultra-low-power VLSI design processor [30], [38] and various other applications in the next generation computing era of Internet of things (IoT) [340]–[342].

VII. SUMMARY AND OUTLOOK

It is an extension of our previous review article, where we had reviewed various emerging spintronic devices [8]. We hope that the present article will inspire the young researchers of the various interdisciplinary area and work as an introductory reference guide for them due to its broad coverage from the device level to the development of hybrid circuits. This article is an effort toward one of the emerging low power techniques developed by the combination of MOS transistors and one of the popular spintronic devices, MTJ, due to its salient features from a circuit perspective.

Starting with MTJ construction, its high and low resistance states are discussed, which directed to use MTJ as a variable resistor that can represent the two meaningful logic states either '0' or '1' for logic computation. Following the spin polarization equation, FM and paramagnetic (or normal metals) materials are characterized by the energy level (E-K) diagram using the S-W model. TMR, a quantum mechanical effect, and consequence of spin-dependent tunneling between FM layers through the barrier layer are also represented in terms of spin polarization. High TMR is needed to read the stored data in MTJ for a reliable read operation in a hybrid circuit. An essential concept of MTJ, MA, is discussed by approximating the equation of MAE by its volume and interface contribution. A typical example of the Pd/Co multilayer consists of an ultrathin layer of Co (2-12 A^0) that has been taken to understand the MA in multilayers. A plot between ($K_{eff}.t$) versus (t) has been plotted. For $K_{eff} > 0, t < t_{Co}, K_i$ is more dominant than K_v; hence PMA occurs. While for $K_{eff} < 0, t > t_{Co}$ the negative slope indicates K_v, hence IPA occurs.

MTJ writing in a hybrid circuit is a necessary process that depends on various switching mechanisms. A quite significant review of different switching mechanisms FIMS, TAS, STT, SHE, STT+SHE, VCMA is well discussed in this article. Landau–Lifshitz–Gilbert-Slonczewski equation is revisited to understand the magnetization dynamics of the FL in the STT switching mechanism. For developing the hybrid circuit, a thorough MTJ model is required, which holds almost all the characteristics and the physics of the MTJ device. Timely updation of the model is another essential requirement. Its easy integration with CMOS using EDA tools will speed up the commercialization of hybrid circuits. A small but significant section on the history and development of various MTJ model has been highlighted. Reliability being one of the critical issues of hybrid circuits, cannot be neglected, so to get a feeling, we start with the basic failure rate bathtub curve used in an IC for reliability analysis. We elaborated on both intrinsic and extrinsic breakdown mechanism and tried to interpret the physics of the E and 1/E model. To have a better understanding, the pinhole growth extrinsic mechanism has been revisited, and the corresponding energy band diagram is discussed for MTJ build of CoFeB electrodes separated by an ultrathin barrier layer of MgO. Finally, the design of LIM based hybrid circuits is discussed.

Moreover, there are various abstraction levels to reach up to system-level, but we have reinvestigated only three important perspectives from material, modeling, and circuit point of view, respectively. In brief, challenges and future prospects at each of these levels are summarised,

1. *From the material perspective-* Find the materials which have high anisotropy, lower damping constant to have better thermal stability. The goal is to achieve the 100% spin injection/detection, and much effort is needed to improve the spin injection and detection efficiency at the interface between the FM layer and tunneling barrier. Material interface properties between the FM layer and the barrier need to be explored to reduce the conductivity mismatch issue. TMR, one of the important characteristics of the MTJ, depends on the type of material used for FL, RL, and tunnel barrier. In general, crystalline MgO with band match structures is preferred over the amorphous AlO_x barrier. The highest TMR reported is 604 % at 300 K and 1144% at 5 K using CoFeB electrodes with the MgO barrier [56]. For error-free read operation in hybrid circuits, MTJ with higher TMR is required. Again MTJ using different switching mechanisms have different requirements. Particularly,
   (i) In STT switching lower threshold current I_{C0} is one of the requirements and can be achieved by using the material with low α, γ, and high g. But reducing I_{C0} corresponds

to higher speed and low power consumption during a write operation (Eq. 21). At the device level, double-barrier MTJ [343]–[345] and double-interface-MTJ, [346], [347] a variant of MTJ, reduce the I_{C0} compared to single barrier MTJ having the same device structure. The interfacial-anisotropy MTJ with double CoFeB(or FeB)/MgO interface structure achieve low I_{C0} and increases Δ by a factor of two due to an increased net anisotropy [346], and allows scaling of MTJ down to around diameter D = 20 nm [347]. Reducing D after 30 nm degrades Δ and limit its use, since, for non-volatilty, Δ for the FL needs to be more than 40 [121]. Shape anisotropy MTJ is the recent development [348], [349] to overcome this scaling issue while maintaining Δ. Here the magnetization switching is solely achieved by current without changing the material for the device. By revisiting the shape anisotropy MTJ and increasing the thickness of FL, Δ can be achieved more than 80 at a 10 nm scale [348].

(ii) In SHE assisted switching the need of large η_{SH} depends on the type of material and is given by Eq. 24. Magnitude of $\vec{J}_s$ depends on the size and type of heavy nonmagnetic metal layer (highly resistive layer with large spin-orbit coupling parameter) above which FL of MTJ is grown.

(iii) In VCMA assisted switching, the switching characteristics vary with a thickness variation of the barrier and the effect of anisotropy. Due to the electric field generated by the applied bias voltage, the spin-orbit interaction at the interface modifies the MA. High MA is preferred for storing the information while, on the other side, the requirement of low MA enables the capability of magnetization switching of MTJ with low power dissipation.

2. *Modeling perspective*– Being an important part of the hybrid circuit, the availability of open-sourced non-proprietary MTJ models are needed for creating interest for young researchers. However, few websites are available, but there is no appropriate single MTJ model available as a reference for circuit designers, which can cover all the characteristics of MTJ (refer section 4). As the research of MTJ is progressing, such a timely review and simultaneously update of the model are the two essential requirements to execute a more realistic design using EDA tools. Another essential requirement is the type of language through which the model is developed, its integration with other technology, and the type of simulator on which it would be executed.
3. *Circuit perspective*- Various hybrid CMOS/MTJ circuits have been reported in the literature since the last two decades in which MTJ is switched by different switching mechanisms timely (mainly STT, SHE, and VCMA effect). The design of low power reduced transistor count, and MTJs, less switching delay, reliability aware, and radiation-hardened novel hybrid circuits are challenging. Reliability, an important characteristic, affects the performance of hybrid circuits and hinders their commercialization process. The other issue is that the circuit developed using the MTJ model may have mismatch or process variation, which may change the performance of the hybrid circuits. During the read operation, the use of a sense amplifier to read the state of the MTJ needed a higher TMR ratio, which depends on the resistance difference between the left and right path. The requirement of a large write current (I_{write}, around μA) to write the value in MTJ reduces the switching delay. In general, while designing to achieve a large I_{write}, the power supply of the write circuit is kept high as compared to the power supply of the sense amplifier.

The use of MTJ brings nonvolatility features in a hybrid circuit. Due to that, we can completely cut-off the power supply without losing the bit stored in MTJ, which eliminates static power dissipation. As soon as the power is switched on, there is no restore operation required for MTJ. Hence the MTJs do not contribute to the additional delay in producing the outputs. While, on the other side, for CMOS based circuits, since complete cut-off of the power supply is not permitted, there will be a significant static power dissipation. These are the major advantages of hybrid circuits over volatile CMOS design. The realization of the MTJ based hybrid circuit is a challenging task and required precise techniques for fabrication [350]. Further, thanks to the 3D integration feasibility of MTJs over CMOS at the back-end process, it reduces the area occupied on silicon and shortens the distance between memory and logic unit in SoC. There is much scope at the backend process to improve, and the intense investigation is required to fabricate more precise prototypes [28], [339], [351]–[353].

From a future perspective, we have highlighted hybrid CMOS/MTJ circuits, which can be further used to develop the ultra-low-power VLSI processor. Moreover, a group of people in Japan expects to realize brain-inspired computing, an example of a nonclassical computing paradigm, using a spintronic device based VLSI design style [30]. Another group of people from the center for brain-inspired computing (C-BRIC) at Purdue University is using MTJ as stochastic neurons and synapses for stochastic computing [354], [355]. Similarly, one more group of people in the CNRS/Thales lab in France is trying to demonstrate how spintronics nanodevices can be used for bioinspired computing [356].

Another well-established area expanding beyond the development of NV logic is the NV STT-MRAM memory, and recently 1 Gb STT-MRAM (ST-DDR4) chip family named as EMD4E001G was manufactured by Everspin technologies [41]. Due to the latest progress in MRAM fabrication [357], [358], ultra-high-density embedded STT-MRAM

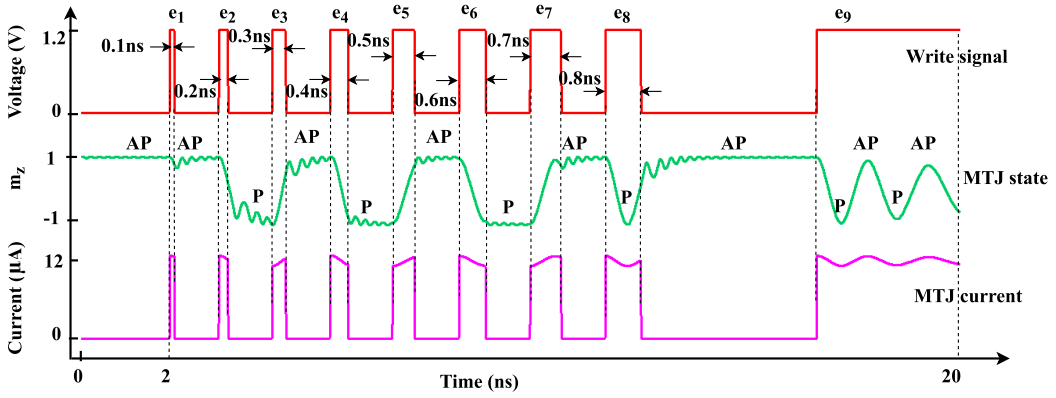


FIGURE 27. Requirement of the write signal and change in magnetization of the FL along z-direction for pMTJ using a precessional VCMA switching mechanism [160].

has opened the way for its use in industrial-grade microcontroller unit (MCU) and IoT applications [359]. MTJ with a high-performance MgO barrier can also be used for flexible wearable spintronic applications, especially for biomedical sensing in early disease diagnosis of HIV-1 antigen p24 [360], low field sensitive sensor for neuronal signal detection, and design of versatile sensors for omnidirectional detection of skin decease. Further, hybrid circuits developed using MTJ have a diversified application due to its ultra-low-power dissipation capability in circuits used in RF communication, energy harvesting, IoT, artificial intelligence-based devices, biosensor, quantum computing computers, and cryogenic nonvolatile RAM [361].

APPENDIX A

To understand the requirement of various pulses used in VCMA switching strategies, we simulated the VCMA-MTJ model file open-sourced in the Spinmodel library using the Cadence tool [362]. For the selected model, if $V_{app} > V_{crit}$ (= 1.0V), the VCMA effect is observed, while for $V_{app} < V_{crit}$ (= 1.0V), the STT effect is observed. Precessional VCMA, precessional VCMA-assisted STT, and thermally activated VCMA-assisted STT switching mechanisms [76], [160] are discussed by simulating the VCMA-MTJ model [362]. Due to the unavailability of the VCMA-assisted SHE MTJ model, we have redrawn the results of previously reported work by Kang *et al.* in 2016 [152].

A. PRECESSIONAL VCMA SWITCHING MECHANISM

In precessional VCMA switching, the effect of the electric field has been used other than STT. Fig. 27 represents the transient analysis of MTJ by applying the write voltage signal of amplitude 1.2 V with various pulse widths of 0.1ns, 0.2ns, 0.3ns, 0.4ns, 0.5ns, 0.6ns, 0.7ns, and 0.8ns. The first epoch (e_1) of width 0.1ns is started at 2ns, but there is no switching in magnetization state (m_z) of FL of MTJ. Further, as the epochs e_2, e_3, e_4, e_5, e_6, and e_7 of the different pulse widths come to its way, the FL state of the MTJ starts changing from AP to P and vice versa accordingly. There is no change in the state of the MTJ for the event e_8. It can be noticed that further increasing the pulse width of the write signal for epoch e_9, m_z of MTJ keeps oscillating between AP-P and damped further. The current flows in MTJ can be simultaneously noticed from the waveform. There is a small variation in the current waveform (pink color) due to the bias effect of the MTJ.

B. PRECESSIONAL VCMA-ASSISTED STT SWITCHING MECHANISM

This model has a lower requirement on the accuracy of the pulse width and can switch the state of the MTJ for smaller pulse width along with V_L where precessional VCMA was failed. The applied signal for precessional VCMA-assisted STT switching is the combination of two voltage pulses, high voltage pulses (V_H) followed by a low voltage pulse (V_L) of different amplitude (Fig. 28 (a)) [164]. The use of V_L also removes the use of an external magnetic field required for magnetization switching in precessional VCMA-assisted STT switching, which makes the design much simpler to be used in MRAM. First voltage pulse V_H induces the precessional oscillation due to the VCMA effect, while V_L determines the polarity and stabilizes the magnetization of the FL owing to the STT effect. Suppose the polarity of the VL is same as that of the VH. In that case, switching takes place from AP to P, or else when the polarity of the V_L is negative, MTJ switches from P to AP. Fig. 28 (b) also shows the applied voltage pulse across the MTJ terminals (T1 and T2), and the corresponding magnetization switching from P to AP or AP to P. MTJ switching delay can also be affected by varying the amplitude of the V_L pulse. It is noted from Fig. 28 (b) that the optimum value of V_H is 1.2V with 0.2ns duration, and V_L is 0.8V with 0.4ns duration for the effective switching action [152]. Transient analysis of the model is performed under the above-specified voltage pulse of the write signal.

C. THERMALLY ACTIVATED VCMA- ASSISTED STT SWITCHING

In this case, the amplitude of the applied voltage pulse follows the condition of $V_{app} < V_{crit}$. In addition to a voltage pulse,

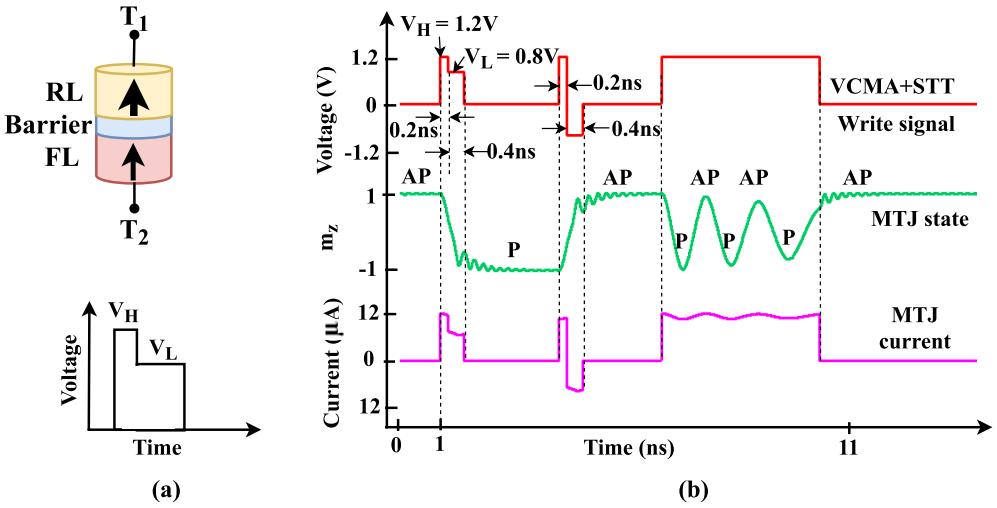


FIGURE 28. (a) MTJ and applied signal for precessional VCMA-assisted STT switching. Application of V_H reduces the energy barrier E_b, then V_L is applied for the switching action to take place. (b) Transient analysis of MTJ switching waveform for precessional VCMA-assisted STT switching (polarity of V_L will decide the state of the MTJ) [160].

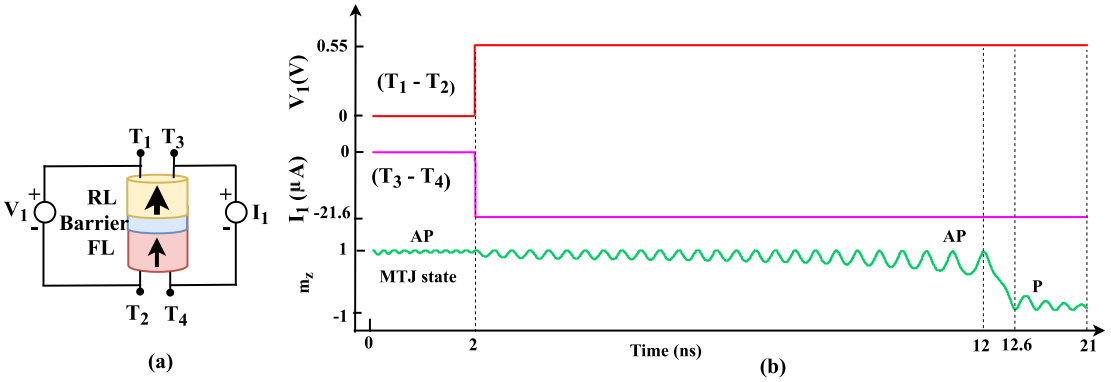


FIGURE 29. (a) MTJ Schematic of thermally activated VCMA-assisted STT switching model used for simulation. A voltage source (V_1) and current source (I_1) are applied to the terminals T_1-T_2 and T_3-T_4. (b) Transient simulation of thermally activated VCMA-assisted STT switching model from ref. [160], [362].

an STT current pulse is needed for switching. Either the voltage pulse or current pulse alone cannot switch the magnetization within the pulse duration, but the combination of both the pulses is able to achieve deterministic switching. The use of voltage pulse first lowers down the energy barrier due to the VCMA effect, while the current pulse used in the STT effect accelerates the switching process by strengthening the thermal activation effect. This method dissipates the highest dynamic energy per bit and the largest switching delay as compared to the techniques (i) and (ii) discussed above [160], limiting its application in MRAM design. In this model, both the voltage and current sources are applied through the terminals T1-T2 and T3-T4, respectively (Fig. 29 (a)). As shown in Fig. 29 (b), the voltage pulse of amplitude 0.55V and STT current pulse of 21.6μA (the STT current density reported in the model is $J_{STT} = 1.1$ MA/cm^2) are simultaneously applied at 2 ns. The magnetization state of the MTJ starts switching from AP state at 12 ns and reaches to P state at 12.6 ns, as shown in Fig. 29 (b).

D. PRECESSIONAL VCMA- ASSISTED SHE SWITCHING MECHANISM

In precessional VCMA-assisted SHE switching-based MTJ devices, the precessional VCMA effect is induced by applying the write signal of required voltage pulse at terminal T_2-T_3, which reduces the barrier height. Further, SHE current pulse is applied at terminals T_1 and T_3 to switch the magnetization of FL state of the MTJ (Fig. 30 (a)). Instead of applying the individual voltage or current pulse, a single combined signal of both can also be used. Kang *et al.* in 2016 developed the magnetic NV flip-flop and compared the results using pure STT, STT assisted SHE, VCMA assisted STT, and VCMA assisted SHE switching mechanisms [152]. They reported that VCMA assisted STT switching mechanism is the best in terms of delay, energy, and energy-delay product compared to other switching mechanisms. In particular, For VCMA assisted SHE switching mechanisms, they choose the write signal of voltage pulse of 1V amplitude with 1 ns width, which is applied to T_2-T_3 (or T_1) to induce the precessional

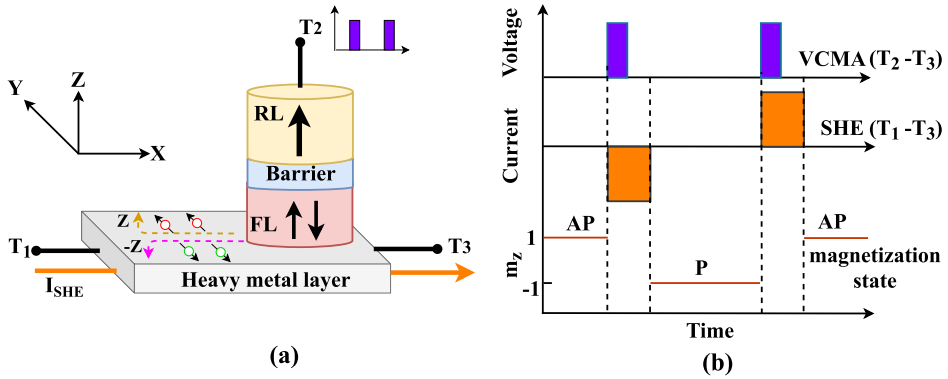


FIGURE 30. (a) Schematic of the precessional VCMA-assisted SHE switching based MTJ with three terminals T_1, T_2, and T_3. (b) Write voltage signal is applied through terminals T_2-T_3, followed by the SHE current passed through the heavy metal between T_1-T_3 terminals. The change in magnetization (m_z) of FL along z-direction from AP to P than AP for pMTJ has been shown for ease of understanding (waveforms are not in scale and reproduced using the ref. [152]).

VCMA effect. In addition to that, a bidirectional current pulse of a particular shape, as shown in Fig. 30 (b) of 2ns is applied between T_1-T_3, which generate a magnetic field of 2.2×10^{11} Amp/m. Initially, the magnetization is in AP states, and by using both the signals, it will be changed to P state.

APPENDIX B

To understand the complete working of hybrid circuits, we have redesigned three 2 input NV-NAND/AND, NV-NOR/OR, NV-XNOR/XOR hybrid circuits from literature using LIM architecture [308]. Further, these circuits are simulated using the Cadence tool with gpdk 45 nm technology library and using the STT-PMA-MTJ model [363]. Three main components of LIM architecture are read circuit, write circuit, and logic network. First, we discussed the read/write operation of MTJ and the circuitry involved in that. From the literature, we choose the PCSA for reading [293] due to its simple architecture and working. The conventional 4T writing circuit is selected to produce a significant I_{write} to change the state of MTJ [302].

A. READ CIRCUIT

Read circuit is used to read the stored bit in MTJs. PCSA consists of 7 MOS transistors and a pair of MTJs. P2, N1, and P3, N2 forms inverter pair whereas P1, P4 are the precharge transistor, and N3 is the evaluation transistor. The state of MTJ pair is always opposite in nature. When MTJ1-MTJ2 is in AP-P state, respectively, it is assumed to store a bit as logic '0', whereas when MTJ1- MTJ2 is in P-AP state, we consider the stored bit as logic '1'. In Fig. 31, MTJ1-MTJ2 pair is assumed in AP-P states, respectively, to be storing a bit '0'. The read circuit works in two phases; precharge phase and evaluation phase.

(i) *In precharge phase-* clock signal (CLK) is at logic '0', Transistors P1, P4, N1, N2 are ON, and transistors P2, P3, N3 are OFF, which sets *OUT* and $\overline{OUT}$ to be at logic '1'. Since the evaluation transistor N3 is OFF, there is no path to discharge the output nodes to the ground (GND). Hence both outputs, *OUT* and $\overline{OUT}$ remain at logic '1'.

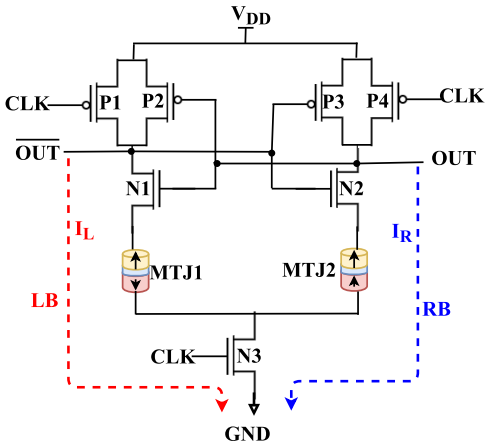


FIGURE 31. Schematic of the current mode PCSA to read the stored value in pair of MTJs. When MTJ1-MTJ2 is configured as AP-P state, *OUT* and $\overline{OUT}$ reads logic '0' and '1', respectively. Reproduced from ref. [293].

(ii) *During the evaluation phase-* CLK signal is at logic '1', which turns the transistor N3 to be ON. This provides a path for *OUT* and $\overline{OUT}$ nodes to GND. Hence current I_L in the left branch (LB) and I_R in the right branch (RB) begins to flow toward GND. But the speed of discharging the *OUT* and $\overline{OUT}$ nodes are different due to the different resistance of MTJ1 and MTJ2. Here AP state of MTJ1 offers high resistance, whereas the P state of MTJ2 offers comparatively less resistance for the I_L and I_R current, respectively. Let the resistance in LB and RB is $R_L(\approx R_{on,N1} + R_{AP})$and $R_R(\approx R_{on,N2} + R_P)$, respectively, while common resistance of transistor N3 has not been included for convenience. As $R_{AP} > R_P$, so $R_L > R_R$, hence I_R is larger thanI_L. This pulls down the *OUT* node quickly to reach the threshold voltage of P2 ($V_{GSp} \leq V_{tp}$; here V_{tp} is the threshold voltage of P2 transistor). As a result, P2 is turned ON, so the $\overline{OUT}$ pulled-up to logic '1'. Whereas

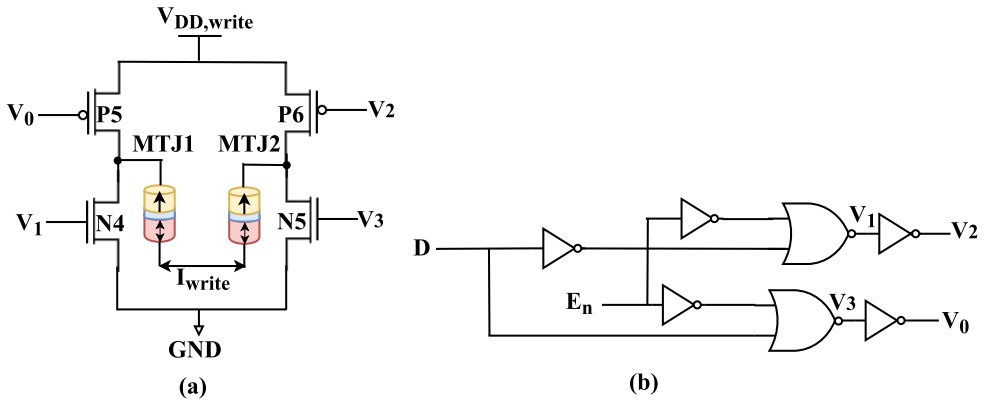


FIGURE 32. (a) 4T-MTJ writing circuit [99], [302]. (b) Control circuit for controlling the I_{write} [99], [302].

TABLE 2. Control inputs, intermediate signals, and the corresponding MTJ states for write circuit [302].

Control inputs		Intermediate signals				MTJs state	
E_n	D	V_0	V_1	V_2	V_3	MTJ_1	MTJ_2
0	X	1	0	1	0	X	X
1	0	0	0	1	1	AP	P
1	1	1	1	0	0	P	AP
Note- X represents the don't care condition							

OUT node continues to discharge to GND and reaches logic '0'. Hence the reading of the bit '0' stored in the MTJ takes place when the MTJ pair is configured as AP-P configuration. When the MTJ pair is configured as P-AP, then *OUT* and $\overline{OUT}$ nodes read logic '1' and logic '0' respectively.

B. WRITE CIRCUIT

In the read circuit, we always use a pair of MTJs having opposite states to store a bit. I_{write} current is used to store/write a bit into the MTJ pair. The I_{write} current should switch both the MTJs together. In 4T writing circuit P5, P6, N4, N5 (Fig. 32 (a)), transistors are used for writing MTJ pair. These transistors are controlled by intermediate signals V_0, V_1, V_2, V_3 generated by the control circuit shown in Fig. 32 (b) [99]. Two transistors P5 and N5 are ON during the write operation, while the other two transistors P6 and N4, are OFF or vice versa. This will enable the bidirectional current to flow. A control signal (E_n) is used to control the writing process, and signal D is used to control the direction of I_{write} current. When E_n signal is '0', no writing action takes place. Table 2 shows various control signals, intermediate signals generated, and the corresponding MTJs states.

C. LOGIC NETWORK

This is the most important module through which the required function is implemented. It can be noted from Fig. 33 (b), (c), and (d) that among all the inputs, one of the inputs is stored in MTJ pair, whereas the rest of the inputs are provided as inputs to the nMOS logic tree. A quite good analysis of the various structure designed for basic logic gates has been reported using the resistive switching mechanism [308]. Two input NV-NAND/AND, NV-NOR/OR, and NV-XNOR/XOR hybrid logic gates have been designed using LIM architecture and verified through circuit simulation. A brief explanation of their operation has been discussed below.

D. DESIGN OF NV-NAND/AND LOGIC

Fig. 33 (b) shows the logical part of the NV- NAND/AND logic gate developed using LIM architecture. Both outputs NAND and AND are produced simultaneously by using true and complementary inputs A and B. Transistors P1, P2, P3, P4, N1, N2, N3 form the PCSA. N4, N5, N6 transistors, MTJ1, and MTJ2 form the logic network. Inputs B, $\overline{B}$ are stored in the MTJ, whereas input A and its complement are applied to nMOS transistors. Assume one of the input combination A= '1' and B= '0', to make B = '0' the pair of MTJ1-MTJ2 is set to AP-P state, respectively. The working of the hybrid *NV-NAND/AND* circuit can be explained in two phases,

(i) *Precharge phase*- here, CLK is set to '0'. In the PCSA part, transistor P1, P4, N1, N2 are ON, whereas P2, P3, and N3 are OFF. Both NAND ($\overline{OUT}$) and AND (*OUT*) output nodes are pulled-up to V_{DD} or logic '1'.

(ii) *Evaluation phase*- here CLK becomes '1', N3 is ON, and transistors P1, P4 is OFF. The output nodes discharge through the evaluation transistor N3 and the logic network. In the logic network part, transistors N4, N6 is ON, whereas N5 is OFF. So, there is a path for both outputs to discharge to GND. But the output discharge process will depend on the resistance offered by the left branch (LB) and right branch (RB). Since MTJ1 is in AP state and MTJ2 is in P state, so the resistance of MTJ1(R_{MTJ1}) is higher than the resistance of the MTJ2 (R_{MTJ2}), i.e., $R_{MTJ1} > R_{MTJ2}$. Hence, the NAND output node sees a high resistance path in LB for the discharge current (I_L), compared to the AND

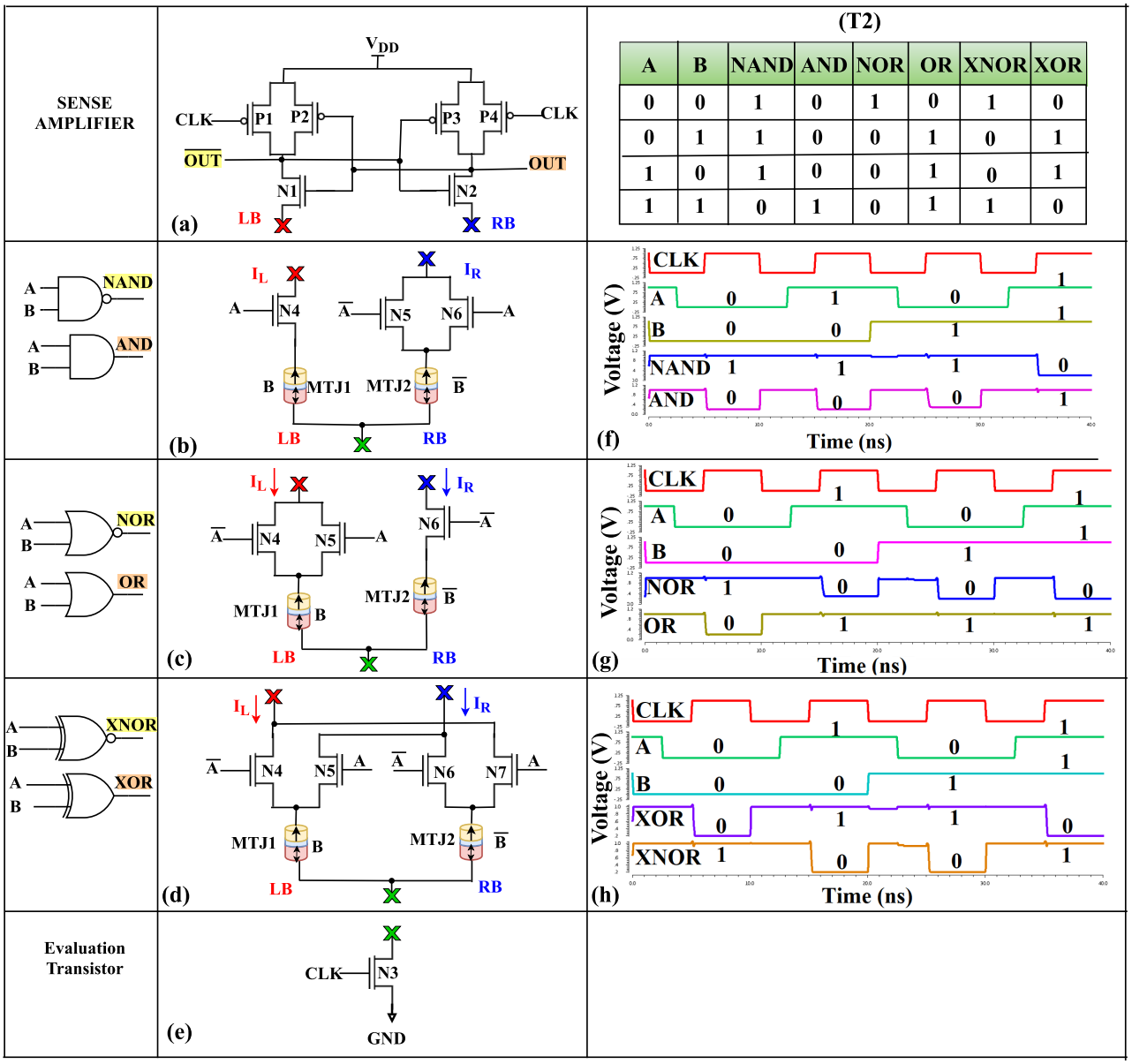


FIGURE 33. (a) Part of the PCSA, whose evaluation transistor (N3) has been shown in (e). It is used for reading the state of the MTJ for all the logic networks shown in (b), (c), and (d). The first column represents the name/gate level structure for the second column components. Logic network for 2 input, (b) NV-NAND/AND logic, (c) NV-NOR/OR logic, and (d) NV-XNOR/XOR logic. For all the logic blocks, the input A/$\bar{A}$ is given to nMOS transistors while B/$\bar{B}$ is represented by MTJs. I_L and I_R represent the current flowing in the LB (red color) and RB (blue color) in (b), (c), and (d), respectively. Red, blue, and green cross indicate the points that need to be connected to build the hybrid circuit. (f), (g) and (h) are the simulated waveforms for NV-NAND/AND, NV-NOR/OR, and NV-XNOR/XOR circuits. Truth table T2 satisfies the waveform shown in figure (f), (g), and (h).

output node, which observes the low resistance path in RB for the discharge current (I_R).

Hence even-though both branches start to discharge simultaneously to GND, $\overline{OUT}$ node discharges slower than the OUT node. Because of the faster discharging of the OUT node, it crosses the threshold voltage of the transistor P2, and it turns ON. As a result, the gate terminal of P3 is pulled to V_{DD}, and hence it is turned OFF. At the same time $\overline{OUT}$ node along with the gate of N2 is pulled up to V_{DD}, which makes OUT node continue to discharge to GND. When the OUT node crosses below the threshold voltage of N1, it is turned OFF. Hence discharge path for the $\overline{OUT}$ node to GND ceases to exist. But N2 is fully ON, facilitating the OUT node to discharge to GND. Hence node voltages for OUT = '0' and $\overline{OUT}$ = '1' are achieved simultaneously in its true and complementary form. Fig. 33 (f) shows the simulated waveform for the hybrid NV-NAND/AND logic verified by T2 in Fig. 33.

E. DESIGN OF NV-NOR/OR LOGIC

Fig. 33 (c) shows the logical structure of the hybrid MTJ/CMOS LIM structure for NV-NOR/OR logic. During

the precharge phase, both NOR ($\overline{OUT}$) and OR (OUT) output nodes are pulled-up to V_{DD} or logic '1'. While during the evaluation phase, based on various input combinations, different analyses can be made. Whenever input A='1', transistors N6, N4 are OFF, and N5 is ON. Therefore, the OUT node of the OR gate remains at logic '1', and the NOR node invariably finds a discharge path to GND. In this case, the state of the MTJ matters little. Whereas for input A='0', N4 in LB and N6 in RB is ON, because of which both NOR as well as OR output nodes find discharge path to GND. For B = '0', assume the pair of MTJ1-MTJ2 is set to AP-P state, respectively, means $R_{MTJ1} > R_{MTJ2}$, i.e., LB offers a high resistance path and RB offers comparatively low resistance path for the output nodes to discharge through GND. Hence NOR node will be pulled up to VDD or logic'1', and the corresponding OR node will be pulled down to logic'0'. In the other case, i.e., A='0' and B='1'; the pair of MTJ1-MTJ2 is set to P-AP state, respectively means $R_{MTJ1} < R_{MTJ2}$, hence OR node will be at logic '1' and NOR node will be at logic '0'. Fig. 33 (g) illustrates the simulated waveform for the hybrid NV-NOR/OR logic verified by T2 in Fig. 33.

F. DESIGN OF NV-XNOR/XOR LOGIC

Fig. 33 (d) represents the logical structure for 2 input NV-XNOR/XOR logic. During the precharge phase, both XNOR ($\overline{OUT}$) and XOR (OUT) output nodes are pulled-up to V_{DD} or logic '1'. While during the evaluation phase, based on various input combinations, different analyses can be made. When A= '0' or A= '1', the output nodes value will strongly depend on input B, which is represented by the pair of MTJ. When A= '0', transistors N5, N7 are OFF whereas N4, N6 are ON, while for A='1' transistors N5, N7 is ON and N4, N6 is OFF. Hence in both cases, there are paths from output nodes to GND. So, the difference in resistance between LB and RB due to MTJ decides the output of the circuit. For example, consider the case when A='0' and B='1'; then transistors N4, N6 are ON, pair of MTJ1-MTJ2 is set in P-AP state, respectively. So $R_{MTJ1} < R_{MTJ2}$, which offers low resistance for LB path to XNOR node ($\overline{OUT}$) and high resistance for the RB path to XOR node (OUT). Hence the output node $\overline{OUT}$ is pulled down to logic '0', and OUT node is pulled-up to logic '1'. Fig. 33 (h) illustrates the simulated waveform for the hybrid NV-XNOR/XOR logic verified by T2 in Fig. 33.

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