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An Image Rejection Ku-Band CMOS Low Noise Amplifier With Bridged-Tee Band-Stop Filter

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ABSTRACT For satellite communication applications, this paper presents an image rejection Ku-band low noise amplifier (LNA) in a 65-nm CMOS process for the Hartley receiver architecture. To achieve high input/output linearity performance, the inductive source degenerated cascode and the capacitive neutralized common-source (CS) amplifier topologies are used in the LNA input and output stages, respectively. To achieve wideband input return loss, the minimum noise figure and high gain performance simultaneously, the inductive source degenerated cascode amplifier is co-designed with the fourth order input impedance matching network. For the image rejection purpose, a bridged-tee band-stop filter is proposed. The measurements show the LNA achieves 14.3-to-18.3 GHz 3 dB bandwidth with 17-to-20 dB power gain, 3.5-to-4 dB noise figure, 17-to-37 dB image rejection and -5 dBm IIP3. Including all pads, the chip occupies a silicon area of 1360 $\times$ 450 μm^2 and consumes 72 mW DC power.

INDEX TERMS CMOS, Ku-band, low noise amplifier (LNA), band-stop filter (BSF), image rejection.

I. INTRODUCTION

To meet explosive growth of the mobile data traffic, smart vehicles and internet of thing (IoT) applications, terrestrial 5G systems provide eMBB (enhanced mobile broadband), uRLLC (ultra-reliable low latency communications) and mMTC (massive machine type communications) services [1]. With advantages of flexibility, large coverage and low cost, the non-terrestrial satellite communication can provide high speed data transfer service for the rural areas and moving platforms (passenger vehicles and aircrafts, high speed trains) [2]. Given above benefits, the satellite communication is regarded as an essential part of 5G infrastructures. Compared to the traditional L- and S- frequency bands, with large bandwidth advantages the Ku-band satellite communication system can achieve a higher data rate with high order modulation schemes.

From the implementation perspective, the RF transceiver can be realized with the superheterodyne or the direct conversion architecture. Compared with the direct conversion architecture, the superheterodyne architecture has the benefits of high frequency selectivity and sensitivity [3]. However, due to two frequency conversion steps, such architecture has image rejection issues, which are critical to meet the high error vector magnitude (EVM) requirements for high order modulation applications. Typically, to improve the image rejection ratio, a surface acoustic wave (SAW) filter can be used in front of the mixer, resulting in a bulky and high cost solution. Considering the high integration level and image rejection requirements, the RF transceiver can be realized with Hartley or Weaver architectures [4] [5]. However, given the mismatch issues, in these architectures the image rejection performance is still limited.

In this paper, an image rejection Ku-band low-noise amplifier (LNA) is realized for the Hartley receiver architecture. To solve the image rejection issue, an integrated bridged-tee band-stop image rejection filter is proposed. In addition, to achieve wideband input return loss and low noise figure performance, the inductive source degenerated cascode amplifier topology is co-designed with its fourth order input matching network, and the stability and impedance matching issues of the capacitive neutralized common-source (CS)

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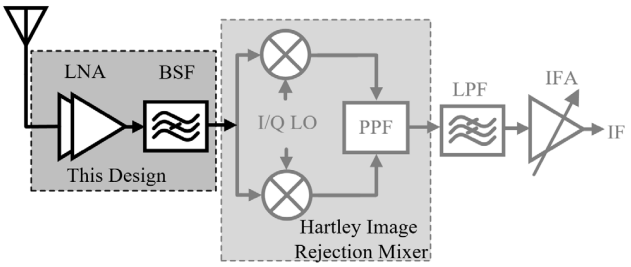

FIGURE 1. Image rejection low noise amplifier for the satellite receiver applications.

amplifier topology are investigated. Fabricated in a 65-nm CMOS process, over the desired operating frequency range (15-to-18 GHz) the measured chip has a maximum image rejection of 37 dB and a minimum noise figure of 3.5 dB, and a maximum power gain of 20 dB.

This paper is organized as follows. Section II illustrates the Hartley receiver architecture and discusses the LNA design in detail. Section III describes design of the proposed bridged-tee band-stop filter. The measurement results are then presented in Section IV. Finally, the conclusion is drawn in Section V.

II. LOW NOISE AMPLIFIER DESIGN

Fig. 1 shows the block diagram of the Ku-band superheterodyne receiver front-end, which consists of a low noise amplifier with an image rejection filter, a Hartley image rejection mixer, a low pass filter (LPF), and an IF amplifier (IFA). With this architecture, the image rejection performance can be improved, and the requirements on the passive polyphase filter (PPF) and I/Q mixer can be relaxed. With this architecture, a CMOS fully integrated solution can be easily achieved.

As shown in Fig. 2, the image rejection LNA consists of two gain stages and a bridged-tee band-stop filter. In particular, at the LNA input the inductive source degenerated cascode amplifier topology is used to realize the input impedance matching to 50 Ω and to improve the input linearity with the negative series-series feedback [6]. To improve the LNA output power and voltage headroom, the capacitive neutralized CS topology is used in the second stage. To enhance the LNA bandwidth, the transformer-based stagger compensation technique is used in the input and inter-stage impedance matching.

A. THE INDUCTIVE SOURCE DEGENERATED CASCODE AMPLIFIER

According to the Friis law, the LNA overall noise performance is dominated by its first stage. In this design, for good noise, gain, input return loss, and bandwidth performance, the LNA input stage is optimized in terms of the active gain cell and the passive matching network, as shown in Fig. 3.

In the active gain cell, a cascode amplifier with a source degeneration inductor L_S is employed and a parallel capacitor C_{ex} is used between the transistor gate and source terminals to realize a co-design of the active gain cell and the fourth order input matching network, achieving simultaneous noise and input matching (SNIM) at the given amount of power dissipation [7], [8]. In order to further describe the working principle of SNIM technique, the amplifier input optimum noise impedance $Z^*_{opt,NF}$ is expressed as follows [9]:

$$Z^*_{opt.NF} = \frac{2}{\omega C_{gs}}\sqrt{\frac{K_r}{K_g}} + \frac{2K_C}{j\omega(C_{ex}+C_{gs})} + j\omega L_S, \quad (1)$$

where K_r, K_g and K_C are functions of C_{ex}/C_{gs} [10]. And the amplifier input impedance Z_{in} can be calculated as:

$$Z_{in} = \frac{2g_m L_S}{C_{ex}+C_{gs}} + \frac{2}{j\omega(C_{ex}+C_{gs})} + j\omega L_S, \quad (2)$$

with C_{gs} and g_m transistor M1 and M2 inherent parasitic capacitance and transconductance, respectively. When both real and imaginary parts in (1) and (2) are equal, the amplifier noise and input impedance match can be realized simultaneously. For amplifier design, with a transistor biasing current density of 0.15 mA/μm [11], its transistor width W determines the amplifier power consumption. To take into account the amplifier power consumption, Fig. 4 (a) shows the simulated relationships between ideal L_S, C_{ex}, transistor width W and $NF_{\min}$ when simultaneous noise and input match are achieved. And Fig. 4 (b) shows the corresponding optimum source and load termination impedance. As indicated, with the compromise between SNIM, power gain, bandwidth, and power consumption, the width of the transistors M1 and M2 are set to be 96 μm ($W = 4W_1$), the C_{ex} and L_S are chosen to be 80 fF and 280 pH, leading to 35 mW power dissipation. At 16 GHz, the corresponding optimum $Z^*_{opt,NF}$ equals to Z_{in}, which is 47-j66 Ω, and the NF_{min} and G_{max} are 1.38 dB and 14.6 dB, respectively. With such impedance, it is difficult to achieve good gain, noise figure, and input return loss simultaneously with high efficiency and compact passive network. To facilitate the input matching network design, C_{ex} is increased to 200 fF and L_S is decreased to 120 pH. At 16 GHz, $Z^*_{opt,NF}$ is 16.6-j38 Ω, and it is close to Z_{in}, which is 16.8-j43 Ω. Accordingly, NF_{min} is slightly decreased to 1.31 dB, and G_{max} is increased to 16.5 dB, making it possible to realize the co-design of the active gain cell and the input matching network, as to be shown shortly. With post-layout simulation, the first stage achieves 16.2 dB maximum available gain and 1.5 dB minimum noise figure at 16 GHz, which is acceptable for the Ku-band LNA [12].

For the input passive matching network, its bandwidth is improved with a transformer-based fourth order matching network. To illustrate this, in Fig. 5 the LNA first stage equivalent circuit is introduced [13], and its input matching network can be modelled as a 2nd order band-pass filter with two pairs of complex poles. With such equivalent circuits, to achieve perfect impedance matching, the relationship between the real part of the active gain cell input impedance Z_{in} (i.e. R_{LNA}) and the source impedance R_S should be:

$$\frac{R_{\rm LNA}}{R_{\rm S}} = \frac{k_1^2}{n^2}, \quad (3)$$

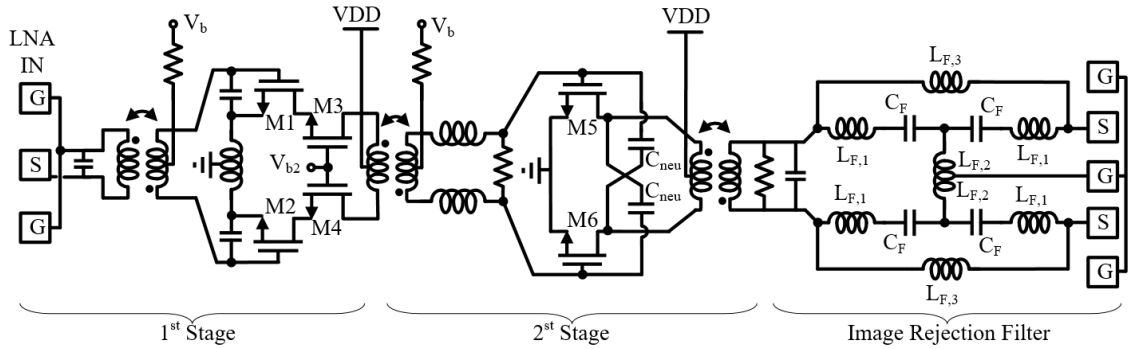

FIGURE 2. Proposed image rejection Ku-band low noise amplifier with bridged-tee band-stop filter.

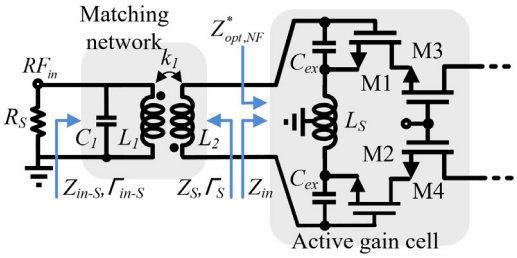

FIGURE 3. Schematic of the inductive source degenerated cascade amplifier with a transformer-based matching network.

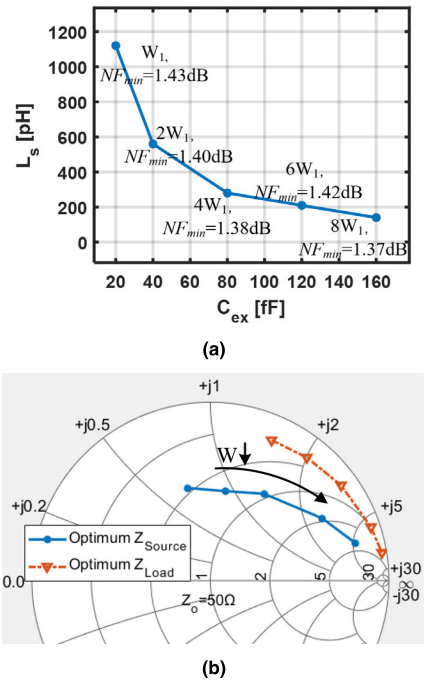

FIGURE 4. (a) Simulated relationships between size of transistors M1, M2 versus C_{ex} and L_S ideally, and (b) corresponding optimum source and load termination impedance, when the noise and input matching are achieved simultaneously at 16 GHz (where W_1 = 18 fingers × 2μm unit width).

where n and k_1 are the turn ratio and coupling factor of primary and secondary inductors L_1 and L_2, respectively. Assuming the quality factor of the input shunt capacitor C_1 is

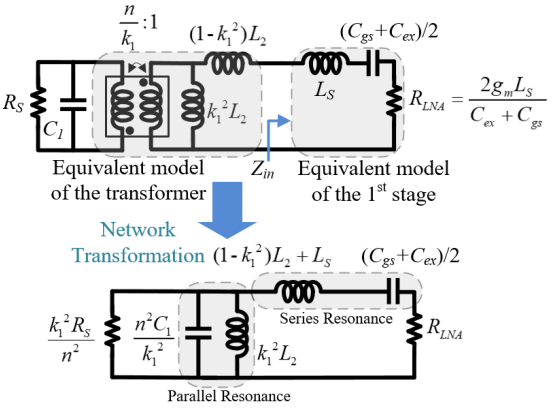

FIGURE 5. Equivalent circuits of the first stage describing the impedance matching strategy.

high, the insertion loss of the input matching network equals to that of the transformer (IL_{MN}), as shown below [14]:

$$IL_{MN} = \frac{1}{1+2\sqrt{(1+\frac{1}{Q_1Q_2k_1^2})\frac{1}{Q_1Q_2k_1^2}}+\frac{2}{Q_1Q_2k_1^2}}, \quad (4)$$

where Q_1 and Q_2 are quality factors of L_1 and L_2. Combining (3) and (4), the ratio of R_{LNA}/R_S is very critical for the insertion loss IL_{MN}. In particular, when $Q_1 = Q_2 = Q_m$, the insertion loss IL_{MN} is shown in Fig. 6. With 96 μm transistor width, due to parasitic elements effect, the post-layout simulated Z_{in} is changed from 16.8-j43 Ω to 21.8-j48 Ω, and the transformer-based high efficiency matching network can be used, e.g. $n = 1$ and $k \approx 0.7$. In this design, the coupling factor k_1, primary and secondary inductors of the transformer are set to be 0.62, 360 pH and 400 pH, respectively. With an inductor Q factor around 19, a good simulated insertion loss of 1.26 dB is achieved.

Fig. 7 shows the impedance matching trajectories. As indicated, with the aforementioned co-design of active and passive devices, the input differential impedance Z_{in-S} approaches R_s, and Γ_s is very close to the optimum input reflection coefficients of the first stage NF and available gain (G_A). In this way, the amplifier can achieve wideband input return loss, minimum NF and high gain performance

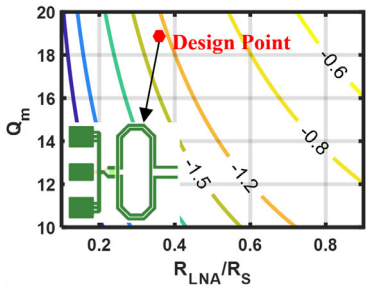

FIGURE 6. Insertion loss of input matching network in dB scale for different Q_m and R_{LNA}/R_S values, and layout of the input matching network.

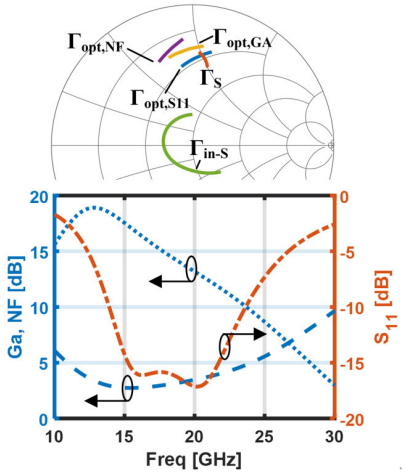

FIGURE 7. Matching trajectories (14 to 20 GHz) of the first stage and simulated NF, G_A and S_{11} of the first stage.

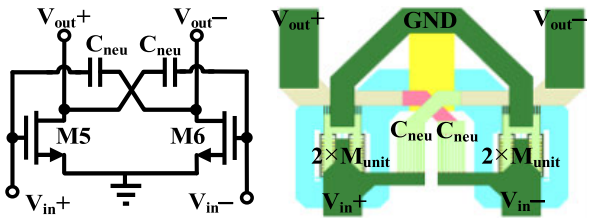

FIGURE 8. Schematic and layout of the capacitive neutralized CS amplifier (transistor M_{unit} with 18 fingers and 2μm unit width).

simultaneously. Note that the realized impedance Γ_s is not located exactly at the $\Gamma_{opt,NF}$ position, and its NF is about 0.3 dB higher than the NF_{min}. For illustration, Fig. 7 also shows the simulated S_{11}, NF and G_A of the first stage. From 15 to 18 GHz, the amplifier G_A is higher than 14.5 dB, and its S_{11} and NF are lower than -10 and 3.1 dB, respectively.

B. THE NEUTRALIZED CS AMPLIFIER

To relax the output voltage headroom, the differential CS amplifier topology is used. However, in Ku-band the transistor Miller capacitor degrades the amplifier stability. To solve this issue, in this design the capacitive neutralization technique is realized with Metal-oxide-Metal (MoM) capacitors, improving the amplifier reverse isolation and simplifying the amplifier design [15]–[17].

Fig. 8 shows the CS amplifier topology and layout. For high linearity performance, in this design each transistor has

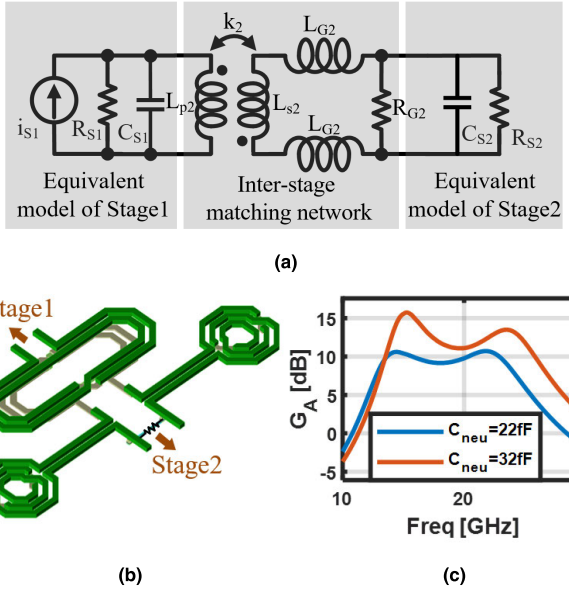

FIGURE 9. Inter-stage impedance matching network (a) equivalent circuit (b) layout, and (c) G_A of the second stage with different C_{neu}.

two gain cells with unit width W_{unit} of 36 μm.The transistor current density is set to be 0.2 mA/μm for optimum f_{max} performance. To realize unconditional stability, the neutralization capacitor C_{neu} should be chosen from following range [18]:

$$1-\frac{1}{\omega C_{gd}}\sqrt{\frac{4g_g^2g_{ds}^2}{g_m^2-4g_gg_{ds}}}\le\frac{C_{neu}}{C_{gd}}\le 1+\frac{1}{\omega C_{gd}}\sqrt{\frac{4g_g^2g_{ds}^2}{g_m^2-4g_gg_{ds}}}, \quad (5)$$

with the Miller capacitor C_{gd}. For unconditional stability, simulation results show the C_{neu} value range is from 0.92 to 1.06 times C_{gd}, and its optimum value is 22 fF.

Fig. 9 (a) and (b) show the equivalent circuit and layout of the inter-stage impedance matching network, which consists of a high-k transformer (L_{p2} = 900 pH, Q_{p2} = 14, L_{s2} = 720 pH, Q_{s2} = 8.5, k_2 = 0.74), two area-efficient spiral inductors (L_{G2} = 500 pH, Q_{G2} = 16) and a 1 kΩ shunt resistor (R_{G2}). Assuming the inductor quality factor is relatively high, the two resonance frequencies $\omega_{H,L}$ of the inter-stage network can be derived as [19]:

$$\omega_{H,L}^2=\frac{1+\frac{n\omega_1^2}{\omega_2^2}\pm\sqrt{\frac{n^2\omega_1^4}{\omega_2^4}-\frac{2\omega_1^2(n-2k^2)}{\omega_2^2}+1}}{\frac{2(n-k_2^2)}{\omega_2^2}}, \quad (6)$$

where ω_1, ω_2 and n are defined as follows:

$$\omega_1=\frac{1}{\sqrt{C_{S1}L_{p2}}},\quad \omega_2=\frac{1}{\sqrt{C_{S2}L_{S2}}},\quad n=\frac{2L_{G2}+L_{S2}}{L_{S2}}.$$

With C_{neu} increased, calculations and simulations show that the second gain stage input capacitor C_{s2} is reduced, and according to (6) the resonance frequencies $\omega_{H,L}$ will shift to

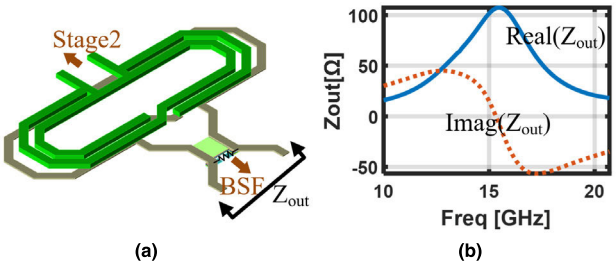

FIGURE 10. (a) Layout, and (b) output impedance of the second stage output matching network.

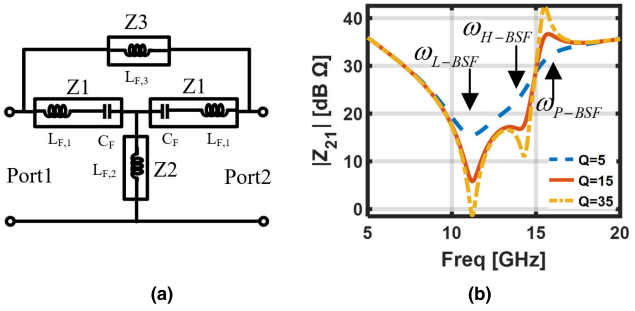

FIGURE 11. (a) Single-ended model of the differential BSF and (b) effect of Q-factor on the transimpedance frequency response of the BSF.

higher frequency. To justify the above neutralization capacitor range and to evaluate its effect on the amplifier frequency response, C_{neu} is increased from optimized value 22 to 32 fF. As indicated in Fig. 9 (c), the second gain stage becomes potentially unstable, and the G_A curve shifts to higher frequency, proving the importance of realizing an accurate C_{neu}. In this design, its interconnect lines are undertaken to take into account in electromagnetic (EM) simulations.

In principle, the band-stop filter (BSF) performance highly depends on its source and load impedance. Accordingly, as shown in Fig. 10(a), the amplifier output impedance matching network is co-designed with the BSF to achieve a high output power and a good image rejection performance. In particular, the BSF output load impedance is 100 Ω, and a transformer is used at the BSF input. By introducing a 280 fF capacitor and a 1kΩ resistor at the transformer output, with the following optimized transformer parameters: L_p = 800 pH, $Q_p = 18$, $L_s = 350$ pH, $Q_s = 7$, $k = 0.61$, the transformer output impedance Z_{out} is about 100 Ω at 15.5 GHz, as shown in Fig. 10 (b). As to be shown in Section III, the BSF input impedance is 100 Ω, thereby realizing a perfect impedance match between the transformer and the BSF. In this way, a high power gain and a good image-rejection performance can be achieved simultaneously. According to simulation results, the amplifier image rejection ratio (IRR) is higher than 22 dB, and the maximum power gain reaches 20 dB.

III. IMAGE REJECTION FILTER DESIGN

For 15-to-18 GHz RF and 14 GHz LO, the receiver IF ranges from 1 to 4 GHz, resulting in 10 to 13 GHz image frequencies, respectively. In this design, the BSF is realized with a bridged-tee circuit, which incorporates a high-pass type tee circuit and a bridged inductor. Fig. 11 (a) shows its single-ended model, whose impedance Z-matrix can be defined as Eq. (7) [20].

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_2 + \dfrac{Z_1^2 + Z_1 Z_3}{2Z_1 + Z_3} & Z_2 + \dfrac{Z_1^2}{2Z_1 + Z_3} \\ Z_2 + \dfrac{Z_1^2}{2Z_1 + Z_3} & Z_2 + \dfrac{Z_1^2 + Z_1 Z_3}{2Z_1 + Z_3} \end{bmatrix}. \quad (7)$$

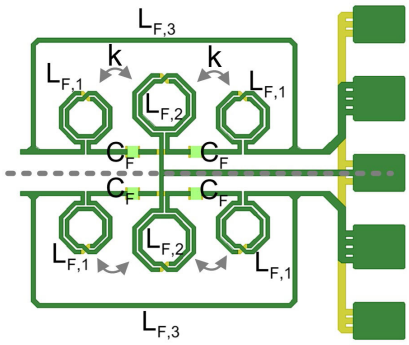

FIGURE 12. Layout of the proposed image rejection filter.

As shown in Fig. 11 (a), Z_1 is comprised of a series band-pass resonator $L_{F,1}$ and C_F, while Z_2 and Z_3 represent the impedance of inductors $L_{F,2}$ and $L_{F,3}$. Their expressions are given by:

$$Z_1 = 1/(j\omega C_{F,1}) + j\omega L_{F,1}, \quad (8)$$

$$Z_2 = j\omega L_{F,2}, \quad (9)$$

$$Z_3 = j\omega L_{F,3}. \quad (10)$$

Assuming the inductor quality factor is high enough and substitute the above impedance values into (7), the BSF has two zeros ω_{H-BSF} and ω_{L-BSF}, which can be calculated by setting Z_{21} to be 0:

$$\omega_{H-BSF,L-BSF} = \sqrt{\frac{L_{F,1}+L_{F,2} \pm L_{F,2}\sqrt{(1-L_{F,3}/L_{F,2})}}{C_F(L_{F,1}^2+2L_{F,1}L_{F,3}+L_{F,2}L_{F,3})}}. \quad (11)$$

According to (11), when $L_{F,2} > L_{F,3}$, the $L_{F,3}/L_{F,2}$ ratio determines the $\omega_{H-BSF}/\omega_{L-BSF}$ ratio. With larger $L_{F,3}/L_{F,2}$ ratio, a wider bandwidth and higher the in-band ripple can be achieved; when $L_{F,2} = L_{F,3}$, there is only one zero; when $L_{F,2} < L_{F,3}$, there is no zero, and the filter does not have the band stop function.

Moreover, the BSF pole ω_{P-BSF} can be derived as:

$$\omega_{P-BSF} = \frac{1}{\sqrt{C_F(L_{F,1} + \frac{1}{2}L_{F,3})}}. \quad (12)$$

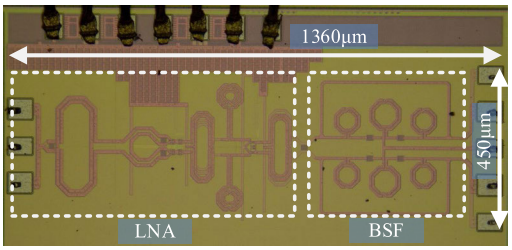

FIGURE 13. Die micrograph of the image rejection Ku-band LNA.

Ideally, the BSF is lossless and its input impedance equals to the transformer output load impedance (100 Ω) at ω_{P-BSF}. As mentioned above, the transformer output impedance is 100 Ω at 15.5 GHz, and the BSF pole ω_{P-BSF} is designed to be 15.5 GHz to achieve low insertion loss and high IRR. Moreover, as the required image rejection frequency range is below 13 GHz, the initial BSF zero ω_{H-BSF} and ω_{L-BSF} are set to be 14.3 and 11.2 GHz, respectively. From the implementation point of view, the limited Q-factor of the passive components may affect the BSF performance, and intense simulations are undertaken to evaluate the passive components effect. As indicated in Fig. 9 (b), when the inductor $Q > 15$, it has less influence on the ω_{P-BSF}, ω_{H-BSF} and ω_{L-BSF}, and high IRR performance can be realized. With optimizations, the layout of the filter is illustrated in Fig. 10. The optimized inductor $L_{F,3}$ value is 400 pH, and $L_{F,2}$ and $L_{F,1}$ values are 480 and 330 pH, respectively. The former inductor ($L_{F,3}$) is realized with transmission line, while the latter two inductors are realized with area-efficient spiral inductors. To achieve a compact BSF, the inductors are laid out closely, and their parasitic magnetic coupling effects (the coupling factor k is 0.04) will reduce the BSF operating frequency. For accurate design, the passive elements are simulated together to taken into account the coupling effects. In this design, the inductor simulated Q factors are higher than 20. In this way, the measured BSF IRR is higher than 17 dB, meeting the receiver requirements.

IV. MEASUREMENTS

Fig. 13 shows the die micrograph of the image rejection LNA. Fabricated in a 65-nm CMOS process, the total chip area including DC pads is 1360 μm × 590 μm with the core area of 0.612 mm^2. With a 1.2 V power supply, the LNA power consumption is 72 mW.

Fig. 14 shows the simulated and measured power gain and input return loss of the LNA. The power gain and input return loss were measured with Keysight N5247A PNA-X network analyzer. The LNA peak gain is 20 dB over a 3 dB bandwidth of 4 GHz, and its S_{11} is lower than -10 dB form 13.5 to 22.5 GHz. With an IF frequency of higher than 1 GHz, Fig. 15 shows the measured image rejection.

The NF is measured with N9030A PXA signal analyzer, and it is shown in Fig. 16. The minimum NF is 3.5 dB at 15 GHz with less than 0.5 dB ripple over the whole operating band.

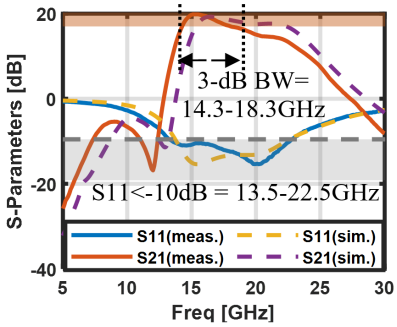

FIGURE 14. Simulated and measured S-parameters.

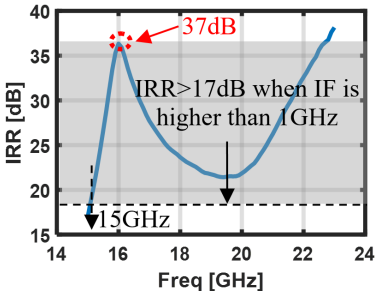

FIGURE 15. Measured image rejection ratio (IRR).

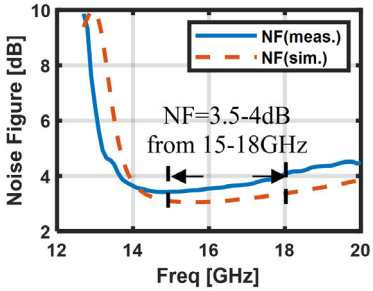

FIGURE 16. Simulated and measured noise figure.

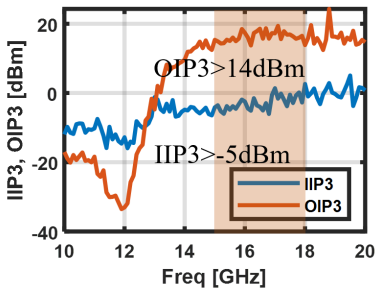

FIGURE 17. Measured IIP3 and OIP3 (10 MHz offset).

By applying two tones with 10 MHz spacing, Fig. 17 shows the measured IIP3 and OIP3 versus frequency. Clearly, from 15 to 18 GHz the IIP3 and OIP3 are better than -5 and 14 dBm respectively. Note that, due to cascading effect, the LNA OIP3 curve is shaped by the BSF loss curve. The LNA large signal IP1dB is better than -15 dBm.

Table 1 compares this work with the state-of-the-art CMOS Ku-band LNAs. As indicated, by combining the inductive

TABLE 1. Performance summary and comparison with state-the-art results.

Ref	Tech	BW [GHz]	Maximum Gain [dB]	Minimum NF [dB]	IIP3 [dBm]	IP1dB [dBm]	Power [mW]
[12]** MTT' 17	65 nm CMOS	14.25-15.75	23.5	5.6-6.3	N.A	-33	27
[21] MWCL'17	65nm CMOS	15.8-30.3	10.2	3.3-5.7	-0.5	N.A	12.4
[22]* JSSC'11	0.13µm BiCMOS	8-18	22	3.8-4.7	N.A	-25	<180
[23] ISCAS'13	65nm CMOS	20.55-24.35	20.46	3.4	N.A	N.A	12
[24] MWCL'12	65nm CMOS	17.5-26	17.9	3.3-5.9	-5	-15	5.6
[25] MTT'11	0.18µm CMOS	3.1-10.3	12.7	2.5-3.9	-3	-12.5	13.4
This Work	**65 nm CMOS**	**14.3-18.3**	**20**	**3.5-4.0**	**>-5**	**>-15*** **	**72**

*Simulated stand-alone LNA **Measured RX RF front-end *** at maximum gain mode

degenerated cascode and capacitive neutralized CS amplifier, with proposed co-design of the impedance matching network and the active gain cell, the LNA exhibits very competitive linearity and noise figure performance.

V. CONCLUSION

In this paper, an image rejection 15-18 GHz LNA with bridged-tee band-stop filter is implemented in a 65-nm CMOS process. The inductive source degenerated cascode and capacitive neutralized CS amplifiers are combined together to achieve high input and output linearity performance. To achieve wideband input return loss, minimum noise figure and high gain performance simultaneously, the cascode amplifier is co-designed with the fourth order input impedance matching network. A bridged-tee band-stop filter is optimized to improve the IRR and to reduce the insertion loss. With measurements, the circuit achieves 20 dB peak power gain, 3.5 dB minimum NF and more than 17 dB image rejection ratio. Moreover, the LNA IIP3 is -5 dBm. This design concept could be widely adopted to realize high image rejection satellite receivers.

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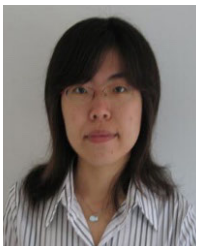

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