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Low-Frequency Noise in CMOS Switched-gm Mixers: A Quasi-Analytical Model

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ABSTRACT Flicker noise contributed by active mixers usually compromises the overall sensitivity level of direct-conversion receivers (DCRs). In this article, a qualitative quasi-analytical model has been developed to in-depth explain the flicker noise mechanism existing in the switched-g_m active mixer in which an improved current source switch is presented for high mixer common-mode rejection ratio (MCMRR). The built model simply explains how frequency translations take place within the mixer. Compact equations are derived to estimate the flicker noise contribution of individual stages at the output. Simulations validate the accuracy of the predictions, and the dependence of flicker noise on local oscillator (LO) slope ratio, period, and other circuit parameters. The high-frequency limitation of the mixer is further estimated by investigating into the tail parasitic capacitance charging and discharging behavior. Furthermore, a switched-g_m pMOS mixer prototype with low flicker noise is implemented in a 0.18-μm CMOS process. It operates at an RF input frequency of 1 GHz and provides a maximal conversion gain of 12.9 dB and an NF of 11.4 dB while a flicker noise corner of 220 kHz and an IIP3 of 3.6 dBm are measured, respectively. The mixer core only consumes 3.3 mW from a 1.8 V supply.

INDEX TERMS Switched transconductor mixers, noise figure (NF), flicker noise, noise transfer function modelling, pMOS, mismatch, mixer common-mode rejection ratio (MCMRR).

I. INTRODUCTION

Direct conversion architectures, with the merits of high integration and low costs, have drawn great attention in the last decades from both industry and academia. However, the direct conversion receiver (DCR) for systems on chip (SOC) target [1] still has been deeply obsessed with a few drawbacks yet to be well addressed, such as flicker noise, dc offset, even-order distortion, and local oscillator (LO) leakage. Undoubtedly, flicker noise among them is a critical issue in the DCR design as it almost degrades the signal-to-noise ratio (SNR) and total noise figure (NF), which eventually results in the deterioration of the receiver's sensitivity [2]. Most of the flicker noise contribution of receivers comes from mixers which thus need to be designed carefully to reduce the flicker noise output targeted for the DCR applications.

Mixers, as one of the fundamental building blocks in receivers to perform the frequency down-conversion function, are generally divided into two categories: active mixers and passive mixers. Compared to passive mixers, active mixers are fairly attractive in many applications because they can provide higher conversion gain, resulting in improved suppression of noise contribution from subsequent stages. Specifically, the active mixers again consist of two categories: Gilbert (transconductor and switch, i.e. GmSw) type and switched-g_m (SwGm) type [3]. In the Gilbert mixer, switch pairs are used to commutate the tail RF current from a transconductance stage under the control of LO large signal, and to complete the frequency conversion from RF to IF. In retrospect, lots of literature have been reported to predict and optimize the thermal noise and flicker noise of

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the GmSw mixer. Thereinto, the noise performance of the GmSw mixer was predicted and modeled in [4]–[7], [28]. Following them are several improved mixer topologies with enhanced performance. Of them, the static current injection has been proposed in [8], [9] to reduce the noise current pulses appearing at the output, by injecting a constant bias current. Then the dynamic current injection has been proposed in [10] by embedding a controlled injection circuit to inject current pulses functioning only at the switching instances, which also can compensate noise current pulses of switch pairs. The two techniques provided an efficient suppression for the thermal and flicker noise resulted from the direct noise mechanism in switch pairs, but the indirect noise mechanism via the equivalent tail capacitance remains troublesome. Therefore, inductors have been added into the static and dynamic current injection Gilbert mixers [11], [12] to resonate with this tail parasitic capacitance (C_P) at the tail node and alleviate the indirect noise mechanism. The two designs both yield good results, but sacrifice chip size because of the use of bulky spiral inductors. To mitigate the issue, a negative impedance circuit sourced by a capacitor is embedded into the mixer to generate active inductive loading and tune out parasitics at the tail net [13]. Furthermore, merging a noise-canceling transconductance stage and current injection structure, the GmSw mixer obtains optimized noise performance [14]–[16], [29]. In contrast, for the SwGm mixer, the RF transconductance instead of RF signal current is switched on/off periodically by a large LO signal to complete frequency down-conversion. Attractive merit in the mixer comes from the cancelled switch pairs' noise appearing at the differential output ports in common-mode style. Although the thermal noise of the mixer is discussed in detail in the paper, flicker noise behavior of that has yet to be clarified with closed-form derivations, which, however, is of importance for the mixer targeted for DCR systems. Meanwhile, notice that fairly small transconductance value for transconductance pairs of the mixer prototype is select to alleviate the loading effect on an LO inverter driver, resulting in over-large NF which greatly hinders its meaningful application in practice. What is more, the pseudo-differential structure of transconductance pairs cannot sustain sufficient common-mode rejection that, however, is widely required by integrated chips for common-mode interference suppression. Moreover, it is still a challenge to investigate the flicker noise behavior of the mixer and balance noise and gain metrics under budgets of low power and good common-mode rejection.

In this article, an improved SwGm mixer based on a current source switching architecture is presented. Compared to [3] where the SwGm mixer topology was first presented, more theoretical analysis, design considerations, and experimental results are included. Moreover, a mixer prototype for DCR applications is designed. The mixer prototype implemented in p-type MOSFETs features low flicker noise output. The presented technical content in the paper is an extended report towards the conference paper [27]. Specifically, the paper is organized as follows. Section II gives the principle of the proposed SwGm mixer. Moreover, a low-frequency noise transfer mechanism is analyzed in detail for the proposed mixer. Closed-form equations are derived to estimate the output flicker noise of the mixer, which is verified by simulations in Section III. In Section IV, a switched transconductor mixer prototype is implemented in full p-type MOSFETs with a lower flicker noise frequency corner and verified by experimental results. Finally, Section V concludes the paper.

II. MIXER CIRCUIT

Shown in Fig.1 is the diagram of the presented dual-balanced switched-g_m mixer employing the improved current source switching architecture (Here, for convenience of expressing, the mixer in nMOS configuration as an example is analyzed and simulated. But the derived equations and resulting conclusions have general meaning.). It consists of transconductance pairs of four common-source configured transistors (M_1, M_2, M_4, and M_5) acting as the RF input stage, a switch stage of M_3 and M_6 in differential style to switch the bias current, I_B that passes through the RF transconductance pairs, and a load stage (R_{L1} and R_{L2}) where a periodic commutated RF signal current is down-converted to the IF signal voltage. In the traditional SwGm circuit, an inverter-configured LO generation directly drives the common source net of the RF transconductance pairs, switching on/off the bias current of that. At half the LO period, the switched-on RF transconductance pairs form a pseudo-differential pair, because the enabled nMOS transistor of the inverter LO generation connected between the tail net of the transconductance pairs and ground, is equivalent with a small resistance due to operating in the triode region. In contrast, the presented SwGm mixer uses simple tail current source switching architecture as the switch stage. That is to say, the transistor, M3 as in Fig.1 is switched on and kept in saturation, acting as the tail current source when a moderate-high LO voltage level is applied to the gate of the transistor. And the transistor M3 is switched off when a low LO voltage level is applied to that. This modification of the mixer topology is fairly beneficial for a common-mode rejection ratio which will be shown in section E. Furthermore, as mentioned above,

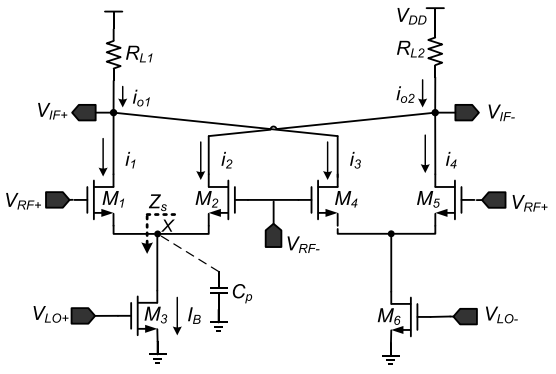

FIGURE 1. Diagram of the improved switched transconductor mixer.

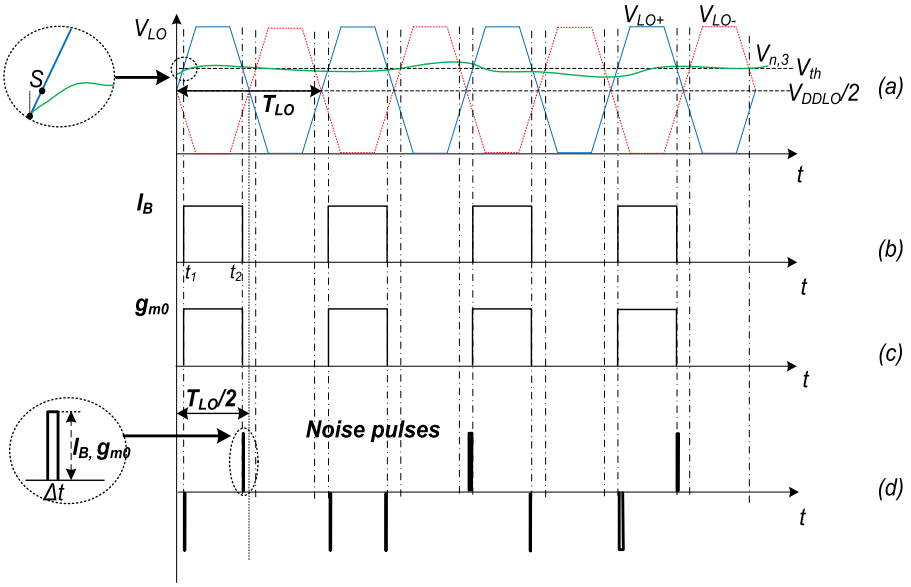

FIGURE 2. (a) Differential trapezoid periodic LO stimulus applied at the switch stage. The mixer output response with respect to LO stimulus decomposed into (b) noiseless switched bias current, (c) noiseless switched transconductance, and (d) noise pulses.

a larger transconductance value for transconductance pairs of the traditional SwGm mixer could expect a low noise but the loading effect accompanied to that could pull down the turn-off level and make the transconductance pairs switch off ineffectively. Alternatively, the LO inverter driver for the traditional SwGm mixer has to use increased supply voltage and inevitably-increased dynamic power dissipation to cope with the loading effect. In contrast, this loading effect mechanism is avoided in the presented mixer by removing the LO inverter driver.

A. CONVERSION GAIN

The proposed mixer operates in OFF overlap mode where switches cannot conduct simultaneously for noise reduction benefit [6]. The low-frequency conversion gain thus is

$$CG = \underbrace{\frac{2}{\pi}\cos\left(2\pi f_{LO} t_1\right)}_{C} g_{m0} R_L \tag{1}$$

where parameter t_1 denotes the switched-on instant of the transconductance pair of M_1 and M_2 while g_{m0} and R_L are the small-signal transconductance of transconductance pairs and load resistor (taking R_{L1}=R_{L2}=R_L). Parameter c characterizes a frequency conversion coefficient.

In practical application, parasitics are of concern to affect the high-frequency performance of circuits. Under LO large-signal driving, C_P charging and discharging will make net voltage, Vx toggle between high and low levels, which will be detailed in part D. When the charging/discharging time is comparable to a LO period, the reduced duty cycle of g_{m0} in Fig.2 is to degrade the frequency conversion coefficient, c, and conversion gain eventually.

B. FLICKER NOISE

Before examining the flicker noise transfer mechanism in the mixer, it is necessary to introduce an analytical flicker noise model of devices. A compact flicker noise model of MOSFETs adopted in the paper is [24]

$$\overline{V_n^2} \cong \frac{K_f}{C_{OX} WL} \frac{1}{f} \tag{2}$$

where K_f is the flicker noise coefficient related to a specific process. Parameters of W, L, C_{ox}, and f stand for width and length of devices, gate oxide capacitance, and frequency, respectively. This model is not as accurate as the BSIM3v3 model. But it serves as an analytical formulation and has been used to model flicker noise of devices for the first-order approximations. Specifically, the SwGm mixer comprises input transconductance pairs, the switch stage, and the output load stage. With the passive output load contribution neglected, flicker noise is present in all the transistors making up these functions in theory. The flicker noise contribution from these parts in the mixer will be detailed in the following analysis.

1) TRANSCONDUCTANCE FLICKER NOISE

To simplify the analysis, the mixer is assumed to switch sharply which is the same as the approximation used in [5]. It means that as in Fig.2, with trapezoid LO stimulus waveforms applied to the mixer, rectangular response pulses of current and transconductance are correspondingly generated. Using strict trapezoid response pulses of that leads to complex formula and is avoided in the paper. Correspondingly, the two

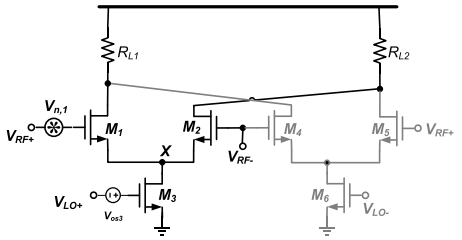

FIGURE 3. Diagram for transconductance flicker noise transfer mechanism analysis.

pulse edges are

$$t_1 = \frac{\left(V_{th} - \frac{V_{DDLO}}{2}\right)}{S}; \quad t_2 = \frac{T_{LO}}{2} - t_1 \tag{3}$$

where S, T_{LO}, V_{DDLO}, and V_{th} are the slope ratio of LO waveform, LO period, enabled level of LO generation, and the threshold voltage of devices.

By examining the flicker noise source of the transconductance transistor M_1 as in Fig.3, it transfers to the IF output only at nearly half the LO period when the transconductance pairs are enabled. Consequently, the time-varying direct flicker noise output current from the transconductance transistor, M_1 is written as

$$\begin{aligned} i_{o,n}(t) &= v_{n,1}(t) \sum_{k=-\infty}^{+\infty} c_k e^{jk2\pi f_{LO}t} \\ &= \sum_{k=-\infty}^{+\infty} c_k V_{n,1}(f + kf_{LO}) e^{jk2\pi f_{LO}t} \end{aligned} \tag{4}$$

where $v_{n,1}(t)$ is the flicker noise source of M_1 in the time domain while the Fourier series denotes the periodic transconductance signal of the transconductance pair over one LO period. According to (4), flicker noise of the transconductance transistor modulates the period varying transconductance and transfers low-frequency noise to dc and harmonics of LO by the coefficient $V_{n,1}(f+kf_{LO})$. By taking k=0, the resulted dc component of the modulated signal at output constitutes interference for the DCRs and yields

$$\begin{aligned} i_{o,n}(f) &= \left(\frac{1}{2} - \frac{2t_1}{T_{LO}}\right) g_{m0} V_{n,1}(f) \\ &= \left(\frac{1}{2} - \frac{2V_{th} - V_{DD,LO}}{ST_{LO}}\right) g_{m0} V_{n,1}(f) \end{aligned} \tag{5}$$

where $V_{n,1}(f)$ is the flicker noise source of M_1 in the frequency domain. As the main flicker noise contributor, transconductance pairs are expected to reduce the noise output by adopting low flicker noise devices with small $V_{n1}(f)$. For k≠0 case, the transferred flicker noise by LO harmonics appears as high-frequency noise at the IF output and is not interested by regular down-conversion applications.

2) SWITCH FLICKER NOISE BY BLOCKERS

In the Gilbert mixer, the flicker noise of each switch affects the turnon/turnoff instant of both switches due to the floating

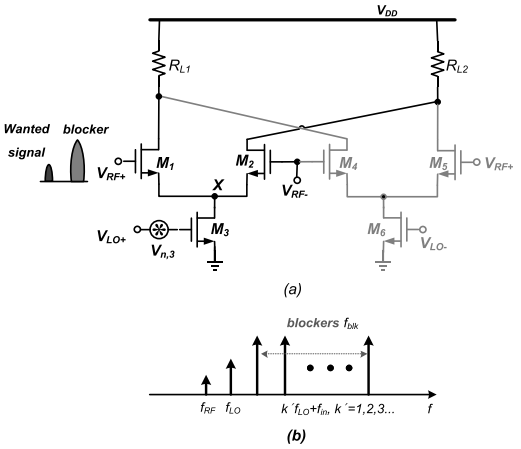

FIGURE 4. (a) Diagram for switch flicker noise transfer mechanism analysis due to (b) blockers coexistence with the wanted signal at RF port.

source voltage of switch pairs. In contrast, since the source voltage is grounded, the flicker noise of each switch only modulates the turnon or turnoff instant (t_1 and t_2) of that switch and does not affect the other in the proposed SwGm mixer. As in Fig.2 and Fig.4, the slowly varying gate-referred flicker noise of switch transistor randomly modulates the turn-on instant which should be ideally located at the time corresponding to LO voltage equaling the threshold voltage of devices. This modulation results in a train of noise pulses which add to the ideal square-wave periodic waveforms of both the dc bias current, I_B, and the transconductance, g_{m0}. Fortunately, I_B will appear at the differential output ports as the common-mode signal $I_B/2$, leading to null output, so does the noise pulses train added to that. However, the noise pulses train added to the transconductance, g_{m0} will appear at the output. Particularly in a situation of series of input block signals applied at specific discrete frequency points, prominent flicker noise output will be contributed by the switch stage. Disclosed in [18] is RF blocker input interacting with noise pulses added to periodically switched transconductor, leading to flicker noise output for passive mixers. Similarly, an estimation of the noise pulses added to the g_{m0}, induced by the flicker noise of the switch transistor M_3, $v_3(t)$ interacting with the input signal $v_i(t)$ of the proposed mixer, is

$$\begin{aligned} i_{o,n}(t) &= \sum_{k=-\infty}^{+\infty} g_{m0} v_i(t)\, \Delta t \\ &\quad \cdot \left[\delta(t - t_1 - kT_{LO}) + \delta(t - t_2 - kT_{LO})\right] \\ &= \sum_{k=-\infty}^{+\infty} \frac{g_{m0} v_i(t)\, v_{n3}(t)}{S} \\ &\quad \cdot \left[\delta(t - t_1 - kT_{LO}) + \delta(t - t_2 - kT_{LO})\right] \end{aligned} \tag{6}$$

where Δt is the width of error pulses which is equal to $v_{n3}(t)/S$ as in Fig. 2. Taking the Fourier transform of the equation gives

the output noise in the frequency domain below

$$
\begin{aligned}
&i_{o,n}(f) \\
&= \sum_{k=-\infty}^{+\infty} \frac{g_{m0}}{ST_{LO}} V_i(f) * V_{n3}(f - kf_{LO}) \\
&\quad \times \left[e^{-jk2\pi f_{LO} t_1} + (-1)^k e^{jk2\pi f_{LO} t_1} \right] \\
&= \begin{cases} \displaystyle\sum_{k=-\infty}^{+\infty} \frac{2g_{m0}}{ST_{LO}} V_i(f) * V_{n3}(f - kf_{LO}) \cos(k2\pi f_{LO} t_1) \\ \qquad\qquad k \in even \\ \displaystyle\sum_{k=-\infty}^{+\infty} \frac{-2jg_{m0}}{ST_{LO}} V_i(f) * V_{n3}(f - kf_{LO}) \sin(k2\pi f_{LO} t_1) \\ \qquad\qquad k \in odd. \end{cases}
\end{aligned}
\tag{7}
$$

Under a certain S, if LO frequency is not high enough, the amplitude weighted sine and cosine items in the equation approach zero and unity, making the noise output with odd k negligible, and even k collapse to the equation (4) in [18]. Generally, it demonstrates that flicker noise output appears both at kf_{LO} and 2f-kf_{LO}, which is the same as the results in the literature. For a given input frequency f_{in}, there could be a series of coexisted blocker frequency, f_{blk} typically located in $k' f_{LO}+f_{in}$ ($k' = 1, 2, 3\ldots$). Then, in the case of $f_{in}=f_{LO}$ for the DCRs, the frequency composition of 2f-kf_{LO} will lead to flicker noise output with k taking even, 2(k′ +1). Interestingly, in the case of k taking odd, there also is flicker noise output transferred by the frequency composition, 2f-kf_{LO} when f_{in} takes $f_{LO}/2$ for superheterodyne receiving. By focusing on the DCR scenario in the paper, and evaluating the worst case with the closest blocking frequency, f_{blk} taking $2f_{LO}$, the resulted IF flicker noise output with k=4 in (7), then yields

$$
i_{o,n3,blk}(f) = \frac{2g_{m0}A_{blk}}{ST_{LO}} V_{n,3}(f) \cos\left(4\pi \cdot \frac{2V_{th} - V_{DD,LO}}{ST_{LO}}\right) \tag{8}
$$

where A_{blk} is the amplitude of the blocking frequency.

The indirect mechanism of flicker noise in the Gilbert mixer is ascribed to the parasitic capacitance at the tail of switch pairs charging and discharging behavior during tail current switching instant [5]. Flicker noise voltage charges this tail capacitance through one ON switch which acts as a source follower at one half LO period, and discharges that through the other ON switch at the other half LO period, leading to the differential flicker noise output current. This indirect noise mechanism does not exist in the current SwGm mixer since the source nets of the switch pair are directly connected to the ground. On the other hand, the tail net of the differential transconductance pair maintains a virtual ground through the enabled switch stage. As a result, the flicker noise of the transconductance stage does not effectively charge or discharge the tail parasitic capacitance C_P, not yielding any similar indirect noise output either.

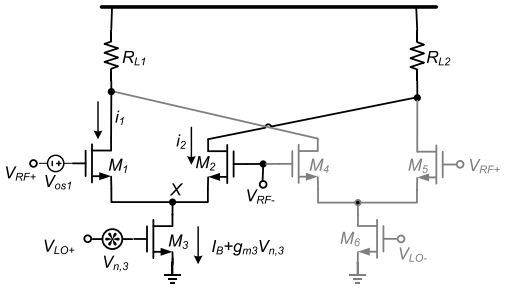

FIGURE 5. Diagram for switch flicker noise transfer mechanism analysis due to mismatch.

3) TRANSCONDUCTANCE FLICKER NOISE DUE TO DC OFFSET

Offset is more or less inevitable for the circuit implementation, which needs to be examined carefully. Similar to the above modulating mechanism, when there is a fixed offset voltage, V_{os3} applied to the switch transistor, M_3 as in Fig.3, the additional flicker noise contribution of RF input stage due to V_{os3} modulating the periodic switched g_{m0} also approximately yields

$$
i_{o,n}(f) = \frac{2g_{m0}V_{n,1}(f)V_{os3}}{ST_{LO}}. \tag{9}
$$

Due to the correlation of two transconductance flicker noises, combining (9)and (5) then leads to

$$
i_{o,n1}(f) = \left(\frac{1}{2} - \frac{2(V_{th} - V_{os3}) - V_{DD,LO}}{ST_{LO}}\right) \cdot g_{m0}V_{n,1}(f). \tag{10}
$$

As disclosed in the equation, without loss of generality, a positive V_{os3} is assumed. It then equivalently enlarges the duty cycle of g_{m0} pulses in Fig.2, leading to the increased noise transfer function. However, due to large ST_{LO}, the effect of V_{os3} on $i_{o,n1}$ is normally small enough to be neglected as shown in Fig.8.

4) SWITCH FLICKER NOISE BY MISMATCH

A mismatch in fabrication also needs to be considered, especially for differential circuits. In practice, mismatch usually is modelled as an offset voltage to simplify analysis [19]. Then, a mismatch in transconductance pairs of the mixer is focused on in this part.

In Fig.5, V_{os1} is the equivalent offset voltage resulted from a mismatch between transconductance pairs. Performing numerical iteration yields the solution of the overdrive voltage V_{ov1} and V_{ov2} of M_1 and M_2. Then by substituting them into I-V and transconductance equations of devices [4], the resulted unbalanced bias current and small-signal transconductance can be obtained, respectively. Then, the unbalanced large-signal current distribution of the differential pair is shown below

$$
i_1 = I_{B1} + \frac{g_{m1}}{g_{m1} + g_{m2}} g_{m3} v_{n,3}(t) \tag{11}
$$

$$i_2 = I_{B2} + \frac{g_{m2}}{g_{m1}+g_{m2}} g_{m3} v_{n,3}(t) \tag{12}$$

where I_{B1} and I_{B2} are the bias current in M_1 and M_2 by enabled LO level. The unbalanced current distribution in transconductance pairs by V_{os1} will lead to the differential mode low-frequency noise output in two mechanisms: One is that noise pulses are added to the bias current in M_1 and M_2 by $v_{n3}(t)$ modulating the turn-on instant time; the other is the small-signal output as in the second item of the equations.

Firstly, the noise current in the time domain by modulated bias current pulses is shown below

$$i_{o,n}(t) = \sum_{k=-\infty}^{+\infty} \frac{\Delta I_B v_{n3}(t)}{S} \cdot [\delta(t - t_1 - kT_{LO}) + \delta(t - t_2 - kT_{LO})] \tag{13}$$

where ΔI_B equals I_{B1}-I_{B2}. We take Fourier transform again and only consider the DCR case. The induced flicker noise output from the switch transistor becomes

$$i_{o,n3,dc}(f) = \frac{2\Delta I_B}{ST_{LO}} V_{n,3}(f). \tag{14}$$

Secondly, by differencing currents of i_1 and i_2 over one LO period, the ac average residual flicker noise leakage current in the frequency domain is

$$i_{o,n3,\mathrm{ac}}(f) = \left(\frac{1}{2} - \frac{2V_{th} - V_{DD,LO}}{ST_{LO}}\right) \frac{g_{m1} - g_{m2}}{g_{m1} + g_{m2}} g_{m3} V_{n,3}(f). \tag{15}$$

The item in bracket indicates the dc component of the time-varying transconductance of M_1 and M_2. The effect of C_P shunting the noise current converted from $V_{n,3}(f)$ is neglected due to interested low-frequency noise traits. In sum, due to device mismatch the common-mode noise source, $v_{n3}(t)$ not only modulates the turn-on instant time of I_{B1} and I_{B2} but also generates unbalanced ac flicker noise currents, leading to differential mode flicker noise output. Simulation has disclosed the corresponding noise contribution of the latter is much larger than that of the former that can be neglected.

C. NOISE FACTOR

Considering the uncorrelation of noise sources V_{n1} and V_{n3} and the number of transconductance transistors and switches, the total flicker noise output current of the proposed mixer is shown as

$$i_{o,n}^2(f) = 4i_{o,n1}^2(f) + 2\left[i_{o,n3,dc}(f) + i_{o,n3,ac}(f) + i_{o,n3,blk}(f)\right]^2. \tag{16}$$

With flicker noise contributions further included, the single side-band (SSB) noise factor (F) for the proposed mixer is

$$F_{SSB} = \frac{\alpha}{c^2} + \frac{2(\gamma + r_g g_{m0}) g_{m0}\alpha + \frac{1}{R_L} + i_{o,n}^2(f)/4KT}{c^2 g_{m0}^2 R_s} \tag{17}$$

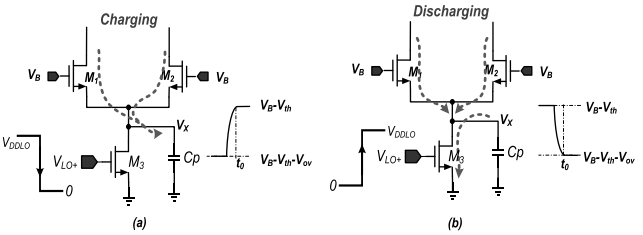

FIGURE 6. Diagram of parasitic capacitance CP (a) charging and (b) discharging at tail net.

where γ is the noise excess factor, and r_g is the gate resistance of the transconductance stage. K and T are Boltzmann constant and temperature with the noise folding factor, α approximately equaling $1\text{-}8t_1 f_{LO}/3$. When the frequency is high enough to make flicker noise negligible, the equation collapses to the thermal noise expression in [3], namely

$$F_{SSB,thermal} = \frac{\alpha}{c^2} + \frac{2(\gamma + r_g g_{m0}) g_{m0}\alpha + \frac{1}{R_L}}{c^2 g_{m0}^2 R_s}. \tag{18}$$

Then, combining (16) and (18) yields an estimation of a flicker noise corner below

$$f_{corner} = \frac{K_f}{C_{OX} WL} \cdot \frac{g_{m0}^2 \left[\frac{1}{2} - \frac{2(V_{th} - V_{os3}) - V_{DD,LO}}{ST_{LO}}\right]^2}{kT\left[\alpha g_{m0}^2 R_s + 2(\gamma + r_g g_{m0}) g_{m0}\alpha + \frac{1}{R_L}\right]}. \tag{19}$$

Especially, the flicker noise mechanism via switches is not included in (19) as discussed in section III. Additionally as disclosed in (17), the common-mode noise contributed by switches can be cancelled by differential configurations except that increasing g_{m0} is all along an effective way to reduce the overall noise factor. More beneficially, the indirect noise mechanism of switches is removed, too. Recently, trapezoid LO instead of sinusoidal one as a way of enhancing frequency-conversion efficiency has been increasingly used in practical scenarios to improve gain and noise [18]. Furthermore, imbalanced phase of differential LOs possibly due to imperfect VCO outputs or unequal delay time of transmission lines also can degrade parameter c and α, and even deteriorate IP2 due to equivalently pushing the mixer into ON overlap mode [19]. Thus it is beneficial to implement trapezoid-shaped LO generation with phase adjustment to trim the differential LO signals in exact off-phase style. In the paper, an inverter-based LO generation is adopted to achieve this goal as in section IV.

D. HIGH-FREQUENCY LIMITATIONS

With increased frequency, the time constant of C_P charging and discharging could become comparable to the LO period, T_{LO}, making the aforementioned trapezoid approximation inaccurate anymore. It is thus necessary to estimate the effect. For analysis simplicity, the distributed parasitic capacitance at the tail net is equivalent to a lumped capacitor C_p. Quantitatively, we have $C_p \approx 2(C_{gs1}+C_{ds1}+C_{sb1}) + C_{gd3}+C_{db3}+C_{ds3}$. Shown in Fig. 6(a) is the diagram of

parasitic capacitance C_P charging at the tail net, where V_B denotes the bias of the transconductance pair. When V_{LO} toggled to ground, the net voltage, Vx initially keeps a low level and the transconductance pair still stays in the saturation region. The current of the transconductance pair then will charge capacitance C_P until V_x is increased to a level lower than V_B with a threshold voltage. Derivation shows the charging time constant below

$$t_0 = \frac{\alpha}{(1-\alpha)} \frac{1}{V_{OV}} \frac{C_p}{2K}. \tag{20}$$

V_{ov} represents the overdrive voltage of transconductance pairs. K depends on the technology and size of devices. Parameter α is defined to describe charged V_x approaching the intermediate variable V_{x0} (typically α takes 0.9)

$$V_{X0} = V_B - V_{th} - (1-\alpha)\, V_{OV} \tag{21}$$

On the other hand, when V_{LO} is toggled to V_{DDLO}, the switch is turned on and the initial high level of V_x, will drop down with the discharging current of C_P flowing away through the current source transistor in saturation. The discharging process in Fig.6(b) can also be derived to obtain the discharging time constant t_0

$$t_0 = \frac{V_{OV} C_p}{I_B}. \tag{22}$$

At the discharging time constant t_0 point, the transconductance pair will fix the V_x around a level lower than V_B with a threshold voltage plus overdrive voltage, i.e., $V_{th} + V_{ov}$. Interestingly, the slow charging in (20) and fast discharging in (22) indicates an unsymmetrical V_x voltage waveform in the time domain, which is validated in section IV.

E. MIXER COMMON-MODE REJECTION RATIO

A large common-mode rejection ratio is highly desirable for integrated chips typically in differential architectures. The metric just indicates that wanted differential input signals are amplified while the unwanted common-mode signal is effectively inhibited. This metric is also widely used to describe the mismatch of differential amplifiers. An extended definition of mixer common-mode rejection ratio (MCMRR) has been introduced in [20] to estimate mismatch appearing in the mixer that in turn, could degrade the feedthrough of mixers eventually. Specifically, performing the corresponding derivation for the proposed mixer leads to the below expression

$$MCMRR = \frac{g_{m1} + g_{m2} + 4 g_{m1} g_{m2} Z_s}{2\,(g_{m1} - g_{m2})} \tag{23}$$

where parameter g_{m1} and g_{m2} donate the transconductance of the transistors M_1 and M_2. There is g_{m1}=g_{m2} =g_{m0} for ideal symmetry previously assumed in the transconductance pair. The MCMMR of the traditional SwGm mixer is the same as the equation in form but is with different Zs due to different operation regions of the switch stage.

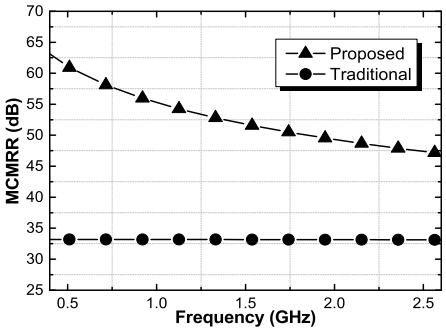

FIGURE 7. Calculated mixer common-mode rejection ratio (MCMRR).

TABLE 1. Parameters used in simulations.

f_{LO}	0.5, 1 GHz	g_{m1}, g_{m2}	12.5 mS
I_B	2.2 mA	V_{ov1},V_{ov2}	97 mV
C_P	0.13 pF	S	6×10^9 V/s
V_{DDLO}	0.7 V	V_B	0.9 V

To compare the MCMRR quantitatively, the traditional SwGm mixer is designed by adjusting the bias of transconductance pairs to keep the power consumption identical to that of the proposed mixer with current source switches. For the calculation of the MCMRR, the parameter values of circuits are acquired from simulations, including the input transconductance, $g_{m0,}$ and equivalent resistance Zs. Specifically, g_{m0} value for the two mixers is 12.5 mS. and Zs value of the traditional SwGm mixer is 55Ω||0.15pF while that of the proposed mixer is 10KΩ||0.13pF. The equation (23) for the two mixers is plotted in Fig. 7 by assuming that there is 5% mismatch between g_{m1} and g_{m2}. It shows that the calculated MCMRR of the proposed mixer is much higher than that of the traditional SwGm mixer across the interested GHz frequency band. Thus, the rejection of common-mode interferences at the gate of switches and the isolation between ports are expected higher in the proposed mixer compared to the conventional SwGm mixer.

III. THEORY VERIFICATION BY SIMULATIONS

To validate the presented flicker noise theory, the mixer in Fig. 1 is simulated in a standard 0.18 um process using Spectre-RF at different LO frequencies. A trapezoid-wave LO stimulus was adopted for both hand calculations and simulations. Other parameters are shown in Table 1 unless otherwise indicated for simulations. A sinusoidal signal with an amplitude of 1 mV and a frequency of 1 MHz, models the low-frequency flicker noise input source at the gate of MOSFETs. The amplitude of the output signal at 1 MHz is taken from the FFT of the output signal. The gain from the noise port to the output is then deduced.

Shown in Fig. 8(a) is the pre-simulated and calculated flicker noise transfer function of the transconductance transistor to the output current. As predicted by (5). The transfer function decreases as the LO frequency goes up,

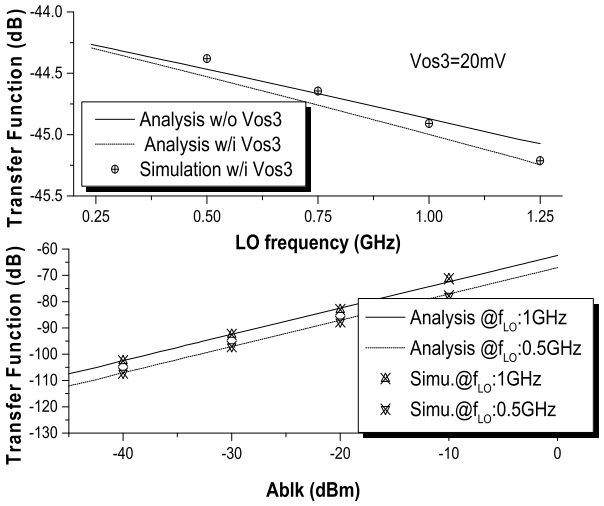

FIGURE 8. Transfer function of the transconductance flicker noise to the output current. (b). Transfer function of the switch flicker noise to the output current in the presence of the blocker with $f_{blk}=f_{LO}+f_{in}$.

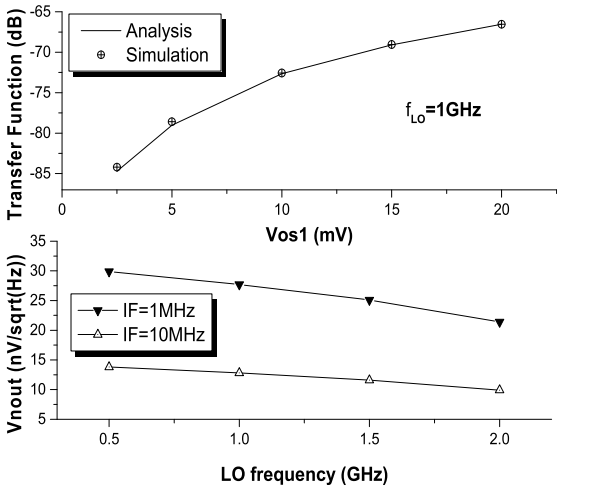

FIGURE 9. Transfer function of the switch flicker noise to the output current noise at the output of the mixer due to mismatch represented by offset voltage, Vos1. (b). Output noise with variations of LO frequency for the mixer.

corresponding to decreased ST_{LO}. Although the transconductance flicker noise transferred to output is decreased with decreased ST_{LO}, the accompanied conversion gain also degrades as disclosed in (1) and (3). Moreover, as in the previous analysis, the transconductance flicker noise is also modulated by the random offset voltage V_{os3} applied to the gate of switches. Thus leakage gain of the transconductance flicker noise to the output current under typical $V_{os3} = 20$ mV with respect to variations of LO frequency is also depicted. Compared to the direct flicker noise mechanism by (5), note that the additional noise contribution in (9) by the offset voltage V_{os3} disturbing switching event is much smaller and negligible. By applying a trapezoid-wave LO under the fixed S but with different LO frequencies, simulation is performed as in the figure where close agreement is seen between the simulation and theory.

Fig. 8(b) shows the simulated and calculated transfer function of the switch flicker noise to the output current of the mixer with respect to the amplitude, A_{blk} when the blocker of $f_{blk}=f_{LO}+f_{in}$ is present at the input of the mixer. The QPSS and QPAC tools are used for simulations. The output flicker noise increases with blocker amplitude, A_{blk}, specifically reaching a simulated value of -77.8 dB and -71.3 for the input amplitude, A_{blk} of -10 dBm under $f_{LO} = 0.5$ and 1 GHz, respectively. To overcome this issue, an LNA preceding the mixer with the frequency-dependent load instead of pure resistive one possibly gains the benefit to filter out these blockers.

Fig.9(a) displays the calculated transfer function of the switch flicker noise to the output current noise, due to mismatch of transconductance pairs modeled by offset voltage, V_{os1} at the gate of the transconductance transistor, M1. For example, V_{os1} taking 10 and 20 mV leads to calculated $\Delta g_m = 0.6$ and 1.3 mS, respectively. The simulation result agrees with the theory very well at $f_{LO} = 1$ GHz. The simulation also indicates, compared to the contribution by mismatched small-signal transconductance, $\Delta g_{m,}$ the contribution by mismatched bias current, ΔI_B is much smaller and can be negligible. With the increased V_{os1}, note that the output flicker noise increases rapidly and can reach the noise transfer contribution due to blocker interference. For example, the noise contribution by $V_{os1} = 12$ mV in Fig.8(a) is equivalent to that by A_{blk} of -10dBm in Fig.7(b) under $f_{LO} = 1$ GHz. The output noise of the proposed mixer as simulated in Fig.9(b) also decreases with increased LO frequency. It validates the removed indirect noise mechanism via parasitics in Section II.B.2). In contrast, that of the Gilbert mixer shows the opposite trend [3]. The indirect noise mechanism in Gilbert mixer can greatly rise up the NF, especially at high frequencies, thus making the SwGm mixer more competitive in this scenario.

According to these obtained flicker noise transfer functions, the predominant flicker noise contributor of the mixer is transconductance pairs. It means that the input-referred flicker noise of transconductance pairs can severely raise the mixer's noise floor at low frequencies. For wideband receivers, things get more troublesome. Flicker noise of switches also can mix with blockers distributed at series of specific frequencies points, and be down-converted to baseband even if transconductance pairs are perfectly matched. With further considerations of inevitable mismatch in practical transconductance pairs, the switch flicker noise also constitutes the other source to the output current noise of the mixer. In the paper, by considering that blockers can be significantly filtered out provided that a saw filter/or n-path filter is [21], [22] preceding the mixer building block along the receiver chain. Moreover, the flicker noise mechanism via the switches can be neglected if the transconductance pairs are also with negligible mismatch by careful layout

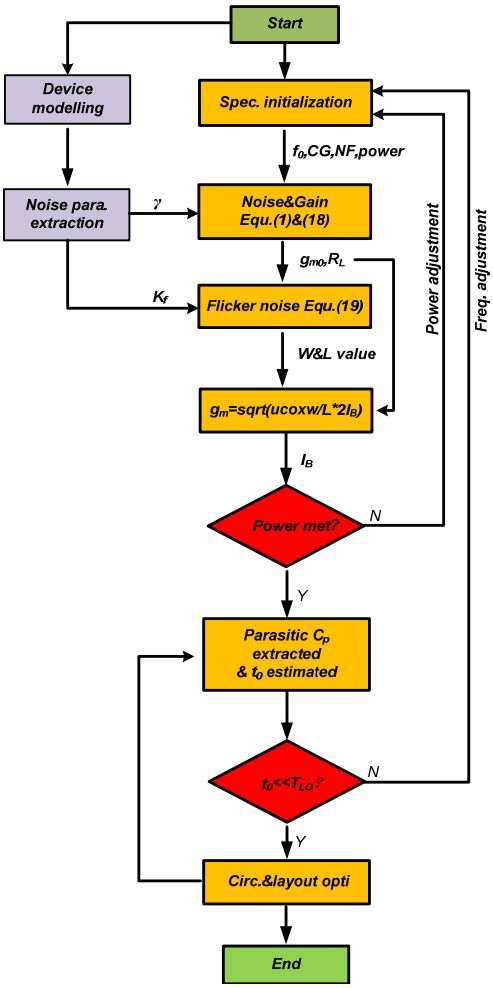

FIGURE 10. Design flow of the proposed mixer.

optimization. The flicker noise of transconductance pairs thus is concentrated on.

As in (2), increasing the scaling size of devices can generally reduce the input-referred flicker noise, but sacrifice certain bandwidth. What's more, according to [23], [24], for devices in a saturation region with the same scaling size, pMOS has much lower input-referred noise compared to nMOS. In addition, smaller overdrive voltage is also beneficial for a low flicker noise target [17]. Here Fig.10 provides a design flow for a low flicker noise pMOS SwGm mixer. Specifically, for tentative specifications of thermal noise figure, NF=10 dB, and conversion gain CG=13 dB, the parameter requirements for $g_{m0} = 11$ mS and $R_L = 800\ \Omega$ is computed by (1) and (18) with typical S as in Table 1. And it is also verified that $t_1 = 27$ ps. To obtain a flicker noise corner of ∼180 kHz, Equ. (19) further determines the width of pMOS transconductance transistors, roughly taking 210 um. Eventually, with the above determined g_{m0} and width of transistors, the dc current of a single transconductance transistor is biased around 0.95 mA while the resulting lower overdrive voltage of $V_{ov} = 95$ mV for transconductance pairs is also

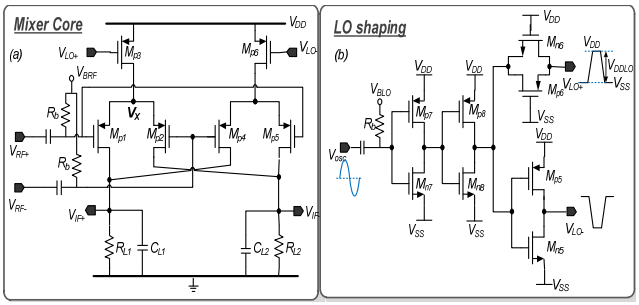

FIGURE 11. (a) Proposed mixer core and (b) LO generation chain.

beneficial for flicker noise consideration. On the other hand, the high-frequency limitation by the tail capacitor also should be checked. After extracting the layout parasitic, the resulting C_P is 710 fF. Then the time delay estimation of $t_0 = 35.5$ ps is resulted by (22). A switching time offset of t_0+t_1 <0.1 ns is thus accumulated in practice. So the high-frequency operation of the mixer still is maintained under $f_{LO} = 1$ GHz. Particularly, the noise parameters of $K_f = 4.5 \times 10^{-25}$ and $\gamma = 1.9$ obtained by device characterization are used for the thermal and flicker noise estimation of the mixer. In sum, to obtain low flicker noise performance, transistors of the proposed mixer core is desirable in pMOS under reduced overdrive voltage. The scaling size of transconductance pairs is moderate large not to degrade the bandwidth of the mixer. In practice, simulations are performed repeatedly to negotiate these metrics in terms of frequency, power consumption, conversion gain, and noise.

IV. MEASUREMENT RESULTS

By following the design flow presented in Fig.10, a mixer prototype with full pMOS configuration in Fig.11 (a) has been further implemented in a standard 0.18-μm RF CMOS technology. The width values of the main components include M_{p1}&M_{p2}: 210 μm, M_{p3}: 150 μm. The length of transistors unanimously takes the minimum process length, 180 nm. The load resistors of $R_L = 800\ \Omega$ are used. Moreover, to perform transconductance pairs switching efficiently, an inverter-based LO generation as in Fig. 11(b) is adopted to shape a sinusoidal LO signal into differential trapezoid signals $V_{LO+/-}$ with the amplitude of V_{DDLO}. An additional logic transmission gate of M_{n6} & M_{p6} with suitable scaling size is introduced to roughly compensate time delay difference between the differential LO signals, $V_{LO+/-}$. Show in Fig.12 is a block diagram of the test setup of the mixer. Measurements by a chip on board (COB) method were reported in comparison with post-simulation results. An off-chip balun generates differential signals for RF input port while a low noise buffer amplifier by LT1007 converts differential outputs to singled-ended one and feed it to test instruments. The mixer core consumes about 1.85 mA from a supply voltage of 1.8 V while the dynamic power of the LO generation chain is about 2 mW at 1 GHz. Fig.12 also displays the layout of the mixer,

TABLE 2. Summary of IF output noise voltage PSD by each component (unit: dBm/Hz with respect to 50Ω).

f_{IF}	Transcond. Pairs		SW	Load stage	RF port	Other	NF (dB)
	1/f noise	Thermal noise					
10 KHz	-130.1	-141.2	-	-152.8	-149.5	-166.2	23.5
Percentage (%)	91.3	7.1	0	0.48	1	0.02	
10 MHz	-162	-141.2	-	-152.8	-149.5	-169	11
Percentage (%)	0.68	81.6	0	5.6	11.9	0.63	

Parameters for simulations: $g_{m1\&}g_{m2}$=11.3 mS, g_{m3}=13 mS, γ=1.9.

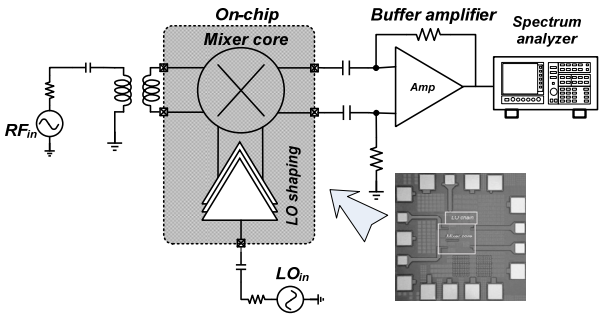

FIGURE 12. Test setup and micrograph of the proposed mixer.

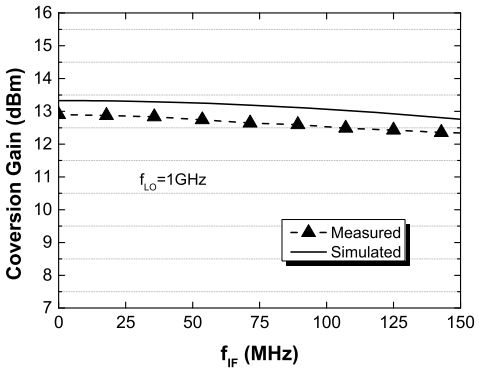

FIGURE 13. Conversion gain with respect to IF when LO frequency, f_{LO} is fixed at 1 GHz.

occupying a size of 634 μm×620 μm with the chip pads included.

With f_{LO} fixed at 1 GHz, the simulated and measured conversion gain of the mixer for the IF, f_{IF} is shown in Fig. 13. The measured conversion gain is 12.9 dB at the IF of 10 MHz. Thanks to the LO generation chain operating, the conversion gain of the proposed mixer is well maintained with a low sinusoidal LO power of −12.5 dBm throughout the paper. Displayed in Fig. 14 are analyzed, simulated, and measured NF_{DSB} with respect to f_{IF}. Lower flicker noise is measured with the corner frequency of around 220 kHz. Theoretical expression in (17) agrees with the measurement well. To further gain knowledge of noise contribution percentage from each component of the mixer, output noise voltage power spectrum density (PSD), is simulated by PSS

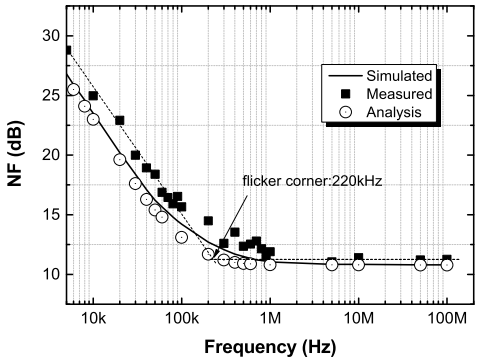

FIGURE 14. NF with respect to the IF frequency, f_{IF}.

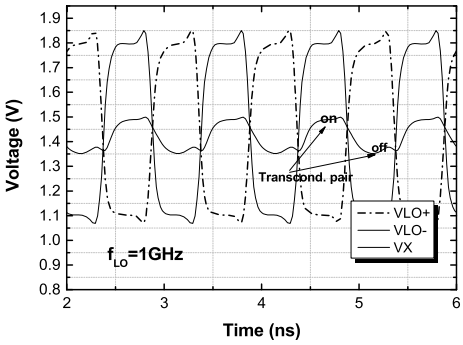

FIGURE 15. Steady-state time-domain response at the tail net.

and PNOISE simulators and tabulated in Table 2 with normalization to dBm/Hz for a 50 Ω system. As expected, the switches only yield canceled common-mode noise output irrespective of IF variations. Demonstrated in Fig. 15 is the simulated steady-state time-domain response waveform of the mixer at f_{LO} = 1 GHz. With the stimulus of trapezoid LO signals $V_{LO+/-}$ toggling between V_{DD} and V_{SS}, the RF input stage is periodically switched on and off along with the time-varying tail net voltage, Vx where the faster charging and slower discharging of C_p are observed in accordance with the theoretical predictions in Section II.D for the proposed mixer in full pMOS. And a two-tone test with 10 MHz separation at 1GHz frequency also indicates a measured IIP3 of 3.6 dBm displayed in Fig.16. By applying a test signal of −30 dBm at one port of the mixer and observing response at another port of that, port isolations of the mixer are measured across the interested frequency band and shown in Fig.17. Due to the current source switching with the improved MCMMR, the mixer has good isolation measurements, where the worst isolation of RF-IF is still below −30dB.

Table 3 summarizes performance comparisons with other previously reported low flicker noise active mixers. The proposed switched-g_m mixer achieves a comparable figure-of-merit (FOM) and flicker noise corner performance even without utilizing state-of-the-art process technology. Compared to the traditional switched-g_m mixer [3], our design achieves much lower NF thanks to the larger transconductance value of g_{m1} and g_{m2}. Mainly to focus on examining

TABLE 3. Performance summaries of proposed mixer and comparison to previously reported mixers.

Parameter	Frequency (GHz)	Maximal CG (dB)	DSB NF* (dB)	IIP3 (dBm)	Flicker corner	No. of Ind	Power (mW)	FOM[d]	Architecture type	CMOS (nm)
[3]JSSC04	2	10	23.7	6	~1 MHz	0	0.6	0.18	SwGm	180
[11]TMTT06	5.2	16.2	9.8	-5	125 KHz	2	7	0.18	Gilbert	180
[12]TMTT08	2.4	11.4	7.8[a]	4.4	-	3	9	0.54	Gilbert	130
[13]JSSC13	0.9	17.6	10.1	11.8	70 KHz	0	19.6	0.57	Gilbert	160
[25]MWCL17	2.1	24.1[c]	4.1	-14.5	150 KHz	4	2.1	0.36	Gilbert	130
[26]MJ11	3.4-6.8	4.3-7.2	13.9-14.4	2-3	NA	4	2.9	NA	SwGm	180
T. W.	**1**	**12.9**	**11.4**	**3.6**	**220** KHz	**0**	**3.3**	**0.24**	SwGm	**180**

*Results at f_{IF}=10MHz; [a]Estimation; [b]Result at f_{IF}=1MHz; [c]with matched S_{11}. [d]FOM= Freq.(GHz).Gain(lin).IIP3(mW)/P_{DC}(mW)/(NF(lin)-1)

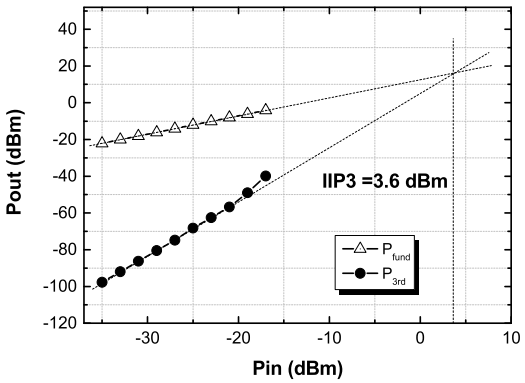

FIGURE 16. IIP3 results at 1 GHz frequency point.

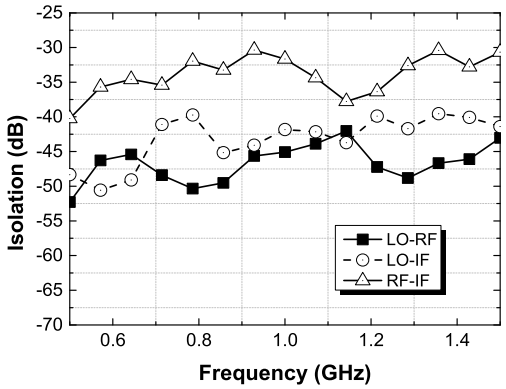

FIGURE 17. Port to port isolations.

the flicker noise transfer mechanism in this article, there is no optimizing technique of inductors resonance exploited in the proposed mixer, to mitigate the limitation of parasitic capacitances to gain and noise of mixers as in [11], [12], [25], [26]. And the proposed mixer achieves good flicker noise corner performance even without utilizing a state-of-the-art CMOS process.

V. CONCLUSION

A quasi-analytical model has been developed to explain the flicker noise mechanisms in the switched-g_m active mixer. Compact equations are derived to estimate the flicker noise contribution of the individual stages of the mixer at the output. Simulations validate the accuracy of the proposed model that provides the necessary insight to design and optimize the mixer for low flicker noise application. A switched-g_m mixer prototype in full p-type MOSFETs is implemented in 0.18 um CMOS process. Results indicate that the proposed mixer with low flicker noise and high common-mode rejection ratio can serve as a potential solution for the popular DCR applications.

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