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Digital and Analog Switching Characteristics of InGaZnO Memristor Depending on Top Electrode Material for Neuromorphic System

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ABSTRACT In this study, we demonstrate both of digital and analog memory operations in InGaZnO (IGZO) memristor devices by controlling the electrode materials for neuromorphic application. The switching properties of the devices are determined by the initial energy barrier characteristics between the metal electrodes and the IGZO switching layer. Digital switching characteristics are obtained after the forming process when Schottky junction occurs at both of top and bottom electrodes. On the other hands, analog resistive switching is achieved when Schottky and Ohmic junctions exist at each side because the applied voltage modulates the Schottky barrier height through the Ohmic contact. In addition, the weight-update properties of the devices are verified depending on identical and incremental pulse schemes. The incremental pulse trains improve the linearity and variation of weight modulation, leading to the stable learning characteristics of neuromorphic system in terms of pattern recognition with MNIST hand-written digit images.

INDEX TERMS Analog switching, BEOL compatible, digital switching, InGaZnO memristor, neuromorphic system.

I. INTRODUCTION

The von Neumann computing architecture separating processing and memory and elements and maximizing the efficiency between them has led the digital era for decades in accordance with the Moore's law of downscaling [1]. However, an inevitable bottleneck of the von Neumann architecture due to the data transfer between processing and memory elements has become a major factor causing significant latency and power consumption [2]. Neuromorphic system is a potential candidate for beyond von Neumann computing era to solve this issue by mimicking a massively parallel processing of biological nervous systems and has recently gained interest by demonstrating cognitive functions including pattern recognition [3]–[13]. Since synaptic devices play a key role of not only storing information but also constructing neural network and transferring signals, various kinds of artificial synaptic devices have been investigated and demonstrated including memristors and transistors [14]–[21]. Typically, synaptic devices are required to have analog switching characteristics considering floating-point weight values of artificial neural network. In addition, synaptic device array needs to be co-integrated with driving circuitry such as an integrate-and-fire neuron circuit, reconfigurable logic, or in-memory computing part in the back-end-of-line (BEOL) process to construct the whole system. In these regards, it is necessary to realize field-effect transistors, digital and analog memories with an identical semiconducting material for the co-integration of them.

Memristive devices have been considered one of the most promising candidates as a synaptic device thanks to their simple structure, low operating voltage, and fast switching

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speed, and the resistive switching behaviors by the redox reaction of oxide-based materials such as TiO_x, TaO_x, WO_x, AlO_x, HfO_x, and $Pr_xCa_{1-x}MnO_3$ (PCMO) have been demonstrated [22]–[30]. In general, digital and analog switching behaviors in a memristive device can be obtained through the formation and rupture of conducting filaments by redox reactions and by oxidation-reduction or charge trapping-detrapping, respectively. Moon *et al.* reported that utilizing Mo as the top electrode (TE) material forms an interfacial oxide layer between of the TE and PCMO layer due to the redox reaction at the interface, and limits the conducting filament to the interfacial oxide layer instead of PCMO layer, providing analog switching properties [31]. Li *et al.* reported that the oxygen-gradient HfO_x layer can be served as a multifunctional memristor having both of digital and analog switching characteristics by the formation of a cone-shape conducting filament [32]. Lin *et al.* also reported the both analog and digital switching behaviors using the Schottky barrier modulation between the TE (Au) and WO_{3-x} layers, and the formation and dilapidation of conductive filaments in the switching layer, respectively [33].

InGaZnO (IGZO) has been widely used in display and flexible electronics thanks to the advantages of high mobility, uniformity, transparency, and low-temperature processing [34]–[40]. In particular, IGZO devices have been recently studied in applications such as wearable healthcare and biosensor, where energy-efficient and flexible logic and memory technologies are needed to process a huge amount of bio-electrical information [41]–[43]. In addition, IGZO transistors have attracted attention as a promising technology of the BEOL compatible field-effect transistor for the co-integration with Si-CMOS circuitry thanks to low-temperature process and highly uniform characteristics [44], [45]. Therefore, it is necessary to implement logic and memory devices in the same substrate with low-temperature and compatible process to each other for wearable and flexible electronics. From this point of view, utilizing IGZO material for both a logic transistor and memory device can be a promising solution for the co-integration of processing and memory elements.

In this study, we demonstrate both digital and analog memory operations in the IGZO memristors with different TE materials: Pd and Mo. The effect of the Schottky barrier between the metal and the IGZO layer on the switching characteristics of the memristors has been studied. In addition, the learning properties of the IGZO memristors as a synaptic device are verified with identical and incremental training pulses for neuromorphic applications. Finally, the effect of the linearity and variation of weight modulation is analyzed in terms of the recognition accuracy for MNIST hand-written digit images.

II. EXPERIMENTAL METHOD

Fig. 1 shows the process flow of the IGZO memristors used in this study. Firstly, 40-nm of Pd for the bottom electrode (BE) was deposited on an SiO_2 (50 nm)/p^+-Si substrate by

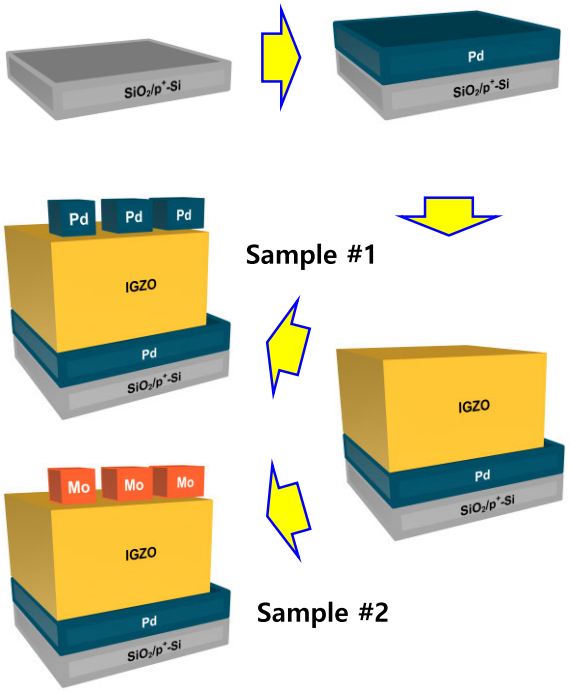

FIGURE 1. Fabrication process of IGZO memristors.

e-beam evaporator, then 80-nm thick IGZO thin film was deposited by sputtering at room temperature with RF power of 150 W and gas flow of $Ar/O_2 = 3/2$ sccm. Finally, 40-nm of Pd (sample #1, S1) and Mo (sample #2, S2) layers were deposited as the TE using an e-beam evaporator and patterned with the shadow mask of which area was $100 \times 300\ \mu m^2$. All the electrical measurements in this study were carried out with Keithley 4200 SCS to evaluate resistive switching characteristics and learning properties with pulse trains; here, all the dc I-V characteristics were measured with a ramp rate of 2 V/s.

III. RESULTS AND DISCUSSION

Figs. 2(a) and (b) show the consecutive double dc sweep I-V characteristics of the IGZO memristors with the different TE materials (Pd and Mo). Here, the sweep direction of the double voltage sweep was $0 \rightarrow V_{negative} \rightarrow 0$ and then $0 \rightarrow V_{positive} \rightarrow 0$. S1 requires a electroforming process performed with 10 mA of the compliance current and 7.5 V of the forming voltage for soft breakdown. In addition, S1 has typical and bipolar switching characteristics with SET and RESET processes during positive sweeps to 6 V and negative sweep to –3.5V, respectively, and features digital and abrupt switching properties. However, S2 exhibits the forming-free switching characteristics and requires 1 μA of much less compliance current even with the identical switching layer in terms of stoichiometry, which implies that S1 and S2 have significantly different conduction mechanisms by the TE. The unrecoverable hard breakdown occurs for S2 when the compliance current was 10 mA which

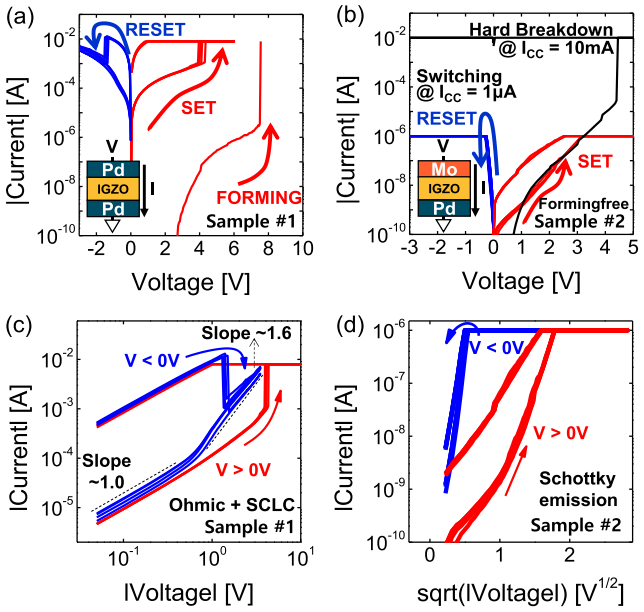

FIGURE 2. Measured I-V switching characteristics of (a) S1 and (b) S2. (c) Log(I)-linear(|V|) and (d) log(I)-sqrt(|V|) plots of the I-V curves for both S1 and S2.

was used for the switching of S1 as shown in Fig. 2(b). Moreover, it is observed that there are gradual switching properties during the consecutive SET (sweep to 5 V) and RESET (sweep to –3 V) processes. In order to analyze the conduction mechanisms of both devices, the I-V curves of S1 and S2 are replotted in log-log and log-square root diagrams as shown in Figs. 2(c) and (d), respectively. S1 shows Ohmic conduction ($I \propto V$) in both high-resistance state (HRS) and low-resistance state (LRS) when positive voltage is applied, while it exhibits ohmic conduction in a low voltage regime, and space-charge-limited-current (SCLC) conduction characteristics ($I \propto V^2$) in a high voltage regime when negatively biased. In contrast, Schottky emission ($\log(I) \propto V^{1/2}$) is dominant all over the voltage regime in the case of S2 for both HRS and LRS.

To understand these behaviors in detail, the flat band diagrams of S1 and S2 are illustrated with work function, electron affinity, and bandgap values in Fig. 3(a), and energy band diagrams in equilibrium of S1 and S2 are depicted in Fig. 3(b). It confirms that a back-to-back Schottky junction is formed in Pd/IGZO/Pd stack of S1, whereas Ohmic and Schottky junctions are made at Mo/IGZO and IGZO/Pd junctions of S2, respectively. In addition, Figs. 3(c) and (d) show the energy band diagrams of S1 and S2 when positively and negatively biased, respectively.

Since the I-V characteristics of S1 are dominated by the Schottky barriers regardless of the polarity of applied voltage due to the back-to-back Schottky junction, the Schottky barrier lowering due to soft breakdown needs to be conducted for resistive switching properties by the migration of oxygen ions. In other words, the forming process under a high positive bias condition in Fig. 2(a) lowers the Schottky barrier height by a strong electric field as shown in Fig. 3(c), then oxygen vacancies start migrating to BE, which forms conductive filaments in the IGZO layer by ionized oxygen vacancies and changes the device state in LRS. When a negative voltage is applied, the migration of oxygen vacancies from BE to TE ruptures the conducting filaments, and the device is switched back to HRS. After this RESET process, the oxygen vacancies construct the filament again when a positive voltage is applied (SET process), and the overall schematic view of these switching behaviors of S1 is described in Fig. 4(a).

On the other hand, the Schottky emission properties of the I-V characteristics of S2 in Fig. 2(d) can be explained not by the Ohmic junction at Mo/IGZO but by the Schottky junction at IGZO/Pd. As shown in Figs. 3(c) and (d), most of the applied voltage drops across the Schottky junction and the IGZO layer despite the polarity of the voltage. When a positive voltage is applied, the migration of oxygen vacancies from TE to BE reduces the Schottky barrier height of IGZO/Pd junction, resulting in the SET process. Since the oxygen vacancies can easily migrate due to the Ohmic junction at Mo/IGZO, S2 exhibits the forming-free switching characteristics and breaks down with the high compliance current (10 mA) as shown in Fig. 2(b). However, when the migration of oxygen vacancies occurs from BE to TE by a negatively applied voltage, this migration in the opposite direction increases the Schottky barrier height of IGZO/Pd junction, resulting in the decrease of the device conductance (RESET process). In other words, these Schottky barrier modulations let S2 have the forming-free and analog-grade switching behaviors since the migration of oxygen vacancies can occur without any soft-breakdown of the IGZO layer due to the Ohmic junction at one side, which can be called as non-filamentary resistive switching characteristics [46]. The overall switching diagram of S2 is illustrated in Fig. 4(b).

In order to verify the switching mechanism difference of S1 and S2 more thoroughly, the Schottky barrier height is extracted using Arrhenius plot of I/T^2 for both devices and each state (LRS and HRS). Fig. 5(a) shows that the Schottky barrier height is considerably changed between two states (0.96 eV at HRS and 0.09 eV at LRS) for S1. This is because the conductive filament formed by a strong electric field directly connects TE and BE at LRS, leading to a significantly low barrier height. On the other hand, the Schottky barrier height difference between two states for S2 is relatively small (0.136 eV at HRS and 0.121 eV at LRS) as shown in Fig. 5(b). Since the switching behaviors of S2 are induced not by the electroforming process but by the migration of oxygen vacancies through the Ohmic junction, the Schottky barrier height can be gradually modulated according to how deep the oxygen vacancies migrate into the IGZO layer from TE. These results also support that the Ohmic and SCLC conductions are dominant for S1 and the Schottky emission is dominant for S2, respectively, as discussed in Figs. 2(c) and (d).

In addition, the identical and incremental pulse schemes are applied to the IGZO memristors to verify the learning characteristics of both S1 and S2 as a synaptic device in

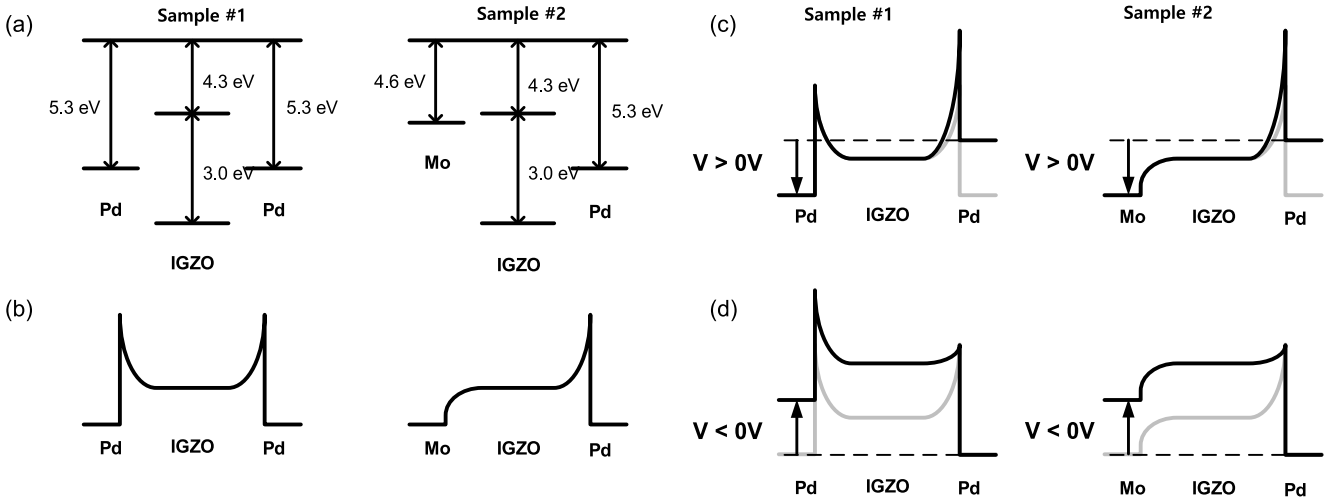

FIGURE 3. (a) Flat band diagrams, and energy band diagrams of Pd/IGZO/Pd (S1) and Mo/IGZO/Pd (S2) memristors in (b) equilibrium, (c) a positively biased condition, and (d) a negatively biased condition.

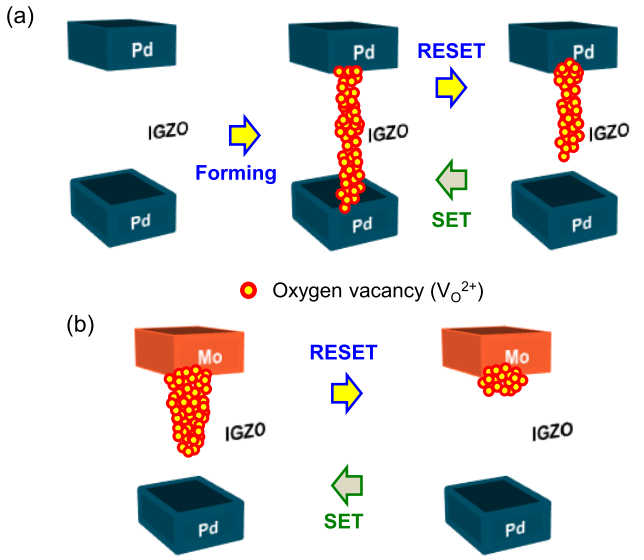

FIGURE 4. Schematic view of switching behaviors of (a) Pd/IGZO/Pd (S1) and (b) Mo/IGZO/Pd (S2) memristors.

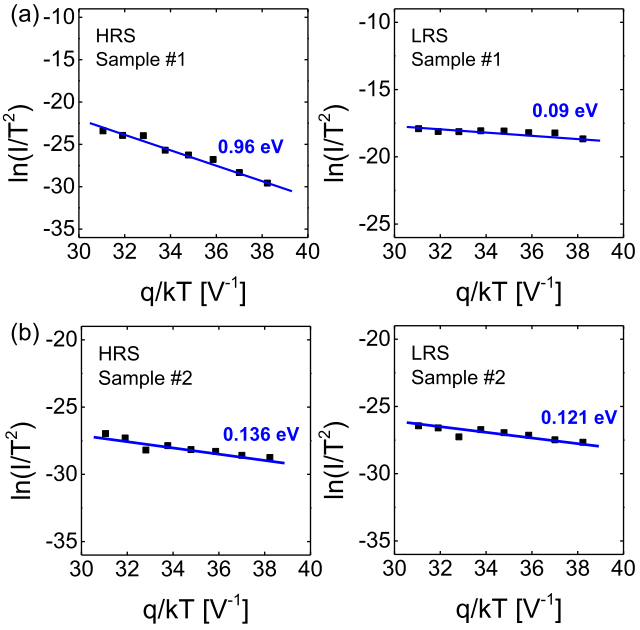

FIGURE 5. Arrhenius plots of I/T^2 for (a) S1 and (b) S2 to extract the Schottky barrier height for each state.

neuromorphic system as shown in Figs. 6(a) and (b). In general, the symmetric and linear weight-update characteristics of synaptic device with regard to conductance are necessary for an accurate weight-mapping of artificial neural network algorithm [47]–[51]. However, most of memristive devices generally have asymmetric and nonlinear switching characteristics during potentiation (SET) and depression (RESET) processes. In order to improve these properties of the IGZO memristors, the time-incremental pulse scheme is utilized by increasing the pulse width of potentiation and depression input signals with the fixed amplitude of potentiation voltage (V_p) and depression voltage (V_d). Considering the switching characteristics of both the samples in Figs. 2(a) and (b), the amplitudes of the training pulses are as follows: V_p for S1 = 4V, V for S1 = –1.5 V, V_p for S2 = 2.8 V, and V_d on for S2 = –1.2 V, while the conductance is measured at 0.5, and 1 V for S1 and S2, respectively. The specific procedure of determining V_p will be discussed below. The pulse widths of the identical pulse train are 2.5 μs and 40 ms for S1 and S2, respectively, whereas the pulse width of the incremental pulse train is set depending on the number of applied pulses (n) as t_{init} (initial pulse width)$\times(1.1)^{n-1}$ where t_{init} = 1 μs and 1 ms for S1 and S2, respectively.

Firstly, the dependency of the V_p on the learning characteristics is verified for both of S1 and S2 using the identical pulse scheme in order to determine the voltage conditions. Here, the number of applied pulses for 1 cycle is 64 for potentiation and depression, respectively, and 5 consecutive cycles are tested.

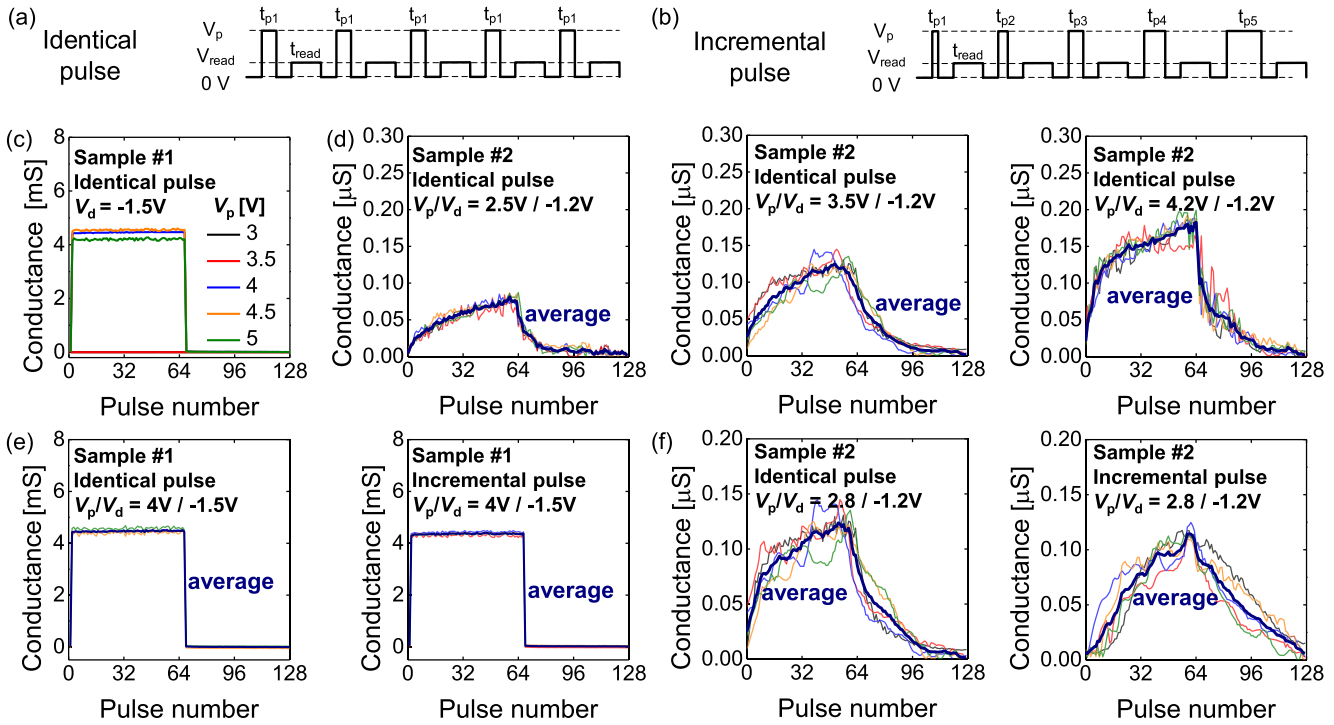

FIGURE 6. Synaptic characteristics of IGZO memristors. (a) Identical pulse scheme. (b) Incremental pulse scheme. Learning characteristics of (c) S1 and (d) S2 depending on V_p. Learning characteristics of (e) S1 and (f) S2 depending on the training pulse schemes.

In the case of S1, the weight is only digitally updated when V_p is higher than 3.5 V as shown in Fig. 6(c). This implies that V_p for S1 needs to be larger than a SET voltage in Fig. 2(a) to change the device state, and V_p under a SET voltage has no influence on the switching behaviors; therefore, V_p for S1 is set as 4 V. In contrast, a higher V_p for S2 provides a wider weight modulation window but degrades the linearity of weight-update as shown in Fig. 6(d). In order to keep a balance between the weight window and linearity, V_p for S2 is set as 2.8 V.

Figs. 6(e) and (f) present how the conductance of S1 and S2 is updated depending on the training pulse schemes, respectively, according to the number of applied potentiation and depression pulses. Despite the pulse scheme, the weight-update properties of S1 shown in Fig. 6(e) are quite digital as the dc switching characteristics in Fig. 2(a), and the conductance of the device is changed in the very first potentiation and depression pulses due to the back-to-back Schottky junction of Pd/IGZO/Pd stack as discussed above. In contrast, the pulse-induced weight-update characteristics of S2 exhibit the symmetric and analog-grade switching by both the pulse schemes, but there is a considerable difference in terms of linearity. As shown in Fig. 6(f), the incremental pulse scheme significantly improves the linearity of weight modulation because the abrupt conductance change in the early stages of the identical pulse scheme can be eased by increasing the pulse width gradually from a relatively short time. Moreover, the variation of weight-update is also improved by the incremental pulse scheme, which is necessary for a stable weight-update protocol.

In order to verify the effect of the linearity and variation of weight-update characteristics, the performance of neuromorphic system composed of the IGZO memristors, S2, having the analog-grade switching behaviors is compared depending on the pulse scheme. The learning characteristics in Fig. 6(f) is used to develop the device model considering both the linearity and variation effects, and each weight value in a single neural network (784 × 10) for the pattern recognition of 28 × 28 gray scale MNIST data is updated following the developed model. The device model for weight-update protocol for this simulation is developed based on the measured amount of conductance change (Δw) in average as a function of a current conductance value (w) and whether w needs to be increased or decreased. The variation effect is considered by varying Δw based on the standard deviation of the measured weight-update characteristics per each training event.

Firstly, the recognition accuracy is compared considering the linearity effect solely with the developed weight-update protocol as shown in Fig. 7(a). The accuracies obtained at 50 epoch by the identical and incremental pulse schemes are 84.92 and 91.34%, respectively, which means the linear weight modulation of the IGZO memeristors effectively improves the performance of the neuromorphic system even without considering the variation effect. In addition, the accuracy is already saturated and stable after 10 epochs with the incremental pulse scheme, whereas the recognition rate is

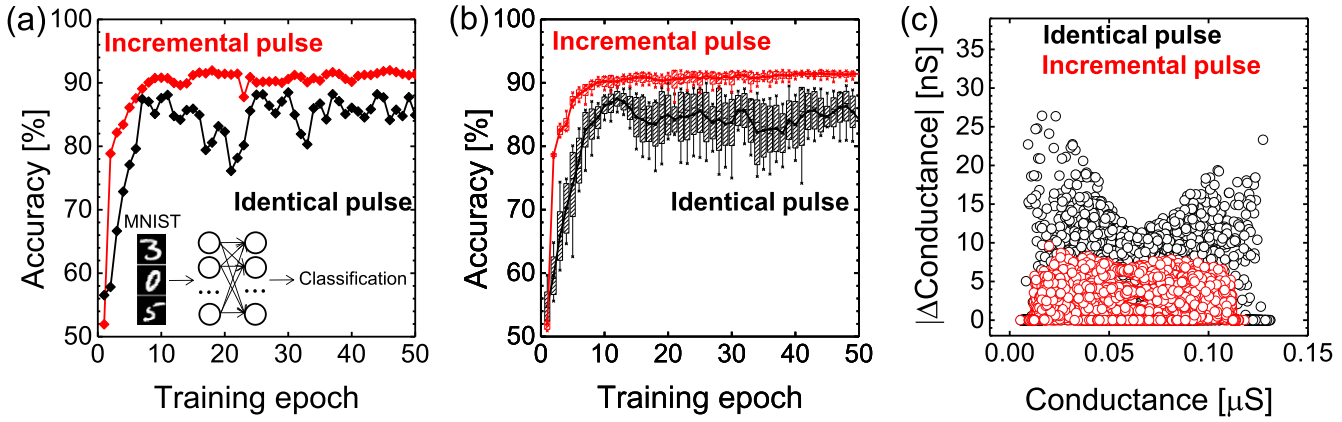

FIGURE 7. Effect of the linearity and variation of weight-update characteristics on the neuromorphic system with the IGZO memristors. (a) Recognition accuracy according to training epoch with the average learning characteristics. (b) Box plot of recognition rate according to training epoch considering the variation effect with 10 trials. (c) The distribution of weight-update values depending on the pulse scheme.

unstable and significantly fluctuates with the identical pulse scheme. This difference becomes more serious when the variation effect is also considered as presented in Fig. 7(b) showing the box plot of the accuracies with 10 trials. In the worst-case scenarios for both pulse schemes, the accuracy drops after one epoch by 10.57% (86.05% → 75.48%) with the identical pulse scheme, but only by 2.09% (91.45% → 89.36%) with the incremental pulse scheme. This can be explained by the fact that high or low weight values near the edge of weight window as a result of a number of trainings can be abruptly changed by a certain training sample which gives an opposite learning trend with others. Fig. 7(c) shows the distribution of the absolute values of weight-update in these two worst cases depending on the pulse scheme. It confirms that the weight values change much greater with the identical pulse scheme when they are located at the edge of the conductance range of the IGZO memristors because of the nonlinear weight-update characteristics; however, the weight values are modulated independently with the current conductance values thanks to the linear weight-update characteristics of the incremental pulse scheme. These results imply that the improved linear and uniform weight-update characteristics by the incremental pulse scheme has a significant influence on the recognition performance of neuromorphic system in terms of accuracy as well as stability.

IV. CONCLUSION

In this study, we have demonstrated that the IGZO memristors can be operated with both the digital and analog switching characteristics depending on the TE material. The switching type was determined by whether TE/IGZO formed Ohmic or Schottky junction. There was the forming process by the strong electric field when the back-to-back Schottky junction was made for the Pd/IGZO/Pd stack (S1), resulting in the Schottky barrier lowering and the abrupt and digital switching properties by the conductive filaments based on oxygen vacancies in the IGZO layer. On the other hand, the Mo/IGZO/PD stack (S2) where the Ohmic and Schottky junction was formed at each side presented the analog switching behaviors because the applied voltage directly affected the modulation of the Schottky barrier height by the migration of oxygen vacancies through the Ohmic junction. In addition, the learning properties of both the samples were investigated depending on the pulse scheme, and the linearity as well as variation of the weight-update characteristics was improved by the incremental pulse train. Lastly, it was verified how this improvement affected the performance of neuromorphic system with the IGZO memristors as a synaptic device by conducting the pattern recognition simulation for MNIST images, and the stable recognition rate over 90% was obtained with the linear weight modulation. We believe these results imply that both the digital and analog memory units can be realized by IGZO material and integrated with IGZO field-effect transistors having the BEOL compatibility according to the applications.

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(Jun Tae Jang and Jungi Min equally contributed to this work.)

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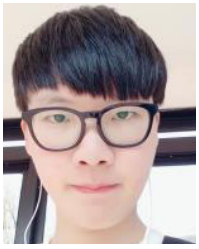

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