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Comprehensive Analysis and Design of Current-Balance Loop in Constant On-Time Controlled Multi-Phase Buck Converter

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ABSTRACT Constant on-time (COT) controlled multi-phase buck converter has been widely used in high-current applications such as computing devices to achieve high entire-load-range efficiency. However, the literature lacks comprehensive analysis and design guide of the current-balance loop in COT control, resulting in possible low efficiency, per-phase current protection false-trigger, and stability issue. To solve the aforementioned issues, dc inductor current equations and small-signal models are proposed for COT control with the current-balance loop. Current-balance loop gain design guideline is then proposed to achieve accurate dc current balance and stability. Experiment and simulation results verify the analysis and the accuracy of the proposed models.

INDEX TERMS Multi-phase converter, constant on-time (COT) control, current-balance, small-signal model.

I. INTRODUCTION

Multi-phase buck converter with constant on-time (COT) control has been widely used in applications requiring low-output-voltage, high-current, and high entire-load-range efficiency such as computing devices and processors [1]–[8]. With the increased computation need from processors, the required output current of converters for computing devices tends to become larger. The multi-phase interleaved buck converter is often used to provide larger output current with reduced output ripple and conduction loss. Constant on-time control is also widely used for these fast-transient loads due to its high light-load efficiency and larger bandwidth design capability.

Fig. 1 shows the circuit diagram of a non-ideal two-phase buck converter with widely used current-mode COT (CMCOT) control considering the parasitic resistances [1]–[5]. V_{in} and V_o represent the input voltage and output voltage, respectively. i_{L1}, i_{L2}, and i_{sum} represent phase1 inductor current, phase2 inductor current, and summation inductor current, respectively. R_{on1} and R_{on2} represent upper switch parasitic resistance in phase1 and phase2, respectively. R_{sr1} and R_{sr2} represent lower switch parasitic resistance in phase1 and phase2, respectively. R_{DCR1} and R_{DCR2} represent inductor DC resistance in phase1 and phase2, respectively. The control scheme reduces circuit complexity by only using one pulse-width modulation (PWM) comparator and summation inductor current for modulation. However, per-phase inductor current is not controlled. Detail control operation will be illustrated in section II.

Multi-phase converter shows thermal and low-efficiency issues if the dc per-phase inductor current is not balanced. As will be analyzed in section II, dc inductor current in each phase will not be the same due to the phase mismatch contributed by manufacturing process error, component parameters mismatch, and asymmetric layout. It will finally lead to reduced efficiency and the thermal problem especially at full-load conditions [9]–[20]. Therefore, converter and control IC manufacturers take the

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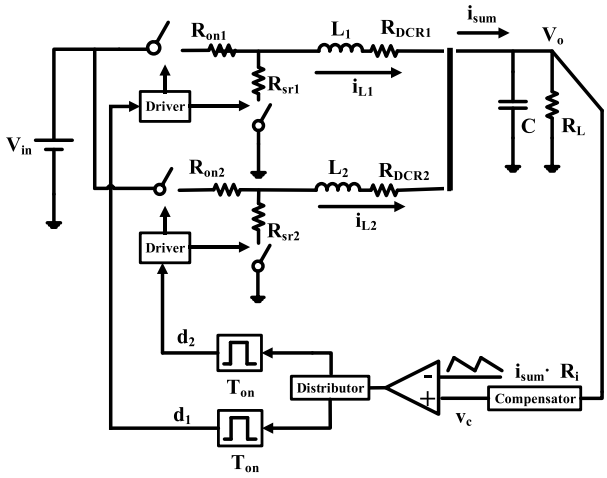

FIGURE 1. Circuit diagram of a non-ideal two-phase buck converter with CMCOT control.

dc current balance as an important specification shown in datasheets.

To overcome the current imbalance problem, active current balance controls were proposed [9]–[20]. In [9], [10], and [19], voltage mode control with a current-balance loop is analyzed. However, dc inductor current equations are not given for close-loop control. For CMCOT control, a current-balance control scheme without a balance loop compensator was reported [11], [14]. As will be shown in Fig. 3, it does not require extra control IC pin and balance loop compensator to achieve current balance control.

However, there is no comprehensive analysis to show the dc current distribution and how to design the current-balance loop parameters for CMCOT control. It results in possible stability issue in current-balance loop. Besides, the imbalanced dc current results in issues such as low efficiency at heavy load, per-phase current protection false-trigger, and thermal issue. Besides, converter and control IC manufacturers cannot determine tolerance band and circuit parameters for current balance.

The contribution of this paper is to propose a comprehensive analysis and design guideline for multiphase buck converter with CMCOT control and current-balance loop. Steady-state per-phase inductor current distribution equations and small-signal model of the current-balance loop are proposed in section III and IV. The analysis can be easily extended to other COT controls and more phase number. With the accurate DC equations, a designer can predict dc per-phase inductor current and design current loop parameters to achieve current balance. Besides, from the proposed small signal model of the current-balance loop, it can predict current-balance loop stability and dynamic current sharing effect during phase number change transient. Section IV shows the simulated and experimental results to verify the proposed models and design guideline.

II. DC CURRENT BALANCE ANALYSIS OF COT CONTROL WITH CURRENT-BALANCE LOOP

Operation of Cot Control With Current-Balance Loop:

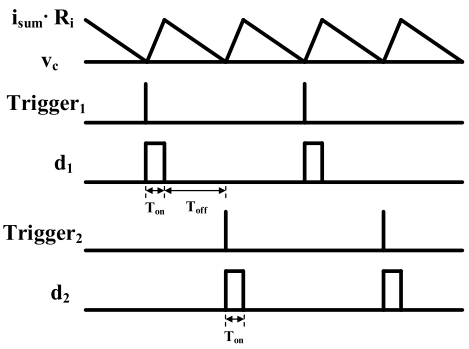

FIGURE 2. Modulation waveform of two-phase CMCOT buck converter.

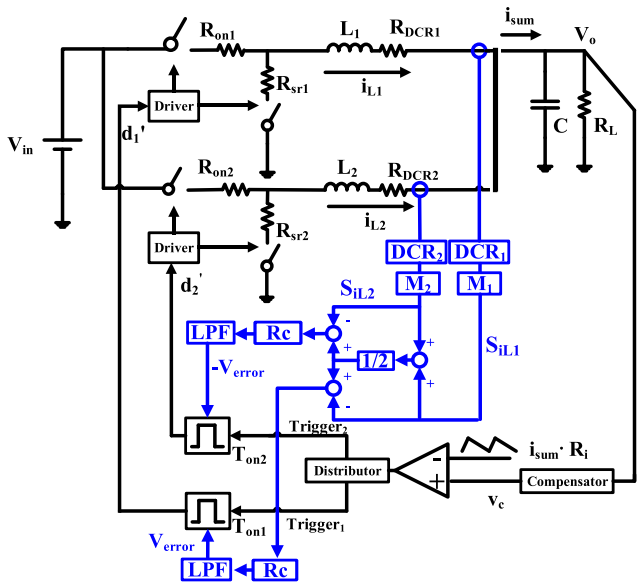

FIGURE 3. Circuit diagram of two-phase CMCOT buck converter with current-balance loop.

Fig. 2 shows the modulation waveforms of two-phase CMCOT buck converter in Fig. 1. There are two feedback signals in the control. One is the compensated output voltage V_c, and the other is the summation current feedback signal $i_{sum}\cdot R_i$, where R_i is the current sensing gain. These two signals determine the turn-on timing of two duty cycles through PWM comparator and distributor. When the two feedback signals intersect, the comparator sends turn-on instant to the distributor. The distributor sends trigger signals to the on-time generators of phase 1 and phase 2 in a rotating manner. Therefore, the two on-time generators take turns issuing fixed on-time to the drivers. Since only the summation current instead of per-phase currents is fed back, and only one PWM modulator is used. The per-phase current is not controlled. As will be derived in this section, the mismatch of parasitic resistances between phases generates unbalanced dc currents. To achieve current balance, per-phase currents have to be sensed to adjust on-time in each phase.

Fig. 3 illustrates two-phase buck converter with CMCOT control and current-balance loop [11], [14]. In the current-balance loop, per-phase inductor currents are sensed. The DCR block represents the sensing gain using direct

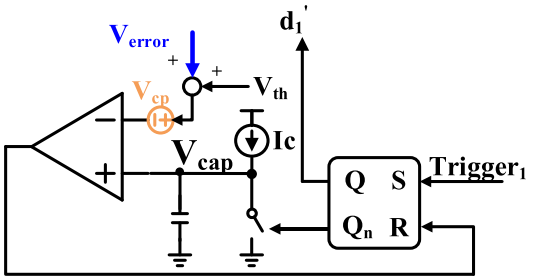

FIGURE 4. Circuit diagram of on-time generator circuit with V_{error} signal.

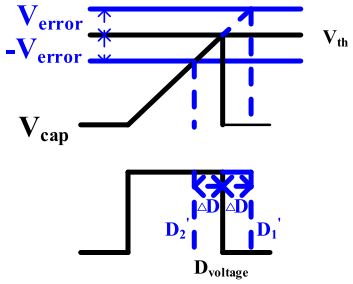

FIGURE 5. Operation waveform of on-time generator circuit in Fig. 4.

current resistance (DCR) sensing method [9]. The total sensing gain is equal to the gain of DCR times M. Then, the two sensed currents S_{iL1} and S_{iL2} are averaged and set as the current reference. The Rc block represents an adjustable gain in the current-balance loop, which can be used to design proper current-balance loop gain. The LPF block represents a low-pass filter to suppress switching ripple.

Current-balance control is achieved by sensing per-phase inductor current and adjusting per-phase on-time. The sensed per-phase inductor current is compared with the current reference and generates an error signal V_{error} to adjust on-time width produced by the on-time generator T_{on1} in Fig. 4. When $Trigger_1$ signal goes high, duty signal d_1' goes high. A constant current Ic charges the capacitor and the voltage of the capacitor V_{cap} increases as shown in Fig. 5. As V_{cap} touches the summation of the threshold voltage V_{th} and V_{error}, the reset signal is triggered and the duty signal will be turned off. V_{cp} represents the offset of the on-time comparator. To avoid the on-time variation due to inductor current ripple, a low-pass filter (LPF) is implemented in current-balance loop to obtain near dc V_{error} signal. When S_{iL1} is larger than the reference current, V_{th} will be subtracted by a negative value. As shown in the operation waveform of Fig. 5, for the phase with larger inductor current, the on-time and duty cycle are smaller than the nominal values to decrease inductor current. At the other phase, the on-time and duty cycle are larger than the nominal values to increase inductor current.

Derivation of DC Inductor Current Distribution:

Dc inductor current distribution equations of two-phase CMCOT buck converter with the current-balance loop are derived below. The derivation is based on continuous conduction mode (CCM) since heavy-load current balance is more important. The derivation process is separated into three steps. Step A analyzes the open-loop converter power stage.

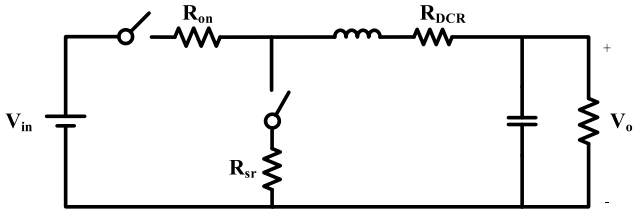

FIGURE 6. Power stage model of a single-phase non-ideal buck converter.

Step B analyzes the converter with the outer loop including the feedback signals of the output voltage and summation current. Step C analyzes the converter with the output voltage and current-balance loop.

A. POWER STAGE

Fig. 6 illustrates the power stage model of a single-phase non-ideal buck converter. The voltage-second balance method is used to derive the relationship between inductor current, the duty cycle D, and parasitic resistances in CCM [9]. On-mode and off-mode inductor voltage equations are derived as (1) and (2), respectively.

$$\text{On-mode: } V_{L,on} = V_{in} - i_L \cdot R_{on} - i_L \cdot R_{DCR} - V_o \quad (1)$$

$$Off - mode : V_{L,off} = -i_L \cdot R_{sr} - i_L \cdot R_{DCR} - V_o \quad (2)$$

According to the inductor volt-second balance, (3) is derived.

$$V_{L,on} \cdot D + V_{L,off} \cdot (1 - D) = 0 \quad (3)$$

Finally, the inductor current i_L can be derived by (1)-(3) as

$$i_L = \frac{\mathrm{D} \cdot V_{in} - V_o}{(1 - \mathrm{D}) \cdot R_{sr} + D \cdot R_{on} + R_{DCR}} \quad (4)$$

This equation shows the relationship between duty cycle and inductor current. This equation will be used later often. For example, if duty cycle is derived, it can be substituted into (4) to obtain inductor current.

B. TWO-PHASE BUCK CONVERTER WITH OUTER LOOP

For a two-phase converter, (4) is applied to obtain (5) and (6), which shows inductor current in phase1 and phase2, respectively. It can be seen that per-phase current is related to per-phase parasitic resistances in the power stage. The summation of these two currents is i_{sum} as shown in (7).

$$i_{L1} = \frac{\mathrm{D}_1 \cdot V_{in} - V_o}{(1 - D_1) \cdot R_{sr1} + D_1 \cdot R_{on1} + R_{DCR1}} \quad (5)$$

$$i_{L2} = \frac{D_2 \cdot V_{in} - V_o}{(1 - D_2) \cdot R_{sr2} + D_2 \cdot R_{on2} + R_{DCR2}} \quad (6)$$

$$i_{sum} = i_{L1} + i_{L2} \quad (7)$$

Combining (5)-(7), the output voltage can be written as

$$V_o = \frac{\left(\frac{\mathrm{D}_1}{\Delta_1} + \frac{\mathrm{D}_2}{\Delta_2}\right) \cdot V_{in} - i_{sum}}{\frac{1}{\Delta_1} + \frac{1}{\Delta_2}} \quad (8)$$

where

$$\Delta_1 = (1 - \mathrm{D}_1) \cdot R_{sr1} + \mathrm{D}_1 \cdot R_{on1} + R_{DCR1},$$
$$\Delta_2 = (1 - \mathrm{D}_2) \cdot R_{sr2} + \mathrm{D}_2 \cdot R_{on2} + R_{DCR2}$$

When the outer loop is added as shown in Fig. 1, two assumptions can be obtained. First, the output voltage is well

regulated to reference voltage V_{ref}. Thus, $V_o = V_{ref}$. Second, the duty cycle in each phase is set to the same value. So $D_{voltage} = D_1 = D_2$. Then, (8) can be rewritten as

$$V_{ref} = \frac{\left(\frac{1}{\Delta_3} + \frac{1}{\Delta_4}\right) \cdot D_{voltage} \cdot V_{in} - i_{sum}}{\frac{1}{\Delta_3} + \frac{1}{\Delta_4}} \tag{9}$$

where,

$$\Delta_3 = \left(1 - D_{voltage}\right) \cdot R_{sr1} + D_{voltage} \cdot R_{on1} + R_{DCR1}$$
$$\Delta_4 = \left(1 - D_{voltage}\right) \cdot R_{sr2} + D_{voltage} \cdot R_{on2} + R_{DCR2}$$

Since input voltage, i_{sum}, and all parasitic resistance values are known, $D_{voltage}$ can be solved. Then, by substituting $D_{voltage}$ into (5) and (6), per-phase inductor current distribution with only voltage regulation loop can be obtained.

C. TWO PHASES BUCK CONVERTER WITH OUTER LOOP AND CURRENT-BALANCE LOOP

After adding the current-balance loop, the per-phase on-time and duty cycle will deviate from its original value $D_{voltage}$ as shown in Figs. 3 to 5. This is the key difference of COT control compared to fixed-frequency control. The duty cycle equations with the current-balance loop can be derived as (10) and (11) from Fig. 4 and Fig. 5. D_1' and D_2' represent the per-phase duty cycle in Fig. 3 when the current-balance loop is implemented. S_{iL1} represents sensed i_{L1}, and S_{iL2} represents sensed i_{L2} in Fig. 3. C is the capacitance of the capacitor in Fig. 4. V_{cp} represents the offset of the on-time comparator.

$$D_1' = D_{voltage} + \frac{C}{K \cdot V_{in}}\left[\frac{(S_{iL2} - S_{iL1})}{2} R_c - V_{cp1}\right] \cdot f_s \tag{10}$$

$$D_2' = D_{voltage} + \frac{C}{K \cdot V_{in}}\left[\frac{(S_{iL1} - S_{iL2})}{2} R_c - V_{cp2}\right] \cdot f_s \tag{11}$$

where

$$S_{iL1} = \left[\frac{D_1' \cdot V_{in} - V_o}{R_{sr1} + R_{DCR1} + D_1'(R_{on1} - R_{sr1})} R_{DCR1} - V_{op1}\right] \cdot M_1$$

$$S_{iL2} = \left[\frac{D_2' \cdot V_{in} - V_o}{R_{sr2} + R_{DCR2} + D_2'(R_{on2} - R_{sr2})} R_{DCR2} - V_{op2}\right] \cdot M_2$$

S_{iL1} and S_{iL2} can be derived from (5) and (6). V_{op1} and V_{op2} represent the offset of the operational amplifier in DCR current sensor.

Finally, the per-phase inductor current distribution i'_{L1} and i'_{L2} with outer loop and current-balance loop are derived as (12) and (13). The dc inductor current after current-balance loop closed can be obtained by substituting (9) and adjusted duty in (10) and (11) into (12) and (13).

$$i'_{L1} = \frac{D_1' \cdot V_{in} - V_o}{\left(1 - D_1'\right) \cdot R_{sr1} + D_1' \cdot R_{on1} + R_{DCR1}} \tag{12}$$

$$i'_{L2} = \frac{D_2' \cdot V_{in} - V_o}{\left(1 - D_2'\right) \cdot R_{sr2} + D_2' \cdot R_{on2} + R_{DCR2}} \tag{13}$$

As can be seen from (12) and (13), the per-phase inductor current is determined by dc duty cycle, which is adjusted by the current-balance loop. The dc inductor current derivation of COT control with the current-balance loop can be extended to a multi-phase converter with any phase number. This is shown in the appendix. Besides, the equations can be used for other COT control schemes such as voltage-mode COT control or ripple-based COT control since the assumption of $V_o = V_{ref}$ is achieved.

TABLE 1. Simulation parameters of Case 1 and Case 2.

Specification	Phase1	Phase2	Unit
Input voltage V_{in}	12		V
Output voltage V_o	1.8		V
Switching frequency f_s	420		kHz
Load current I_{load}	40		A
Inductor value L	0.15		µH
DC resistance of inductor R_{DCR}	450		µΩ
Sensing gain Rc	300		kΩ
Mirror gain M_1	0.1695		mΩ
Comparator offset V_{cp}	3		mV
Opamp offset V_{op}	0.3		mV
Case 1			
Upper MOS resistance R_{on}	8	8	mΩ
Lower MOS resistance R_{sr}	2	2	mΩ
Case 2			
Upper MOS resistance R_{on}	6	4.25	mΩ
Lower MOS resistance R_{sr}	2	1.025	mΩ

TABLE 2. Simulation verification of per-phase inductor currents in Case 1.

	Simulation	Calculation	Error (%)
D_1	15.56%	15.52%	-0.25%
D_2	15.56%	15.52%	-0.25%
I_{L1}	20A	20A	0%
I_{L2}	20A	20A	0%

Simulation Verification of dc Inductor Current Equations: To verify the derived dc per-phase inductor current equations, SIMPLIS circuit simulations are conducted for two-phase CMCOT buck converter with the current-balance loop in Fig. 3. The simulation accuracy of SIMPLIS is widely proved in many power electronics research papers [1]–[6]. Table 1 shows the simulation conditions for two cases. Case 1 has matched per-phase parameters. Case 2 has large mismatched per-phase parasitic resistances. Table 2 compares the simulated per-phase inductor currents with the calculation based on the derived equations. The error is defined as the error percentage of simulation compared to calculation. It proves that per-phase inductor currents are equal if per-phase parameters are matched. Besides, the calculation matches with simulation.

Table 3 verifies the derived equations for mismatched per-phase parasitic resistances case. Compared with the per-phase currents without current-balance loop, the unbalanced

TABLE 3. Simulation verification of per-phase inductor currents in Case 2.

	Simulation	Calculation	Error (%)	w/o balance loop
D_1	15.50%	15.46%	-0.27%	15.40%
D_2	15.33%	15.29%	-0.25%	15.40%
I_{L1}	19.62A	19.58A	-0.22%	15.65A
I_{L2}	20.38A	20.42A	0.21%	24.35A

TABLE 4. Monte Carlo analysis parameters.

Specification	Value	Standard deviation(σ)	Unit
Input voltage V_{in}	12	0%	V
Output voltage V_o	1.8	0%	V
Upper MOS resistance R_{on}	6.8	3.33%	mΩ
Lower MOS resistance R_{sr}	1.375	3.33%	mΩ
DC resistance of inductor R_{DCR}	490	1.2%	uΩ
Sensing gain R_c	468.83	1%	kΩ
Mirror gain M_1	0.1695	0.17%	mΩ

percentage of per-phase current is muchly reduced by ten times when current-balance loop is implemented. It proves the effectiveness of current-balance loop. According to the two cases shown above, it verifies that calculation results fit simulation results with less than 0.3% error. Thus, these equations can be used to predict current distribution when designing the circuit.

Design of Current-Balance Loop Parameters Based on the Derived dc Equations:

Monte Carlo method is used to design sensing gain (R_c) and other parameters to meet per-phase current distribution specification. From the results, it shows how to design the standard deviations of components and current-balance loop parameters to meet the current balance specification, which is important for converter and control IC manufacturers.

An example of a five-phase CMCOT buck converter with 120 A output current is illustrated here. Table 4 gives the parameters and their standard deviations for Monte Carlo analysis. Due to the manufacturing process error, there are standard deviations in parameters including parasitic resistances and control parameters. Excel software is used to randomly generate 1000 sets of parameters with described standard deviation shown in table 4. These parameters are substituted into dc equations derived in the appendix to obtain 5000 per-phase current distributions and are plotted in Fig. 7.

As Fig. 7 shows, when sensing gain Rc is 10kΩ, current distribution among each phase has a larger mismatch and the standard deviation is 324 mA. If Rc is increased by ten times from 10kΩ to 100kΩ, the Monte Carlo results are shown in Fig. 8. It is obvious, when Rc increase, the current distribution is more concentrated. The standard deviation (σ) decreases from 324 mA to 225 mA.

From the Monte Carlo results, it is obvious that the current balance performance becomes better with increased Rc. However, the limitation of the Rc value, which is related to stability and transient performance, is not specified. Due to this reason, the small-signal analysis will be described in the next section.

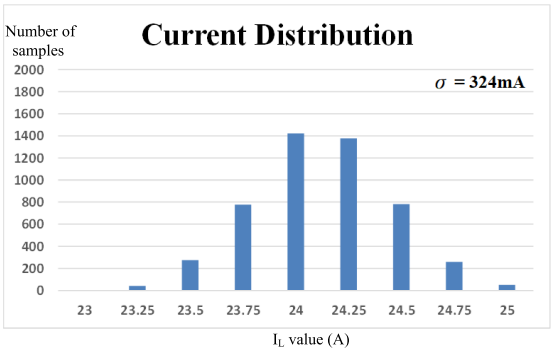

FIGURE 7. Monte Carlo per-phase current distributions when Rc=10kΩ.

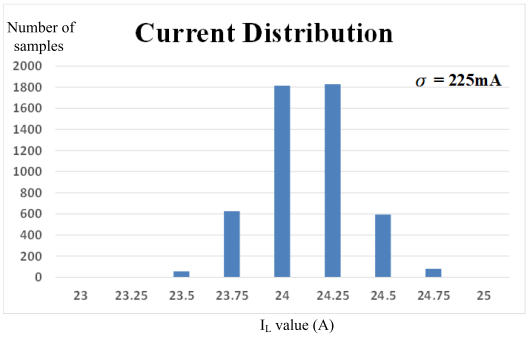

FIGURE 8. Monte Carlo per-phase current distributions when Rc=100kΩ.

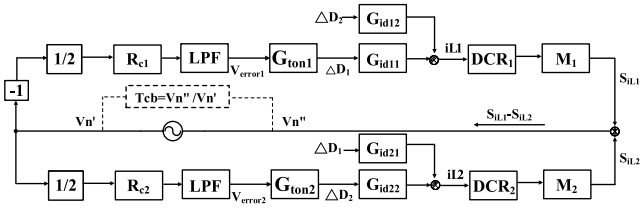

FIGURE 9. Small-signal model of the current-balance loop of CMCOT control shown in Fig. 3.

III. SMALL-SIGNAL MODEL AND DESIGN CONSIDERATION OF CURRENT-BALANCE LOOP

In this section, the small-signal model of the current-balance loop in CMCOT control shown in Fig. 3 will be derived. Except for the steady-state current distribution analysis, the small-signal model of the current-balance loop is another important information to design the current-balance circuit. It can be used to predict system stability and optimize phase number change performance. Finally, the effect of current-balance loop to output voltage response will be illustrated from the complete model including the voltage regulation loop.

A. SMALL-SIGNAL MODEL OF CURRENT-BALANCE LOOP

Fig. 9 illustrates the small-signal model of the current-balance loop of CMCOT control shown in Fig. 3. The model is derived using a similar approach of reference [10]. The current-loop gain can be measured by breaking S_{iL1}-S_{iL2} path. DCR_1 and DCR_2 are the DCR current sensing gain in two phases, respectively. M_1 and M_2 are current mirror gain in two

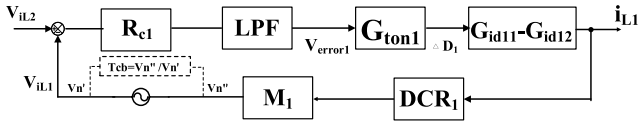

FIGURE 10. Simplified small-signal model of current-balance loop in Fig. 9.

phases, respectively. R_{c1} and R_{c2} are the adjustable sensing gain of the current-balance loop in two phases, respectively. LPF represents a low pass filter gain. G_{ton1} and G_{ton2} represent the transfer functions of the on-time generator from error voltage, V_{error}, to duty cycle in two phases, respectively. It can be derived from Figs. 4 and 5, where the derivation is shown in the appendix. G_{id} represents the transfer function from the duty cycle to the inductor current and is derived in [10]. The model in Fig. 9 is comparable with Fig. 3. For example, The input of R_{c1} block equals -(S_{iL1}-S_{iL2})/2. V_{error1} is the input of on-time generator gain G_{ton1}, which generates duty cycle perturbation ΔD_1 and affects inductor currents.

The model in Fig. 9 can be simplified to Fig. 10 assuming the parameters are matched or with little difference between phases. If there is a disturbance on current-balance loop, the perturbation in different phases has the same amount but with different signs. Due to this reason, the perturbation in different phase will perfectly be canceled at the output voltage. Therefore, the current-balance loop can be decoupled with the outer loop, and the model in Fig. 9 can be simplified to Fig. 10 [10].

The current-balance loop gain is defined as $T_{cb} = V_n/V_n'$, which breaks the path of $S_{iL1} - S_{iL2}$. Thus, current-balance loop gain T_{cb} can be expressed as

$$T_{cb} = G_{ton1}\cdot(G_{id11} - G_{id12}) \cdot DCR_1 \cdot M_1 \cdot R_c \cdot LPF \quad (14)$$

Moreover, T_{cb} can be derived by substituting transfer function of each block in Fig. 10 into (14) as

$$T_{cb} = A \cdot \frac{1}{1+\frac{s}{w_{pole1}}} \cdot \frac{1}{1+\frac{s}{w_{pole2}}} \quad (15)$$

where

$$A = \frac{R_{c1}M_1R_{DCR1}}{V_{in}} \cdot \frac{V_{in} - I_o(R_{on1} - R_{sr1})}{D\cdot(R_{on1} - R_{sr1}) + (R_{sr1} + R_{DCR1})}$$

$$f_{pole1} = \frac{D_1\,(R_{on1} - R_{sr1}) + (R_{sr1} + R_{DCR1})}{2\pi L}$$

$$f_{pole2} = \frac{1}{2\pi R_{LPF} C_{LPF}}$$

I_o is the load current. From (15), it can be seen that dc current-balance loop gain is related to sensing gains such as R_{c1} and M_1 and parasitic resistances. There are two poles in the loop gain. One is determined by power stage parameter and the other is determined by the low-pass filter in LPF block. Therefore, the design of current-balance loop must be careful to avoid possible stability issue due to insufficient phase margin.

To verify the derived current-balance loop gain, SIMPLIS simulation is used and the simulation parameters are shown in Table 5. Fig. 11 shows the comparison of calculation and simulation of current-balance loop gain T_{cb} when Rc=400kΩ. The locations of the two pole frequencies are also shown. It can be seen that the calculation result fits simulation up to one-fifth of switching frequency. The model discrepancy near the switching frequency range is due to the sideband effect [21]. If Rc increases, T_{cb} will increase, too. It means that the balance effect becomes more obvious, but the phase margin (PM) decreases. Fig. 12 shows the bode plot of T_{cb} when R_c=8MegΩ. It can be seen that low-frequency gain of T_{cb} becomes higher, but the phase margin is only 11 degrees. If Rc gets even larger, the system will become unstable when PM < 0°.

Figs. 13 and 14 show the phase number change transient response waveforms of the converter in Fig. 3 with different Rc values. Before 100us, only phase1 of the converter is working and the output current is 40 A. At 100us, phase2 and current-balance loop turn-on simultaneously. It can be observed from Figs. 13 and 14 that the control scheme without a current-balance loop has the slowest per-phase current transient response. The control scheme with current- balance loop PM=30 degree (Rc=6000kΩ) case exhibits an overshoot in phase2 inductor current, which may falsely trigger the per-phase current protection implemented in the controller.

TABLE 5. Simulation parameters for section III.

Specification	Value	Unit
Input voltage V_{in}	12	V
Output voltage V_o	1.8	V
Upper MOS resistance R_{on}	4.5	mΩ
Lower MOS resistance R_{sr}	1.2	mΩ
Inductor value L	0.15	μH
DC resistance of inductor R_{DCR}	490	μΩ
Mirror gain M_1	0.1695	mΩ
Sensing gain R_c	400	kΩ
Low pass filter resistance R_{LPF}	1	MegΩ
Low pass filter capacitance C_{LPF1}	3.94	pF

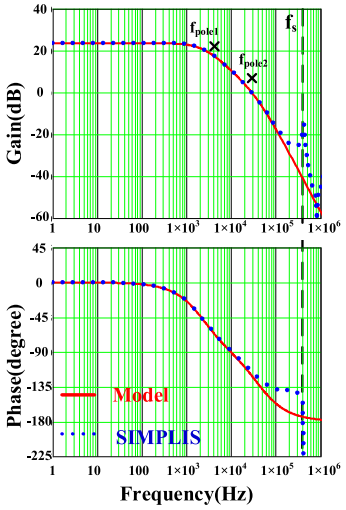

FIGURE 11. Bode plot of current-balance loop gain with Rc=400 kΩ.

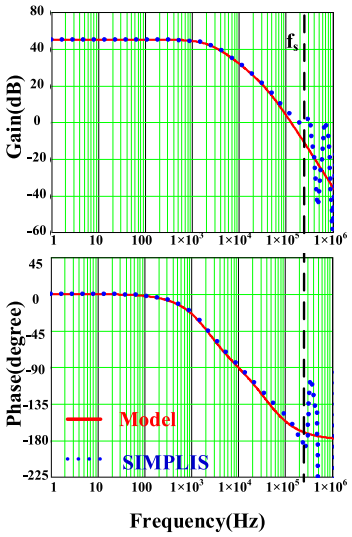

FIGURE 12. Bode plot of current-balance loop gain with Rc=8000 kΩ.

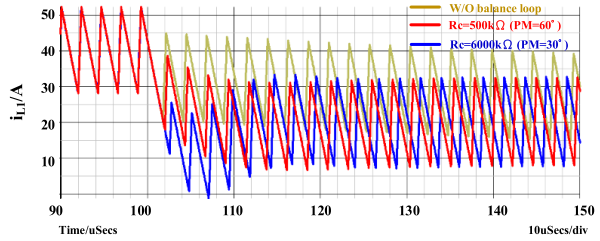

FIGURE 13. Phase1 inductor current waveforms with different Rc value at phase number change transient.

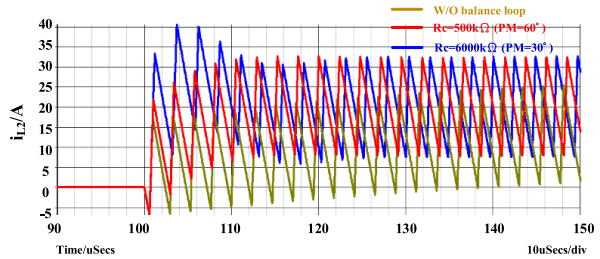

FIGURE 14. Phase2 inductor current waveforms with different Rc value at phase number change transient.

B. COMPLETE SMALL-SIGNAL MODEL AND OUTPUT VOLTAGE RESPONSE

The decoupling between the current-balance loop and the outer loop is important. It will be shown that the balance loop is independent of the outer loop if switching ripple component is well filtered by the current-balance loop. That is, the gain of T_{cb} at switching frequency is much below unity.

Fig. 15 shows the complete small-signal model of CMCOT control with current-balance loop and outer loop as shown in Fig. 3. Various transfer functions such as $i_{L1}(s)/v_c(s)$ and $i_{L2}(s)/v_c(s)$ are the same as those derived in CMCOT control using describing function method [1], [2], [22]. Zo(s) is the network transfer function consisted of the output capacitor and load resistor. The transfer function $k_2(s)$ models the effect of output voltage perturbation effect on average summation

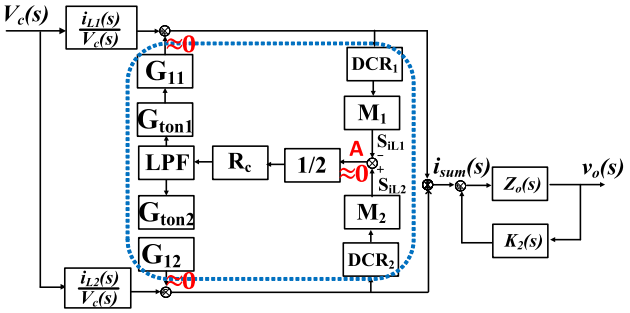

FIGURE 15. Complete small-signal model of CMCOT control with current-balance loop.

inductor current. The blocks within the blue dash in Fig. 15 represents the current balance circuit. Assuming the parameters of two phases are matched. When there is a disturbance on $V_c(s)$ such as load transient happens, the perturbation on $i_{L1}(s)$ and $i_{L2}(s)$ are the same. Therefore, the two signal S_{iL1} and S_{iL2} will cancel at point A. That is, the perturbation will not go into the current-balance loop, and the outer loop is independent of current-balance loop at load transient.

Therefore, the control-to-output transfer function G_{vc} of CMCOT control with current-balance loop is the same as its counterpart for CMCOT control without balance loop. (16)-(18) shows the transfer functions of Fig. 15, where G_{vc} is the same as the reported transfer functions of CMCOT control without balance loop [1], [2], [22]. S_f is the falling slope of sensed inductor current.

$$G_{vc}(s) = \frac{v_{out}(s)}{V_c(s)} = \frac{f_s}{s_f}(1 - e^{-sT_{on}})\frac{V_{in}}{sL} \cdot \frac{Zo(s)}{1 - Zo(s) \cdot K_2(s)} \tag{16}$$

$$Zo\,(s) = R_L//(R_c + \frac{1}{sC}) \tag{17}$$

$$K_2(s) = \frac{i_{sum}(s)}{v_{out}(s)}\bigg|_{V_c(s)=0} = \frac{2T_{on}}{2L} \tag{18}$$

Fig. 16 verifies the derived G_{vc} transfer function of Fig. 15 by simulations. The bode plot results with different sensing gain are matches with the model. It can be seen that control-to-output transfer function does not affect by different Rc values in current-balance loop or removing current-balance loop ($R_c = 0$ case). Moreover, two simulation waveforms are shown in Figs. 17 and 18 for load transition response from 40A to 160A. The load transient response of output voltage and inductor currents does not affect by balance loop gain.

However, G_{vc} is affected by the balance loop gain if the gain of T_{cb} at switching frequency is not much below unity. Fig. 19 shows the Bode plot of G_{vc} with excessive R_c. Since T_{cb} has around unity gain at switching frequency for $R_c = 8\text{MegΩ}$ Case as shown in Fig. 12, the simulated G_{vc} shows deviation from the model. Fig. 20 shows the simulated output voltage load transient waveforms with excessive R_c. It can be seen that the outer voltage transient response shows oscillation which is affected by current-balance loop when Rc is increased to 8 MΩ. Thus, there is a limitation on

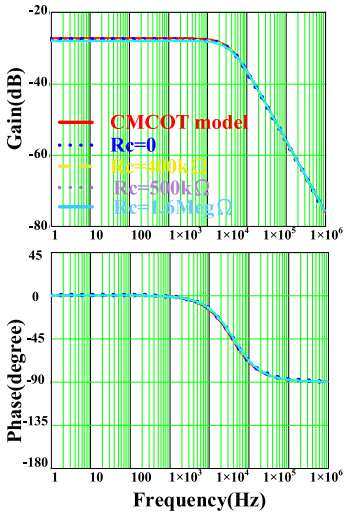

FIGURE 16. Simulation verification of G_{vc} of Fig. 15 with different sensing gain (R_c) in current-balance loop.

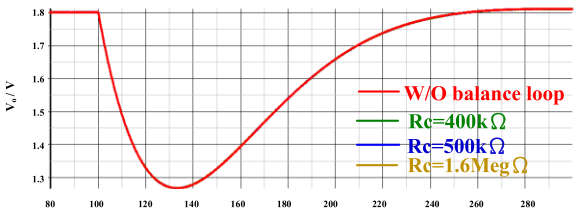

FIGURE 17. Simulated output voltage waveform at load transient with different Rc.

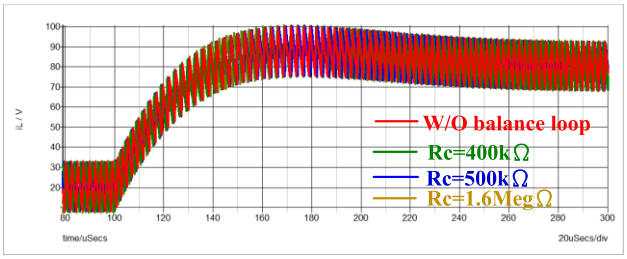

FIGURE 18. Simulated per-phase inductor current waveform at load transient with different Rc.

maximum Rc increasing to obtain better dc current balance without suffering the coupling effect between the outer loop and balance loop.

C. VERIFICATION OF SIMPLIFIED CURRENT-BALANCE LOOP MODEL AT MISMATCH CONDITIONS

The current-balance loop model in Fig. 10 is simplified based on the assumption of a matched condition; however, it will be shown that this model is still valid in the practical condition where phase mismatch happens. Fig. 10 is simplified from Fig. 9. As shown in Fig, 21, by defining loop gain around phase one as Loop A and loop gain around phase two as Loop B, Tcb can be expressed as (Loop A + Loop B).

For the matched case, Loop A = Loop B. Thus, Tcb=2* Loop A. For the mismatched cases, Tcb=loop A *(1+x%) + loop A *(1-x%) =$\text{Tcb}_{(\text{balance})}$. Thus, the simplified current-balance loop can be used in mismatched cases.

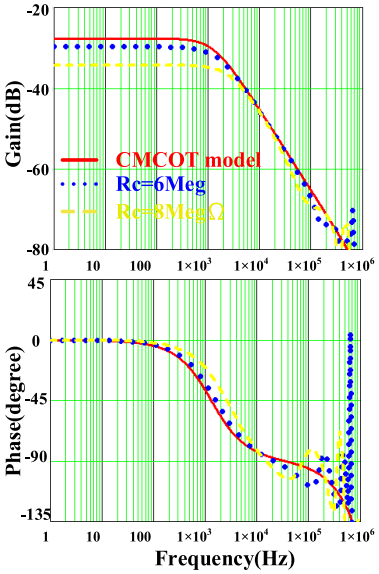

FIGURE 19. Simulation verification of G_{vc} with excessive sensing gains (Rc).

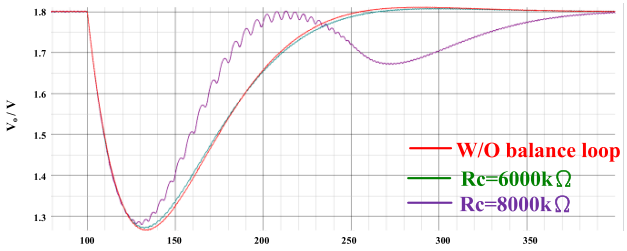

FIGURE 20. Simulated output voltage load transient waveforms with excessive sensing gain (Rc).

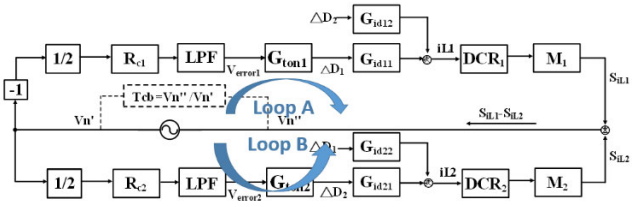

FIGURE 21. Small-signal model of the current-balance loop in Fig. 9 indicating two loops.

SIMPLIS simulations are used to verify the analysis with mismatched cases. The simulation parameters are based on Table 5. Fig. 22 shows the Bode plot of current-balance loop gain with mismatched inductance value where the inductance in phase one and phase two are 0.15*1.035 μH and 0.15*0.965 μH, respectively. Fig. 23 shows the Bode plot of current-balance loop gain with mismatched DCR value where the DCR in phase one and phase two are 490*1.05 $\mu\Omega$ and 490*0.95 $\mu\Omega$, respectively. It can be seen that the simulated loop gains with per-phase L or DCR mismatch fit with the model and also matched cases.

D. DESIGN GUIDELINE FOR CURRENT-BALANCE LOOP

Based on the analysis in section II and III, it is suggested to increase the designed dc gain of the current-balance loop

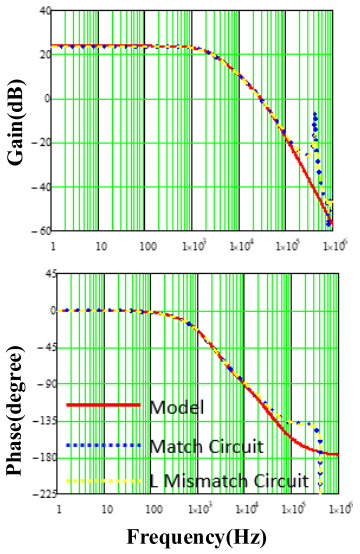

FIGURE 22. Bode plot of current-balance loop gain with mismatched inductance value.

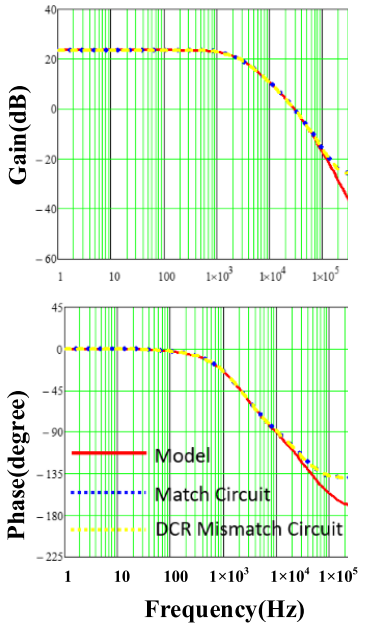

FIGURE 23. Bode plot of current-balance loop gain with mismatched DCR value.

gain T_{cb} until its phase margin reduced to around 60 degrees. The higher dc gain refers to better dc inductor current balance. The 60-degrees phase margin design is not only to ensure the stability of balance-loop, but also to achieve proper per-phase current transient response without overshoot after phase number change.

Besides, the gain of T_{cb} at switching frequency shall be designed much below unity. Then, the design of outer loop can be decoupled from current-balance loop. Besides, the load transient response will not be affected by current-balance loop.

IV. SIMULATION AND EXPERIMENTAL RESULTS

An experimental platform for the two-phase CMCOT buck converter with current-balance loop is built as shown in Fig. 24. The control circuit is built with discrete components; therefore, the switching frequency is reduced to 120 kHz to reduce discrete components delay effect to the control. The test parameters and working conditions for the experiments are listed in Tables 6.

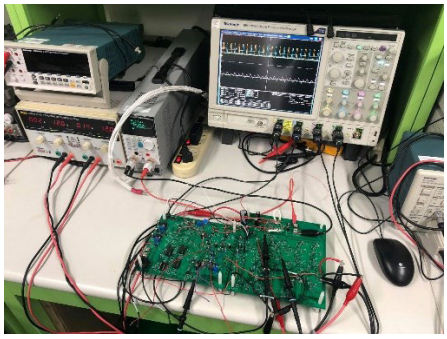

FIGURE 24. Experimental platform for the two-phase buck converter.

TABLE 6. Experiment parameters and working condition.

Specification	Phase1 parameter	Phase2 parameter	Unit
Input voltage V_{in}	12		V
Output voltage V_o	1		V
Switching frequency f_s	120		kHz
Load current I_{load}	6		A
Upper MOS resistance R_{on}	8.3		mΩ
Lower MOS resistance R_{sr}	2.3		mΩ
Inductor value	0.36		μH
DC resistance of inductor R_{DCR}	20.8	10.8	mΩ
R_{DCR} multiply M_1	200		mV/A
Low pass filter resistance R_{LPF}	14.3		kΩ
Low pass filter capacitance C_{LPF}	6.8		nF

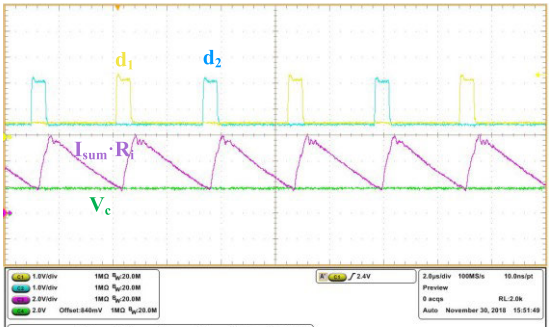

FIGURE 25. Measured modulation waveform of CMCOT control.

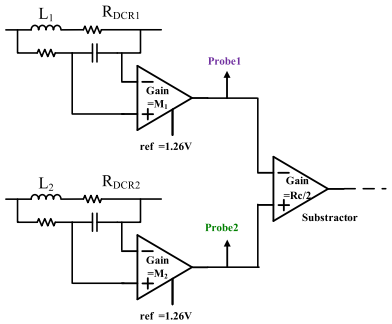

FIGURE 26. Measurement circuit for dc current distribution.

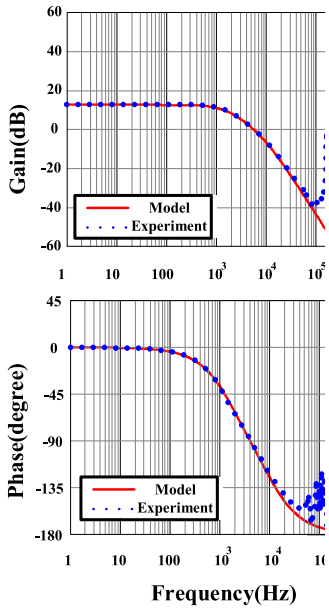

FIGURE 27. Experimental T_{cb} verification of CMCOT control with Rc=2/3.

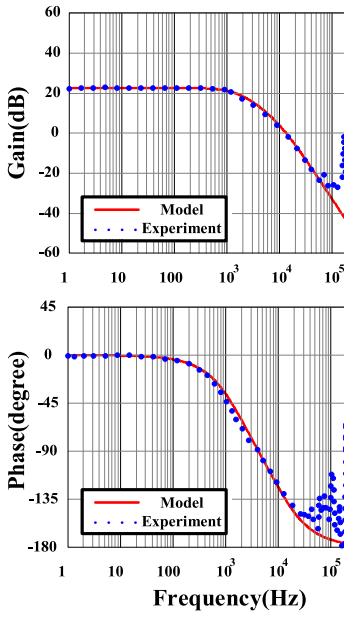

FIGURE 28. Experimental T_{cb} verification of CMCOT control with Rc=2.

Fig. 25 shows the measured modulation waveform of CMCOT control scheme. It matches the description in Fig. 2, where two-phase duty cycles are triggered in a rotation manner when sensed summation current signal touches control signal V_c. Fig. 26 shows the measurement circuit for dc inductor current distribution. Probe1 and Probe2 are the measurement point of the two phases, respectively. Two instrumental amplifiers and DCR current sensing method are used to sense per-phase inductor current. The gain of M_1 and R_{c1} can refer to the gain of amplifiers. Since they are implemented using discrete components. The gain of M_1 and R_{c1} are at different scale compared to simulation results, which is based on integrated circuit parameters. The output of substractor is the point to break when measuring current-loop gain T_{cb}.

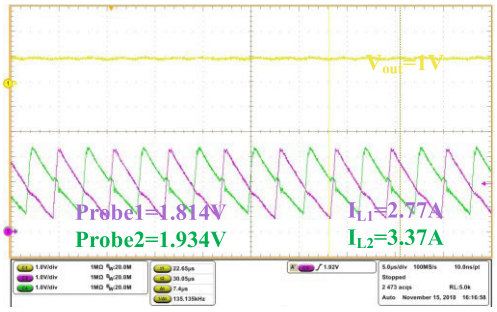

FIGURE 29. Measured steady state inductor current distribution without current-balance loop.

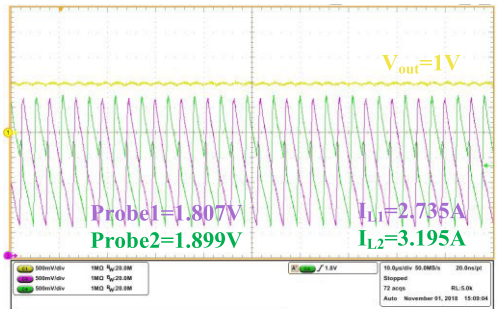

FIGURE 30. Measured steady state inductor current distribution with Rc=2/3.

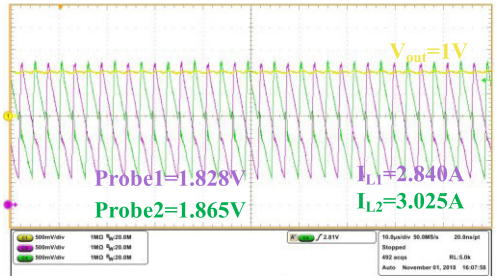

FIGURE 31. Measured steady state inductor current distribution with Rc=2.

Figs. 27 and 28 verify the model of current-balance gain T_{cb} of CMCOT control with various Rc values. The frequency response is measured using the Bode 100 network analyzer. It indicates that the results of the proposed small-signal model are in excellent agreement with the measurements within one-fifth of switching frequency. The measured gain and phase near switching frequency also agrees with simulation results, where the side-band effect is revealed.

Fig. 29 shows the measured steady-state inductor currents for CMCOT control without current-balance loop. The purple and green waveform represents the sensed voltage of Probe1 and Probe2, respectively, in Fig. 26. Using the dc values of these two waveforms, the dc inductor currents can be calculated as shown in Fig. 29. It can be seen that I_{L1} and I_{L2} have 0.6 A difference. Figs. 30 and 31 show the measured results of CMCOT control with current-balance loop but different Rc value. The difference between I_{L1} and I_{L2} is 0.46 A for Rc=2/3, and 0.19 A for Rc=2, respectively. It is shown that current-balance loop reduces current mismatches

between phases. When Rc is larger, inductor currents tend to be more balanced.

V. CONCLUSIONS

In the paper, a comprehensive analysis and design is proposed for current-balance loop in constant on-time controlled multi-phase buck converter. The steady-state current distribution equations are firstly derived. Monte Carlo analysis based on the proposed equations is then conducted to predict current distribution. It is shown that larger sensing gain Rc in current-balance loop achieves more balanced inductor current distribution. The small-signal model of the current-balance loop is proposed. These analysis results provide current-balance loop gain T_{cb} design guideline to achieve required dc current balance performance, stability, transient response, and decoupled design between voltage loop and current-balance loop. Experiment and simulation verify the analysis.

APPENDIX

A. EXTEND DC CURRENT BALANCE ANALYSIS OF COT CONTROL WITH CURRENT-BALANCE LOOP FOR N-PHASE CONVERTERS

The dc per-phase inductor current derivation in section II can be extend to the converters with any number of phases. The derivation follows the same steps in section II. Assume the converter has n phases. First, (5) and (6) are extended to (19) to (21). (7) is rewrite as (22).

$$i_{L1} = \frac{\mathrm{D}_1 \cdot V_{in} - V_o}{(1-D_1)\cdot R_{sr1} + D_1 \cdot R_{on1} + R_{DCR1}} \tag{19}$$

$$i_{L2} = \frac{D_2 \cdot V_{in} - V_o}{(1-D_2)\cdot R_{sr2} + D_2 \cdot R_{on2} + R_{DCR2}} \tag{20}$$

$$\vdots$$

$$i_{Ln} = \frac{D_n \cdot V_{in} - V_o}{(1-D_n)\cdot R_{srn} + D_n \cdot R_{onn} + R_{DCRn}} \tag{21}$$

$$i_{sum} = i_{L1} + i_{L2} + \cdots + i_{Ln} \tag{22}$$

The output voltage can be written as (23) by extending (8) to n phases.

$$V_o = \frac{\left(\frac{\mathrm{D}_1}{\Delta_{11}} + \frac{\mathrm{D}_2}{\Delta_{21}} + \ldots + \frac{\mathrm{D}_n}{\Delta_{n1}}\right)\cdot V_{in} - i_{sum}}{\frac{1}{\Delta_{11}} + \frac{1}{\Delta_{21}} + \ldots + \frac{1}{\Delta_{n1}}} \tag{23}$$

where

$$\begin{aligned}
\Delta_{11} &= (1-\mathrm{D}_1)\cdot R_{sr1} + \mathrm{D}_1 \cdot R_{on1} + R_{DCR1},\\
\Delta_{21} &= (1-\mathrm{D}_2)\cdot R_{sr2} + \mathrm{D}_2 \cdot R_{on2} + R_{DCR2}\\
&\vdots\\
\Delta_{n1} &= (1-\mathrm{D}_n)\cdot R_{srn} + \mathrm{D}_n \cdot R_{onn} + R_{DCRn}
\end{aligned}$$

When the outer loop is closed, it can be assumed that $V_o = V_{ref}$ and $D_{voltage} = D_1 = D_2 = \ldots = D_n$. So (23) is rewritten as (24) to obtain reference voltage $\mathrm{V_{ref}}$.

$$V_{ref} = \frac{\left(\frac{1}{\Delta_{12}} + \frac{1}{\Delta_{22}} + \ldots + \frac{1}{\Delta_{n2}}\right)\cdot D_{voltage}\cdot V_{in} - i_{sum}}{\frac{1}{\Delta_{12}} + \frac{1}{\Delta_{22}} + \ldots + \frac{1}{\Delta_{n2}}} \tag{24}$$

where,

$$\begin{aligned}
\Delta_{12} &= \left(1-\mathrm{D_{voltage}}\right)\cdot R_{sr1} + \mathrm{D_{voltage}}\cdot R_{on1} + R_{DCR1},\\
\Delta_{22} &= \left(1-\mathrm{D_{voltage}}\right)\cdot R_{sr2} + \mathrm{D_{voltage}}\cdot R_{on2} + R_{DCR2}\\
&\vdots\\
\Delta_{n2} &= (1-\mathrm{D}_n)\cdot R_{srn} + \mathrm{D_{voltage}}\cdot R_{onn} + R_{DCRn}
\end{aligned}$$

After adding the current-balance loop, the per-phase duty cycles is deviated from $\mathrm{D_{voltage}}$ and is represented below using the same procedure when deriving (10) and (11).

$$\begin{aligned}
D_1' &= D_{voltage} + \frac{C}{K\cdot V_{in}}\\
&\quad\times\left[\left(\frac{S_{iL1}+S_{iL2}+\ldots+S_{iLn}}{n} - S_{iL1}\right)R_c - V_{cp1}\right]\cdot f_s\\
D_2' &= D_{voltage} + \frac{C}{K\cdot V_{in}}\\
&\quad\times\left[\left(\frac{S_{iL1}+S_{iL2}+\ldots+S_{iLn}}{n} - S_{iL2}\right)R_c - V_{cp2}\right]\cdot f_s\\
&\vdots\\
D_n' &= D_{voltage} + \frac{C}{K\cdot V_{in}}\\
&\quad\times\left[\left(\frac{S_{iL1}+S_{iL2}+\ldots+S_{iLn}}{n} - S_{iLn}\right)R_c - V_{cpn}\right]\cdot f_s
\end{aligned} \tag{25}$$

where

$$\begin{aligned}
S_{iL1} &= \left[\frac{D_1'\cdot V_{in} - V_o}{R_{sr1} + R_{DCR1} + D_1'(R_{on1} - R_{sr1})}R_{DCR1} - V_{op1}\right]\cdot M_1\\
S_{iL2} &= \left[\frac{D_2'\cdot V_{in} - V_o}{R_{sr2} + R_{DCR2} + D_2'(R_{on2} - R_{sr2})}R_{DCR2} - V_{op2}\right]\cdot M_2\\
&\vdots\\
S_{iLn} &= \left[\frac{D_n'\cdot V_{in} - V_o}{R_{srn} + R_{DCRn} + D_n'(R_{onn} - R_{srn})}R_{DCRn} - V_{opn}\right]\cdot M_n
\end{aligned}$$

Finally, the derived dc per-phase inductor currents of COT control with current-balance loop is written as (26) to (28) and can be solved by substituting (25) into below equations.

$$i_{L1}' = \frac{D_1'\cdot V_{in} - V_o}{\left(1-D_1'\right)\cdot R_{sr1} + D_1'\cdot R_{on1} + R_{DCR1}} \tag{26}$$

$$i_{L2}' = \frac{D_2'\cdot V_{in} - V_o}{\left(1-D_2'\right)\cdot R_{sr2} + D_2'\cdot R_{on2} + R_{DCR2}} \tag{27}$$

$$\vdots$$

$$i_{Ln}' = \frac{D_n'\cdot V_{in} - V_o}{\left(1-D_n'\right)\cdot R_{srn} + D_n'\cdot R_{onn} + R_{DCRn}} \tag{28}$$

B. DERIVATION OF ON-TIME GENERATOR TRANSFER FUNCTIONS G_{ton}

$\mathrm{G_{ton1}}$ and $\mathrm{G_{ton2}}$ in Fig. 9 represent the transfer functions of the on-time generator from the error voltage, $\mathrm{V_{error}}$, to duty cycle in two phases, respectively. It can be derived from Figs. 4 and 5. Based on the current and voltage relation of

the capacitor, C, in the on-time generator in Fig. 4, (29) and (30) are derived as below.

$$C \cdot \hat{V}\text{error} = Ic \cdot \hat{T}on = Ic \cdot \hat{d}/f_s \tag{29}$$

$$C \cdot V_{TH} = Ic \cdot Ton = Ic \cdot D/f_s \tag{30}$$

where (29) shows the relation between perturbed error voltage, $\hat{V}$error, and perturbed duty cycle, $\hat{d}$.

Assume the adaptive on-time generator is implemented to reduce switching frequency variation due to the variation of input and output voltages. Then (31) and (32) are obtained.

$$V_{TH} = V_o \tag{31}$$

$$Ic = k \cdot V_{in} \tag{32}$$

By assuming $D = V_o/V_{in}$, (33) can be obtained as below by combining (30) to (32).

$$f_s = k/C \tag{33}$$

Finally, G_{ton} can be derived as (34) by substitute (33) into (29).

$$G_{ton} \triangleq \frac{\hat{d}}{\hat{V}\text{error}} = \frac{1}{V_{in}} \tag{34}$$

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