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Device Design Guideline of 5-nm-Node FinFETs and Nanosheet FETs for Analog/RF Applications

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ABSTRACT Analog/RF performances of 5-nm node bulk fin-shaped field-effect transistors (FinFETs) and nanosheet FETs (NSFETs) were investigated and compared thoroughly using fully-calibrated TCAD. NSFETs have greater current drivability and gate-to-channel controllability than FinFETs under the same footprint, thus achieving larger intrinsic gain. But the cutoff frequencies (F_t) of FinFETs and NSFETs are comparable due to larger gate capacitances (C_{gg}) of NSFETs compensating DC performance improvements. Gate resistances (R_g) of NSFETs are larger because of their metal gate (MG) configuration surrounding the channels, longer MG height by the top-most NS spacing region, and the bottom transistor, thus degrading maximum oscillation frequency (F_{max}). Device design guidelines of FinFETs and NSFETs are also studied for better intrinsic gain, F_t, and F_{max}. Intrinsic gain is improved by better electrostatics, whereas F_t increases by greater current drivability over C_{gg}. For larger F_{max}, careful device design is required to compensate between R_g, C_{gg}, output resistance, and F_t. Overall, NSFETs outperform FinFETs in terms of intrinsic gain, F_t, and F_{max}, thus NSFETs are promising for analog/RF applications.

INDEX TERMS 5-nm node, FinFETs, NSFETs, nanosheet, intrinsic gain, cutoff frequency, maximum oscillation frequency, analog, RF, gate resistance.

I. INTRODUCTION

Si fin-shaped field-effect transistors (FinFETs) have been scaled down to 10-nm node through higher aspect ratio and layout optimization [1]. FinFETs started to substitute planar MOSFETs through design-technology co-optimization in terms of performance, power, and area for system-on-chip applications [2]. However, there are several technical concerns to be considered for further scaling. Thinner fin is required to maintain good electrostatics, but instead degrades carrier mobility and induces larger threshold voltage (V_{th}) variation [3]–[5]. Fin depopulation lowers layout design flexibility by quantizing the drive current [3].

Meanwhile, Si nanosheet FETs (NSFETs) have been introduced to increase the channel effective widths (W_{eff}) for greater current drivability under the same footprint while maintaining superior electrostatics through gate-all-around (GAA) structure [6]. In addition, NSFETs can adjust the drain currents (I_{ds}) by changing the NS width (W_{NS}), which enables CMOS-compatible layout design [3], [7], [8].

Currently, FinFETs have substituted planar MOSFETs for analog/RF applications due to better electrostatics achieving high intrinsic gain (G_mR_o) and volume inversion lowering 1/f noise [9]–[11]. But large gate resistance (R_g) from complex fin array structure and parasitic capacitance (C_{para}) limits the performance boosts of cutoff frequency (F_t) and maximum oscillation frequency (F_{max}) in the following technology node [12], [13]. Analog/RF performances of NSFETs have been investigated in terms of NS channel thickness (T_{NS}) and W_{NS} for better analog/RF figure-of-merits (FoM) (G_mR_o, F_t, F_{max}) [14]. But there are no qualitative analyses of analog/RF FoM and no explanations comparing to FinFETs.

Thus, the analog/RF performances of FinFETs and NSFETs were investigated thoroughly using fully-calibrated TCAD. After structural analyses of FinFETs and NSFETs, device design guidelines for best analog/RF FoM were presented. Also, the small-signal equivalent circuits of FinFETs and NSFETs, validated by matching all the Y parameters,

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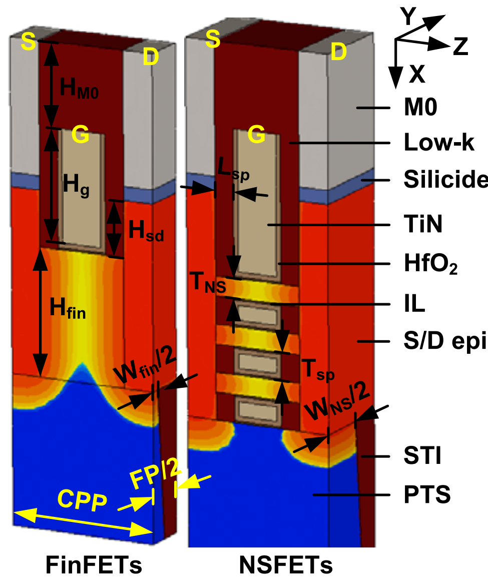

FIGURE 1. 3-D schematic diagrams of bulk FinFETs and NSFETs. Geometrical parameters and materials are specified.

TABLE 1. Geometrical Parameters of The Bulk FinFETs and NSFETs. Reference Values are underlined.

Geometrical Parameters		Values (nm) FinFET	NSFET
CPP	Contacted poly pitch	54	
FP	Fin pitch	34	
NP	NS pitch		W_{NS} + 28
L_g	Gate length	18	
L_{sp}	Spacer length	7	
H_g	Gate height	40	
H_{M0}	M0 height	30	
H_{sd}	S/D height	20	
W_{fin}	Fin width	5, 6, <u>7</u>, 8, 9	
H_{fin}	Fin height	38, 42, <u>46</u>, 50, 54	
T_{NS}	NS thickness		5, 6, <u>7</u>, 8, 9
T_{sp}	NS spacing thickness		8, <u>10</u>, 12, 14, 16
W_{NS}	NS width		7, 10, 20, 30, <u>40</u>, 50
N_{NS}	The number of NS channels		1, 2, <u>3</u>, 4, 5

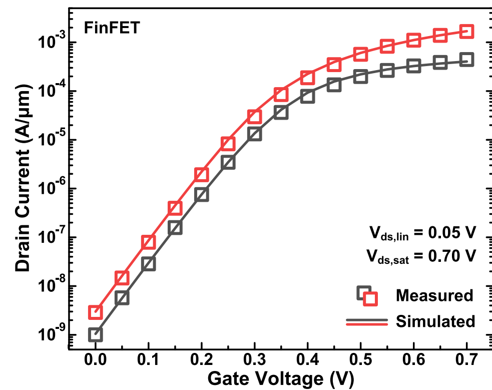

FIGURE 2. Bulk FinFETs calibrated to Intel [1].

were analyzed and provided for the further study of non-linear and noise equivalent circuit models.

II. DEVICE STRUCTURE AND SIMULATION METHOD

All the bulk FinFETs and NSFETs were simulated using Sentaurus TCAD [15]. Drift-diffusion transport model was self-consistently calculated along with Poisson and carrier continuity equations. Density-gradient model was used to consider the quantum confinement effects within the channels. Slotboom bandgap narrowing model was used for the doping-dependent bandgap changes. Quasi-ballistic effect was considered by including low-field ballistic model. Mobility and generation-recombination models, and stress-induced modifications of bandgap, effective mass, and mobility were equivalent as in [16], [17].

Fig. 1 shows the 3-D schematic diagrams of FinFETs and NSFETs. Geometrical parameters and materials are specified, and their values are given in Table 1. NS pitch (NP) is equivalent to two times of fin pitch (FP) as the W_{NS} is 40 nm, which is the reference value in this work. Their process flows are equivalent to [16], [17]. Source/drain (S/D) height (H_{sd}), gate height (H_g), and M0 height (H_{M0}) are referred from several TEM images [7], [11]. All the devices have the S/D doping of 2×10^{20} cm^{-3} and the punch through stopper (PTS) doping of 2×10^{18} cm^{-3} to minimize the leakage currents flowing below the gate. Contact resistivity at the S/D epi/silicide interface is fixed to $1 \times 10^{-9} \Omega \cdot$ cm^2.

As shown in Fig. 2, TCAD parameters were calibrated by fitting the I_{ds} of the 10-nm node FinFETs [1]. Subthreshold swing and drain-induced barrier lowering were fitted first by changing S/D doping profiles. Then, Monte Carlo simulation was performed to fit ballistic coefficient and saturation velocity. Finally, mobility parameters related to surface roughness scattering were tuned to fit the I_{ds} in the linear region. Equivalent oxide thickness is 1.0 nm, consisting of SiO_2 (0.7 nm) and HfO_2 (1.7 nm). Metal gate resistivity (ρ_{MG}) is 2000 $\Omega \cdot \mu$m, which is the same as TiAl, n-type workfunction metal [18], [19], and low-k dielectric constant is 9.0. Operation voltage (V_{DD}) is fixed to 0.7 V.

III. RESULTS AND DISCUSSION

Fig. 3 shows the analog/RF performances between FinFETs and NSFETs. Equivalent circuit parameters between FinFETs and NSFETs are analyzed in appendix. Intrinsic gain is obtained by multiplying transconductance (G_m) with output resistance (R_o), whereas F_t and F_{max} are extracted at the frequency where the current gain ($|h_{21}|$) and the power gain (MUG) curves are unity through the linear extrapolation at 10 GHz. NSFETs have lerger $G_m R_o$ than FinFETs because NSFETs have better electrostatics and larger W_{eff} than FinFETs under the same footprint. There is a cross-over of $G_m R_o$ between NSFETs and FinFETs at small I_{ds} near 10^{-7} A/μm because NSFETs have larger dopant penetration into the channel, which decreases the R_o. Larger dopant penetration is induced by Ge intermixing which assists more phosphorus dopants diffusing into the channels [20]–[22]. On the other

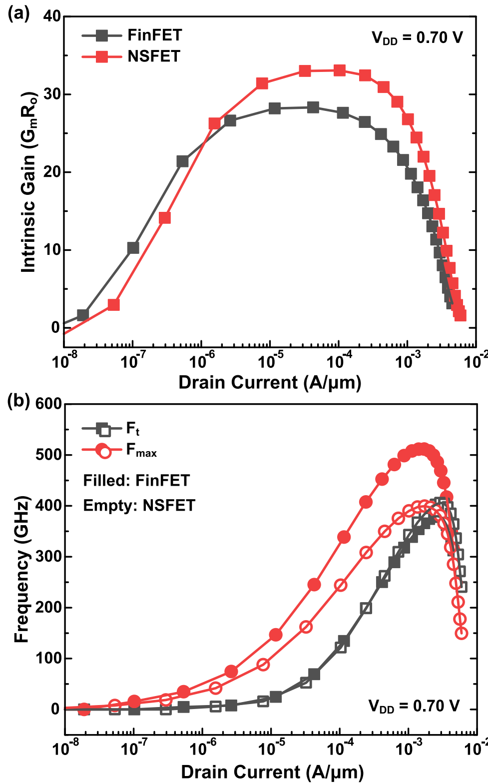

FIGURE 3. (a) G_mR_o, (b) F_t, F_{max} of FinFETs and NSFETs.

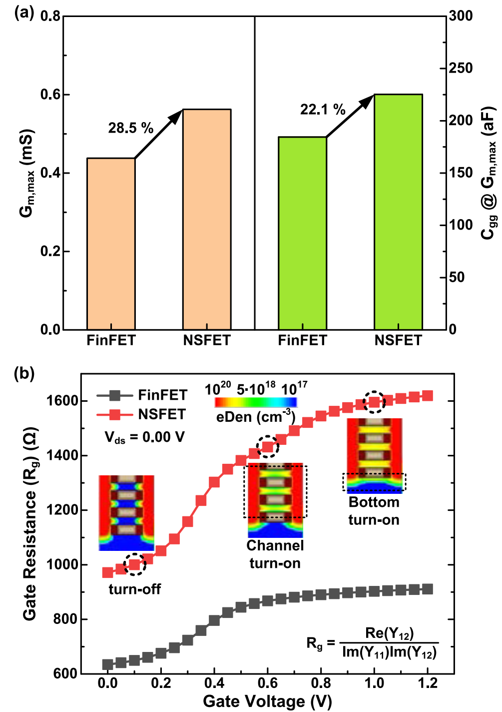

FIGURE 4. (a) Maximum G_m ($G_{m,max}$) and C_{gg} at the $G_{m,max}$ point and (b) gate resistance (R_g) of 2-fin FinFETs and NSFETs under the same footprint.

hand, NSFETs have almost similar F_t but smaller F_{max} than FinFETs.

Since DC parameters were well calibrated, G_mR_o of FinFETs and NSFETs were reasonable within the measured data [10], [11], [23]–[25]. F_t and F_{max} were slightly larger than the measured data [10], [11], [23]–[25] because the parasitic RC components of metal interconnects are not included in this TCAD work. But FinFETs and NSFETs would have the same metal-line configurations under the same CPP. Thus it is valid to compare the analog/RF performances quantitatively between FinFETs and NSFETs even in the front-end-of-line level.

Fig. 4 shows maximum G_m ($G_{m,max}$), gate capacitance (C_{gg}), and R_g of 2-fin FinFETs and single three-stacked NSFETs under the same footprint. G_m was extracted from the derivative of I_{ds}-V_{gs} curve where V_{gs} is gate-source voltage, and C_{gg} was extracted from C_{gg}-V_{gs} curve at a specific V_{gs} point. F_t is proportional to G_m/C_{gg}, whereas F_{max} is inversely proportional to R_g. Although $G_{m,max}$ increases by 28.5 % from fin to NS, C_{gg} increases as well because the NSFET has larger W_{eff} by large W_{NS} of 40 nm inducing greater overlap (C_{ov}) and outer-fringing (C_{of}) capacitances between gate and S/D [16]. R_g was obtained using Y parameters at the drain voltage (V_{ds}) of 0 V as $Re(Y_{12})/(Im(Y_{11})Im(Y_{12}))$ [26]. There is other method to extract R_g as $Re(Y_{11})/Im(Y_{11})^2$ [27], but these two methods give almost the same R_g values (not shown). NSFETs have greater R_g than FinFETs due to their complex metal gate (MG) configuration encircling around the channel. Also, top-most NS spacing region lengthens the MG height and increases the R_g. In addition, as shown in the insets of Fig. 4b, NSFETs have additional turn-on of the bottom transistor at high gate voltage (V_{gs}), thus increasing the R_g further.

Fig. 5 shows G_mR_o, F_t, and F_{max} of FinFETs having different fin width (W_{fin}) and fin height (H_{fin}). G_m decreases but R_o increases much as the W_{eff} (= W_{fin}+ 2×H_{fin}) decreases, so G_mR_o increases. Especially, smaller W_{fin} reduces the current drivability, which is related to the G_m, but also decreases the short-channel effects (SCEs), rising R_o greatly. Model equations of F_t and F_{max} are simply given by [14]

$$F_t = \frac{G_m}{2\pi C_{gg}} \tag{1}$$

$$F_{max} = \frac{F_t}{\sqrt{4R_{g,int}(G_{ds} + 2\pi F_t C_{gd})}} \tag{2}$$

where $R_{g,int}$ is the intrinsic gate resistance decomposed from the S/D resistance (R_{sd}), G_{ds} is output conductance (= $1/R_o$), and C_{gd} is gate-drain capacitance. $R_{g,int}$ consists of MG resistance and intrinsic channel resistance. Simulation and model results of F_t are F_{max} are well matched for all the W_{fin} and H_{fin} splits (Fig. 5). R_{sd} is extracted using Y-function method [28], and $R_{g,int}$ is calculated as

$$R_{g,int} = R_g - \frac{1}{4}R_{sd}. \tag{3}$$

The detailed derivation of $R_{g,int}$ is shown in appendix.

Larger W_{eff} increases G_m rather than C_{gg} and thus increases F_t (left of Fig. 6). But H_{fin} shifts C_{gg} greatly while

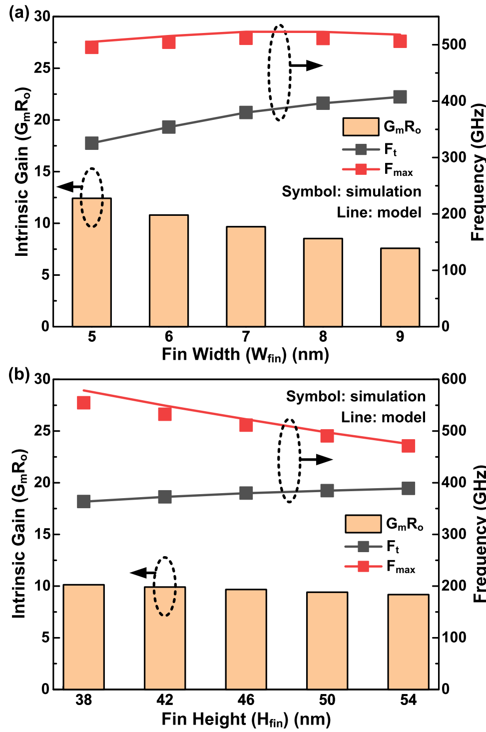

FIGURE 5. Analog/RF FoM of FinFETs having different (a) W_{fin} and (b) H_{fin} splits.

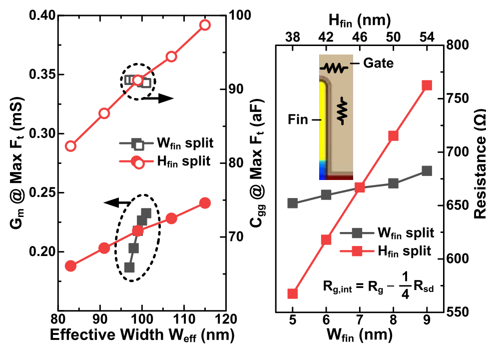

FIGURE 6. G_m and C_{gg} at the maximum F_t point (left) and intrinsic gate resistance ($R_{g,int}$) decomposed from R_{sd} (right).

W_{fin} does not, thus F_t increase is not as large as that for the W_{fin} splits. For larger W_{fin}, larger C_{ov} but smaller inversion capacitance due to V_{th} results in constant C_{gg}. This trend is different depending on the S/D doping profile; FinFETs having smaller junction gradients increase C_{para} and C_{gg} as the W_{fin} increases [29], [30]. C_{para} includes the C_{of} between gate and S/D epi and extension, the C_{ov} related to the junction gradients within the channel, and the contact capacitance between gate and S/D metal-lines [29]. Phosphorus from S/D is segregated at the channel/oxide interface much as the W_{fin} decreases [31]. F_{max} is almost similar irrespective of the W_{fin}, whereas F_{max} decreases greatly as the H_{fin} increases. The only difference of F_{max} between W_{fin} and H_{fin} splits comes from the $R_{g,int}$ (right of Fig. 6). As the H_{fin} increases, longer MG height increases the $R_{g,int}$ and thus reduces the F_{max}.

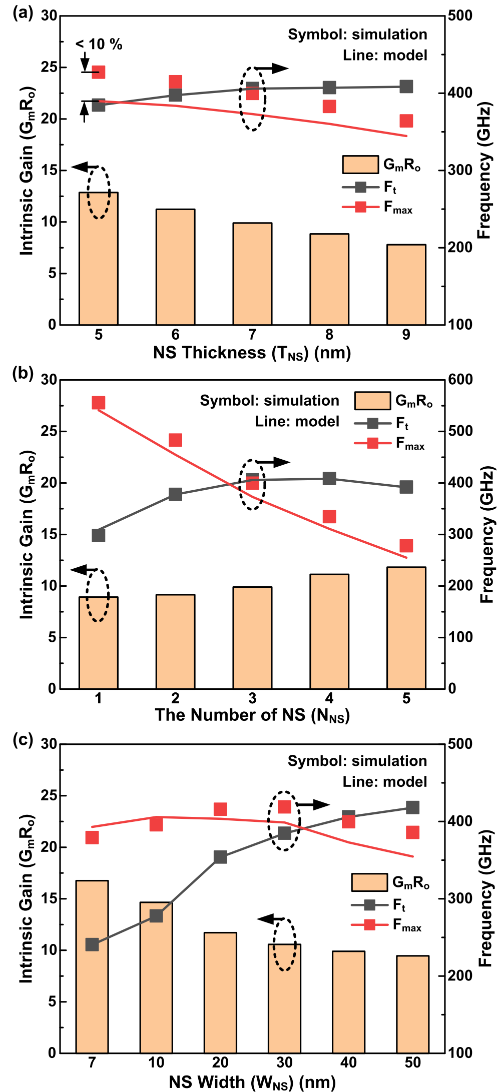

FIGURE 7. G_mR_o, F_t, F_{max} of NSFETs having different (a) T_{NS}, (b) N_{NS}, and (c) W_{NS} splits. Maximum error of F_{max} is below 10 %.

But as the W_{fin} increases, larger F_t compensates larger $R_{g,int}$ by thinner MG height and thus the F_{max} is almost the same.

Fig. 7 shows G_mR_o, F_t, and F_{max} of NSFETs having different NS thickness (T_{NS}), the number of NS channels (N_{NS}), and W_{NS}. Similar to FinFETs, thinner T_{NS} and W_{NS} increase the G_mR_o by enhancing the gate-to-channel controllability and by increasing the R_o much. On the other hand, greater N_{NS} at the W_{NS} of 40 nm maintains the SCEs while increasing G_m greatly rather than R_o decrease, which arises to larger G_mR_o. Although simulation and model results of F_t are equivalent, F_{max} is not because the $R_{g,int}$ contains the bottom transistor which, however, does not affect DC/AC performances of NSFETs greatly as the S/D over-etching is not severe [32]. To match simulation and model results of F_{max}, $R_{g,int}$ value excluding the bottom transistor is required.

F_t trends as a function of T_{NS}, N_{NS}, and W_{NS} are explained as follows. Larger T_{NS} and W_{NS} increase G_m rather than C_{gg}, thus increase F_t. Greater N_{NS} also increases G_m due

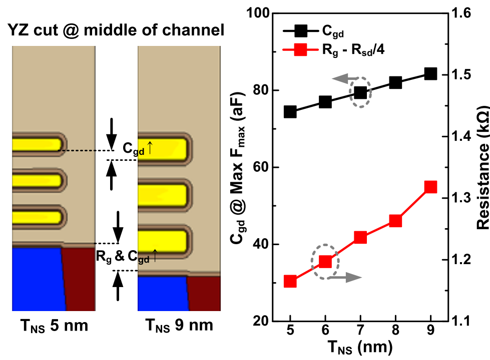

FIGURE 8. 2-D schematic views of NSFETs with T_{NS} of 5 and 9 nm at the middle of channel (left) and C_{gd} and $R_{g,int}$ of NSFETs with different T_{NS} (right).

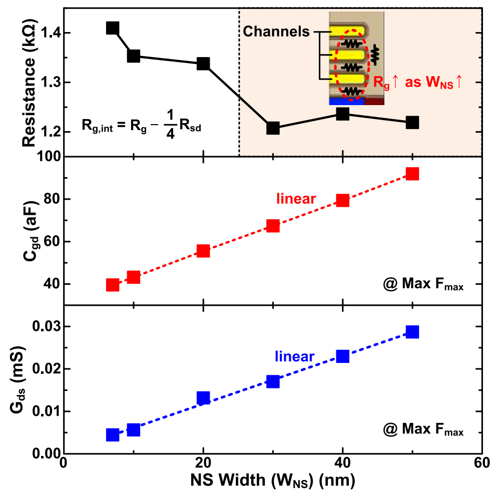

FIGURE 9. $R_{g,int}$, C_{gd}, and G_{ds} of NSFETs with different W_{NS}.

to larger W_{eff} but increases C_{para} of the NS spacing regions and thus C_{gg} critically. Increasing rate of the I_{ds} (and G_m) is smaller than increasing rate of the C_{gg} as the N_{NS} increases because longer carrier paths are needed to flow the bottom-side NS channels [17]. Fig. 8 explains the F_{max} trends as a function of T_{NS}. As the T_{NS} changes from 5 to 9 nm, greater W_{eff} (= 2× (W_{NS}+ T_{NS})× N_{NS}) increases C_{gd} and longer MG height increases $R_{g,int}$ and C_{gd}, thus decreasing F_{max}. Significant decrease of F_{max} for greater N_{NS} can be explained by larger $R_{g,int}$ and C_{gd} from longer MG height.

Fig. 9 shows $R_{g,int}$, C_{gd}, and G_{ds} of NSFETs with different W_{NS}. W_{NS} does not change the MG height but increases the NS spacing width (the inset of Fig. 9). There is a compensation of $R_{g,int}$ between wider NP and longer NS spacing width, so the $R_{g,int}$ does not decrease above the W_{NS} of 30 nm. On the other hand, both C_{gd} and G_{ds} increase linearly as the W_{NS} increases. Consequently, the F_{max} increases as the W_{NS} changes from 7 to 30 nm, and then decreases due to the constant $R_{g,int}$ along with the continuous increases of C_{gd} and G_{ds} as the W_{NS} increases above 30 nm.

Thinner NS spacing thickness (T_{sp}) decreases the S/D epi size, but the channel stresses are not varied much; 0.78 GPa to 0.70 GPa as the T_{sp} changes from 16 to 8 nm. Since the

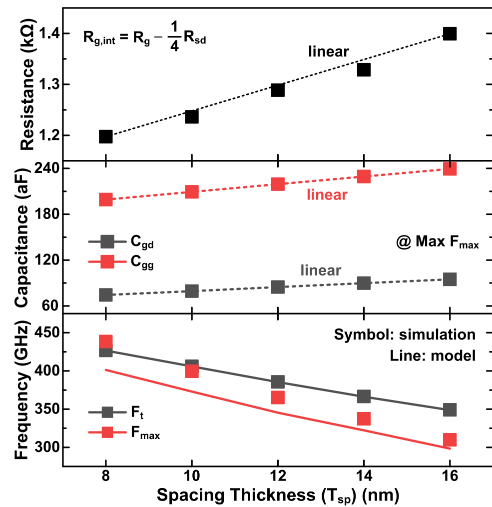

FIGURE 10. $R_{g,int}$, C_{gg}, C_{gd}, F_t, and F_{max} of NSFETs with different T_{sp}.

TABLE 2. Device Design Guideline for Best G_mR_o, F_t, and F_{max}.

Analog/RF FoM		Device Design	Max.
FinFET	G_mR_o	W_{fin} =5 nm, H_{fin} = 38 nm	12.7
	F_t	W_{fin} = 9 nm, H_{fin} = 54 nm	413 GHz
	F_{max}	W_{fin} = 7 nm, H_{fin} = 38 nm	555 GHz
NSFET	G_mR_o	T_{NS} = 5 nm, N_{NS} = 2, W_{NS} = 7 nm	20.1
	F_t	T_{NS} = 9 nm, N_{NS} = 3, W_{NS} = 50 nm	441 GHz
	F_{max}	T_{NS} = 5 nm, N_{NS} = 1, W_{NS} = 40 nm	604 GHz

R_{sd} is affected dominantly by the S/D extension rather than the S/D epi [33], the S/D epi size does not affect the I_{ds}. Thus, the DC performance metrics (G_m, R_o, and G_{ds}) of the NSFETs are almost the same. Fig. 10 shows analog/RF parameters including F_t and F_{max} of NSFETs with different T_{sp}. $R_{g,int}$, C_{gd}, and C_{gg} decreases linearly as the T_{sp} decreases due to the shorter MG height. This results in the increases of F_t and F_{max}. Thinner T_{sp} may increase the $R_{g,int}$ by increasing the ρ_{MG} [34], so there may be a F_{max} bottleneck at a certain T_{sp} in reality, which is beyond the scope of this article.

Table 2 summarizes the device design guideline to attain the best G_mR_o, F_t, and F_{max} of FinFETs and NSFETs. For FinFETs, best G_mR_o is obtained by reducing W_{fin} for better gate-to-channel controllability and also by reducing H_{fin} for larger R_o rather than smaller G_m. Best F_t is achieved when both W_{fin} and H_{fin} increase for larger current drivability. Best F_{max} is at shorter H_{fin} when shorter MG height is formed for smaller C_{gg} and $R_{g,int}$.

NSFETs have similar device design guidelines as FinFETs for best G_mR_o, F_t, and F_{max}. For all the cases, T_{sp} should decrease to reduce C_{gg} and $R_{g,int}$ while maintaining the same DC performances. Thinner T_{NS} and W_{NS} increase G_m much compared to R_o decrease, which is thus preferable to increase the G_mR_o, but at the N_{NS} of 2. Best F_t is obtained when both T_{NS} and W_{NS} increase for larger current drivability, but at the N_{NS} of 3. Greater N_{NS} increases G_m as well as C_{gg} but

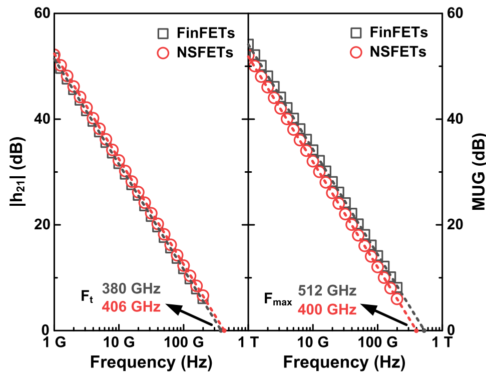

FIGURE 11. $|h_{21}|$ and MUG of FinFETs and NSFETs for the extraction of F_t and F_{max}.

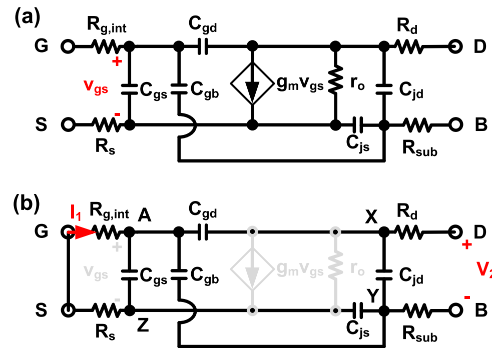

FIGURE 12. Equivalent circuits of FinFETs and NSFETs (a) in general case and (b) for Y_{12} (= I_1/V_2) when the V_{ds} is zero. Two-port configuration was applied; node G and D are connected to port 1 and 2, respectively, and the node S and B are grounded.

the increasing rate of G_m becomes smaller as N_{NS} increases, so there is an optimal point for the best F_t ($N_{NS} = 3$). For the best F_{max}, the W_{NS} of 40 nm is optimal by balancing between $R_{g,int}$ and F_t at the T_{NS} and N_{NS} of 5 nm and 1, respectively, where the $R_{g,int}$ is small. Maximum values of G_mR_o, F_t, and F_{max} for FinFETs and NSFETs are also provided in Table 2. Overall, NSFETs outperform FinFETs through proper device design, which are expectable for analog/RF applications.

IV. CONCLUSION

Analog/RF performances of FinFETs and NSFETs were thoroughly analyzed using fully-calibrated TCAD. NSFETs have larger G_mR_o than FinFETs due to the GAA structure enhancing the gate-to-channel controllability and larger W_{eff} increasing current drivability under the same footprint. But large $R_{g,int}$ including top-most NS spacing and bottom regions degrades the F_{max} of NSFETs over FinFETs. There are several modifications of geometrical parameters to improve G_mR_o, F_t, and F_{max}. G_mR_o is maximized by decreasing W_{fin} and H_{fin} for FinFETs (T_{NS} and W_{NS} for NSFETs), whereas F_t is maximized when the devices have large current drivability by increasing W_{fin} and H_{fin} for FinFETs (T_{NS} and W_{NS} for NSFETs). More N_{NS} over 3 increases the I_{ds} but degrades analog/RF performances due to much larger C_{gg}. Maximum F_{max} is obtained by decreasing $R_{g,int}$, achieved by smaller H_{fin} for FinFETs (N_{NS} for NSFETs), but without decreasing F_t much. Overall, NSFETs have larger G_mR_o, F_t, and F_{max} than FinFETs, which is thus promising for analog/RF applications.

APPENDIX

Fig. 11 shows the frequency-dependent $|h_{21}|$ and MUG from 1 to 200 GHz of FinFETs and NSFETs. Through linear extrapolation in the semi-log plots of $|h_{21}|$ and MUG near 10 GHz, F_t and F_{max} were obtained at 0 dB, respectively. All the F_t and F_{max} values of FinFETs and NSFETs were extracted using this method.

R_g is calculated as $\mathrm{Re}(Y_{12})/(\mathrm{Im}(Y_{11})\mathrm{Im}(Y_{12}))$, and imaginary parts of Y_{11} and Y_{12} are simply ωC_{gg} and $-\omega C_{gd}$, respectively [20], [21]. Real part of Y_{12} is obtained by using KCL at four nodes (X, Y, Z, A) of Fig. 12b as

$$V_X\left(1/R_d + j\omega C_{gd} + j\omega C_{jd}\right) + I_1 j\omega R_{g,int}C_{gd} - V_2/R_d = V_Y j\omega C_{jd} \quad (4)$$

$$V_X j\omega C_{jd} - V_Y\left(j\omega C_{js} + j\omega C_{jd} + j\omega C_{gb} + 1/R_{sub}\right) + V_Z j\omega C_{js} = I_1 j\omega R_{g,int}C_{gb} \quad (5)$$

$$V_Z\left(1/R_s + j\omega C_{js} + j\omega C_{gs}\right) + I_1 j\omega R_{g,int}C_{gs} = V_Y j\omega C_{js} \quad (6)$$

$$V_X j\omega C_{gd} + V_Y j\omega C_{gb} + V_Z j\omega C_{gs} = -I_1\left(1 + j\omega R_{g,int}C_{gg}\right) \quad (7)$$

where C_{js} and C_{jd} are the junction capacitances at source and drain, respectively, C_{gb} is gate-to-bulk capacitance, R_{sub} is substrate resistance, and C_{gs} is gate-to-source capacitance. Since there are four equations and five variables (V_X, V_Y, V_Z, V_2, I_1), we can make this into one equation in terms of V_2 and I_1 as (assuming that the second-order terms (ω^2) in the denominator and the higher-order terms (ω^3, ω^4, ω^5) are negligible at low frequency)

$$Y_{12} \equiv \left.\frac{I_1}{V_2}\right|_{V_1=0} \cong -j\omega C_{gd} + \omega^2 R_{sub}C_{jd}C_{gb} - \omega^2 R_{g,int}C_{gg}C_{gd} - \omega^2 R_d C_{gd}\left(C_{gd} + C_{jd}\right) \quad (8)$$

and the real part of Y_{12} is expressed as

$$Re\left(Y_{12}\right) = \omega^2 R_{sub}C_{jd}C_{gb} - \omega^2 R_{g,int}C_{gg}C_{gd} - \omega^2 R_d C_{gd}\left(C_{gd} + C_{jd}\right). \quad (9)$$

Using $\mathrm{Im}(Y_{11})$, $\mathrm{Im}(Y_{12})$, and eq. (9), R_g is calculated as

$$R_g = R_{g,int} + \frac{C_{jd} + C_{gd}}{C_{gg}}R_d - \frac{C_{jd}C_{gb}}{C_{gg}C_{gd}}R_{sub}. \quad (10)$$

Because F_{max} is extracted at high V_{gs}, C_{gb} and C_{jd} can be ruled out. And at the V_{ds} of 0 V, R_d and C_{gg} can be approximated as $R_{sd}/2$ and $C_{gg}/2$, respectively. Finally, R_g can be simplified as

$$R_g = R_{g,int} + \frac{1}{4}R_{sd}. \quad (11)$$

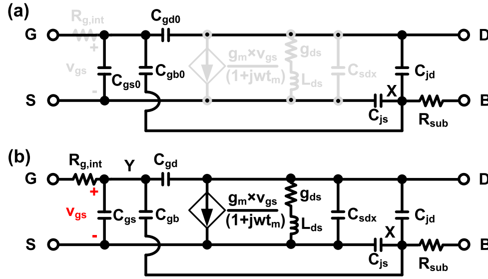

FIGURE 13. Equivalent circuits of FinFETs and NSFETs after de-embedding R_s and R_d (a) at off state and (b) on state. Two-port configuration was applied; node G and D are connected to port 1 and 2, respectively, and the node S and B are grounded.

Fig. 13 shows the equivalent circuits of FinFETs and NSFETs after de-embedding R_s and R_d extracted from Y-function method [22]. This de-embedding was done as

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} - \begin{bmatrix} R_s & R_s \\ R_s & R_s + R_d \end{bmatrix} = \begin{bmatrix} Y_{11}^{int} & Y_{12}^{int} \\ Y_{21}^{int} & Y_{22}^{int} \end{bmatrix} \quad (12)$$

where Z parameters are converted from Y parameters and Y^{int} parameters are the Y parameters after de-embedding R_s and R_d [35]. Parameters were extracted first at off state (V_{gs} = 0 V) where inversion channel was not formed and thus its components were negligible. Y^{int} parameters at off state are obtained by using KCL at one node (X) of Fig. 13a as

$$\frac{V_X}{R_{sub}} + (V_X - V_2) \cdot j\omega C_{jd} + V_X \cdot j\omega C_{js} + (V_X - V_1) \cdot j\omega C_{gb} = 0. \quad (13)$$

This equation can be represented as V_X in terms of V_1 and V_2. The currents flowing into G and D nodes are given by

$$I_1 = (V_1 - V_2) \cdot j\omega C_{gd0} + V_1 \cdot j\omega C_{gs0} + (V_1 - V_X) \cdot j\omega C_{gb0} \quad (14)$$

$$I_2 = (V_2 - V_Y) \cdot j\omega C_{gd0} + (V_2 - V_X) \cdot j\omega C_{jd} \quad (15)$$

where C_{gs0}, C_{gd0}, and C_{gb0} are the parasitic components of C_{gs}, C_{gd}, and C_{gb} at off state, respectively. Eqs. (14) and (15) can be formed in the matrix form as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11}^{int} & Y_{12}^{int} \\ Y_{21}^{int} & Y_{22}^{int} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \quad (16)$$

Assuming the second-order terms (ω^2) in the denominator and the higher-order terms (ω^3, ω^4, ω^5) are negligible at low frequency, real and imaginary parts of Y^{int} to extract the parameters in Fig. 13a are

$$Im\left(Y_{11}^{int}\right) \approx \omega\left(C_{gd0} + C_{gs0} + C_{gb0}\right) \quad (17)$$

$$Im\left(Y_{12}^{int}\right) \approx -\omega C_{gd0} \quad (18)$$

$$Im\left(Y_{22}^{int}\right) \approx \omega\left(C_{jd} + C_{gd0}\right) \quad (19)$$

$$Re\left(Y_{22}^{int}\right) \approx \omega^2 R_{sub} C_{jd}^2. \quad (20)$$

These components are equivalent to those for conventional MOSFETs at off state [27]. C_{gd0} and C_{jd} are extracted first using eqs. (18) and (19), respectively. C_{gs0} and C_{js} are extracted using $Im(Y_{12}^{int})$ and $Im(Y_{22}^{int})$ at the V_{ds} of 0 V. Then, C_{gb0} is extracted using eq. (17). At last, R_{sub} is extracted using eq. (20).

TABLE 3. Extracted parameters of 2-fin FinFETs and NSFETs under the same footprint at the V_{ds} of 0.7 V.

Parameters	Values	
	FinFET	NSFET
g_m	0.484 mS	0.711 mS
g_{ds}	26.8 µS	36.2 µS
C_{gs}	101 aF	131 aF
C_{gd}	68.0 aF	79.5 aF
C_{gb}	15.2 aF	18.1 aF
C_{sdx}	15.1 aF	35.1 aF
L_{ds}	3.84 nH	5.02 nH
τ_m	0.103 ps	0.182 ps
$R_{g,int}$	516 Ω	889 Ω
R_{sub}	38.0 kΩ	82.3 kΩ
C_{js}	5.02 aF	6.65 aF
C_{jd}	4.65 aF	5.91 aF
C_{gs0}	69.0 aF	80.0 aF
C_{gd0}	65.0 aF	74.8 aF
C_{gb0}	2.19 aF	3.53 aF
R_{sd}	878 Ω	891 Ω

* R_{SD} IS EXTRACTED AT THE V_{DS} OF 0.05 V.

Next, all other parameters are extracted at on state in Fig. 13b. Using the same assumptions above, All the Y^{int} components are simplified as

$$Y_{11} \approx j\omega C_{gg} + \omega^2 R_{g,int} C_{gg}^2 \quad (21)$$

$$Y_{12} \approx -j\omega C_{gd} - \omega^2 R_{g,int} C_{gd} C_{gg} \quad (22)$$

$$Y_{21} \approx g_m - j\omega\left(g_m\tau_m + C_{gd} + R_{g,int} C_{gg} g_m\right) - \omega^2 R_{g,int} C_{gg}\left(g_m\tau_m + C_{gd}\right) \quad (23)$$

$$Y_{22} \approx g_{ds} + j\omega\left(C_{gd} + C_{jd} + C_{sdx} - L_{ds} g_{ds}^2 + g_m R_{g,int} C_{gd}\right) + \omega^2 (R_g C_{gd}^2 + g_m\tau_m R_{g,int} C_{gd} + g_m R_{g,int}^2 C_{gg} C_{gd} + R_{sub} C_{jd}^2) \quad (24)$$

where L_{ds} and τ_m are the drain-source inductance and the time constant which represent the inertia of the inversion carriers as the V_{gs} change fast [36], and C_{sdx} is the source-drain capacitance due to drain-induced barrier lowering effect [35]. Each parameters except $R_{g,int}$, R_{sub}, and C_{jd} can be given by

$$g_{ds} \approx Re\left(Y_{22}\right)|_{\omega=0} \quad (25)$$

$$g_m \approx Re\left(Y_{21}\right)|_{\omega=0} \quad (26)$$

$$C_{gd} \approx -\frac{Im\left(Y_{12}\right)}{\omega} \quad (27)$$

$$C_{gs} \approx -\left.\frac{Im\left(Y_{12}\right)}{\omega}\right|_{V_{ds}=0V} \quad (28)$$

$$C_{gb} \approx -\frac{Im\left(Y_{11}\right)}{\omega} - C_{gd} - C_{gs} \quad (29)$$

$$\tau_m \approx -\frac{1}{g_m}\left(\frac{Im\left(Y_{21}\right)}{\omega} - C_{gd}\right) - R_{g,int} C_{gd} \quad (30)$$

$$L_{ds} \approx \frac{\tau_m}{g_{ds}} \quad (31)$$

$$C_{sdx} \approx \frac{Im\left(Y_{22}\right)}{\omega} - C_{gd} - C_{jd} + L_{ds} g_{ds}^2 - g_m R_{g,int} C_{gd}. \quad (32)$$

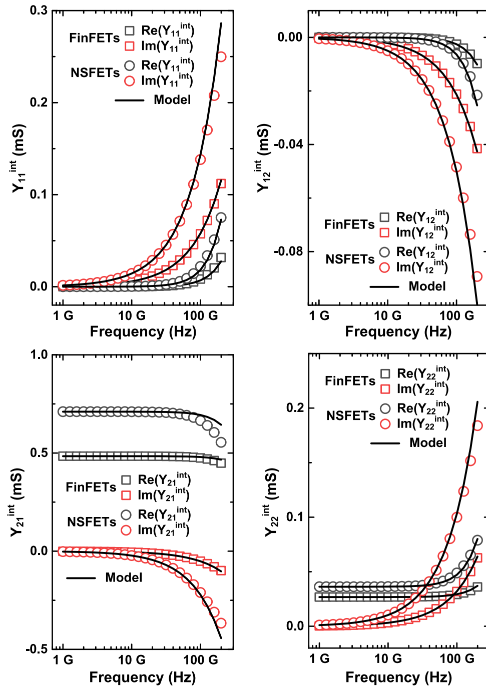

FIGURE 14. Y^{int} **parameters between model (lines) and TCAD (symbols) at the** V_{gs} **and** V_{ds} **of 0.70 V.**

Table 3 summarizes all the parameters extracted at the V_{ds} of 0.7 V. $R_{g,int}$ changes as a function of V_{ds} because the inversion channel shrinks by larger V_{ds}, so the $R_{g,int}$ values in Table 3 are smaller than those in Figs 6 and 8. All the C_{gg} components (C_{gs}, C_{gd}, C_{gb}) and C_{para} components (C_{gs0}, C_{gd0}, C_{gb0}) of NSFETs are greater than those of FinFETs because the NSFETs have larger W_{eff} of 282 nm inducing larger inversion capacitance and C_{of} than the FinFETs having the W_{eff} of 198 nm under the same footprint. Also, NSFETs have greater C_{js} and C_{jd} due to larger S/D epi area adjoining to the PTS layer. Larger L_{ds} and τ_m for NSFETs indicate that the devices respond to the V_{gs} much slowly than FinFETs. Fig. 14 compares the Y^{int} parameters between model (lines) and TCAD (symbols), validating that the equivalent circuits proposed in Fig. 13 are applied well to FinFETs and NSFETs up to 200 GHz. Slight deviation at high frequency is because the second-order terms (ω^2) in the denominator and the higher-order terms (ω^3, ω^4, ω^5) are not negligible.

REFERENCES

[1] C. Auth, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buehler, V. Chikarmane, G. Ding, and Q. Fu, "A 10 nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig.*, Dec. 2017, pp. 673–676.

[2] S. Yang, Y. Liu, M. Cai, J. Bao, P. Feng, X. Chen, L. Ge, J. Yuan, J. Choi, P. Liu, and Y. Suh, "10nm high performance mobile SoC design and technology co-developed for performance, power, and area scaling," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. 70–71.

[3] J. Cai, "Device technology for 3 nm node and beyond," in *IEDM Tech. Dig.*, Dec. 2019, pp. 1–59.

[4] W. Maszara, "MOSFET scaling knobs and future alternatives," in *IEDM Tech. Dig.*, Dec. 2018, pp. 1–56.

[5] D.-W. Kim, "CMOS transistor architecture and material options for beyond 5nm node," in *Proc. VLSI Short Course*, Jun. 2018, pp. 1–57.

[6] N. Loubet, T. Hook, P. Montanini, C.-W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita, J. Zhang, X. Miao, J. Wang, and A. Young, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *VLSI Tech. Dig.*, Jun. 2017, pp. 230–231.

[7] N. Loubet, S. Kal, C. Alix, S. Pancharatnam, H. Zhou, C. Durfee, M. Belyansky, N. Haller, K. Watanabe, T. Devarajan, and J. Zhang, "A novel dry selective etch of SiGe for the enablement of high performance logic stacked Gate-All-Around NanoSheet devices," in *IEDM Tech. Dig.*, Dec. 2019, pp. 242–245.

[8] S. C. Song, B. Colombeau, M. Bauer, V. Moroz, X.-W. Lin, P. Asenov, D. Sherlekar, M. Choi, J. Huang, B. Cheng, C. Chidambaram, and S. Natarajan, "2nm node: Benchmarking FinFET vs nano-slab transistor architectures for artificial intelligence and next gen smart mobile devices," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. 206–207.

[9] E.-Y. Jeong, M. Song, I. Choi, H. Shin, J. Song, W. Maeng, H. Park, H. Yoon, S. Kim, S. Park, B. H. You, H.-J. Cho, Y. C. An, S. K. Lee, S. D. Kwon, and S.-M. Jung, "High performance 14nm FinFET technology for low power mobile RF application," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. 142–143.

[10] B. Sell, B. Bigwood, S. Cha, Z. Chen, P. Dhage, P. Fan, M. Giraud-Carrier, A. Kar, E. Karl, C. J. Ku, and R. Kumar, "22FFL: A high performance and ultra low power FinFET technology for mobile and RF applications," in *IEDM Tech. Dig.*, Dec. 2017, pp. 685–688.

[11] J. Singh, J. Ciavatti, K. Sundaram, J. S. Wong, A. Bandyopadhyay, X. Zhang, S. Li, A. Bellaouar, J. Watts, J. G. Lee, and S. B. Samavedam, "14-nm FinFET technology for analog and RF applications," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 31–37, Jan. 2018.

[12] V. Subramanian, A. Mercha, B. Parvais, M. Dehan, G. Groeseneken, W. Sansen, and S. Decoutere, "Identifying the bottlenecks to the RF performance of FinFETs," in *Proc. 23rd Int. Conf. VLSI Design*, Jan. 2010, pp. 111–116.

[13] G. Crupi, D. M. M.-P. Schreurs, J.-P. Raskin, and A. Caddemi, "A comprehensive review on microwave FinFET modeling for progressing beyond the state of art," *Solid-State Electron.*, vol. 80, pp. 81–95, Feb. 2013.

[14] V. Jegadheesan, K. Sivasankaran, and A. Konar, "Impact of geometrical parameters and substrate on analog/RF performance of stacked nanosheet field effect transistor," *Mater. Sci. Semiconductor Process.*, vol. 93, pp. 188–195, Apr. 2019.

[15] Synopsys Inc., Mountain View, CA, USA, Version O-2018.06, 2018.

[16] J.-S. Yoon, J. Jeong, S. Lee, and R.-H. Baek, "Systematic DC/AC performance benchmarking of Sub-7-nm node FinFETs and nanosheet FETs," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 942–947, Aug. 2018.

[17] J.-S. Yoon, J. Jeong, S. Lee, and R.-H. Baek, "Optimization of nanosheet number and width of multi-stacked nanosheet FETs for sub-7-nm node system on chip applications," *Jpn. J. Appl. Phys.*, vol. 58, no. 12, pp. 1–5, Mar. 2019.

[18] S. Hung, "Multi-Vt engineering and gate performance control for advanced FinFET architecture," in *Proc. IEDM Short Course, Appl. Mater.*, Dec. 2017.

[19] R. Bao, S. Hung, M. Wang, K. Chung, S. Barman, S. A. Krishnan, Y. Yang, W. Tang, L. Li, Y. Lin, M. S. Chan, Z. Chen, X. Miao, M. Hopstaken, R. A. Conti, H. Jagannathan, M. P. Chudzik, D. McHerron, B. S. Haran, and S. Natarajan, "Novel materials and processes in replacement metal gate for advanced CMOS technology," in *IEDM Tech. Dig.*, Dec. 2018, pp. 253–256.

[20] N. R. Zangenberg, J. Fage-Pedersen, J. L. Hansen, and A. N. Larsen, "Boron and phosphorus diffusion in strained and relaxed Si and SiGe," *J. Appl. Phys.*, vol. 94, no. 6, pp. 3883–3990, Sep. 2003.

[21] J. Jeong, J.-S. Yoon, S. Lee, and R.-H. Baek, "Threshold voltage variations induced by $Si_{1-x}Ge_x$ and $Si_{1-x}C_x$ of sub 5-nm node silicon nanosheet field-effect transistors," *J. Nanosci. Nanotechnol.*, vol. 20, pp. 1–6, Aug. 2020.

[22] J.-S. Yoon, S. Lee, J. Lee, J. Jeong, H. Yun, and R.-H. Baek, "Reduction of process variations for sub-5-nm node fin and nanosheet FETs using novel process scheme," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2732–2737, Jul. 2020.

[23] V. Passi and J.-P. Raskin, "Review on analog/radio frequency performance of advanced silicon MOSFETs," *Semicond. Sci. Technol.*, vol. 32, pp. 1–123004-20, Nov. 2017.

[24] R. Singh, K. Aditya, S. S. Parihar, Y. S. Chauhan, R. Vega, T. B. Hook, and A. Dixit, "Evaluation of 10-nm bulk FinFET RF performance—Conventional versus NC-FinFET," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1246–1249, Aug. 2018.

[25] H.-J. Lee, S. Rami, S. Ravikumar, V. Neeli, K. Phoa, B. Sell, and Y. Zhang, "Intel 22nm FinFET (22FFL) process technology for RF and mm wave applications and circuit design optimization for FinFET technology," in *IEDM Tech. Dig.*, Dec. 2018, pp. 316–319.

[26] S. H.-M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz," *IEEE Trans. Electron Devices*, vol. 46, no. 11, pp. 2217–2227, Nov. 1999.

[27] M. Je, J. Han, H. Shin, and K. Lee, "A simple four-terminal small-signal model of RF MOSFETs and its parameter extraction," *Microelectron. Rel.*, vol. 43, no. 4, pp. 601–609, Apr. 2003.

[28] R.-H. Baek, C.-K. Baek, S.-W. Jung, Y. Y. Yeoh, D.-W. Kim, J.-S. Lee, D. M. Kim, and Y.-H. Jeong, "Characteristics of the series resistance extracted from Si nanowire FETs using the Y-function technique," *IEEE Trans. Nanotechnol.*, vol. 9, no. 2, pp. 212–217, Mar. 2010.

[29] J.-S. Yoon, E.-Y. Jeong, C.-K. Baek, Y.-R. Kim, J.-H. Hong, J.-S. Lee, R.-H. Baek, and Y.-H. Jeong, "Junction design strategy for Si bulk FinFETs for system-on-chip applications down to the 7-nm node," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 994–996, Oct. 2015.

[30] J.-S. Yoon, C.-K. Baek, and R.-H. Baek, "Process-induced variations of 10-nm node bulk nFinFETs considering Middle-of-Line parasitics," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3399–3405, Sep. 2016.

[31] F. Lau, L. Mader, C. Mazure, C. Werner, and M. Orlowski, "A model for phosphorus segregation at the silicon-silicon dioxide interface," *Appl. Phys. A Solids Surf.*, vol. 49, no. 6, pp. 671–675, Dec. 1989.

[32] J. Jeong, J.-S. Yoon, S. Lee, and R.-H. Baek, "Comprehensive analysis of source and drain recess depth variations on silicon nanosheet FETs for sub 5-nm node SoC application," *IEEE Access*, vol. 8, pp. 35873–35881, Feb. 2020.

[33] J.-H. Hong, S.-H. Lee, Y.-R. Kim, E.-Y. Jeong, J.-S. Yoon, J.-S. Lee, R.-H. Baek, and Y.-H. Jeong, "Impact of the spacer dielectric constant on parasitic RC and design guidelines to optimize DC/AC performance in 10-nm-node Si-nanowire FETs," *Jpn. J. Appl. Phys.*, vol. 54, no. 04DN05, pp. 1–5, Feb. 2015.

[34] X. Miao, R. Bao, U. Kwon, K. Wong, W. Rausch, W. Weng, R. Wachnik, S. Grunow, V. Narayanan, X. Li, and S. Krishnan, "An analytical metal resistance model and its application for sub-22-nm metal-gate CMOS," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 384–386, Apr. 2015.

[35] I. Man Kang and H. Shin, "Non-quasi-static small-signal modeling and analytical parameter extraction of SOI FinFETs," *IEEE Trans. Nanotechnol.*, vol. 5, no. 3, pp. 205–210, May 2006.

[36] Y. Tsividis and C. McAndrew, *Operation and Modeling of The MOS Transistor*, 2nd ed. New York, NY, USA: Oxford Univ. Press, 1999, pp. 467–489.

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