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2:1 Injection-Locked Frequency Dividers Using Multi-Resonance Spiral-Inductor Resonator

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ABSTRACT This article describes two low-power and wide locking range capacitive cross-coupled divide-by-2 injection-locked frequency dividers (ILFDs) implemented in TSMC standard 0.18 μm processes. The ILFDs are based on a differential VCO with one direct injection MOSFET for coupling the external signal to the spiral-inductor resonator. The first/second ILFD uses five/three on-chip inductors in series with parasitic varactors as a multi-resonance resonator. Three measured features are identified. The ILFDs have two non-overlapped locking ranges at low input power, they have two free-running oscillation frequency bands, and the frequency tuning versus gate bias of cross-coupled transistors shows the frequency tuning hysteresis. The power consumption of the 5-L ILFD core is 5.43 mW and the locking range is 6.07 GHz (116.395%) from 2.18 to 8.25 GHz at injection power P_{inj} =0 dBm. At the supply voltage of 1.1 V, the divider's free-running oscillation frequency is 3.13 GHz. The die area of the 2$^{\text{nd}}$ chip is 0.865 $\times$ 0.872 mm^2. The locking range at low input power is larger for the 5-L resonator ILFD.

INDEX TERMS Varactor-less divide-by-2 injection-locked frequency divider, frequency tuning hysteresis, distributed resonator, tunable resonator.

I. INTRODUCTION

The study of *LC* divide-by-2 injection-locked frequency divider (ILFD) [1] attracts intensive attention because they are widely used to process frequency signal. The bottom-series injection ÷2 ILFD [2] has limited locking range because the injection signal experiences a large tail capacitance to reduce the injection efficiency and the direct injection ILFD [3], [4] becomes the main stream of ILFD design. The often-cited ILFD design parameters cover phase noise, locking range and power consumption. The RF locking range can be enhanced through the resonator modification, with which the ILFD is robust to the inevitable shift of the center operating frequency caused by the process variations and supply voltages. Fig. 1(a) shows a direct-injection ILFD using distributed *LC* network [5] by reducing the capacitance in shunt with injection FET [6]. The distributed *LC* network consists of inductors L_1-L_6, distributed capacitors ($C_{11} \sim C_{41}$) and capacitor C_{p}. All passive elements are lumped and tank resonant frequency is un-tunable. Injection FETs are also distributed to in shunt the pairs of inductors [7], the measured and simulated locking range shows single-band-like locking range. A dual-resonator ILFD [8], [9] with varactor tuning leads to wider locking range because the two locking ranges associated with the two resonant frequencies can be merged to a single-band locking range. Fig. 1(b) shows a triple-resonance resonator ILFD with varactor tuning voltages (V_{T1}, V_{T2}) [10]. Triple-resonance ILFD is an extension of dual-resonance ILFD. Some publications about distributed resonator ILFD lack experimental justification because process drifting may lead to incorrect conclusion. The ILFD with varactor tuning enables the experimental verification of the multi-resonance effect on the locking range by looking at the performance variation with tuning bias. In addition, V_{G} in Fig. 1(b) is an external voltage, which is helpful to vary the ILFD property.

For the circuit in Fig. 1(b), depending on the size of varactors ($C_{11} \sim C_{41}$), two types of ILFD can be identified. In type 1, the size is small, as varactor capacitance increases, the oscillation frequency decreases and no dual-band tuning

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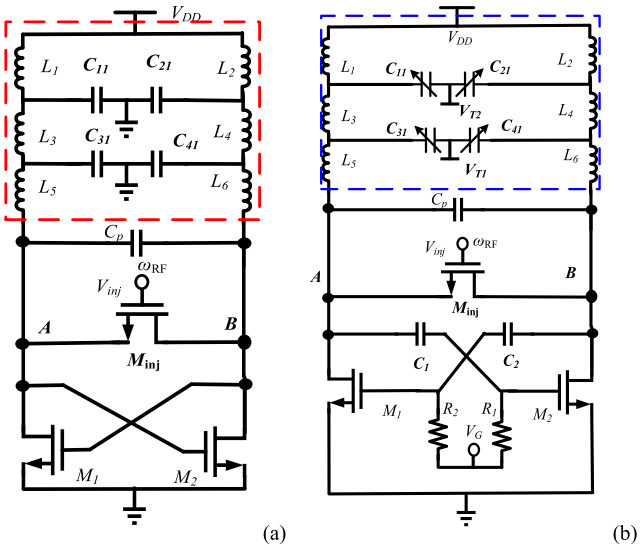

FIGURE 1. Schematics of the divide-by-2 ILFDs with distributed resonator.

range exists. In type 2, the varactor size is large, as varactor capacitance increases, the oscillation frequency switches frequency bands at certain tuning voltage from high-band to low-band and dual-band tuning range exists. A dual-resonance *LC* ILFD using the latter design shows that the tuning range can have two frequency bands while tuning the varactor control voltage [11]. A sharp transition in free-run oscillation frequency can be found and it is a behavior in forbidden oscillation frequency region. The net locking range can span over all the ILFD self-oscillation frequencies. The previous multi-resonance 2:1 ILFDs use analog varactors to tune the resonant frequencies for wide-band optimization and experimental verification.

This article designs wide-locking range varactor-less ÷2 ILFDs with a distributed spiral resonator. The circuits use five or three on-chip inductors to exploit the effect of distributed spiral resonator as a multi-resonance resonator. The distinct of this work and others are no analog capacitors and varactors are embedded to the resonator. At low RF injection power, the two ILFDs show two measured non-overlapped locking ranges, a property of dual-the gate with bias-controlled varactor. To confirm that the ILFDs have two resonant frequencies, the gate bias of the capacitive cross-coupled FETs is used to change the ILFD oscillation frequency and the free-running oscillation frequency shows the sharp transition in frequency tuning effect and frequency tuning hysteresis [11], [12], which is an effect of dual-resonance resonator with bias-controlled varactor. At injection power of 0 dBm, the designed 5-L ÷2ILFD has one-band locking range from 2.18 GHz to 8.25 GHz. This indicates multi spiral inductors can be used to construct distributed resonator for wide-band locking range design. Following this line, the ILFD circuit [13] uses only one on-chip inductor can have multi-band locking ranges, because the single inductor is a multi-resonance distributed resonator.

II. CROSS-COUPLED 2:1 ILFD WITH 5-INDUCTORS

A. CIRCUIT DESIGN OF THE 5-L 2:1 ILFD

Fig. 2(a) is a circuit evolved from Fig. 1(b) by removing ($C_{11} \sim C_{41}$) and depicts the test ÷2 ILFD circuit with inductors L_1- L_5 and a parasitic active capacitor C_p as the resonator. The switching transistors (M_1, M_2) in conjunction with capacitors (C_1, C_2) and resistors (R_1, R_2) are used to generate the negative resistance to compensate for the *LC* tank loss. FETs (M_3, M_4) are ILFD output buffers and M_5 with a dc gate bias V_{inj} is an injection mixer. The parasitic diodes explicitly drawn in Fig. 2(a) are bias-dependent. As V_G increases, the ILFD-core voltage swing increases, the average capacitance of C_p decreases accordingly. Based on the lumped inductor model, the above ILFD has one frequency band and one locking range. If the five inductors are remodeled to include the parasitic capacitors, the resonator is a multi-resonance resonator. Fig. 2(b) shows the differential 5-L resonator model for the ILFD. One half circuit model uses three single-π inductors in series, the parasitic MOSFET varactor C_p and channel resistance R_i of FETs are added to the resonator. The multi-resonance resonator may have two resonant frequencies and the ILFD can have two measured locking ranges associated with two resonant frequencies. Because of parasitic MOSFET varactors, varying bias-dependent oscillation voltage swing changes the average capacitance and the oscillation frequency. The mathematical formulation of locking range [14] for single-band ILFD with a parallel *RLC* resonator has been derived before and it can be extended to a dual-resonance ILFD circuit.

Fig. 3 depicts the simulated free-run oscillation frequency f_{osc} of the prelayout divide-by-2 ILFD. The tuning range of the designed ILFD shows dual-band tuning property. Increasing V_G leads to lower f_{osc}. Removing some inductors increases f_{osc}, but the dual-band behavior disappears in the simulated voltage region. Fig. 4(a) shows simulated oscillation frequency f_{osc} of the divide-by-2 ILFD versus V_G, f_{osc} decreases as V_G increases or V_{inj} decreases because of larger voltage swing. At V_{inj} =1.6 V, f_{osc} decreases from 3.7 GHz to 2.6 GHz as V_G increases from 0.53 V to 0.65 V. Fig. 4(b) also shows simulated f_{osc} decreases as V_G increases or V_{inj} decreases because of larger voltage swing. At V_G =0.575 V∼0.75 V, no dual band frequency tuning is simulated and no high-band resonant frequency is present. Fig. 4(c) shows simulated oscillation frequency f_{osc} of the pre-layout divide-by-2 ILFD, it shows frequency tuning hysteresis [11], [12], which is supported by the experimental data. The frequency-band transition voltage V_G is lower than the opposite case while V_G is tuned from high value to low value because the average capacitance is smaller at higher V_G. At V_{DD} =1.1 V, V_G =0.6 V, V_{inj} =1.65 V, the simulated locking range at P_{inj} =-15 dBm is from 4.5 GHz to 9.0 GHz, which is divided to three regions. The high-band is from 7.7 GHz to 9.0 GHz, the low-band is from 4.5 GHz to 6.4 GHz, and in between the above regions, the ILFD is locked to the input signal but the output contains other smaller unrelated frequency signal. The simulated locking range at

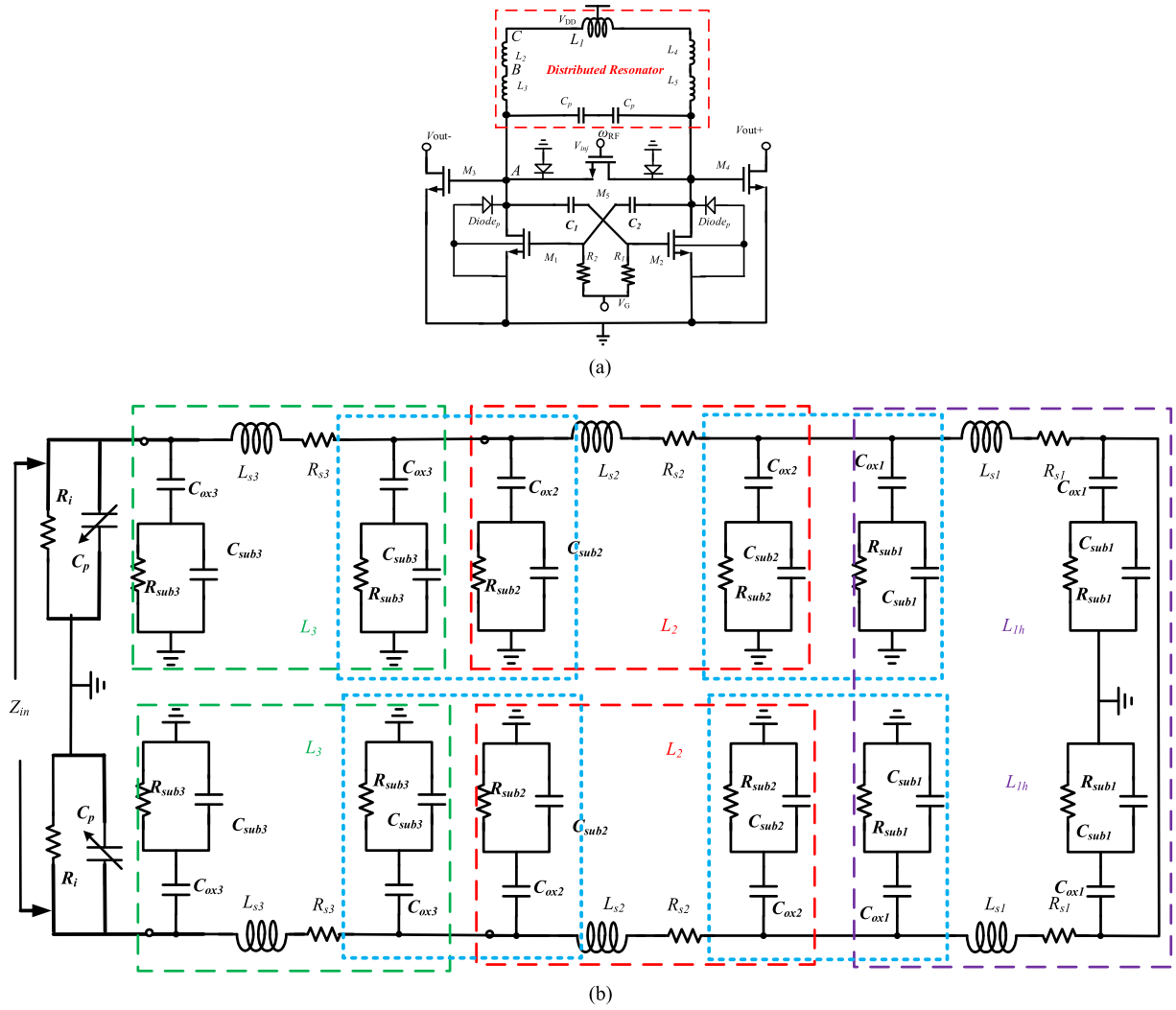

FIGURE 2. (a) Schematic of the 5-L divide-by-2 ILF (b) Differential 5-L resonator model of resonator with lumped elements.

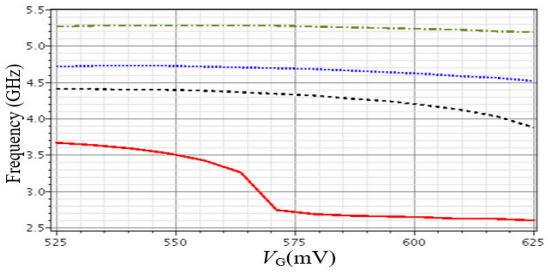

FIGURE 3. Simulated oscillation frequency f_{osc} of the prelayout divide-by-2 ILFD. Red: designed one. Black: without 1.8 nH L_1. Blue: without 1.27 nH L_2. Green: without 1.81 nH L_3. V_{DD} =1.1 V and V_{inj} = 1.5 V.

P_{inj} =0 dBm is from 4.3 GHz to 10.3 GHz. No concurrent signals is simulated.

B. EXPERIMENTAL OF THE 5-L 2:1 ILFD

The LC tank ÷2 ILFD has been designed and fabricated in the TSMC 0.18 μm SiGe BiCMOS technology. The die micrograph is shown in Fig. 5. The die size including the output buffers and input/output pads is 0.865 × 0.872 mm^2. At V_{DD} =1.1 V and V_{inj} =1.8 V, V_G =0.7 V, the current and power consumption of the ILFD-core are 4.94 mA and 5.434 mW respectively.

Fig. 6(a) shows the input sensitivity plot for the ÷2 ILFD biased at V_{DD} =1.1 V, V_{inj} =1.5 V and V_G =0.65, 0.7, 0.73 V. At V_{inj} =1.8 V and V_G = 0.7 V, an external injected signal power P_{inj} of 0 dBm provides a locking range 6.07 GHz (116.395%) from 2.18 to 8.25 GHz. The maximum FOM is 21.42, and it is equal to (locking range percentage)/(power dissipation in mW). At low injection power, dual-band locking ranges are measured. At V_G =0.65 V and P_{inj} of -12 dBm provides a locking range 2.2 GHz from 4.9 to 7.1 GHz. Fig. 6(b) shows the locking range, oscillation frequency, and power consumption dependence on V_G at V_{DD} =1.1 V and V_{inj} =1.5 V. The power decreases with decreasing V_G because of small channel conductance. An abrupt oscillation frequency transition is found around

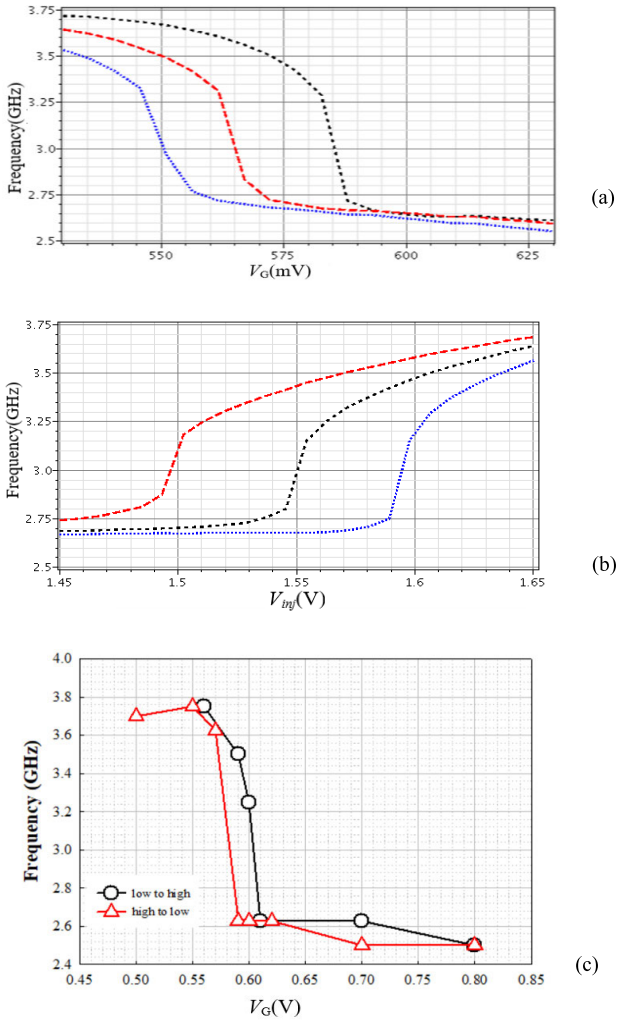

FIGURE 4. Simulated oscillation frequency f_{osc} of the prelayout divide-by-2 ILFD. (a). V_{DD} =1.1 V and V_{inj} =1.6(black), 1.5(red), 1.4 V (blue). V_G =0.7V. (b). V_{DD} =1.1 V and V_{inj} =1.6V. V_G =0.575(black), 0.585 (red), 0.565 V (blue). (c) Simulated oscillation frequency f_{osc} of the pre-layout divide-by-2 ILFD. V_{DD} =1.1 V, V_{inj} =1.65 and V_{buffer} =0.8 V.

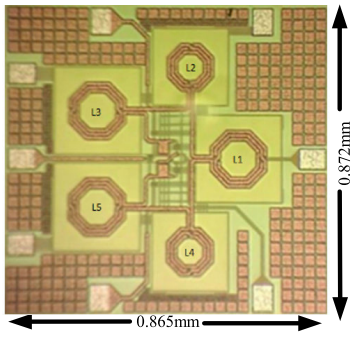

FIGURE 5. Chip micrograph for the 5-L divide-by-2 ILFD.

V_G =0.7 V while tuning V_G. The varactor-less ILFD has two operation frequency bands. If the five inductors in Fig. 2 are used as lumped inductors, the oscillation frequency has only one frequency band, even the bias voltages are varied to vary the capacitances of varactors. Therefore the parasitic capacitance of inductors must be accounted for. If no parasitic MOSFET varactor is present, the oscillation frequency will not have abrupt frequency change while tuning bias to change oscillation voltage swing. So tuning V_G to 0.7 V the ILFD can exploit the overlapping of locking ranges. Fig. 6(b) shows as V_G increases from 0.7 V, the ILFD free-runs at low-band, low-band-end locking range increases, while high-ended locking range changes little. Fig. 6(c) shows measured tuning range, power consumption and locking range at P_{inj} =0 dBm versus V_{inj}. Around V_{inj} = 1.6 V, the circuit switches the frequency band. Both Fig. 6(b) and Fig. 6(c) show dual-band tuning range. Fig. 6(d) shows the measured tuning curve by tuning V_G in the increasing voltage and in the decreasing voltage directions. Oscillation frequency f_{osc} is a function of V_G and V_{inj} and the tuning range shows the *hysteresis* effect [11], [12], where the oscillation frequency depends on the direction of bias tuning direction. This is also an evidence that the ILFD uses a multi-resonance resonator. At V_G =0.7 V and V_{inj} =1.6V two resonant modes are possible and they depend on the voltage tuning history. At V_G =0.7 V and V_{inj} =1.7 V only one frequency tuning curve is measured because smaller voltage swing.

Fig. 7(a) describes two measured output spectra from the free-run frequency divider and the locked ÷2 ILFD. The locked output spectrum shows a lower side-band output power and the locked circuit follows the injection source in phase noise. Fig. 7(b) plots two phase noises measured from the injection-locked circuit and the injection source. At the frequency offset of 1 MHz the locked phase noise shows -132.01 dBc/Hz, while the phase noise of -126.36 dBc/Hz is from the injection-reference, the locked phase noise is smaller than the injection signal by 5.65 dBc/Hz.

III. CROSS-COUPLED 2:1 ILFD WITH 3-INDUCTORS

A. CIRCUIT DESIGN OF THE 3-L 2:1 ILFD

Three spiral inductors may be configured with a property similar to a resonator with five inductors for a dual-resonance ILFD. The *LC* tank ILFD shown in Fig. 8 uses single capacitive cross-coupled (CC) pair and three on-chip inductors as the resonator. The *LC* resonator comprises inductors L_1, L_2 and L_3 and parasitic varactor C_p. The parasitic varactors include source-body diode and drain-body diodes of M_5, and drain-body diodes and gate-source capacitors of switching FETs M_1, M_2. The injection signal is ac-applied to the gate of injection FET M_5 with dc gate bias V_{inj}.

Fig. 9(a) shows simulated pre-layout oscillation frequency versus V_G. Case 1 and case 2 show one tuning range of reference circuits by deleting L_1 and reducing N respectively. Increasing the number of fingers N of FETs M_1, M_2 leads to low-band frequency at V_G =0.75 V. As N increases, the oscillation frequency at V_G =0.55 V decreases because C_p increases. Fig. 9(a) shows dual-band tuning range similar to Fig. 3. Tuning FET and inductor size leads to dual-band tuning range. Fig. 9(b) shows the simulated sensitivity plot

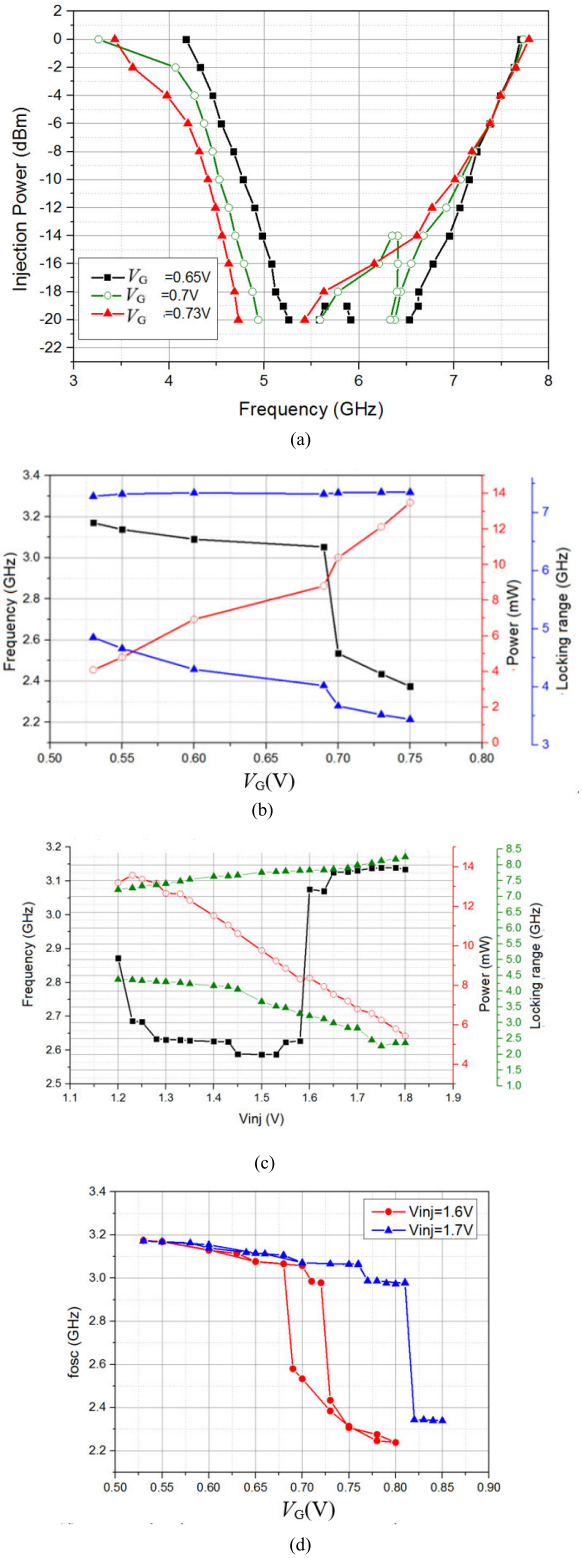

FIGURE 6. (a) Measured input sensitivity. V_{DD} =1.1 V and V_{inj} =1.5V. V_{buffer} =0.8 V. (b) Measured locking range at P_{inj} =0 dBm, power consumption, oscillation frequency vs V_{inj}. V_{DD} =1.1 V and V_{inj} =1.5 V. (c) Measured tuning range, power consumption and locking range at P_{inj} =0 dBm versus V_{inj}. V_{DD} =1.1 V, V_b =0.8V, and V_G =0.7 V (d). Measured tuning range vs V_G. V_{DD} =1.1 V and V_{inj} =1.6, 1.7 V.

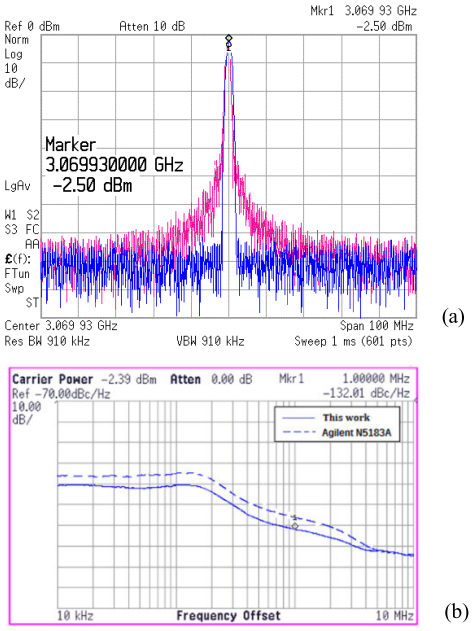

FIGURE 7. (a) Measured spectra of the free-running and locked ILFD. (b). Measured phase noises of the injection-reference and locked ÷2 ILFD. V_{DD} =1.1 V and V_{inj} =1.5 V, V_G =0.7 V. P_{inj} = 0 dBm. Injection signal f_{inj} = 6.14 GHz.

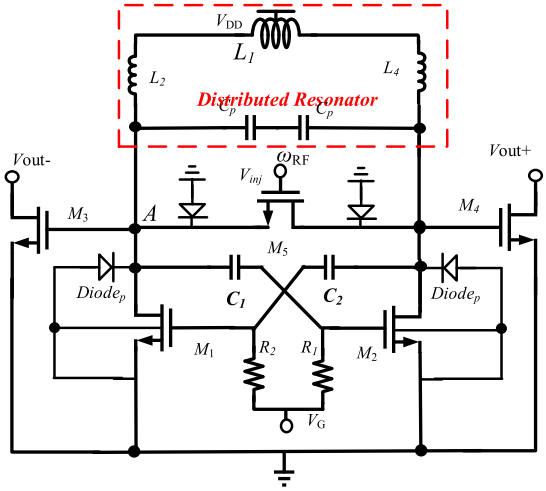

FIGURE 8. Schematic of the designed 3-LILFD.

using the foundry-supplied inductor models. The threshold voltage V_{TH} of M_5 is 0.75 V and M_5 is dc-biased below and near the threshold voltage. The V_{TH} of M_1 is 0.53 V and M_1 is dc biased above threshold voltage. At V_G =0.65 V, an external injected signal power of 0 dBm provides a single-band locking range 7.4 GHz from 3.2 GHz to 11.6 GHz. An external injected signal power of -12 dBm provides a low-band locking range 2.2 GHz from 4.2 GHz to 6.4 GHz and a high-band locking range 2.0 GHz from 8.4 GHz to 10.4 GHz.

At V_G =0.55 V, a single-band locking range is found. At V_G =0.55/0.65/0.8V the free-running oscillation

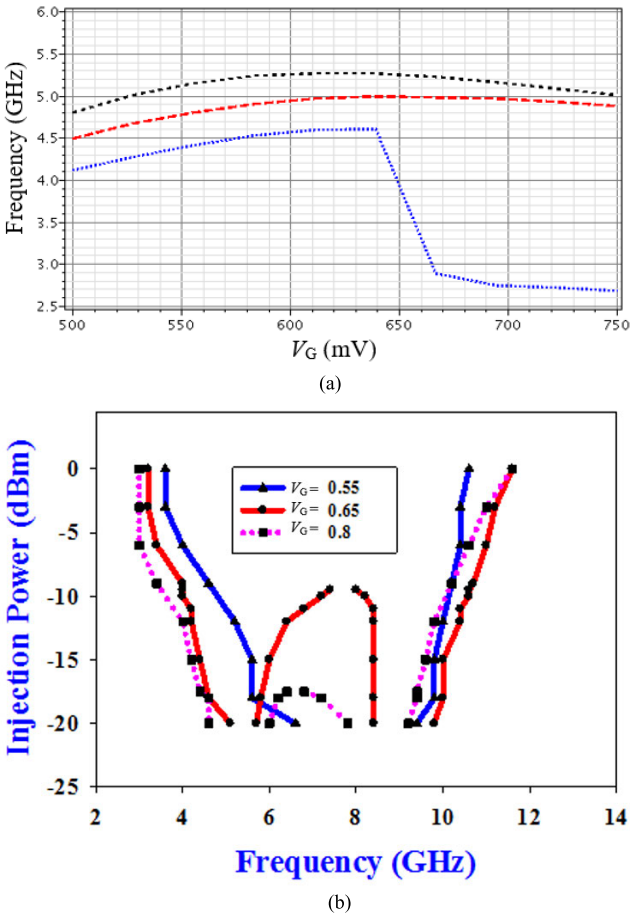

FIGURE 9. (a) Simulated pre-layout oscillation frequency vs V_G. V_{DD} =1.15 V and V_{inj} =1.75 V. Black dashed L_1 =0, N=16. Red solid, N=10. Blue dashed, N=16. N: number of MOSFET fingers. (b) Simulated pre-layout sensitivity. V_{DD} =1.15 V, V_G =0.55, 0.65, 0.8 V, and V_{inj} =1.75 V.

frequency is f_{osc} =4.4/2.75/2.6 GHz. As V_G increases, the voltage swing increases, f_{osc} decreases, and the oscillation frequency shows dual-band behavior because capacitor C_p is a tunable parasitic varactor.

B. EXPERIMENTAL OF THE 3-L 2:1 ILFD

The *LC* tank 3-L 2:1 ILFD has been designed and fabricated in the TSMC 0.18 μm CMOS technology. The chip area of the 0.18 μm ILFD shown in Fig. 10 is 1.058 × 0.862 mm^2,

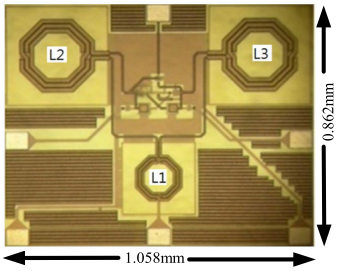

FIGURE 10. Chip micrograph for the 3-L 2:1 ILFD.

it uses three symmetric octagonal inductors. In the divide-by-2 mode, the gate-source overdrive of M_5 is close to the threshold voltage for maximum locking range and the mixer is a linear mixer.

Fig. 11(a) shows the measured tuning range versus V_{inj} and V_G. The low-band and high-band operation can be obtained by tuning V_{inj} and V_G. Low power consumption is obtained at low V_G and by tuning V_{inj}. Fig. 11(b) shows measured tuning range at V_{DD} =1.2 V and V_{inj} =1.7 V for the 2nd ILFD. It shows frequency hysteresis loop, that is, the tuning curves are different while V_G is tuned from 0 V to 1 V and from 1 V to 0 V. The high-band oscillation frequency is about 3.3 GHz and the low-band oscillation frequency is 2.4 GHz. As inductors and parasitic capacitors are not tunable in first order approximation, the tuning range is related to the parasitic varactors in MOSFETs. Increasing V_G enlarges voltage swing and varies the average capacitance of parasitic MOSFET varactor. The drain-body and source-body diodes of M_3 and the drain-body diodes of M_1 and M_2 are the main varactors. Gate-source and gate-body capacitors of MOSFETs form the secondary parasitic varactors

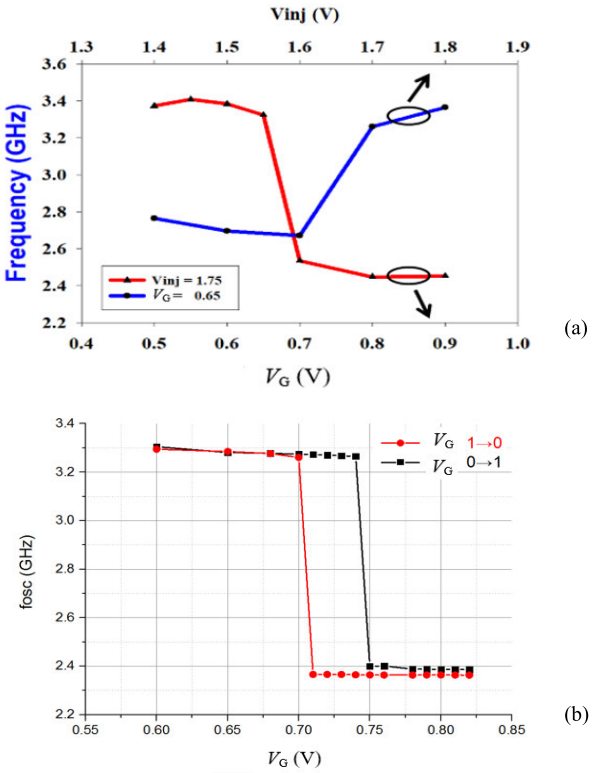

FIGURE 11. (a) Measured locking range versus V_{inj} or V_G. V_{DD} =1.15 V and V_{buffer} =0.8V. (b) Measured tuning range. V_{DD} =1.2 V and V_G =0.73 V, V_{inj} =1.7 V. V_{buffer} =0.8 V. ÷2 ILFD.

Fig. 12(a) shows the measured input sensitivity plot for the divide-by-2 ILFD biased at V_{DD} =1.15 V and three V_Gs. V_G can be used to optimize the ILFD performance. At V_G =0.65V, an external injected signal power of 0 dBm

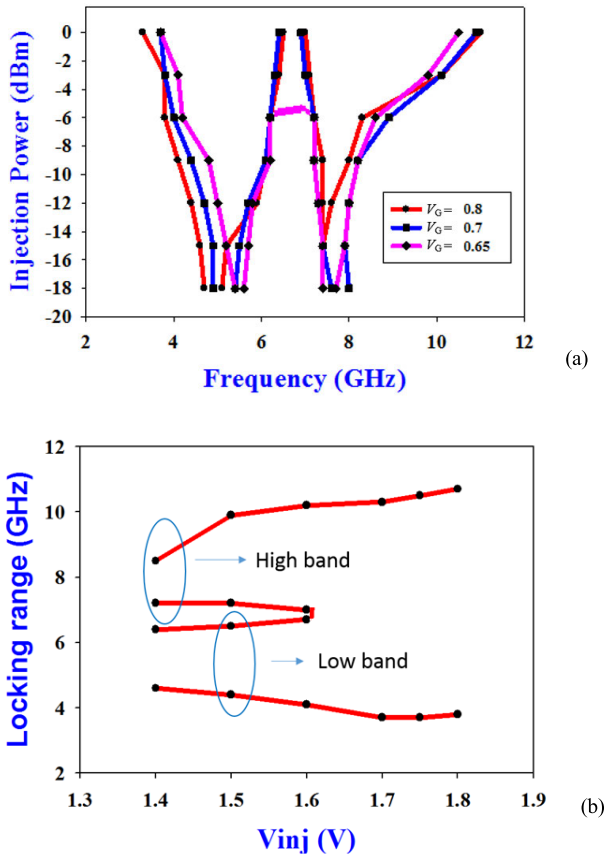

FIGURE 12. (a) Measured input sensitivity. V_{DD} =1.15 V and V_{inj} =1.75 V. (b) Measured locking range. V_{DD} =1.15 V and V_G =0.65 V. P_{inj} =0 dBm.

provides a locking range 6.8 GHz (95.77%) from 3.7 GHz to 10.5 GHz. The current and power consumption of the ILFD without buffers are 8.3 mA and 9.545 mW respectively. At V_G =0.7V, an external injected signal power of 0 dBm provides a low-band locking range 2.7 GHz (53.46%) from 3.7 GHz to 6.4 GHz and a high-band locking range 4 GHz (44.9%) from 6.9 GHz to 10.9 GHz. At V_G =0.8V, an external injected signal power of 0 dBm provides a low-band locking range 3.2 GHz (65.3%) from 3.3 GHz to 6.5 GHz and a high-band locking range 4 GHz (44.4%) from 7 GHz to 11 GHz. Fig. 12(b) shows the locking range at P_{inj} =0 dBm as a function of V_{inj}. As V_{inj} increases both the high band and low-band locking ranges increases to merge the dual-band locking ranges into a signal-band locking range. At V_{inj} < 1.6 V the ILFD has dual locking ranges because injection mixer conversion gain decreases as V_{inj} decreases. Table 1 is the performance comparison of ÷2 ILFDs. These ILFDs show good performance.

IV. SIMULATION OF OTHER 2:1 ILFDs

The section simulates an ILFD with 1-L resonator and 2-L resonator. The simulated 1-L ILFD circuit is the same as Fig. 2(a), except it uses only inductor L_1. Fig. 13 shows

TABLE 1. Performance comparison of CMOS ÷2 *LC* ILFDs.

ref	Pin (dBm)	V_{DD} (V)/ Pdiss(mW)	FOM	Locking range GHz
[1]	0	0.75/ 4.5	8.52	3.14~4.63(38.35%)
[8]	0	1.5/12.32	8.56	3~9.7(105.51%)
[15]	0	1.5/7.65	8.55	7.3~14.4(65.44%)
[16]	0	0.9/16.56	5.6	3.7~10.1(92.75%)
[17]	0	1.8/4.8	5.23	20.1~25.86(25.1%)
[18]	10	0.9/16.56	5.6	3.7~10.1(92.7%)
This5L	0	1.1/5.434	21.42	2.18~8.25(116.4%))
This3L	0	1.15/ 6.785	14.116	3.7~10.5(95.77%)

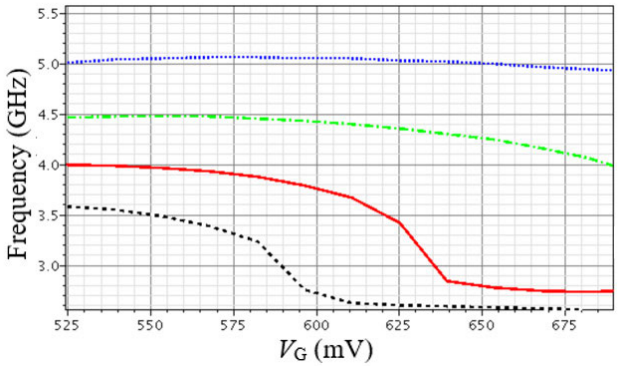

FIGURE 13. Simulated pre-layout oscillation frequency vs V_G. V_{DD} =1.1 V and V_{inj} =1.6 V. V_G =0.525~0.675V. Inner radius=75 μm, L=7.67nH (black dotted), Inner radius =65 μm, L=6.35 nH (solid red), Inner radius=55 μm, L=5.2 nH (green dash), Inner radius=45 μm, L=4.17 nH (blue dot). 1-L ILFD.

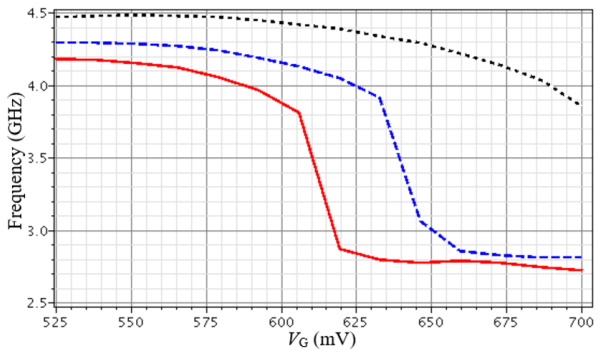

FIGURE 14. Simulated pre-layout oscillation frequency vs V_G. V_{DD} =1.1 V, V_{inj} =1.6 V and V_G =0.525~0.7V. Inner radius=55 μm, L=5.2 nH. W=90 μm (black dash). W=112.5 μm (blue dash). W=135 μm (solid line). 1-L ILFD.

simulated pre-layout oscillation frequency versus V_G. The ILFDs with L=7.67nH and L=6.35 nH shows dual-band tuning range. At L=6.35 nH, V_{DD} =1.1 V and V_{inj} =1.6 V, the locking range at P_{inj} =0 dBm at V_G =0.55V is from 4.2 GHz to 10.1 GHz; the locking range at V_G =0.625V is from 4 GHz to 11.1 GHz; the locking range at V_G =0.75V is from 3.9 GHz to 11.6 GHz. At L=6.35 nH, V_{DD} =1.1 V and V_{inj} =1.3 V, the locking range at V_G =0.55V is from 4.6 GHz to 10.2 GHz; the locking range at V_G =0.625V is from 4.4 GHz to 10.5 GHz; the locking range at V_G =0.75V

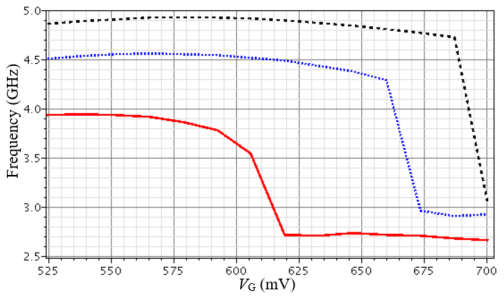

FIGURE 15. Simulated pre-layout oscillation frequency vs V_G. V_{DD} =1.1 V, V_{inj} =1.6 V and V_G =0.525∼0.7V. Inner radius=75 μm, L=2.62nH (black dash), Inner radius=85 μm, L=3.05 nH (blue dot), Inner radius=105 μm, L=3.75 nH (red solid). 2-L ILFD. 3-turn inductor.

is from 4.0 GHz to 10.4 GHz. Fig. 14 shows simulated pre-layout oscillation frequency versus V_G. The channel width of switching transistors (M_1, M_2) is changed. At W=90 μm, f_{osc} decreases with V_G and it shows only frequency band. At W=112.5 μm, f_{osc} decreases with V_G and it shows dual frequency bands at 4.29 GHz and 2.8 GHz, the band transition V_G is around 0.65 V. At W=135 μm, f_{osc} decreases with V_G and it shows dual frequency bands at 4.18GHz and 2.74 GHz, the band transition V_G is around 0.619 V. Increasing channel width increases the size of C_p, and increases the voltage swing to increases the value of C_p. The simulated 2-L ILFD circuit is the same as Fig. 2(a), except it uses only inductors L_3 and L_5. Fig. 15 shows simulated pre-layout oscillation frequency versus V_G for the 2-L ILFD. As inductance decreases, the oscillation frequency becomes higher and the band transition voltage V_G shifts to higher voltage.

V. CONCLUSION

This article designs varactor-less ÷2 ILFDs with wide locking range and high FOM. The experimental ILFDs use either five or three on-chip inductors in series to exhibit multi-resonance locking ranges. Despite no analog varactor and varactor tuning, gate bias of switching FETs can vary the free-running ILFD oscillation frequency and the frequency tuning hysteresis effect is measured. The experimental of tuning hysteresis, dual-band oscillation frequency and dual-band locking range proves that the parasitic capacitors in inductors and FETs concurrently enable the 2:1 dual-resonance resonator ILFD function and frequency tuning is used to optimize the locking range. The 5-L ILFD shows wide locking range at -12 dBm input power. The ILFD design approach with multi-inductors and without varactors is simple and high valuable for reliable ÷2 frequency divider design. By varying the FET and inductor sizes, 1-L or 2-L resonator ILFD also shows dual-band tuning range, this is important while it is often ignored in circuit operation interpretation.

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