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Design of a Wideband Surface Mountable Suspended Integrated Strip-Line Technology

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ABSTRACT This paper presents a low-loss surface mountable suspended integrated strip-line (SISL) technology. A DC-20 GHz thru transmission line and an eleventh-order generalized Chebyshev lowpass filter (LPF), with a cutoff frequency of 18 GHz, are simulated, fabricated, and measured to demonstrate the first-ever surface mountable suspended strip-line designs. Measured results of the thru line show less than 1 dB of insertion loss and greater than 10 dB of return loss across the 20 GHz bandwidth. Moreover, measured results of the LPF show less than 1 dB of insertion loss and greater than 10 dB return loss across the 18 GHz passband, as well as greater than 30 dB of suppression above 19 GHz. The proposed SMT SISL technology also has advantages of compact size, light-weight, low cost, and elimination of the extended circuit to be a multi-layer board following the trend to reduce the size, weight, power, and cost (SWaP-C).

INDEX TERMS Chebyshev, lowpass filter (LPF), surface mount technology (SMT), suspended integrated strip-line (SISL).

I. INTRODUCTION

The advancement in next-generation radar and communication systems has increased the demand for small form factor components that maintain system performance. The filter is a critical component in these systems which should preserve a large signal-to-noise ratio (i.e. low loss) while offering sharp roll-off and large stopband attenuation at receiver inputs. Ideally, the filter will also come in low profile packages that maintain ease of design and fabrication to minimize size, weight, and cost. Surface mount technology (SMT) allows for the manufacturing of smaller components and a higher component density circuit board as well as offering a simple fabrication process when compared to board-integrated components. SMT also performs better under shock and vibration conditions due to its lower mass and limited cantilevering.

Traditionally, suspended substrate strip-line (SSS) filters offer low-loss and wideband performance [1], [2]. SSS filters achieve these desirable characteristics by suspending a thin substrate (surrounded by air) within a metal cavity. Since the electric field exists mainly within the air, the effective relative permittivity is close to unity (across a wide frequency range) and the loss tangent is minimized, which keeps the dispersion and dielectric losses small, respectively. However, SSS technology requires bulky metalized packaging that does not allow for surface mount-ability and is expensive to fabricate. In [3] and [4], the authors present the substrate integrated suspended line technology as a viable alternative to SSS filters.

The substrate integrated suspended line is a quasi-board-embedded air-suspended technology that helps to overcome the fabrication difficulties and size limitations of SSS [5]. The technology relies on a standard multi-layer printed circuit board (PCB) fabrication process and has been widely used in component design such as filters [3], [4], couplers [6], [7], amplifiers [8], and antennas [9]. By enclosing the transmission line, using standard PCB materials, the authors were able to eliminate the need for machining out cavities in bulky metals; yet, still preserve the desirable characteristics of SSS components. However, the grounded coplanar waveguide (CPWG) trace and the suspended component exist on a middle substrate layer and the upper two substrates act essentially as a localized PCB cap. This PCB

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cap sacrifices the surface mount-ability as there is no readily available SMT feeding mechanism. In [10] and [11], the authors took the quasi-board-embedded approach from [3], [4] and developed the suspended integrated strip-line (SISL) technology, which is a fully-board-embedded design made possible by placing the CPWG trace on the top copper layer of the stack-up and accessing the suspended line layer through a vertical via transition. This transition is critical for offering an SMT SISL design as the signal enters and exits on the outer top copper on which a solder pad can be placed (the design of which is highlighted in Section IV) to allow for a ''flip-chip'' SMT feeding mechanism, not possible with previous SISL implementations. By offering an SMT SISL technology, only the SISL component needs to be multi-layer rather than the entire extended circuit easing the fabrication and reducing the overall size, weight, and cost.

In this paper, a design methodology is presented to enable a surface mountable SISL technology. To verify the feasibility of the design process, a previously designed DC-20 GHz SISL thru transmission line and an eleventh-order generalized Chebyshev lowpass filter (LPF) with an 18 GHz cutoff frequency (f_c) are simulated, fabricated, and measured demonstrating that all fully-board embedded SISL components can be implemented in an SMT fashion. This is, to the authors' knowledge, the first demonstrated air-suspended strip-line technology that has surface mount capabilities and shows the widespread applicability of the SISL technology in radio frequency (RF) and microwave systems.

II. SISL TECHNOLOGY

Fig. 1 shows an exploded 3-D view of the SISL technology. Substrates 1 and 5 are 10-mil-thick Rogers 6006 material, Substrates 2 and 4 are 30-mil-thick Rogers 6002 material, and Substrate 3 is a 5-mil-thick Rogers 6002 material. The top copper of Substrate layer 1 (M1) contains the CPWG trace and the starting point of the vertical via transition. The vertical via connects the CPWG trace to the strip-line trace on M6, which connects to the SISL component on M6 within the air cavity. Substrate layers 2 and 4 have a cutout to establish the air cavity above and below Substrate 3. It is important to note that copper layers M3, M5, and M7 have the same patterning as M4, and copper layer M9 is the same as M10. As seen in Fig. 1, the SISL structure requires a minimum of five substrate layers; however, additional substrate layers could be added to realize more complex quasi-lumped element or distributed circuit elements in the air cavity, but the overall structure and the proposed surface mounting technique will be the same. Surrounding the air cavity are plated through-vias, effectively creating a metal wall, to suppress excitation of parallel plate modes in the extended substrate, and increase isolation from nearby embedded circuits.

The location of the plated through-hole vias should be carefully placed in the design as their presence, along with metal layer 2 (M2) and layer 9 (M9), create an effective waveguide around the air cavity. This can cause the excitation of parasitic waveguide modes; specifically, the TE_{10} waveguide mode,

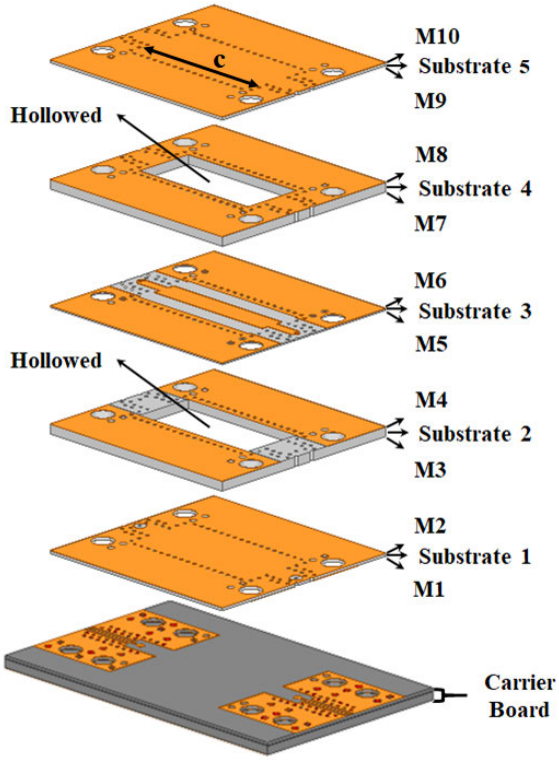

FIGURE 1. 3-D view of DC-20 GHz SISL thru with SMT carrier board (Note: the SISL component is inverted for "flip-chip" surface mounting).

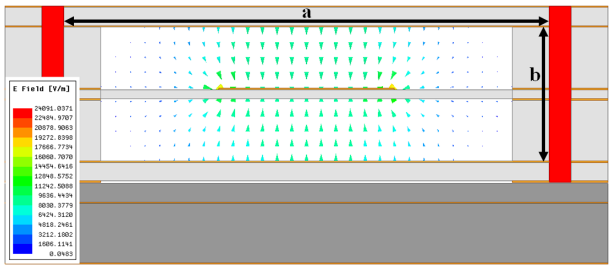

FIGURE 2. Vector plot of the E-field in the SISL air cavity.

since the width (a) of the cavity is greater than the height (b) of the cavity, and the TE_{101} waveguide resonant cavity mode, since $c > a > b$ where c is the length of the cavity. These dimensions are shown in Figs. 1 and 2.

If the effective waveguide becomes too large and the TE_{10} mode is excited at a frequency that is within the desired component's passband, mode-splitting will occur degrading the performance and usable bandwidth of the SISL design. Therefore, it is pertinent to ''push" the cutoff frequency of the TE_{10} mode beyond the desired bandwidth. The TE_{10} cutoff frequency can be calculated using

$$(f_c)_{10} = \frac{v}{2a\sqrt{\varepsilon_{r_{eff}}}} \tag{1}$$

where v is the speed of light and $\varepsilon_{r_{eff}}$ is the effective relative permittivity inside the air cavity. As can be seen in Figs. 2 and 3, the majority of the electric- and magnetic-fields are captured within the air. Therefore, the effective relative

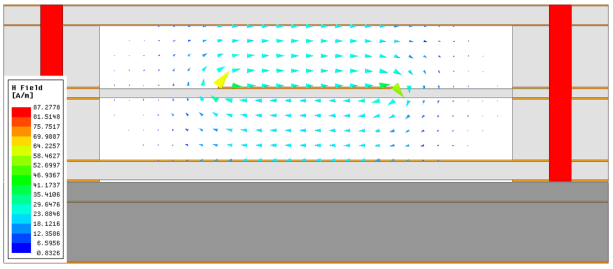

FIGURE 3. Vector plot of the H-field in the SISL air cavity.

permittivity can be approximated as 1.0 to yield a conservative calculated cutoff frequency. In general, if the desired cutoff frequency is known, ideally comfortably above the highest frequency of the desired bandwidth, then the width (a) can be solved for providing the maximum allowed width of the cavity design.

Beyond the TE_{10} dominant waveguide mode, a TE_{101} waveguide resonant cavity mode can also be excited due to the vias at the input and output of the SISL air cavity that are used to increase the operation bandwidth of the stripline transmission line. If the resonant mode occurs during the SISL component bandwidth, like before, mode-splitting occurs ultimately affecting the usable bandwidth. Therefore, it is again desirable to "push" this resonant mode high in frequency. However, it should be noted that this resonance can degrade the high-side stopband performance of filters, so other techniques like defected ground structures [12] might also need to be employed. Regardless, the TE_{101} resonant frequency can be calculated using

$$(f_r)_{101} = \frac{v}{2\sqrt{\varepsilon_{r_{eff}}}}\sqrt{\left(\frac{1}{a}\right)^2 + \left(\frac{1}{c}\right)^2} \tag{2}$$

where $\varepsilon_{r_{eff}}$ is again the effective relative permittivity inside of the air cavity, which can also be approximated 1.0 for the same reason as mentioned above [13]. Assuming a resonance high in frequency is desired, and the width a has already been solved for to ensure no TE_{10} mode propagation, the length c can be solved for providing the maximum allowed length of the cavity design.

In addition to the precise design of the air cavity, it is important to accurately design the via transition to operate over the desired passband bandwidth. For the fully-board-embedded SISL design, the characteristic impedance of the vertical via transition is designed to match the CPWG and strip-line characteristic impedance of 50 Ω. This allows each portion (CPWG, strip-line, and via transition) to be designed separately and then brought together with minimal mismatch concerns. In [14], a via can be modeled as an LPF with the primary limitation on high-frequency use being the series inductance. The associated inductances and capacitances for the SISL via transition are shown in Fig. 4. Based on this geometry, the main constraint on the high-frequency operation is the thickness of Substrate layer 2 (and therefore layer 4 assuming symmetry about Substrate 3) since via inductance increases as a function of length. In general,

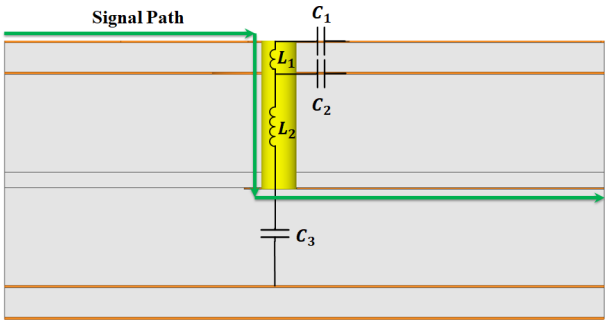

FIGURE 4. Side-view of the CPWG-to-strip-line vertical via transition to illustrate the associated inductance and capacitances.

there is a major trade-off space when deciding the thickness of Substrate layer 2 as it is desirable to maximize this thickness to reduce the parallel-plate capacitance (C_3) and reduce complexities associated with sequential lamination fabrication processes with embedded air-cavities. Yet, the thickness must be minimized to reduce the largest series inductance (L_2) to push the effective LPF cutoff frequency of the via transition above the highest intended frequency of operation.

After thicknesses are chosen and the via inductances are known, the next step is to adjust the anti-pads around the via. The anti-pads should be made large enough such that there is no LPF effect on the propagating signal, but made small enough to ensure that the total capacitance (C) yields a characteristic impedance (Z_o) of 50 Ohms based on

$$Z_o = \sqrt{\frac{L}{C}} \tag{3}$$

where L is the total inductance of the via transition.

Fig. 5 shows the ANSYS HFSS simulated S-parameters of the vertical via transition before and after tuning the design. In the "original design", the cutoff frequency is greater than 20 GHz, as seen by the flat S_{21} response. However, the via transition is not well matched at higher frequencies. Running a port simulation at multiple frequencies showed that the characteristic impedance is greater than 50 Ohms. This is

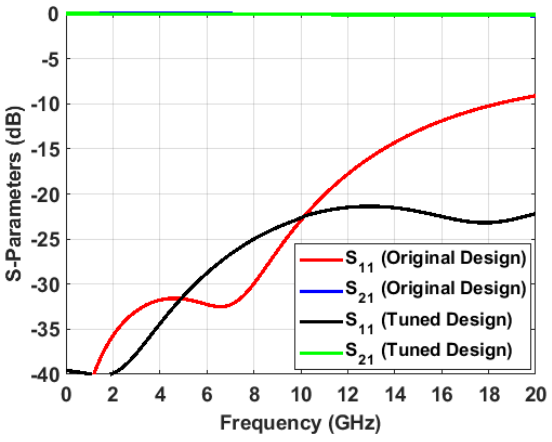

FIGURE 5. HFSS simulated S-parameters of the multi-layer vertical via transition before and after tuning the inductance and capacitance values.

corrected in the "tuned" design by increasing the via anti-pads, which reduces C in (3) resulting in a 50-ohm match.

The two SISL designs used in this paper to demonstrate the SMT SISL proof-of-concept are a DC-20 GHz thru-line and an eleventh-order generalized Chebyshev LPF with a cutoff frequency of 18 GHz. It should be noted that the primary focus of this paper is on the design procedure that allows for surface mountability of SISL components as described in section IV. Design details of the thru transmission line can be found in [10]. For the Chebyshev LPF design, a brief explanation is included in Section III and discussed in further detail in [11].

III. CHEBYSHEV LOWPASS FILTER DESIGN

The proposed SISL LPF is based on the generalized Chebyshev lowpass prototype developed in [1]. This prototype satisfies a generalized Chebyshev response with an equiripple passband, three transmission zeros at infinity, and the remainder at a finite frequency close to the cutoff frequency. Its selectivity is very close to that of an elliptic filter but can achieve very flat group delay in the passband making it ideal for wideband filters. The generalized Chebyshev lowpass prototype is shown in Fig. 6 for an arbitrary order N.

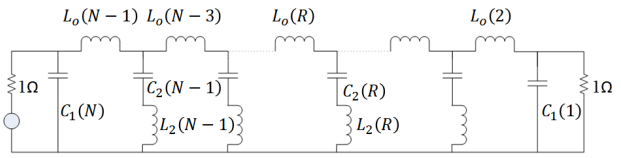

FIGURE 6. Generalized Chebyshev LPF prototype for filter order N.

The generalized Chebyshev element values for different order (N) filters are solved for using the alternating-pole technique in [1]. Moreover, the normalized frequency where ($N = 3$) transmission zeros occur (ω_o) and the normalized band-edge frequency (ω_1) are solved for using the Newton-Raphson technique and are also provided for different N. The former frequency is used when calculating the distributed line lengths and the latter frequency is used to determine the filter order. For the proposed LPF, the design criteria is a cutoff frequency of 18 GHz with at least 15 dB of return loss and 50 dB of insertion loss by 20 GHz. Given these parameters, an eleventh-order filter is needed to meet the design goals. The element values (g-coefficients) and normalized frequencies for the eleventh-order generalized Chebyshev LPF prototype are shown in Table 1 and Table 2, respectively, from [1]. Note that the LPF prototype is symmetrical about the center inductor $L_0(6)$. For any odd order generalized Chebyshev prototype, the design will be symmetrical about the center inductor.

The ideal LC model can be realized after a frequency and impedance scaling is performed using the cutoff frequency and element values from Table 1. The capacitor values are calculated using

$$C = \frac{C_n(R)}{Z_o \omega_c} \tag{4}$$

TABLE 1. Calculated element values for an eleventh-order generalized Chebyshev LPF prototype using an alternating-pole technique [1]

N = 11		R.L. > 20 (dB)
R	Element	I.L. > 50 (dB)
11	$C_1(11)$	1.04297
10	$L_0(10)$	0.935065
	$L_2(10)$	0.984313
	$C_2(10)$	0.787121
8	$L_0(8)$	0.786767
	$L_2(8)$	0.794605
	$C_2(8)$	0.975041
6	$L_0(6)$	0.807267
	$L_2(6)$	0.794605
	$C_2(6)$	0.975041
4	$L_0(4)$	0.786767
	$L_2(4)$	0.984313
	$C_2(4)$	0.787121
2	$L_0(2)$	0.935065
1	$C_1(1)$	1.04297

TABLE 2. Calculated normalized frequencies using an iterative Newton-Raphson technique [1].

		R.L. > 20 (dB)
Order	Frequency	I.L. > 50 (dB)
11	ω_o	1.13609
	ω_1	1.06853

where $C_n(R)$ are the element values from Table 1, Z_o is the characteristic impedance of the system, and ω_c is the cutoff frequency in rad/sec. The inductor values are calculated using

$$L = \frac{Z_o L_n(R)}{\omega_c} \tag{5}$$

where $L_n(R)$ are also the element values from Table 1. Using these equations, the inductance and capacitance values for the ideal LC circuit model can be calculated and are shown in Table 3. The eleventh-order generalized Chebyshev prototype with calculated component values is provided in Fig. 7. This LC circuit model is built in the Keysight ADS software and simulated to verify the calculated values and the filter performance. The simulated S-parameters are shown in Fig. 8. The cutoff frequency is right at 18 GHz with a return loss greater than 20 dB across the passband and greater than 50 dB of insertion loss at 20 GHz.

TABLE 3. Calculated inductance (nH) and capacitance (pF) values for the ideal LC circuit model.

N = 11	R.L. > 20 (dB)		I.L. > 50 (dB)	
R	Capacitor	(pF)	Inductor	(nH)
11	$C_1(11)$	0.184438		
10	$C_2(10)$	0.139194	$L_0(10)$	0.413389
			$L_2(10)$	0.435162
8	$C_2(8)$	0.172425	$L_0(8)$	0.347827
			$L_2(8)$	0.351293
6	$C_2(6)$	0.172425	$L_0(6)$	0.356890
			$L_2(6)$	0.351293
4	$C_2(4)$	0.139194	$L_0(4)$	0.347827
			$L_2(4)$	0.435162
2			$L_0(2)$	0.413389
1	$C_1(1)$	0.184438		

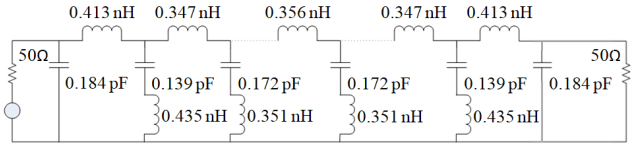

FIGURE 7. Generalized Chebyshev LPF prototype for an eleventh-order filter with calculated inductance and capacitance values.

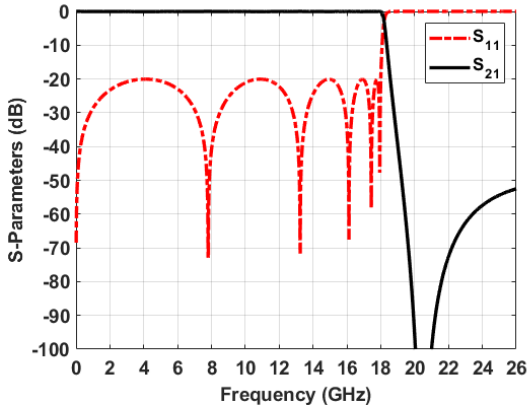

FIGURE 8. ADS simulated S-parameters of the eleventh-order Generalized Chebyshev ideal LC circuit model.

Given the small component values, compounded with self-resonant frequency limitations of lumped-element inductors and capacitors, the filter is converted from its current lumped-element design to a distributed design using LC equivalent transmission lines. This is accomplished using basic circuit theory and Richard's Transformations [15]. The distributed length and width of the shunt LC circuits, which can be realized as shunt open-circuit stubs, are derived using design equations from [16]–[18]. The distributed network for the series inductors is a series short-circuit stub. These distributed dimensions are derived in [16] by equating the series impedance of the π-network with the series short circuit stub. For brevity, the final distributed dimensions, fabrication, and non-SMT SISL filter performance are shown in [11].

IV. SURFACE MOUNTABLE DESIGN

In making the SISL designs surface mountable, several adjustments were made to the previous designs to maximize performance. Fig. 9 is a zoomed-in view of M1, from Fig. 1, of the SISL thru-line before and after the re-design. As can be seen, the annulus around the signal via pad is removed. As previously mentioned, the parasitic capacitance (C_1) from the via pad to the annulus ground plane is minimized to push the cutoff frequency of the via transition above 20 GHz. However, in the "flip-chip" SMT design shown in Fig. 10, the electric-field distribution around the via pad is captured within the carrier board substrate as opposed to air. This increases the effective parasitic capacitance (C_1) and reduces the match quality that was previously corrected for. Therefore, the copper around the via pad needs to be removed further to push the cutoff frequency beyond the

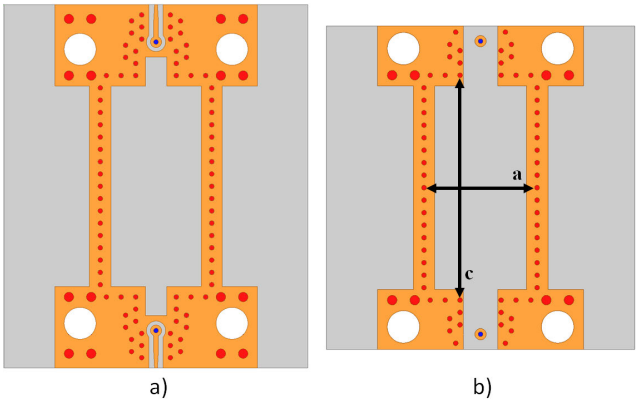

FIGURE 9. Top-down view of the a) connectorized thru and b) surface mountable thru design (M1 from Fig. 1).

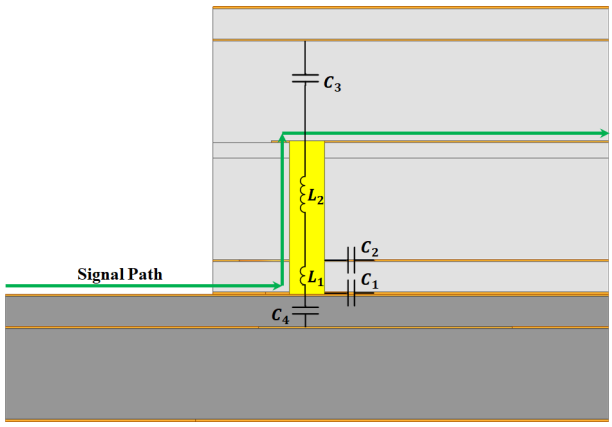

FIGURE 10. Side-view of the "flip-chip" SMT CPWG-to-strip-line vertical via transition to illustrate the associated inductance and capacitances.

operating frequency of the SISL components. Traditionally, this is accomplished by increasing the size of the annular via anti-pad (as previously done); however, the size of an annulus becomes increasingly large to reduce these parasitic effects, removing too much ground plane in the strip-line area after the carrier board CPWG trace and before the via. This ultimately increases the return current path negating any positive effect increasing the anti-pad had. Therefore, a rectangular anti-pad is used to get rid of the capacitances while still providing a sufficient ground plane. Another modification to the original design is the removal of the CPWG trace to the vertical via transition since it is not needed for the SMT design. The only remaining copper is the circular via pad, which is needed to solder the SISL design to the carrier board.

An exploded diametric view of the carrier board, designed to hold the SMT SISL component, is shown in Fig. 11. The surface mount carrier board is a two-layer stack-up using a 10-mil-thick Rogers 6006 substrate for the top substrate layer (Substrate layer 6) and a 30-mil-thick Rogers 4350b substrate for the bottom substrate layer (Substrate layer 7). The 30-mil-thick board is used solely to provide mechanical rigidity to the 10-mil RF circuit board so edge-launch connectors could be placed for testing purposes. The diameter of the via pad on L1 is chosen to be twice the size of the via transition

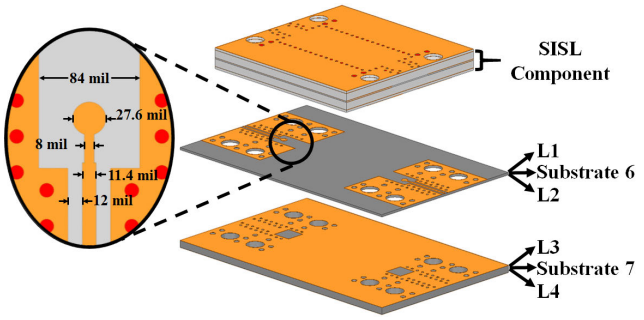

FIGURE 11. A 3-D view of carrier board with SMT SISL component.

via pad adhering to traditional PCB design procedures, which is also the same diameter of the via pad on M1 shown in Fig. 9 b). The CPWG trace, designed using guidelines in [19], is identical to the trace in [11] since the top substrate for both the carrier board and SISL components are the same material. In the cross-section, where the SMT component sits on the carrier board, the CPWG trace transitions into a strip-line trace, where the width is reduced to 8 mils to maintain 50 Ω impedance and minimize reflections. Additionally, a rectangular cutout is made in copper layer 3 (L3) to minimize the parasitic parallel capacitance (C_4) that has the same low pass effect previously mentioned. The width of the cutout in L3 is 84 mil (identical to the cutout width in M1) and the length is also 84 mil. Lastly, copper layer L2 has the same patterning as L3 and L4 is a solid ground plane.

V. FABRICATION

The SMT SISL components and the carrier board are fabricated using standard PCB processing techniques discussed in [10] and [11]. The carrier board design is fabricated in-house and the SISL components were fabricated by Accurate Circuit Engineering (ACE). The carrier board is a two-layer stack-up, using previously mentioned substrates, and is fabricated as follows. First, the top copper of Substrate layer 7 (L3) is milled using an LPKF ProtoMat S103 PCB prototype milling machine, while the bottom copper of Substrate layer 6 (L2) is completely etched off. Next, the substrates are laminated together with 2-mil-thick DuPont Pyralux LF0200 sheet adhesive. After lamination, the through-hole vias are drilled followed by a chemical copper plating process to provide a strong ground connection between layers. Finally, the top copper layer (L1) and bottom copper layer (L4) are milled and the carrier boards are individually routed. The overall size of the carrier board is $30.3 \times 19 \times 1.1$ mm^3.

With the carrier board fabricated, the next step is to mount the SMT SISL components. The signal pad is coated with solder paste as well as a large portion of the ground pad and ran through a reflow oven, using a standard recipe in a nitrogen environment, to ensure a strong connection is made. Southwest Microwave solder-less edge launch connectors (292-06A-5) are attached to both sides of the carrier board for testing. Fig. 12 is a photograph of the surface mount

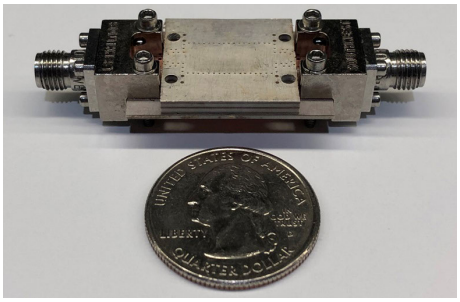

FIGURE 12. Photograph of the fabricated SMT SISL.

SISL LPF attached to the carrier board and connectorized for testing.

VI. SIMULATED AND MEASURED RESULTS

The SMT SISL components are simulated in ANSYS HFSS with port excitation at the reference plane of the 3D connector models provided by Southwest Microwave. A full finite-element-method simulation in HFSS is chosen to capture all of the parasitic effects in the SMT region. The components are measured using a Keysight N5225 PNA that has been calibrated to the reference plane of the edge-launch connectors using a Keysight N4691-60006 electronic calibration module. Thus, the measurement setup is limited to a maximum frequency of 26.5 GHz due to the 3.5mm calibration module. Simulated and measured S-parameters are shown in Figs. 13 and 14 for the thru-line and LPF, respectively. Both designs show good agreement between simulated and measured results. It should be noted that the stopband performance of the LPF is measured to be greater than approximately 30 dB from 19 to 26 GHz. However, the distributed stubs and air cavity start to resonate at 27.5 GHz, and further degradation of the stopband performance starts to occur due to the commensurate line nature of the filter.

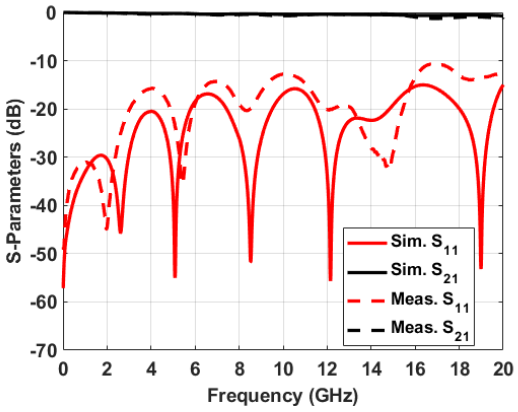

FIGURE 13. Simulated and measured S-parameters of the SMT SISL thru.

The proposed SMT SISL LPF is compared to other air-suspended technologies in Table 4. The proposed LPF has the advantage of being self-packaged (i.e. does not require additional mechanical shielding) and surface-mountable

TABLE 4. Comparison of LPFs in air-suspended technologies.

Reference	Technology	f_c (GHz)	Filter Order	Insertion Loss (dB)	Return Loss (dB)	30 dB Stopband Bandwidth (GHz)	Group Delay (ns)	Self-packaging	SMT Capable
[20]	SSS	18	11	< 0.75 dB	> 11.5	19-30 ($1.67f_c$)	0.08-0.46	No	No
[21]	SSL	5	5	< 0.5 dB	> 15	7.5-20 ($4f_c$)	N/A *	No	No
[11]	SISL	18	11	< 0.6 dB	> 12	19.5-26 ($1.44f_c$)	0.26-0.62	Yes	No
This work	**SMT SISL**	**18**	**11**	**< 1.0 dB #**	**> 10.5**	**19-26 ($1.44f_c$)**	**0.31-0.73**	**Yes**	**Yes**

*: The data are not available in the reference. #: The measured insertion loss of the SMT SISL LPF includes the losses associated with the carrier board.

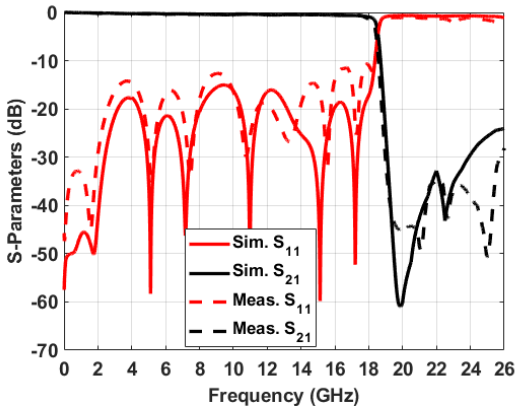

FIGURE 14. Simulated and measured S-parameters of the SMT SISL LPF.

while still maintaining low loss. Moreover, the increased insertion loss and group delay is to be expected as the measured results for the SMT SISL component includes the carrier board CPWG transmission lines in addition to the LPF itself. Furthermore, the proposed SMT SISL suffers from slightly higher insertion loss, due to the increased return current path and the vertical via transition, when compared to the other air-suspended technologies where the filter exists on the same metal layer as the input/output transmission lines. However, the insertion loss associated with the vertical via transition could further be minimized through the use of a multi-transition vertical via as shown in [22], [23]. This technique could readily be accomplished in the current SISL architecture by providing a single via transition per substrate layer (i.e. M1 to M2, M3 to M4, and M5 to M6). If additional via transitions are desired, the single Substrate 2 layer could be implemented using several thinner board layers that add up to the thickness of Substrate 2, and single vertical via transitions could be executed in between each of these layers.

VII. CONCLUSION

In this paper, the authors have demonstrated the first air suspended strip-line technology with surface mount capabilities. This is accomplished by re-designing the input/output feed structure of a fully-board-embedded SISL technology to create a convenient feeding mechanism for surface mountability. For proof-of-concept, a DC-20 GHz thru line and 18 GHz generalized Chebyshev LPF are used to illustrate the feasibility of this design. Both the thru-line and LPF display measured insertion losses less than 1 dB and return losses greater than 10.5 dB across their respective passbands. Ultimately, this SMT SISL design eliminates the need for the extended circuit, which contains other system components (i.e. amplifiers, mixers, attenuators, etc.), to be multi-layered offering a low cost and high-performance component solution for next-generation radar and communication systems.

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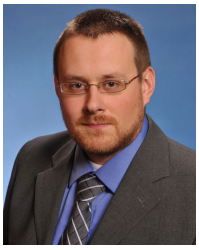

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