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Analyses of Pinned Photodiodes With High Resistivity Epitaxial Layer for Indirect Time-of-Flight Applications

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ABSTRACT This article analyzes the performance of pinned photodiode (PPD) for Time-of-Flight(ToF) applications on high resistivity epitaxial wafers. Due to its wide depletion region, high epitaxial resistivity PPDs feature some key advantages in collecting photogenerated charges. This article compares the demodulation contrast of the same pixel design on epitaxial wafers with different resistivity at near-infrared wavelength to analyze their performance. By comparing the simulated profile of pixels with different epitaxial resistivity, the characteristics of the PPD pixel on high resistivity epitaxial wafer when collecting photogenerated charges are concluded. This article also discusses the effects of using high resistivity epitaxial wafer with various design parameters. It is found that the use of high resistivity epitaxial wafer can greatly improve crosstalk performance, allow pixels to work at higher modulation frequencies, and enable large-sized pixels to have good demodulation capabilities.

INDEX TERMS Pinned photodiode, time-of-flight, ToF, high resistivity, CMOS image sensor.

I. INTRODUCTION

In recent years, 3D imaging technology has become a research focus. Compared to 2D imaging technology, 3D image sensors significantly improves the anti-interference and accuracy of identification. In addition, it can avoid time-consuming subsequent software processing, thereby improving the imaging speed. Due to its advantages, 3D imaging can be used in augmented reality, autonomous driving, medical electronics, mobile payment, and intelligent security. As a 3D imaging technology, IToF [1] has the advantages of moderate detection distance, favourable accuracy, high system integration, and low cost. It is currently a technology with great research value.

PPD is a pixel structure commonly used in IToF technology. Compared with other pixel structures, the power consumption of the PPD structure is usually lower. In addition, due to the pinning layer, the surface dark current of the PPD is relatively low. However, the horizontal electric field is weak from PPD to floating diffusion (FD) in the standard PPD structure, which hinders its application in 3D imaging.

Several methods have been proposed to optimize the standard PPD for 3D imaging. The optimization methods can be divided into two types. One is to optimize the potential of transfer gate(TG) channel between the PPD and the floating diffusion(FD). [2]–[5] describe this kind of optimization method, which eliminates the potential barrier in the carrier path by changing the overlap length of the pinning layer and the transfer gate, adjusting the anti-punch-through implantations, and modifying the position of the p-well mask. These changes will speed up the transfer of photon carrier from the PPD region to FD. The other one is to optimize the potential profile of n-well in PPD. [3], [4], [6], [7] achieve this by adjusting the shape of the pixels. [8], [9] introduce the effect of the pinning potential of PPD. [6], [10], [11] introduce the staircase doping profiles of n-well generated from step implantation, which can optimize the lateral electric field of n-well. Especially, by changing the angle of implantation and the thickness and position of the photoresist, [11] realizes the staircase doping profiles by only one mask.

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In addition to the above methods, using a high resistivity epitaxial(epi) wafer instead of adjusting subtle implantation or changing masks is also a good way to increase the charges transfer speed. For a photodiode, or for a one-sided abrupt n^+-p junction, the width of the depletion region of the P region can be expressed as

$$W = \sqrt{\frac{2\varepsilon_s \psi_{bi}}{qN_A}} \tag{1}$$

where ε_s represents the dielectric constant of the semiconductor, ψ_{bi} represents the built-in potential of the diode, q represents element charge, and N_A represents the acceptor doping concentration. For non-degenerate semiconductors, the built-in potential of the PN junction and the resistivity of the P-type semiconductor are

$$\psi_{bi} \approx \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2} \tag{2}$$

$$\rho = \frac{1}{q\mu_p N_A} \tag{3}$$

where N_D is the donor doping concentration, k is the Boltzmann constant, T is the temperature, n_i is the intrinsic carrier concentration, and μ_p is the hole mobility. For silicon semiconductors, when the impurity concentration is low, the hole mobility is almost constant despite the change of boron impurity concentration, which is about 500cm^2/V·s at 300K [12]. Then the relationship between the width of the depletion region and the resistivity at 300K can be obtained, as shown in Fig. 1.

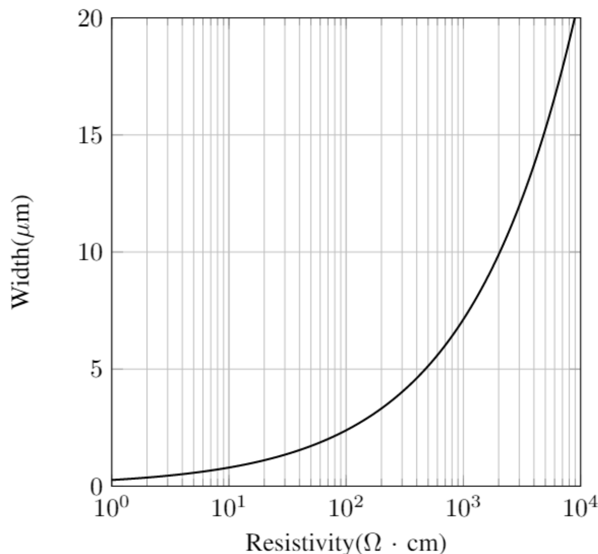


FIGURE 1. Relationship between the width of the depletion region and the resistivity of the p-type side of a one-sided abrupt silicon n^+-p junction.

According to [13], (1) is the 1-D PN junction depletion region width formula derived from the Poisson equation. However, the width of the depletion region of an actual device does not perfectly match (1); it is less than the calculated value, but the trend is almost the same. It can be seen from Fig. 1 that the higher the resistivity, the wider the depletion region of the photodiode. Since the drift transfer time of the charges in the depletion region is proportional to the distance and the diffusion transfer time is proportional to the square of the distance [11], a wider depletion region will at least facilitate the vertical transfer, so the use of high resistivity epi wafer can enhance the performance of the image sensor.

At present, researches on the use of high resistivity epi wafer have been conducted to optimize the image sensor, and many of them introduce PDD with high resistivity epi wafer. For example, [14]–[17] improve the performance of the image sensor with high resistivity epi wafer, and [16] takes advantage of the characteristics of high resistivity epi wafer to reduce crosstalk between pixels. [17]–[19] use the high resistivity epi wafer to improve the PPD ToF sensors' performance. With high resistivity epi wafer [19] makes the sensor have higher quantum efficiency at both near-infrared (NIR) and soft Xray wavelength. Reference [18] uses a high resistivity epitaxy to widen the depletion region and use a low resistivity substrate to increase the recombination of the electrons in the deep inside of the Si substrate. Reference [19] uses a gradual resistivity epitaxy to achieve the same goal as [18].

The same pixel design on epi wafers with resistivities of high, middle and low are simulated, so as to know the effects of epi resistivity on the performance of pixels and that on the collection of photogenerated charge. The low resistivity is about $10\Omega \cdot$ cm, while the middle resistivity is about an order of magnitude larger than the low resistivity, the high resistivity is about an order of magnitude larger than the middle resistivity, and the epi thickness is 10μm. This article also discusses the crosstalk performance of pixels with different epi resistivities. Simulation results show that high epi resistivity significantly improves crosstalk performance. In addition, the influence of parameters, such as modulation frequency, p-well mask position, and pixel size, on ToF PPD pixels using high resistivity epi wafers, are also analyzed to comprehensively demonstrate the advantages of high resistivity epi wafers. It can be found that pixels on high resistivity epi wafers can work at relatively high modulation frequencies and allow large-sized pixels to still have good demodulation capabilities, but at the same time, they are more sensitive to p-well mask position. This article does not discuss the effect of the pixel shape. Pixels with the same epi resistivity may have unknown effects due to different pixel shapes, so this article only discusses TCAD 2D simulation. The simulations in this article are all conducted with 850nm wavelength NIR light.

II. DEVICE AND PERFORMANCE METRICS

A. DEVICE FOR SIMULATION

The structure proposed in [20] is used for simulation. As shown in Fig. 2, this structure contains a PPD as a photosensitive area and two FDs located symmetrically on both sides of the PPD to collect electrons.

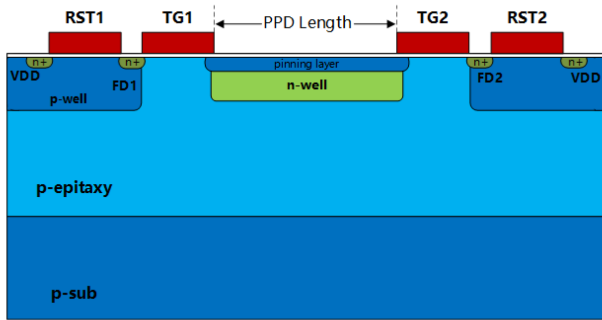


FIGURE 2. Device for simulation, a PPD structure with two floating diffusions.

Generally, the measurement of IToF requires recording the amplitude from four designed phase differences - between the sampling window of the pixel and the emitted light - which are set at 0°, 90°, 180°, 270°. With these four amplitudes and related algorithms, the distance between the pixel and the measured object [21] can be estimated. The advantage of the PPD structure with two FDs used in this article is that it can store charges of two phase difference in one exposure. By irradiating the PPD twice with NIR light, four amplitudes can be recorded, resulting in a higher imaging frame rate. In addition, this structure can suppress background noise.

B. PERFORMANCE METRICS

Demodulation contrast is used as the metric to measure the performance of the pixel in TCAD simulation. The higher the demodulation contrast(DC), the higher speed of charge transfer, the better the pixel's ability to separate charge, and the higher the performance of the pixel. The method in [6] is used to estimate the DC. The potential difference V1 of FD1 and the potential difference V2 of FD2 are respectively used to replace the number of collected electrons of FD1 and FD2, so that DC can be estimated by the (4).

The control of each gate in the simulation is shown in Fig. 3, and the simulation is divided into two phases. The first is the reset phase. RST1 and RST2 are turned on at the same time, and two TGs are also turned on during this time, thereby depleting the electrons in the pixel. After a certain period of time, RST1, RST2, TG1, and TG2 are all turned off, marking the completion of the reset, and the potentials of FD1 and FD2 are recorded as FD1reset and FD2reset, respectively. The second phase is the exposure phase, where the photosensitive area of the pixel will be illuminated by NIR light with a certain frequency simulated by TCAD. At the same time, TG1 and TG2 are respectively controlled to have the same phase as the NIR light and have the opposite phase to the NIR light. The exposure phase ends after a certain integration time, and the potentials of FD1 and FD2 are respectively recorded as FD1expo and FD2expo. The potential difference between FD1reset and FD1expo is V1 in the (4), and V2 is the potential difference between FD2reset and FD2expo.

$$DC = \frac{V_1 - V_2}{V_1 + V_2} \tag{4}$$

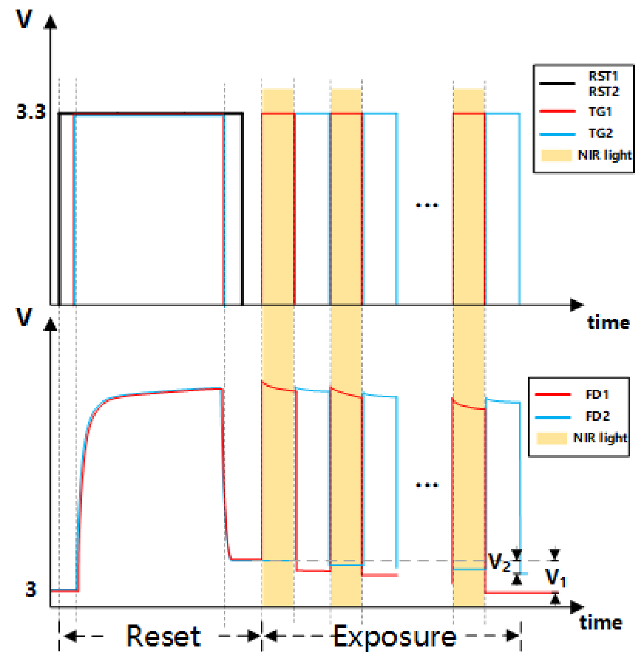


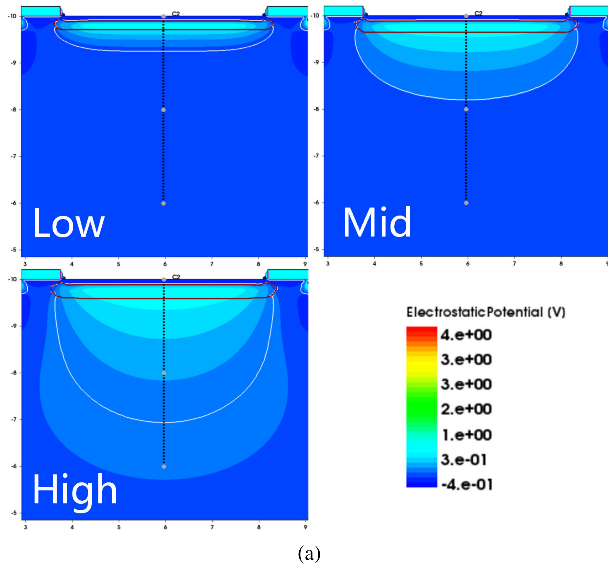
FIGURE 3. The timing diagram of RST and TG, and the waveform of floating diffusions. The yellow phases mean the NIR light is turned on.

III. THE CHARACTERISTICS OF HIGH RESISTIVITY EPITAXIAL WAFER

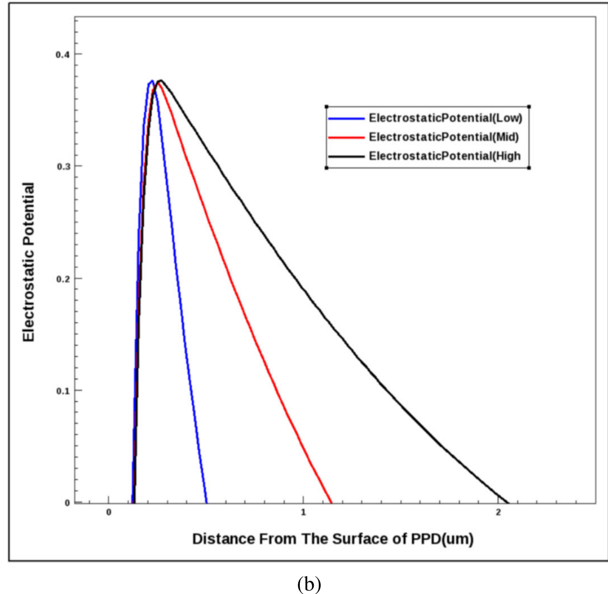
To explore the effect of high resistivity epi wafer, this article will use PPDs with high, mid, and low epi resistivities respectively for simulation. The high resistivity is an order of magnitude larger than the mid resistivity, and the mid resistivity is an order of magnitude larger than the low resistivity. Firstly the performance of the three PPDs will be compared by TCAD simulation. Then, by analyzing the profile of pixels and the potential drop of FDs, the characteristics of collecting charges using pixels with high resistivity epi wafer can be known, and then the cause of their DC differences can be figured out. The simulation in this section will be performed with the condition of 20MHz modulation frequency.

A. PERFORMANCE COMPARISON OF PIXELS WITH THREE DIFFERENT RESISTIVITY EPI WAFER

Fig. 4 shows the potential profile of the three PPDs with different resistivity epi wafer and the 1-D potential profile along the dotted line after reset. The pinning potential of the three PPDs are adjusted to be the same. From the figure, it can be seen that, the PPD depletion region widens as the epi resistivity increases. As mentioned earlier, the large width of the depletion region is conducive to the vertical collection of charges. Simulations with various pinning potential are performed to learn what effect the three resistivity epis will cause on DC at different pinning potentials. The pinning potential can be regulated by adjusting the implantation energy and dose of n-well [22]. Fig. 5 is the relationship between DC and pinning potential of pixels with three different resistivity epis.



(a)



(b)

FIGURE 4. Static electronic potential after reset: (a)the epi resistivity increase from left to right, from top to bottom(Low, Mid, High). The white lines illustrate the edge of the depletion region, and the red lines represent the pn junction (b)1D electronic potential profile of dotted lines in (a).

It can be seen from Fig. 5, when the pinning potential is too high, the high pinning potential of the high epi resistivity pixel leads to a strong negative effect on the lateral collection, and the DC drops rapidly. However, with appropriate pinning potential, the DC increases significantly as the resistivity of epi increases. The reason why using high resistivity epi wafer can improve DC markedly will be figured out from the perspective of photogenerated charges collection.

B. COLLECTION OF PHOTOGENERATED CHARGES

In order to explain the reason for the high DC of pixels with high resistivity epi wafer, the collecting charges process of the three pixels with different epi resistivities are compared. Their pinning potential are the same and adjusted to the 0.4V case showed in Fig. 5. The profile of pixels at several points in the first integration period will be shown. Fig. 6 shows the potential profile, electron density profile, and electron current density profile of the low resistivity and high resistivity pixels at 1, 24, and 49 ns of the first integration period. Based on this, three characteristics of collecting photo-generated charges of PPDs with high resistivity epi wafer can be known.

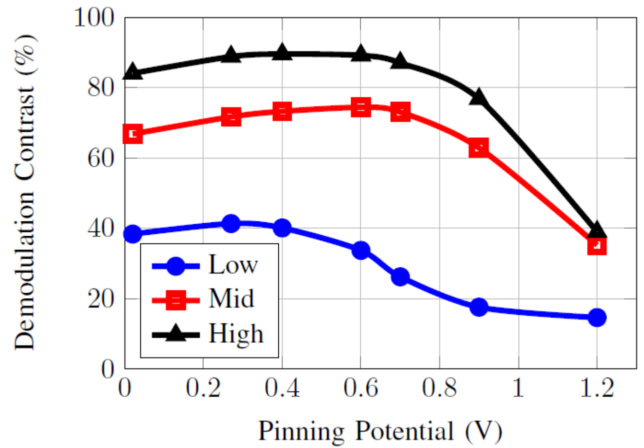


FIGURE 5. Simulated demodulation contrast with various pinning potential.

WIDE COLLECTION RANGE

In the case of using NIR light, a large number of photogenerated charges will be distributed at high depth in the epi, which makes them difficult to collect. However, Fig. 6 shows the wide and approximately elliptical depletion region of the high resistivity PPD, which gives it a wider collection range in the epi. As shown in Fig. 6a and Fig. 6b, when the FD1 collects electrons, the PPD with the high resistivity epi wafer allows photogenerated charges diffuse into the drift electric field from higher depth in the epi. In addition, the shape of its depletion region makes less photogenerated charges diffuse into non-photosensitive areas such as TG and RST, thereby allowing more charges to be collected into the n-well.

In contrast, the PPD depletion region of the low resistivity epi is narrow and the collection range is small, so that at 24 ns, there are still a lot of electrons that are difficult to collect deep in the epi, and more electrons diffuse into the non-photosensitive area, as shown in Fig. 6b. This also means that pixels with low resistivity epi wafer will leave out more photogenerated electrons that can be collected by FD2.

In addition, due to the wider collection range, as shown in Fig. 6c, pixels with high resistivity epi wafer can collect more photogenerated charges. In fact, the high epi resistivity pixel almost depletes the photogenerated charges at about 35 ns, while the low epi resistivity pixel still left many photogenerated charges at 49 ns.

SHORT LATERAL CHARGE TRANSFER DISTANCE

Without the staircase doping profile, the lateral electric field in the n-well would be weak, resulting in a low charge transfer

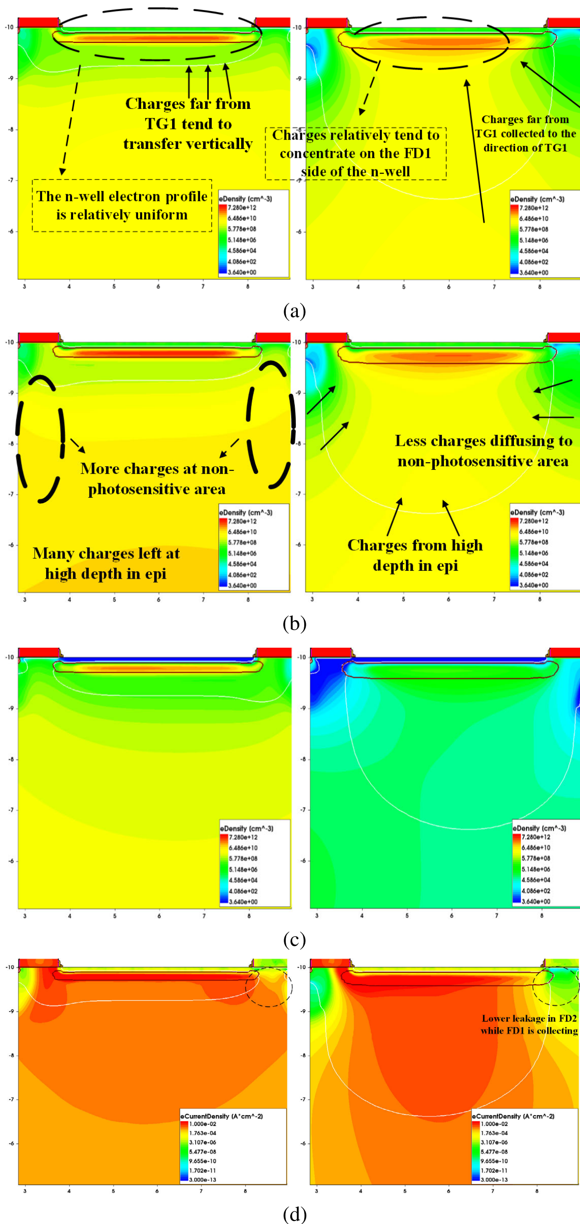


FIGURE 6. The PPDs with low epi resistivity are in the left column, and with high epi resistivity are in the right column: (a)-(c)electron density at 1, 24 and 49 ns. (d)electron current density at 24 ns.

speed, so that after the FD1 collection is completed, there are still many charges remaining in the n-well and collected by the FD2. This is one of the main reasons that hinder the performance improvement of PPD devices, and the characteristics of high resistivity epi wafer can solve this problem to a certain extent.

Fig. 6a and Fig. 6d respectively show the electron density of the two at 1 ns and the n-well electron current density of them at 24 ns. It can be found that, due to the wide and elliptical depletion region of the pixel with high resistivity epi wafer, the photogenerated charges far from TG1 are collected to the direction of TG1 from the high depth of the epi. This makes the charges in the high resistivity epi relatively tend to concentrate on the FD1 side of the n-well compared to charges in the low resistivity epi, reducing the lateral transfer distance in the n-well.

The n-well electron profile of the low epi resistivity pixel is relatively uniform, because the depletion region of the low epi resistivity pixel is narrow, and its shape makes the charges far from TG1 tend to transfer vertically before approaching the n-well. This results in relatively more electrons on FD2 side of the n-well; that is to say, compared with high resistivity epi wafer, some electrons in the n-well with low resistivity epi wafer will have a longer lateral transfer distance and cannot be collected by FD1, so that FD2 collects more electrons than high epi resistivity pixel's FD2 do.

LOW LEAKAGE

Leakage in FD2, while FD1 is collecting charges, is another reason for the low DC of low epi resistivity pixel. The shape of the high epi resistivity PPD depletion region makes the photogenerated electrons at the closed TG (TG2 in FD1 collection and TG1 in FD2 collection) more easily collected into the n-well. In Fig. 6b and Fig. 6d, at the closed TG, both the electron density and the electron current density of the high epi resistivity pixel are relatively low, indicating the leakage of the high epi resistivity pixel is lower. When the pixel with low resistivity epi wafer is in the exposed phase, although the TG is closed, the leakage makes its FDs collect a certain number of charges, resulting in a slight decrease in DC. But this factor has relatively little effect on DC.

To visualize how they collect charges, simulations are performed to show the potential drop of FD1 and FD2 during the first integration period, and Fig. 7 gives the simulation results which is in accordance with our above description about the collection of charges of PPD pixels with different epi resistivities. It can be seen from Fig. 7, from 0 to 25 ns, for the pixel with high resistivity epi wafer, the rate of potential drop is higher than the other two for the better collection ability of the high epi resistivity pixel, and the FD2 potential drop of the low epi resistivity pixel is the highest among all for the more leakage of the low epi resistivity pixel, with the TG1 turned on. From 25 to 50 ns, when the TG2 is turned on, the electrons left in the n-well of the high epi resistivity pixel is much less than that of the other two pixels and are nearly depleted at about 35 ns, so that the potential drop is low and remain almost unchanged after 35 ns.

IV. INFLUENCE OF USING HIGH RESISTIVITY EPITAXIAL WAFER

A. CROSSTALK

NIR light can be beamed into the depth of a silicon epi wafer. Generally, the absorption range of NIR light by silicon epi wafer is much larger than the depletion width. This makes the photo-generated charges deep in the epi easily diffuse to neighboring pixels, causing crosstalk. Especially when the epi is thick, the crosstalk will be more serious. The use of

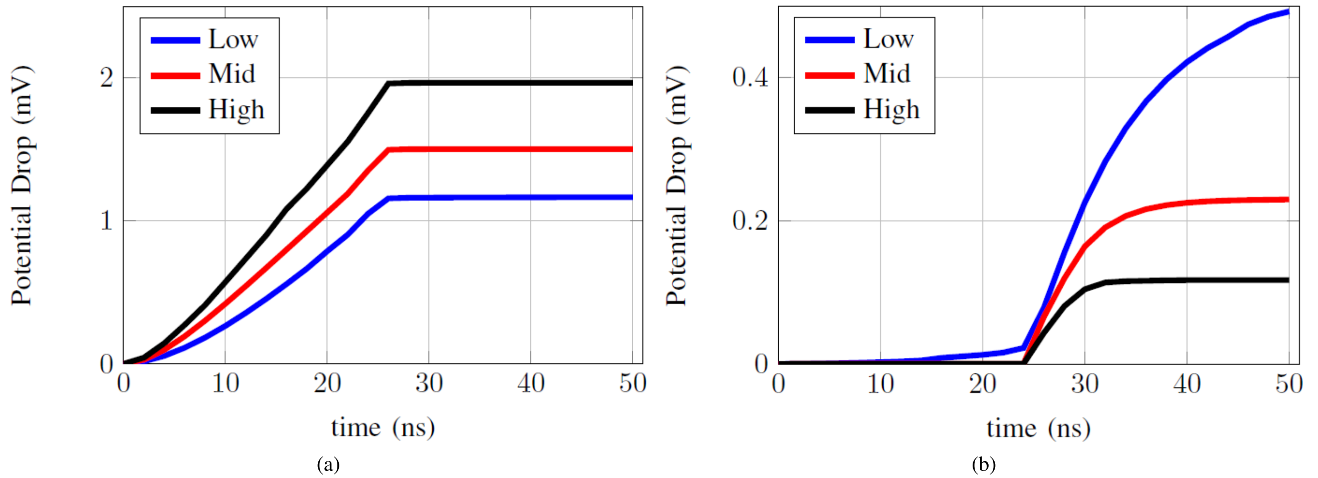


FIGURE 7. The potential drop of FD output voltages during the first integration period: (a)FD1 potential drop. (b)FD2 potential drop.

high resistivity epi wafer can solve this problem to a certain extent.

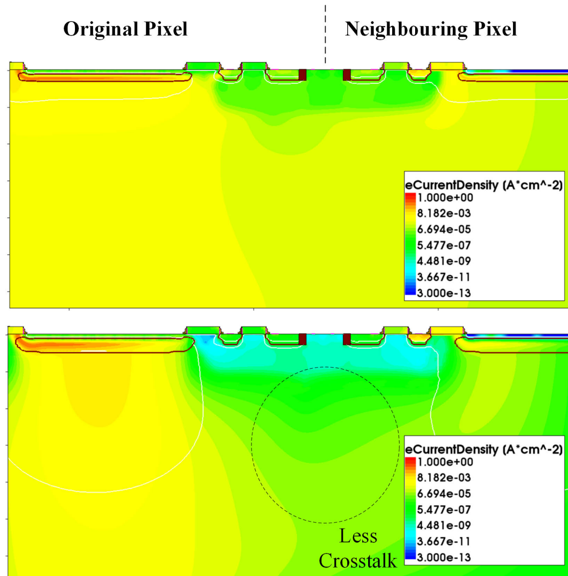


FIGURE 8. Electron current density profile of crosstalk simulation. The upper and the lower are PPDs with low epi resistivity and high epi resistivity respectively.

A neighboring pixel is added based on the simulation in Section III, and the NIR light only illuminates the original pixel. Fig. 8 shows the electron current density profile of two pairs of neighboring pixels using high resistivity epi wafer and low resistivity epi wafer at the 24th ns in an integration period. It can be seen that a pixel with low epi resistivity results in the large number of electrons transferred to the neighboring pixels, and the electron current density in the neighboring pixels is high. From the discussion in Section III, the pixels with high epi resistivity have a wider collection range. It can collect the photo-generated charges at high depth in the epi and prevent the charges from diffusing

TABLE 1. Simulation results of the ratio of photogenerated electrons collected by neighboring pixels.

Epi Resistivity	Crosstalk Ratio	DC
Low	25.4%	46.1%
Mid	13.9%	76.6%
High	3.0%	87.6%

into the non-photosensitive area, so that the crosstalk can be reduced. Table 1 shows the effect of different epi resistivity on crosstalk performance. The crosstalk performance is estimated by the ratio of the potential difference caused by the electrons collected by the neighboring pixel to the total potential difference.

It can be seen from the simulation results in Table 1 that the use of the high resistivity epi wafer greatly reduces the crosstalk ratio. That is to say, the high resistivity epi wafer can equip the pixels with a higher demodulation capability and significantly improves the pixel crosstalk performance at the same time.

B. P-WELL MASK POSITION

In Fig. 2, the high concentration of p-well that isolates FD and epi can effectively control the width of the depletion region of FD and PPD, and is usually used to prevent leakage of PPD devices [24]. According to the [3], the potential profile in a pixel is sensitive to the p-well position. The distance between p-well and PPD affects the potential profile at the channel and PPD, which may cause a potential barrier on the transfer path of charges. The simulation result in this article shows that this phenomenon will be more obvious due to the increase in the epi resistivity.

From the simulation results shown in Fig. 9, it can be known that when the position of the p-well mask is closer to the n-well, the electron transmission path between n-well and FD is prone to generate a potential barrier, resulting in lower DC. When the position of p-well is moved away from n-well,

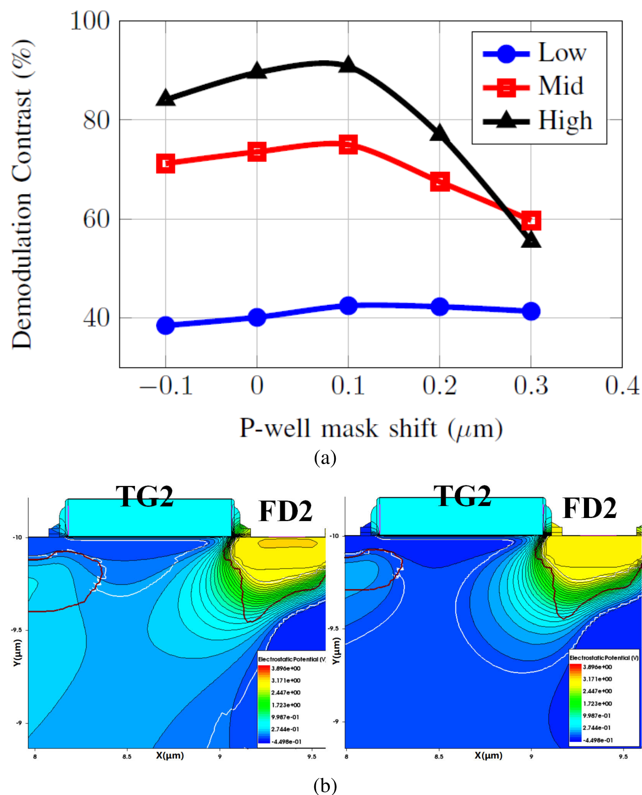


FIGURE 9. (a)Simulated DC with various P-well mask position. the negative x direction means moving toward the n-well, while the positive x direction means moving away from the n-well. (b)Electronic potential profile of FD2 while TG2 closed. The left and the right are PPDs with high epi resistivity and low epi resistivity respectively.

the potential barrier gradually disappears, causing a higher lateral transfer speed, which improves DC. However, when the position of p-well is further away from n-well, the leakage at FDs become serious, so that even when TG is turned off, FDs still collect a large number of electrons from epi, which makes DC drop.

When the p-well mask moves away from the n-well by the same position, both the PPD and FD depletion regions of high epi resistivity PPD become much wider compared with the low resistivity epi wafer, making the leakage more serious. When p-well mask is moved away from n-well by 0.3 μm, the PPD and FD depletion regions of high epi resistivity PPD are even connected together, and this phenomenon does not occur in low epi resistivity pixel, as shown in Fig. 9b. This leads to a significant drop in DC of high epi resistivity PPD pixel, while the DC of low epi resistivity PPD pixel hardly changes with the position move of the p-well mask, as shown in Fig. 9a.

C. MODULATION FREQUENCY

The demodulation frequency and accuracy are positively correlated [23]. In some specific applications, higher recognition accuracy is needed, which requires a higher modulation frequency. But a higher modulation frequency means a shorter collection time, and more charges cannot be collected by

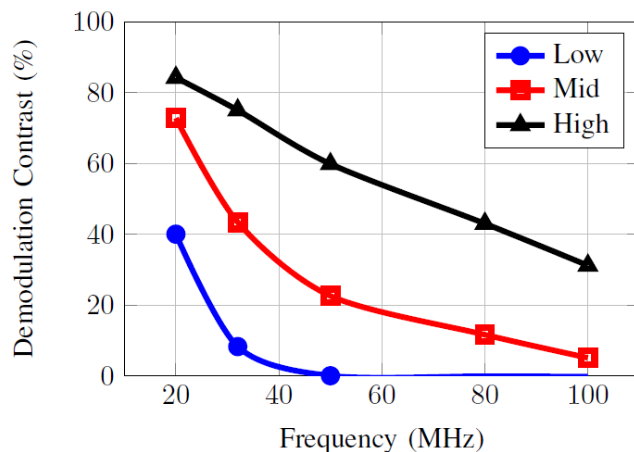


FIGURE 10. Simulated demodulation contrast with various modulation frequencies.

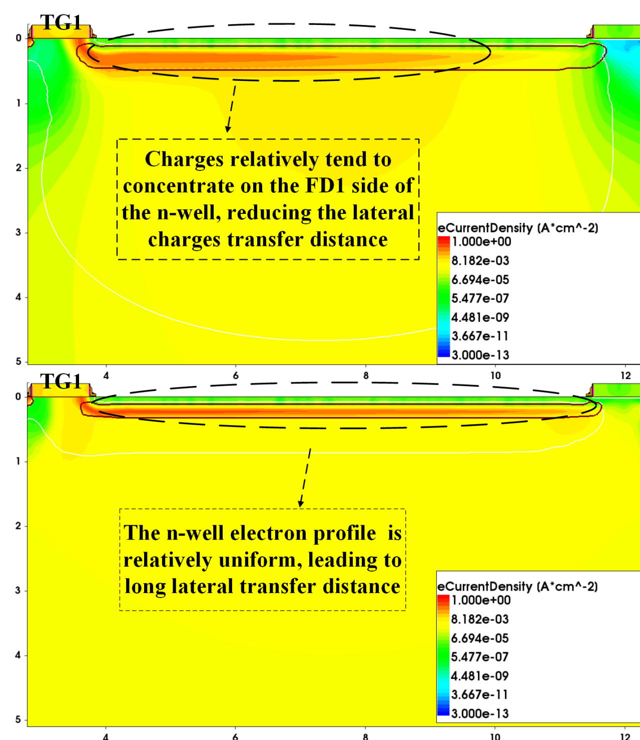


FIGURE 11. Electron current density profile with a PPD length of 7μm. The upper and the lower are PPDs with high epi resistivity and low epi resistivity respectively.

FD1 and thus FD2, resulting in a decrease of DC. One of the benefits of using a high resistivity epi wafer is that pixels can operate with higher modulation frequencies.

Fig. 10 shows that with the increase of the modulation frequency, the rate of DC drop increases with the decrease in epi resistivity, which means the DC of the pixel with low epi resistivity decreases the most drastically. The pixels with low epi resistivity can hardly work at 50MHz since its DC is only about 10%. The DC of the pixel with mid epi resistivity drops rapidly from above 70% to below 40%, while the DC of

pixels with high epi resistivity still remains at more than 60%. Even with the modulation frequency of 80MHz, the DC of the pixel with high epi resistivity is still close to 50%.

D. PPD LENGTH

In a 2D simulation, the pixel size can be adjusted by changing the PPD length in Fig. 2. A longer PPD means a larger light-sensing area, which helps increase quantum efficiency. However, an excessively long PPD will cause a long region of slow lateral charge transfer in the n-well. According to the analysis in section III, high resistivity epi wafer is beneficial to reduce the lateral charges transfer distance in n-well, as shown in Fig. 11. Therefore, the use of high resistivity epi wafer can overcome the slow lateral transfer of long PPD length to a certain extent, and at the same time, can achieve a higher quantum efficiency.

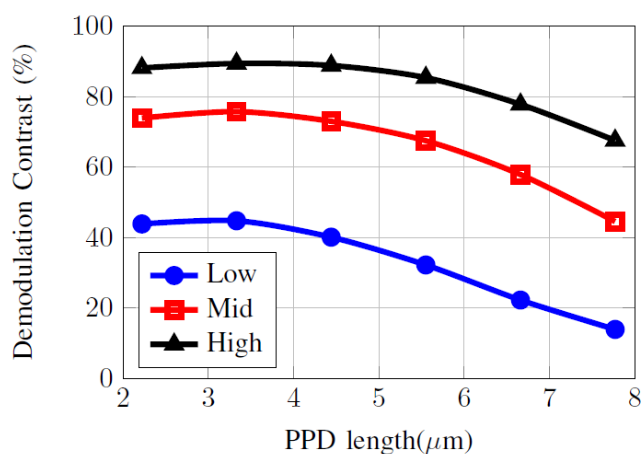


FIGURE 12. Simulated DC with various PPD length.

As shown in Fig. 12, all three have a slight DC decrease when the PPD length is short, which is consistent with the description in [3]. In this case, due to the short horizontal transfer distance, the vertical transfer dominates the collection of charges. With the increase of the PPD length, the high epi resistivity pixel has a slightly lower DC drop rate than the mid and low epi resistivity pixels.

V. CONCLUSION

We compared silicon-based PPD pixels with three different epi resistivities by 2D TCAD simulation at 850nm near-infrared wavelength. The high demodulation contrast of the high epi resistivity PPD pixel is mainly due to its relatively wide depletion region. The wide depletion region allows a wider range of photogenerated charges to be collected and prevents photogenerated charges from diffusing to non-photosensitive areas. And the shape of the wide depletion region is also beneficial to the reduction of the lateral transfer distance of charges in the n-well. At the same time, a wide depletion region can also reduce leakage. These characteristics of high epi resistivity PPD pixels enable it to reduce crosstalk, to work at higher modulation frequencies, and to allow larger pixels to operate. However, using high resistivity epi wafer also makes the pixel more sensitive to the position of the p-well mask. Although high resistivity epi wafer greatly improves the performance of the pixel, the excessive epi resistivity may have an unpredictable effect on the peripheral analog circuits of the pixel. Therefore, the selection of the epi resistivity ought to be weighted to consider the above all factors.

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