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3D EXIT Charts for Analyzing the 5G 3GPP New Radio LDPC Decoder

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ABSTRACT Low Density Parity Check (LDPC) codes have been selected to provide channel coding for data in the next generation of wireless communication standard referred to in practice as the 3GPP New Radio (NR). In contrast to the LDPC codes adopted in previous standards, the NR LDPC code can be considered to be a concatenation of a core LDPC code and a Low Density Generator Matrix (LDGM) code. This particular feature has the advantage of offering flexible coding rate, but it prevents the application of conventional extrinsic information transfer (EXIT) chart analysis. This article characterizes this problem and addresses it using a novel reinterpretation of the NR LDPC factor graph. Based on this factor graph, a novel 3D EXIT chart technique is conceived for our three-stage scheme, which facilitates the visual characterisation of the NR LDPC decoder's iterative decoding convergence process for the first time. The proposed EXIT chart analysis accurately visualizes the mutual information exchange amongst the components of the NR LDPC decoder, which was not facilitated by the conventional 2D EXIT chart. We demonstrate the power of this technique by using it to design a novel iterative decoding activation order for the NR LDPC decoder, which reduces the decoding complexity by approximately 17% compared to a conventional flooding decoder. This is achieved without degrading its error correction capability. We conclude by discussing several other opportunities for exploiting the proposed 3D EXIT chart technique to improve the design of concatenated LDPC and LDGM codes.

INDEX TERMS NR LDPC code, EXIT chart analysis, NR LDPC decoder design.

I. INTRODUCTION

Channel coding is a fundamental element in modern wireless communication system, since it facilitates an infinitesimally low Bit Error Ratio (BER) at near-capacity spectral and/or power efficiencies. In the 3GPP New Radio (NR) standard of Fifth Generation (5G) wireless communication [1], Low Density Parity Check (LDPC) codes have been adopted for protecting the data channel. Although LDPC codes are mature, the NR LDPC code adopts a refined structure that is significantly different from those of previous standards. In general, an LDPC code can be uniquely specified by its Parity Check Matrix (PCM) [2], defining its encoder and decoder. More specifically, the NR LDPC code can be considered to be a concatenation of a core LDPC code and an extension Low Density Generator Matrix (LDGM)

based code. Correspondingly, the PCM of the NR LDPC code is comprised of two parts, including a core LDPC part and an LDGM based extension [3]. This LDGM part can be punctured in order to provide rate-flexibility and an Incremental Redundancy Hybrid ARQ (IR-HARQ) capability. However, in order to support puncturing, the Variable Nodes (VNs) in the LDGM part of the PCM all have a degree of one. In this article, we will demonstrate that the presence of these degree-one variable nodes prevents the application of conventional Extrinsic Information Transfer (EXIT) chart analysis [4] for characterising the iterative decoding convergence of the NR LDPC code. It also prevents the use of EXIT charts as a powerful tool of characterising the capacity-approaching capability [5] of the NR LDPC code, or for designing the iterative decoding activation order [6] or the control of early termination strategies [7], for example.

Against this background, this article introduces several novel techniques as listed below.

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TABLE 1. Knowledge-gap analysis and our novel contributions contrasted to the existing literature.

	[10]	[11]	[3]	[12]	[13]	[14]	[15]	[16], [17]	Proposed
Conventional LDPC design	✓	✓	✓	✓	✓	✓	✓	✓	✓
NR LDPC Analysis			✓		✓	✓	✓	✓	✓
Factor graph rearrangement of NR LDPC									✓
Conventional EXIT analysis	✓	✓		✓		✓			✓
3D EXIT charts									✓
2D EXIT chart projection							✓		✓
EXIT based LDPC code design		✓		✓					✓
EXIT based NR LDPC decoding schedule					✓	✓	✓	✓	✓

- 1) In order to fix the failure of conventional EXIT chart analysis for the NR LDPC code, we propose a novel reinterpretation of its factor graph that is more suitable for EXIT chart analysis. In the new factor graph, the core and extension VNs and Check Nodes (CNs) are separated into two groups that are connected by the corresponding edges, which can be adapted with a change of coding rate.
- 2) Based on this factor graph, a novel pair of more detailed 3D EXIT charts are produced by treating the LDPC and LDGM parts of the PCM separately. We show that these 3D EXIT charts correctly visualize the iterative convergence of the NR LDPC decoder.
- 3) Following this, we propose a more accurate 2D EXIT chart, which is obtained using a projection of 3D EXIT chart. By using this 2D EXIT projection, not only is the EXIT tunnel state more straight-forward to observe, but also more EXIT chart properties can be investigated, such as the area underneath the curve and the distance from the channel capacity [8].
- 4) In order to demonstrate the capability offered by our novel EXIT chart analysis, we show that by using the most appropriate decoding component activation order, our scheme imposes a lower complexity than a conventional LDPC decoder based on a flooding schedule. More specifically, the proposed decoder activation order exploits the unique insight provided by our EXIT chart analysis that the Mutual Information (MI) [9] in the LDGM part of the 3GPP NR LDPC decoder will converge promptly after a few iterations, with any further iterative decoding actions within the LDGM part becoming redundant. Motivated by this, the proposed NR LDPC decoder is specifically designed to only activate the LDPC part of the PCM during the later decoding iterations.

In Table 1 we provide the associated knowledge-gap analysis and contrast our novel contribution to the existing literature at a glance.

The rest of this article is structured as follows. In Section II, the special features of the NR LDPC code and its design

are detailed with the help of a simplified PCM. A novel reorganized factor graph is also conceived for the NR LDPC decoder in this section, in order to allow the MI exchange to be illustrated comprehensively. Section III discusses three different types of EXIT charts designed for the NR LDPC decoder, including the conventional 2D EXIT chart analysis of Section III-A, our novel 3D EXIT chart analysis of Section III-B and our novel 2D EXIT chart projection of Section III-C. Note that all of these subsections rely on block diagrams and simulation results, which consider the effect of changing the LDPC coding rate using puncturing and repetition. According to the EXIT chart analysis of the former sections, Section IV introduces the proposed LDPC decoder. The performance of this decoder is characterised using Block Error Rate (BLER) simulation results that are compared to those of a conventional flooding-based LDPC decoder in both Additive White Gaussian Noise (AWGN) and uncorrelated Rayleigh fading transmission environments. We show that the proposed decoder has approximately 17% complexity reduction compared to the conventional flooding-based LDPC decoder. Finally, Section V will summarise this article and give suggestions for further investigations according to the proposed EXIT chart based technique.

II. NEW RADIO LDPC CODE DESIGN

The NR LDPC is specified using a pair of BGs, 51 lifting factors Z_c having values of up to 384, and eight sets of circulants [1], which facilitate the support of a wide variety of different combinations of block lengths K' and coding rates R . Each BG is a binary matrix of 0s and 1s that governs the formation of the PCM used at runtime during LDPC encoding or decoding. The two BGs of NR LDPC namely BG1 and BG2, are comprised of four sub-matrices, namely the LDPC matrix, the LDGM matrix, an identity matrix and a zero matrix [3], where Fig. 1 presents a simplified version of BG2 accordingly. As shown in Fig. 1, BG2 has $N_c \leq 42$ rows and $N_v \leq 52$ columns, depending on the coding rate R selected at run-time, as it will be detailed below. The LDPC sub-matrix comprises the first $N_{cc} = 4$ rows and the first $N_{vc} = 14$ columns of BG2. Below the LDPC matrix

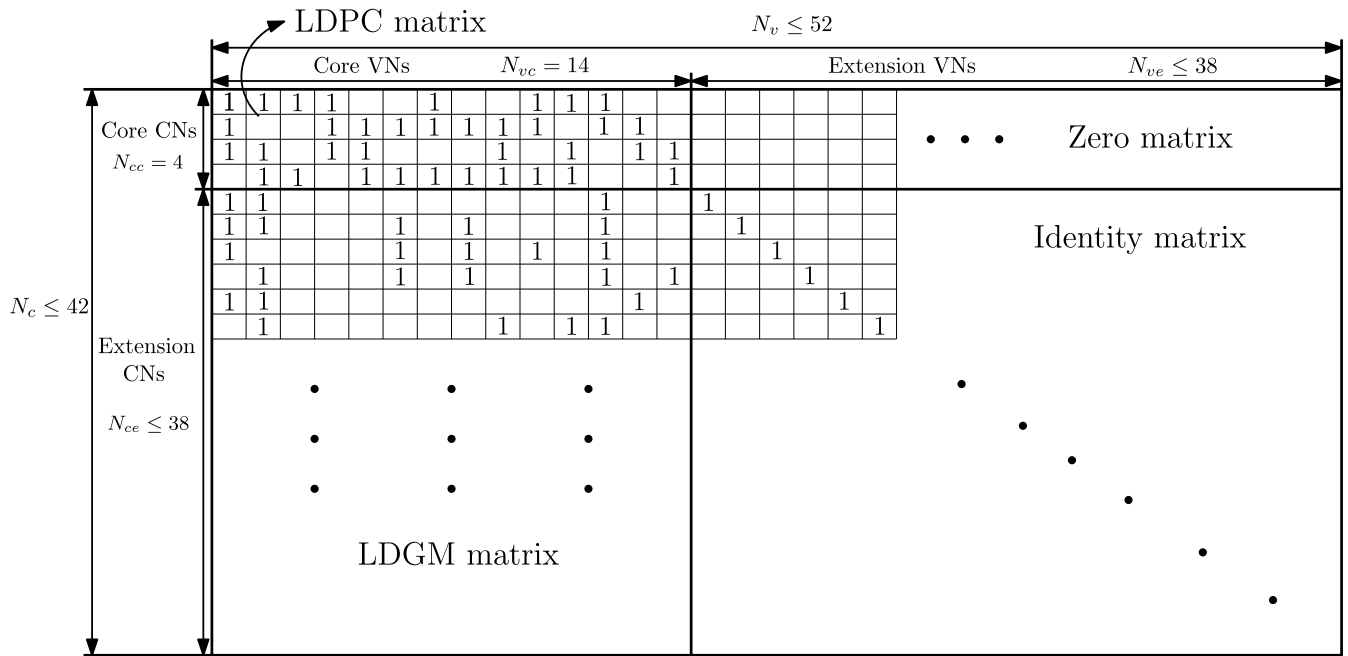


FIGURE 1. Structure of BG2 of 5G NR LDPC code. Note that for BG 1 $N_{vc} = 26$, $N_{ve} \leq 42$, $N_{cc} = 4$, $N_{ce} \leq 42$, $N_c \leq 42$ and $N_v \leq 68$ in the absence of puncturing.

we portray the LDGM matrix, which has $N_{ce} \leq 38$ rows and $N_{vc} = 14$ columns, depending on the coding rate R . Compared to the LDPC sub-matrix, it may be observed that the LDGM sub-matrix has a much sparser distribution of binary values of 1. To the right of the LDPC matrix is a zero matrix, which has all values set to zero and comprises $N_{cc} = 4$ rows as well as $N_{ve} \leq 38$ columns. To the right of the LDGM matrix is an identity matrix, having $N_{ve} \leq 38$ rows and the same number of $N_{ce} \leq 38$ columns. By contrast, BG1 comprises $N_c \leq 46$ rows and $N_v \leq 68$ columns, which has different parameters that are decomposed as $N_{vc} = 26$, $N_{ve} \leq 42$, $N_{cc} \leq 4$ and $N_{ce} \leq 42$.

As mentioned above, the NR LDPC code has a design that supports a flexible coding rate R for supporting adaptive coding and modulation in the face of time-varying channel conditions. More specifically, rate matching is achieved using puncturing in a manner that changes the BG shown in Fig. 1. To elaborate further, the coding rate $R = K/(N_v - 2)$ is related both to the number of information bits, which is proportional to the number of systematic columns $K = N_v - N_c$, and to the number of encoded bits, which is proportional to $N_v - 2$. Here, the subtraction of 2 is employed since the first two columns of the BG are always punctured for attaining an improved performance [3], regardless of the desired coding rate R . Additional puncturing may also be used for removing a number of extension columns, and an equal number of extension rows that share binary 1 values with these columns in the identity matrix. In this way, N_v may be reduced below 68 in the case of BG1 and below 52 in the case of BG2, hence increasing the coding rate $R = K/(N_v - 2)$.

In order to illustrate the MI exchange in the NR LDPC decoder more comprehensively, this article introduces a novel re-interpretation of the factor graph, as shown in Fig. 2 for the example of BG2. In contrast to the conventional factor graph of an LDPC decoder comprising one group of VNs and CNs [18], Fig. 2 arranges the VNs and CNs into four groups, namely core VNs, core CNs, extension VNs and extension CNs. More specifically, the $N_{vc} = 14$ VNs included in the LDPC and LDGM matrices of BG2 comprise the core VNs, while the $N_{cc} = 4$ CNs considered by the LDPC and zero matrices comprise the core CNs. Hence, the remaining $N_{ve} \leq 38$ VNs starting from column 15 are the extension VNs, while the $N_{ce} \leq 38$ CNs starting from row 5 are extension CNs, as shown in Fig. 1. In total, there are $N_v \leq 52$ VNs and $N_c \leq 42$ CNs, in correspondence with the number of columns and rows in BG2, as described above. By considering the effect of puncturing as mentioned above, the number of extension VNs and CNs will be reduced by the application of rate-matching. In the rearranged factor graph of Fig. 2, the $N_{cc} = 4$ core CNs are positioned at the left-hand side, since they are only connected to the core VNs. By contrast, the $N_{ce} \leq 38$ extension CNs are placed on the right-hand side, where they are connected not only to the core VNs, but also to a single corresponding extension VN each. Finally, the core VNs are positioned in the middle, where they are connected to both sides. In all cases, the edges between the VNs and CNs correspond to the ones shown in Fig. 1. For example, the 1 in the top 1 left element of Fig. 1 indicates that V_{c1} and C_{c1} are connected, as shown in Fig. 2 as well. Additionally, the number of connections spanning from a CN

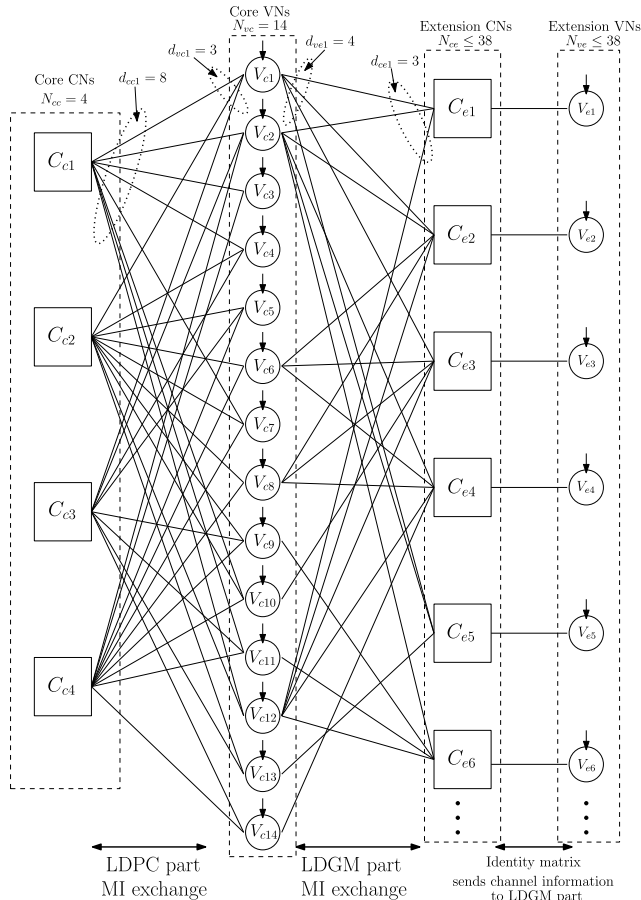


FIGURE 2. The factor graph of Base Graph 2 in the case where the number of extension nodes is $N_{Ve} = 6$.

to the VNs or vice versa is referred to as the degree of the respective node, as shown for some examples in Fig. 2. For instance, there are 8 different VNs connected to C_{c1} , which therefore has a degree of $d_{cc1} = 8$.

With the aid of the BG and factor graph introduced above, the PCM of a NR LDPC decoder can be directly constructed. Generally speaking, the PCM is a “lifted” version of the BG exemplified in Fig. 1, which expands it to support long information block lengths. As mentioned above, the NR LDPC supports 51 different values for the lifting factor Z_c having values of up to 384. Furthermore, the number of information bits is given by $K = 22 \times Z_c$ for BG1 and $K = 10 \times Z_c$ for BG2. In order to obtain the PCM, the BG exemplified in Fig. 1 is enlarged by a factor of Z_c , by transforming each 1-valued element in Fig. 1 into a $Z_c \times Z_c$ rotated identity matrix. Here, the particular rotation applied for each 1-valued element of the BG is selected depending on the value of the lifting factor Z_c . A similar effect may be observed in the factor graph exemplified in Fig. 2. More specifically, each VN and CN in the BG factor graph corresponds to a set of Z_c VNs or CNs in the PCM factor graph. Furthermore, each edge in the BG factor graph corresponds to a set of Z_c edges in the PCM factor graph, where the corresponding rotation

dictates, which of the Z_c VNs is connected to which of the Z_c CNs.

III. EXIT CHART ANALYSIS OF THE NR LDPC CODE

In this section, several different forms of EXIT chart analysis are applied to the NR LDPC decoder. Section III-A characterises the conventional two-dimensional EXIT analysis of the NR LDPC decoder, where we detail why the MI exchange is not characterised correctly. Motivated by this, Section III-B will present the proposed three-dimensional EXIT chart analysis based on the novel factor graph representation of Fig. 2. For the sake of convenience, we introduce a novel 2D projection of our 3D EXIT chart in Section III-C, which gives more direct visualization of the EXIT chart tunnel opening, without a complex combination of 3D surfaces. In particular, we show that this projection solves the MI exchange deficiency we observed in the conventional 2D EXIT chart analysis.

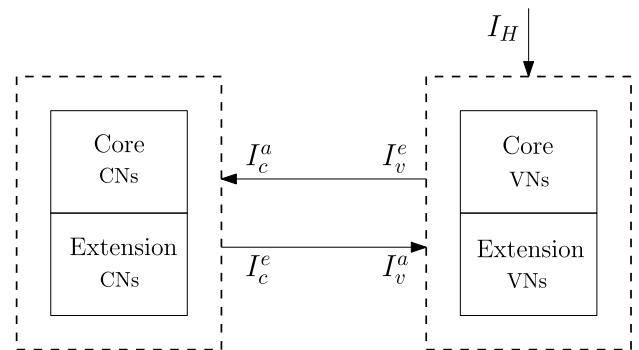


FIGURE 3. The block diagram of NR LDPC decoder relying on the conventional structure for analysis using 2D EXIT charts.

A. CONVENTIONAL TWO-DIMENSIONAL EXIT ANALYSIS

As discussed in Section II, the NR LDPC code has a structure which is different from that of a conventional LDPC code. Motivated by these unique characteristics of the NR LDPC code, we rearranged the factor graph into the novel form presented in Fig. 2. However, in the conventional view of LDPC decoding and EXIT chart analysis, the core and extension VN decoders should be considered as a single integrated variable node decoder (VND). Likewise, the core and extension CN decoders are conventionally considered as a single integrated check node decoder (CND). More specifically, a block diagram of the conventional view of an LDPC decoder used for EXIT chart analysis is shown in Fig. 3, in which the MI is exchanged between the integrated CN and VN decoders. Here, the information passed from the VNs to the CNs is characterised by the MI I_v^e and regarded as the *extrinsic* information provided by the VN decoder of Fig 3, which is characterised by the MI I_c^a and becomes the *a priori* information entered into the CN decoder of Fig 3. Similarly, the information passed from the CNs to the VNs is characterised by the MI I_c^e and considered as the *extrinsic* information generated by the CN decoder, which is characterised by the MI I_v^a and regarded as the *a priori* information provided for

the VN decoder. Additionally, the VN decoder receives the channel's output information, which is characterised by MI I_H and remains constant throughout the decoding iterations.

The conventional 2D EXIT chart, may be drawn using the semi-analytic method of [4], where the equations may be adjusted for adopting our notation for the NR LDPC code, as presented in (1) and (2) below:

$$I_v^e(I_v^a, I_H) = \sum_{i=1}^{N_{vc}+N_{ve}} \frac{J\left(\sqrt{(d_{vci} + d_{vei} - 1)[J^{-1}(I_v^a)]^2 + [J^{-1}(I_H)]^2}\right)}{(d_{vci} + d_{vei})^{-1} \cdot \sum_{i=1}^{N_{vc}+N_{ve}} (d_{vci} + d_{vei})} \quad (1)$$

$$I_c^e(I_c^a) = \sum_{i=1}^{N_{cc}+N_{ce}} \frac{\left(1 - J\left(\sqrt{d_{cci} + d_{cei} - 1} \cdot J^{-1}(1 - I_c^a)\right)\right)}{(d_{cci} + d_{cei})^{-1} \cdot \sum_{i=1}^{N_{cc}+N_{ce}} (d_{cci} + d_{cei})} \quad (2)$$

For convenience, we summarise our notation in Table 2. Note that the analysis of [4] assumes a flooding-based decoder activation order [2] and the employment of the sum-product decoding algorithm [19]. Here, (1) evaluates the average *extrinsic* MI I_v^e generated by the VN decoder as a function of the *a priori* MI I_v^a provided for the VN decoder and the channel's output MI I_H , where $J(\cdot)$ and $J^{-1}(\cdot)$ are empirical functions, as characterised in the Appendix of [4]. In order to support the irregular construction of the NR LDPC PCM, (1) considers the degree distribution of different VNs.

TABLE 2. Table of notations and corresponding definition in Equation (1) and (2).

Notation	Definition
N_{vc}/N_{ve}	Number of VNs in core/extension part
N_{cc}/N_{ce}	Number of CNs in core/extension part
d_{vci}/d_{vei}	Degree of i th core/extension VN
d_{cci}/d_{cei}	Degree of i th core/extension CN
I_v^a/I_v^e	The <i>a priori</i> / <i>extrinsic</i> MI of VN decoder
I_c^a/I_c^e	The <i>a priori</i> / <i>extrinsic</i> MI of CN decoder
I_H	The MI of channel information

Likewise, (2) computes the average *extrinsic* MI I_c^e generated by the CN decoder as a function of both the *a priori* MI I_c^a that entered into the CN decoder and of the degrees of the various CNs.

Fig. 4 presents four different conventional 2D EXIT charts obtained using (1) and (2), where I_v^a and I_c^e are presented on the x-axis, while I_v^e and I_c^a are scaled on the y-axis, since the output of the CND becomes the input of the VND and vice versa during iterative decoding. Fig. 4 characterises the NR LDPC code having a coding rate of $R = 1/3$ and a block length of $K' = 3000$. Here, Fig. 4 (a) and (c) adopt BG 1, but different channel Signal-to-Noise Ratios (SNRs) of -1 dB and -3 dB. Likewise, Fig. 4 (b) and (d) adopt BG 2 and the same pair of channel SNRs. This is motivated by the fact that an SNR of -1 dB is sufficient for a $1/3$ coding rate NR LDPC

decoder to reach a BLER of 10^{-4} , while the BLER for the same decoder at -3 dB is close to 1.

In each EXIT chart of Fig 4, there are two crossing curves, each of which exclusively depends on the operation of the respective VN or CN decoders according to the EXIT function of (1) and (2), respectively. In the process of iterative LDPC decoding using a conventional flooding schedule, Logarithmic Likelihood Ratios (LLRs) are exchanged between the CN and VN decoders, as may be characterized by measuring the MIs I_v^a/I_c^e and I_v^e/I_c^a after each operation of the VND and CND. These measurements may be plotted as a stair-shaped line termed as a trajectory [20] between the VND and CND curves of Fig. 4. Each successive step in this trajectory characterises the evolution of each successive MI after a single decoding iteration.

Although the strong error-correction performance of the NR LDPC decoder has been confirmed by BLER simulation [3], conventional EXIT chart analysis suggests that the MI exchange in the decoder cannot fully converge to the $(I_c^e, I_v^e) = (1, 1)$ point at the top-right corner of Fig. 4, which is typically assumed to be a prerequisite for achieving an almost infinitesimally low BLER. However, in the case of VNs having a degree of $d_{vci} + d_{vei} = 1$, the numerator of (1) will become equal to I_H , preventing an I_v^e of 1, even when I_v^a has a value of 1. Hence, it is the presence of degree-1 VNs [21] in the NR LDPC code that prevents convergence to the $(1, 1)$ point in the conventional EXIT chart analysis.

It may however be observed that somewhat unexpectedly, the NR LDPC decoder is capable of attaining a low BLER at channel SNRs that are associated with a closed EXIT chart tunnel. The conflict between the BLER simulation results and conventional 2D EXIT chart analysis reveals that a new EXIT chart analysis technique is needed for analysing the MI exchange of the NR LDPC decoder. Motivated by this, we propose a novel technique for the EXIT chart analysis of the NR LDPC decoder, which is discussed in Sections III-B and III-C.

B. PROPOSED THREE-DIMENSIONAL EXIT CHART ANALYSIS

Motivated by the deficiency of the conventional 2D EXIT chart demonstrated in Fig. 4, a more sophisticated EXIT chart technique is proposed in this section for analysing the MI exchange of the NR LDPC decoder. The proposed method is based on the reorganized factor graph of Fig. 2, which is characterised using the block diagram of Fig. 5 for illustrating the MI exchange. Similar to Fig. 2, Fig. 5 is organized by relying on the core CNs, core VNs, extension CNs and extension VNs positioned from left to right. The MI provided for the core CNs is referred to as the *a priori* information (I_{cc}^a) of the core CN, which is provided by the *extrinsic* information forwarded from the core VNs to the core CNs (I_{vc}^e). Similarly, the MI (I_{cc}^e) provided by the core CNs of Fig. 5 is referred to as the *extrinsic* information output of the core CNs, which is entered as the *a priori* information (I_{vc}^a) into the core VNs. Finally, the MI that is received from the channel is termed as I_H .

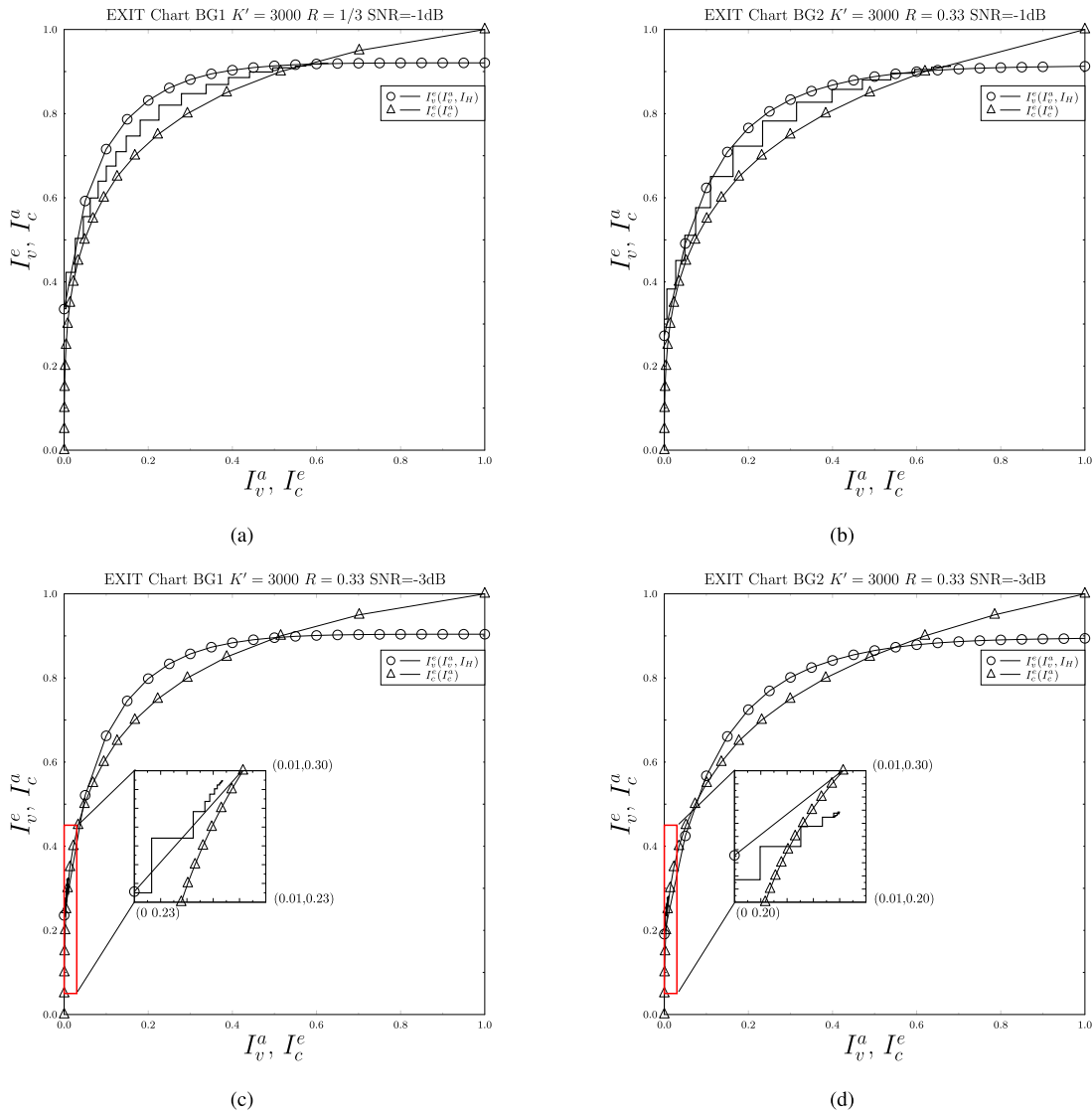


FIGURE 4. Conventional 2D EXIT charts for a $K' = 3000$ bit 5G NR LDPC flooding decoder with $R = 1/3$ and different combinations of SNR and base graph, namely: (a) SNR = -1 and BG 1, (b) SNR = 1 and BG 2, (c) SNR = -3 and BG 1, (d) SNR = -3 and BG 2. Each trajectory is a snapshot obtained during the decoding of a single codeblock.

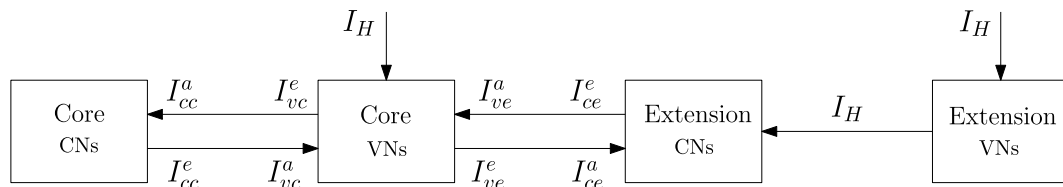


FIGURE 5. The block diagram of NR LDPC decoder with structure according to the factor graph of Fig. 2.

The other MI terms of Fig. 5 adopt a similar terminology to those described above, as summarised in Table 2 and 3. Note that the information exchange between the extension VNs and extension CNs is different from the others, since the extension VNs has a degree of 1. Owing to this, the extension VNs similarly pass on the channel's output information I_H ,

as shown in Fig. 5. Therefore, the MI exchange between the extension VNs and extension CNs would not be improved by iterative decoding.

Similar to the scheme of Fig. 3, the scheme of Fig. 5 may be characterised by Equations (3), (4), (5) and (6), as shown at the bottom of the next page, which are appropriately adapted

TABLE 3. Table of additional notations and corresponding definitions in Equations (3), (4), (5) and (6).

Notation	Definition
I_{vc}^a/I_{vc}^e	The <i>a priori/extrinsic</i> information of core VNs in respect to core CNs
I_{ve}^a/I_{ve}^e	The <i>a priori/extrinsic</i> information of core VNs in respect to extension CNs
I_{cc}^a/I_{cc}^e	The <i>a priori/extrinsic</i> information of core CNs
I_{ce}^a/I_{ce}^e	The <i>a priori/extrinsic</i> information of extension CNs

from [4] to evaluate the *extrinsic* information terms of I_{vc}^e , I_{ve}^e , I_{cc}^e and I_{ce}^e . Note that the activation order of decoding nodes in Fig. 5 is exactly the same as in Fig. 3, which considers the VND and CND as separate blocks. Similar to (1) and (2) related to Fig. 3, these equations characterize the degree distributions of the corresponding blocks in Fig. 5. More specifically, the information transmitted from the extension VNs to extension CNs is regarded as the channel's output information that affects the *extrinsic* information (I_{ce}^e) of the extension CN decoder. Therefore, I_{cc}^e , I_{ce}^e is dependent on the channel SNR, which is quantified by I_H .

According to (3) to (6), in Fig. 2 the core VN decoder has the pair of outputs I_{vc}^e and I_{ve}^e , which are affected not only by I_{vc}^a but also by I_{ve}^a , giving two independent variables and two dependent variables. Hence they cannot be comprehensively characterized by a 2D EXIT chart. Instead, a pair of 3D EXIT charts may be used to visualize the MI exchange of the NR LDPC decoder. Indeed, compared to the conventional 2D EXIT chart, the generation of 3D EXIT charts for the NR LDPC decoder requires more computations for the sake of calculating a pair of independent variables. However, the 3D EXIT chart considers the MI exchange in the decoder more intelligently at the cost of an increased complexity. For example, Fig. 6 presents two pairs of 3D EXIT charts

for an NR LDPC decoder using BG 1 and a coding rate of $R = 1/3$. In Fig. 6 (a) and (b), the channel SNR is -1 dB, while in Fig. 6 (c) and (d), the channel SNR is adjusted to -3 dB. Here, one of the 3D EXIT charts characterises the MI exchange between the core CNs and the core VNs of Fig. 5, which is referred to as the LDPC part MI exchange in Fig. 2.

By contrast, the other 3D EXIT chart characterizes the MI exchange between the core VNs and the extension CNs of Fig. 5, which is referred to as the LDGM part MI exchange. More specifically, we propose a pair of 3D EXIT charts having an x-axis that characterises I_{vc}^a , which is provided by the *extrinsic* information I_{cc}^e output by the core CN decoder. By contrast, the y-axis of both EXIT charts is used to characterise I_{ve}^a , which is provided by the *extrinsic* information I_{ce}^e output of the extension CN decoder. In one of the 3D EXIT charts, the z-axis characterises I_{vc}^e , which becomes the *a priori* information provided for the core CN decoder I_{cc}^a . Hence, the EXIT chart characterises the LDPC part MI exchange between the core VN decoder and the core CN decoder. Furthermore, the z-axis of the other 3D EXIT chart characterises I_{ve}^e , which becomes the *a priori* information provided for the extension CN decoder I_{ce}^a , characterising the LDGM MI exchange. As shown in Fig. 6 (a), the surface $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$ characterises the *extrinsic* MI I_{vc}^e generated by the core VND entered into the core CND, which is dependent on I_{vc}^a , I_{ve}^a and I_H . To elaborate a little further, the surface $I_{cc}^e(I_{cc}^a)$ represents the *extrinsic* MI I_{cc}^e that the core CND outputs as a function of the *a priori* information I_{cc}^a , which is then entered into the core CND of Fig 5. Similarly, in Fig. 6(b), the surface $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ gives the *extrinsic* MI I_{ve}^e generated by the core VND and entered into the extension CND, which is dependent on I_{vc}^a , I_{ve}^a and I_H . Furthermore, the surface $I_{ce}^e(I_{ce}^a, I_H)$ gives the *extrinsic* MI I_{ce}^e generated by the extension CND as a function of I_{ce}^a and I_H in Fig. 5.

As exemplified in Fig 6, both VN decoder surfaces $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$ and $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ are affected by the channel SNR. By contrast, only the extension part of the CN decoder

$$I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H) = \sum_{i=1}^{N_{vc}} \frac{J \left(\sqrt{(d_{vc_i} - 1) \cdot [J^{-1}(I_{vc}^a)] + d_{ve_i} \cdot [J^{-1}(I_{ve}^a)] + [J^{-1}(I_H)]^2} \right)}{d_{vc_i}^{-1} \cdot \sum_{i=1}^{N_{vc}} d_{vc_i}} \quad (3)$$

$$I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H) = \sum_{i=1}^{N_{ve}} \frac{J \left(\sqrt{d_{vc_i} \cdot [J^{-1}(I_{vc}^a)] + (d_{ve_i} - 1) \cdot [J^{-1}(I_{ve}^a)] + [J^{-1}(I_H)]^2} \right)}{d_{ve_i}^{-1} \cdot \sum_{i=1}^{N_{ve}} d_{ve_i}} \quad (4)$$

$$I_{cc}^e(I_{cc}^a) = \sum_{i=1}^{N_{cc}} \frac{\left(1 - J \left(\sqrt{d_{cc_i} - 1} \cdot J^{-1}(1 - I_{cc}^a) \right) \right)}{d_{cc_i}^{-1} \cdot \sum_{i=1}^{N_{cc}} d_{cc_i}} \quad (5)$$

$$I_{ce}^e(I_{ce}^a, I_H) = \sum_{i=1}^{N_{ce}} \frac{\left(1 - J \left(\sqrt{(d_{ce_i} - 1) \cdot [J^{-1}(1 - I_{ce}^a)]^2 + [J^{-1}(1 - I_H)]^2} \right) \right)}{d_{ce_i}^{-1} \cdot \sum_{i=1}^{N_{ce}} d_{ce_i}} \quad (6)$$

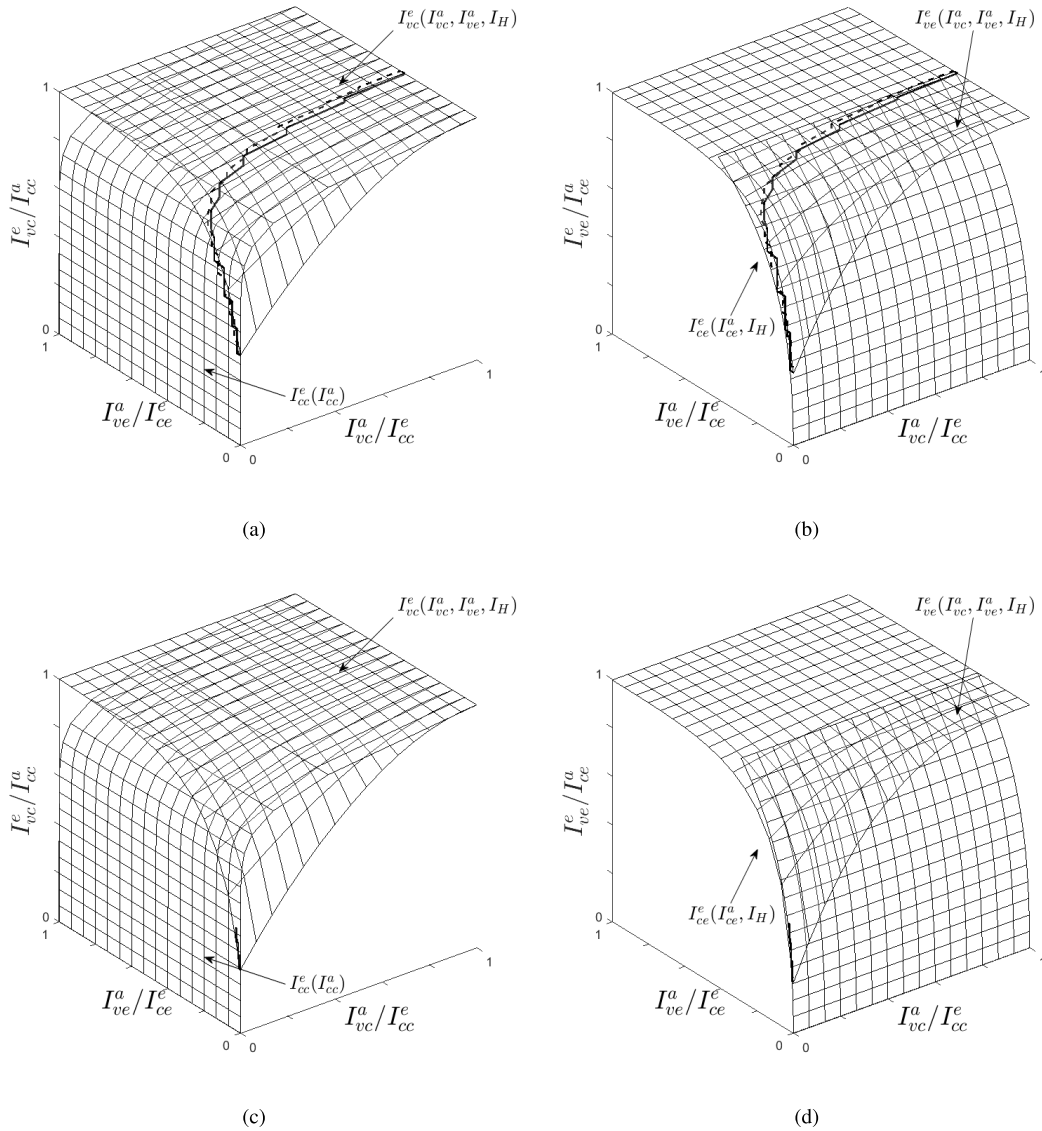


FIGURE 6. 3D EXIT chart for a K=3000-bit flooding 5G NR LDPC decoder, using BG 1, R = 1/3 and different AWGN channel SNRs, including: (a) LDPC EXIT chart at SNR = -1dB, (b) LDGM EXIT chart at SNR = -1dB, (c) LDPC EXIT chart at SNR = -3dB and (d) LDGM EXIT chart at SNR = -3dB. The continuous line represents to the predicted trajectory that bounced between EXIT surfaces while the dashed line corresponds to the the bit-by-bit Monte-Carlo simulation. The associated activation-order of the components in Fig. 5 is defined by Fig. 7.

surface $I_{ce}^e(I_{ce}^a, I_H)$ is a function of the channel SNR. Due to the existence of degree-one VNs, the value of $I_{ce}^e(I_{ce}^a, I_H)$ will be directly affected by the channel’s output information I_H , which can be observed from (6). Furthermore, the value of $I_{cc}^e(I_{cc}^a)$ is calculated by using the conventional equation (5).

Using the EXIT surfaces for the VND and CND of both the core and extension parts, a trajectory representing the MI exchange across the successive iterations of the LDPC decoder may be predicted. Fig. 7 provides a flow chart for illustrating how the predicted trajectory may be generated. At the beginning of the iterative decoding process, the *a priori* MIs $I_{vc}^a, I_{ve}^a, I_{cc}^a, I_{ce}^a$ are all initialised to 0, which means that our trajectory is starting from the (0,0,0) point at the corner

of both plots in Fig. 6. As the first step, the channel’s output information I_H is forwarded to the VND. Since both the core CND and extension CND of Fig. 5 are unaffected by this, the MI values of I_{vc}^a and I_{ve}^a are kept as 0. However, the MI values of I_{ce}^a and I_{cc}^a are updated by I_{ve}^e and I_{vc}^e , which can be determined by the VND surfaces seen in Fig. 6, according to the function $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ and $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$. Therefore, the trajectory moves upwards from the (0,0,0) point to the lowest corner of the VND surfaces, as shown using solid lines in both plots of Fig. 6. Next, the NR LDPC decoder begins its iterative decoding process, which starts by operating the core and extension CNDs of Fig. 5. The iterative decoding operations will continue until the number of iterations i

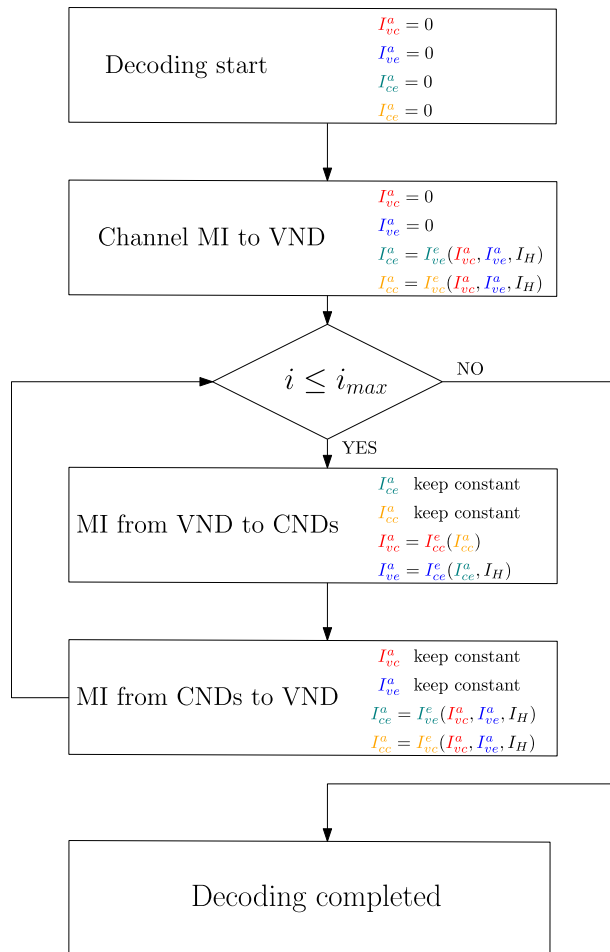


FIGURE 7. Flow chart of calculating the NR LDPC decoder's decoding trajectory. Formally defining the activation-order of the components in Fig 5.

exceeds the maximum affordable number of iterations i_{max} . Since the VND is not affected, the MI values of I_{ce}^a and I_{cc}^a remain unchanged from the previous step. However, the MI values of I_{vc}^a and I_{ve}^a are updated by the output of the CNDs, as characterised by the functions of $I_{cc}^e(I_{cc}^a)$ and $I_{ce}^e(I_{ce}^a, I_H)$, as well as by updating the position of the trajectories in the plots of Fig. 6 using the CND surfaces. More specifically, the trajectory moves from the corner of the VND surfaces towards the point calculated on the CND surfaces. Following this, the VND may be operated again and similar to the first step, new MI values of I_{ce}^a and I_{cc}^a can be obtained by using the surface functions $I_{ce}^e(I_{ce}^a, I_H)$ and $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$, but this time with the updated values of I_{vc}^a and I_{ve}^a obtained from the previous step. In this way, the trajectory in both plots of Fig. 6 moves from the previous position reached on the CND surfaces to the new calculated position on the VND surfaces. As shown in Fig. 7, these steps will continue until the iterative decoding process is completed. Finally, if the channel SNR is sufficiently high and if a sufficient number of decoding iteration has been completed, then the MI exchange between CND and VND will converge and the MI of I_{ce}^a and I_{cc}^a should approach 1. In summary, the predicted trajectory is

generated by bouncing between the EXIT surfaces of Fig. 6, according to the alternated activation of the VNDs and CNDs. Accordingly, the trajectories of Fig. 6 have been predicted and plotted as solid lines. In order to validate this prediction, we also introduced simulated trajectories in Fig. 6(a) and (b) as dashed lines. These are obtained by performing an iterative decoding process using the alternated activation of the VNDs and CNDs, while measuring the MI of the LLRs exchanged after each step. As shown in Fig. 6, a good match is observed between the solid and dashed trajectories in each case, configuring the accuracy of the proposed approach.

In contrast to the conventional 2D EXIT chart analysis of Section III-A, both 3D EXIT functions of the VN decoders $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$ and $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ are able to reach $I_{vc}^e = 1$ and $I_{ve}^e = 1$. Therefore, using the proposed 3D EXIT chart, the open/closed state of the EXIT chart's tunnel is a function of the channel SNR, which affects all the functions $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$, $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ and $I_{ce}^e(I_{ce}^a, I_H)$. For instance, the trajectory shown in Fig. 6 (a) and (b) reveals that the iterative decoding process can converge to $I_{vc}^e = 1$ and $I_{ve}^e = 1$ at an SNR of -1 dB in AWGN channel. In this scenario, the tunnel can be considered to be open, which means that the decoder is expected to obtain low BLER. However, if the channel SNR is decreased to -3 dB as shown in Fig. 6 (c) and (d), the trajectory will be curtailed at the intersection of the EXIT functions before reaching $I_{vc}^e = 1$ and $I_{ve}^e = 1$. This behaviour reveals that the NR LDPC decoder is incapable of decoding the received bit sequence successfully at a channel SNR of -3 dB. In conclusion, the proposed 3D EXIT chart accurately characterizes the MI exchange within the NR LDPC decoder and determines whether the decoder is capable of attaining a low BLER at a prescribed channel SNR.

C. TWO-DIMENSIONAL PROJECTION OF THE EXIT CHART OF THE NR LDPC DECODER

As presented in Section III-B, our proposed 3D EXIT charts can determine, whether the EXIT tunnel is open or closed, but this requires simulation of the stair-case shaped decoding trajectory and is not immediately apparent from visual inspection. In order to present this result in a straight-forward manner, in this section we propose a 2D projection of our novel 3D EXIT charts, as shown in Fig. 8 and inspired by [15]. As discussed in Section III-A, the failure of conventional 2D EXIT charts to accurately predict the NR LDPC code's performance is due to the degree-one extension VNs, which prevent the extension CNs from providing *extrinsic* LLRs having a mutual information of 1. Hence, in Fig. 8, the extension CNs and extension VNs are combined with the core VNs, in order to enable the resultant combined VN decoder to provide *extrinsic* LLRs having a MI of 1. A 2D EXIT chart may then be used for characterising the iterative decoding convergence between the core CN decoder and the combined VN decoder. However, in order to facilitate this, a particular decoding schedule must be assumed, which ensures that the combined VN decoder behaves as if it were memoryless,

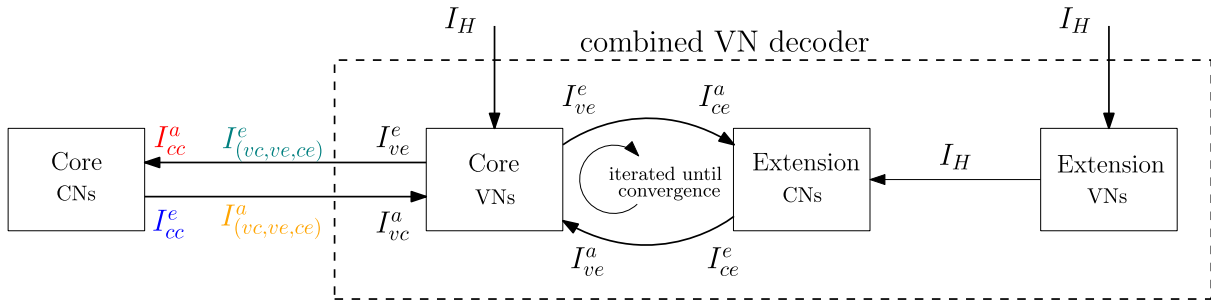


FIGURE 8. Block diagram of NR LDPC decoder that considers the core VNs, extension CNs and extension VNs as a combined VN decoder. The activation-order of the components is formally defined in Fig. 9.

associated with an *extrinsic* MI that depends only on the *a priori* and channel MIs, but not on any internal state. In the first step of this schedule, the channel’s output information I_H will be forwarded to all VNs. As shown in Fig. 8, the proposed schedule performs several MI exchange iterations between the core VNs and the extension CNs, until the $I_{ve}^e, I_{ce}^a, I_{ve}^a$ and I_{ce}^e information becomes fully converged. Then the *extrinsic* information $I_{(vc,ve,ce)}^e$ provided by the combined VN decoder becomes the *a priori* information I_{cc}^a of the core CNs. After the inner calculation within the core CNs, the resultant *extrinsic* information I_{cc}^e will be forwarded to the combined VN decoder as its *a priori* input information $I_{(vc,ve,ce)}^a$. Therefore, the 2D EXIT chart of this system represents the combination of $I_{(vc,ve,ce)}^e$ versus $I_{(vc,ve,ce)}^a$ and I_{cc}^a versus I_{cc}^e .

Instead of using simulations to draw the 2D EXIT projection of the NR LDPC in [15], we conceive a novel method relying on equations (3) to (6). In order to unambiguously specify this method, Fig. 9 introduces a flow chart of the corresponding decoding process. As discussed above, the 2D EXIT projection illustrates the combination of $I_{(vc,ve,ce)}^e$ versus $I_{(vc,ve,ce)}^a$ and I_{cc}^a versus I_{cc}^e , which are initialised to 0 as presented in Fig. 9. At the beginning of the decoding process, the channel’s output MI I_H is passed to the core VNs, and extension VNs as shown in Fig. 9. Hence the channel’s output MI that is passed to the extension VNs is directly forwarded to the extension CNs, by the degree-1 extension VNs of Fig. 8. In the first step, we focus on the effect of passing the channel’s output MI to the core VNs. According to the equations of Section III-B, the *extrinsic* information I_{ve}^e that is passed from the core VNs of Fig. 8 to the extension CNs is calculated as $I_{ve}^e = I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ according to (4), where I_{ve}^a and I_{vc}^a are initialised to 0.

In the next step of Fig. 9, the iterative decoding process begins its operation. More specifically, the MI will be first iteratively exchanged between the core VNs and extension CNs, in a process referred to as inner iteration in Fig. 8 and Fig. 9. The *extrinsic* information I_{ve}^e generated by the core VNs will then be passed to the extension CNs as the *a priori* information I_{ce}^a . In response, the *extrinsic* MI that is passed from the extension CNs to the core VNs of Fig. 8 is evaluated by (6) as $I_{ce}^e = I_{ce}^e(I_{ce}^a, I_H)$. Similar to the first step,

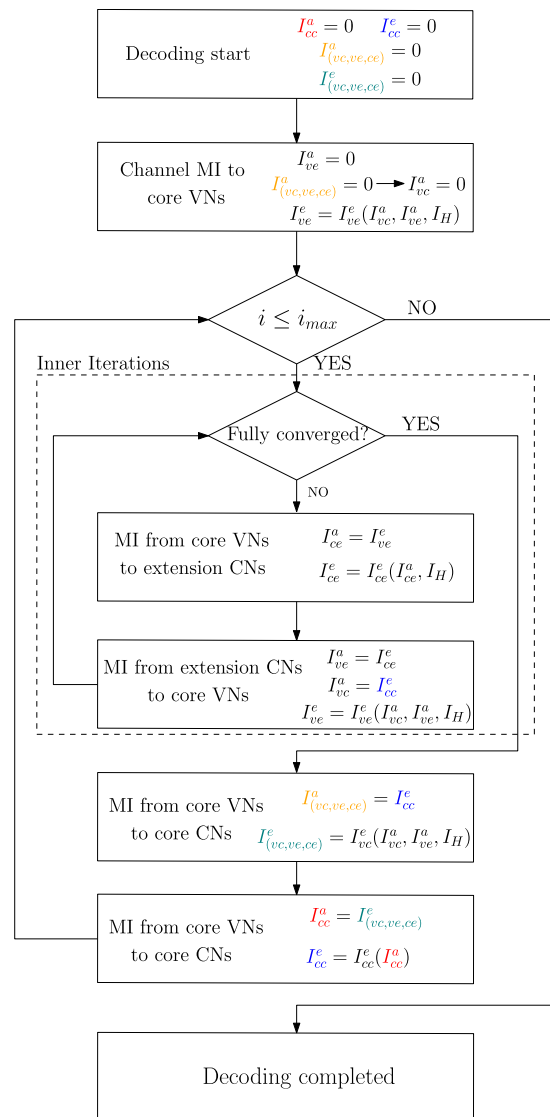


FIGURE 9. Flow chart of the decoding process of NR LDPC decoder, when considering the core VNs, extension CNs and extension VNs as the combined VN decoder of Fig. 8.

the *extrinsic* MI I_{ve}^e will be further updated and passed back to the extension CNs of Fig. 8 and so on. Note that throughout this inner iteration process, the *a priori* information I_{vc}^a

provided by the core CNs of Fig. 8 will remain constant. In this way, the inner iteration comprises an alternated MI exchange between the core VNs and the extension CNs, which continues until the MI is fully converged and stop improving. For example, in Fig. 4 of Section III-A, the trajectory stops at the cross-over point between $I_v^e(I_v^a, I_H)$ and $I_c^e(I_c^a)$ curve, whereupon convergence is obtained. The aim of the inner iteration of this alternated operation of the NR LDPC decoder is to determine the cross-over point between the $I_{ce}^e(I_{ce}^a, I_H)$ and $I_{ve}^e(I_{vc}^a, I_{ve}^a, I_H)$ curves, as a function of I_{vc}^a .

Once the MI exchange between the core VNs and the extension CNs of Fig. 8 has become fully converged, the *a priori* information I_{ve}^e can be considered to be a saturated value. According to (3) and discussed in Section III-A, the *extrinsic* information $I_{(vc,ve,ce)}^e$ that is forwarded by the combined decoder constituted by the amalgamated core VNs, extension CNs and extension VNs to the core CNs may be formulated as $I_{vc}^e(I_{vc}^a, I_{ve}^a, I_H)$. In this way, the EXIT function of the combined VN decoder of Fig. 8 may be obtained by plotting $I_{(vc,ve,ce)}^e$ versus $I_{(vc,ve,ce)}^a$. This EXIT function may then be compared to the core CN decoder's EXIT function, which is obtained by plotting I_{cc}^e versus I_{cc}^a . Fig. 10 shows the proposed 2D EXIT projection for several different scenarios. For a comprehensive comparison, Fig. 10 (a) and (b) correspond to different channel SNR, but the same coding rate of $R = 1/3$. By contrast, Fig. 10 (c) and (d) employ different coding rates R , but the same channel SNR of -1 dB. As shown in Fig. 10 (a), the curves that represent the CN decoder and the VN decoder do not cross over until the channel SNR drops to -1 dB. In other words, a 1/3 coding rate NR LDPC decoder with BG1 can be predicted to have adequate error-correction performance when the SNR is higher than -1 dB, which is a conclusion in contrast to the one suggested by the closed tunnel in the conventional 2D EXIT chart of Fig. 4. Similarly, Fig. 10 (b) gives the same conclusion when BG2 is utilized. Likewise, Fig. 10 (c) offers the conclusion that the EXIT chart tunnel will be open when the coding rate is lower than $R = 2/5$ at a channel SNR of -1 dB. Similarly, for BG2, Fig. 10 (d) has a similar suggestion, namely that a coding rate of less than $R = 2/5$ will give adequate error-correction performance. The reliability and accuracy of the 2D EXIT projection will be verified by simulations that will be presented in Section IV-B. As shown in Fig. 11 (a), the BLER curve for the case of BG1 with $R = 1/3$ begins to decay around an SNR of -1dB, which verifies the EXIT chart result of the Fig. 10 (b). The 2D EXIT projection not only corrects the deficiency of the conventional 2D EXIT chart of Fig. 4, but also offers a clear view of whether the EXIT tunnel is open or closed.

In order to further verify the accuracy of our proposed 2D EXIT chart projection, we plot a snap-shot trajectory in Fig. 10 (d), which characterises the MI exchange of the outer iteration during a simulated iterative decoding process. As illustrated by Fig. 9, each outer iteration comprises the

exchange of the saturated MI $I_{(vc,ve,ce)}^e$ forwarded by the combined VN decoder to the core CN decoder of Fig. 8. More specifically, the *extrinsic* information gleaned from the inner iteration represents the *a priori* input information I_{cc}^a of the core CN of Fig. 8 in the outer iteration. During this exchange, the MI of the exchanged LLRs is quantified and plotted for advancing the trajectory along the $I_{(vc,ve,ce)}^e$, I_{cc}^a axis of Fig. 10 (d). After completing the operations of the core CN, the *extrinsic* LLRs that are passed from the core CNs of Fig. 8 to the combined VN decoder are used for advancing the trajectory along the $I_{(vc,ve,ce)}^a$, I_{cc}^e axis of Fig. 10(d). The *a priori* information $I_{(vc,ve,ce)}^a$ produced by the inner iteration will then be used for finding the next fully converged *extrinsic* information $I_{(vc,ve,ce)}^e$ before the start of the next outer iteration in Fig. 9. Hence, the staircase-shaped trajectory will move towards the (1,1) point of the 2D projection of the EXIT chart until the affordable number of iterations is exhausted. The simulated trajectory presented in Fig. 10 (d) is approximately bounded by the CND and VND EXIT curves, which validates our proposed 2D EXIT projection method.

IV. FIXED-SCHEDULE SYSTEM DESIGN

The EXIT chart analysis of Section III has revealed a remarkable characteristic of the NR LDPC, which is related to its MI exchange during the decoding process. By exploiting these observations, this section will propose a novel component activation order for improving the error correction capability and for reducing the complexity compared to that of the conventional flooding based LDPC decoder. Here, the component activation order is fixed, hence avoiding the dynamic run-time calculation of complex parameters [22]. The proposed design is discussed in Section IV-A, while the corresponding performance versus complexity is characterised in Section IV-B.

A. FIXED-SCHEDULE DECODER

The MI exchange inside the NR LDPC decoder of Fig. 5 has been illustrated in Fig. 6. More specifically, in Fig. 6(a) and (b), the MI can be seen to converge along the I_{vc}^a/I_{cc}^e axis in the last few iterations, where it can therefore be reasoned that it is mainly the core CNs that contribute. During those iterations, there is almost no improvement along the I_{ve}^a/I_{cc}^e axis which is affected by the contribution of the extension CNs of Fig. 5. As described in Section III, a low BLER is achieved when the iterative decoding trajectory reaches $I_{cc}^e = 1$. In order for this to happen at the lowest complexity, it is desirable to activate the core CNs of Fig. 5 in every iteration, since the core LDPC code has a strong error correction capability. However, in the later iterations, the extension CNs stop making significant contributions, hence it is desirable to focus on the core CNs of Fig. 5 alone. Therefore, we propose a novel NR LDPC decoder activation order, in which the extension CNs can be deactivated for

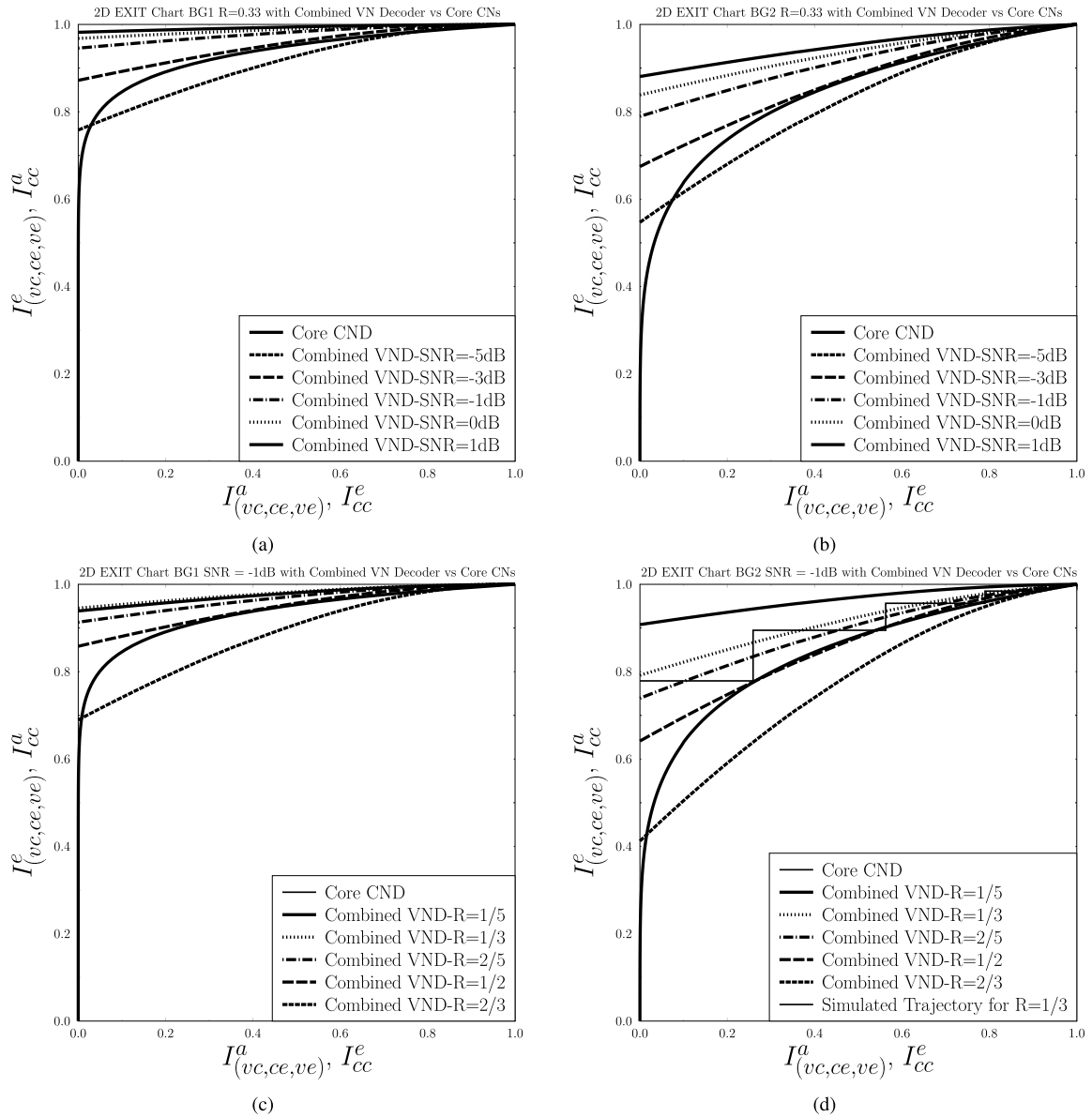


FIGURE 10. Proposed 2D EXIT chart projection for the flooding based 5G NR LDPC decoder. $R = 0.33$ is used in (a) and (b) for BG 1 and BG 2 at different channel SNRs, while $SNR = -1dB$ is used in (c) and (d) for BG 1 and BG 2 at various coding rates R . A trajectory snap-shot is presented in (d), which was obtained during the iterative decoding of a specific LDPC code-block. The schematic of Fig. 8 and flow chart of Fig. 9 is used.

the last few decoding iterations, since they would no longer contribute to the MI convergence.

In the proposed regime, the decoding activation order is decided in advance of iterative decoding. In a practical implementation, the number of iterations to be performed before switching to the core-only mode can be stored in a Look-Up Table (LUT), as a function of both the channel SNR and coding rate. The LUT can be populated during an off-line design process, relying on the 3D EXIT charts of Section III-B. More specifically, we recommend adopting full iterations based on Fig. 7 until the value of I_{ce}^e reaches 99.99% of its fully converged value, before switching to the core-only mode. We have also investigated the value of 99%

and 99.9%, but 99.99% was found to strike the best BLER performance versus complexity trade-off.

B. PERFORMANCE OF THE PROPOSED LDPC DECODER

1) PERFORMANCE OF THE PROPOSED LDPC DECODER IN AWGN CHANNELS

This section characterizes the BLER performance of our novel regime of Section IV-A, for the case of the NR LDPC code in an AWGN channel. We adopt a flooding based NR LDPC decoder as our benchmark. Our results are presented in Figure 11 and were collected by using BG2 for an information length of $K' = 1000$ bits. In order to demonstrate the versatility of the proposed regime, we use a low coding rate

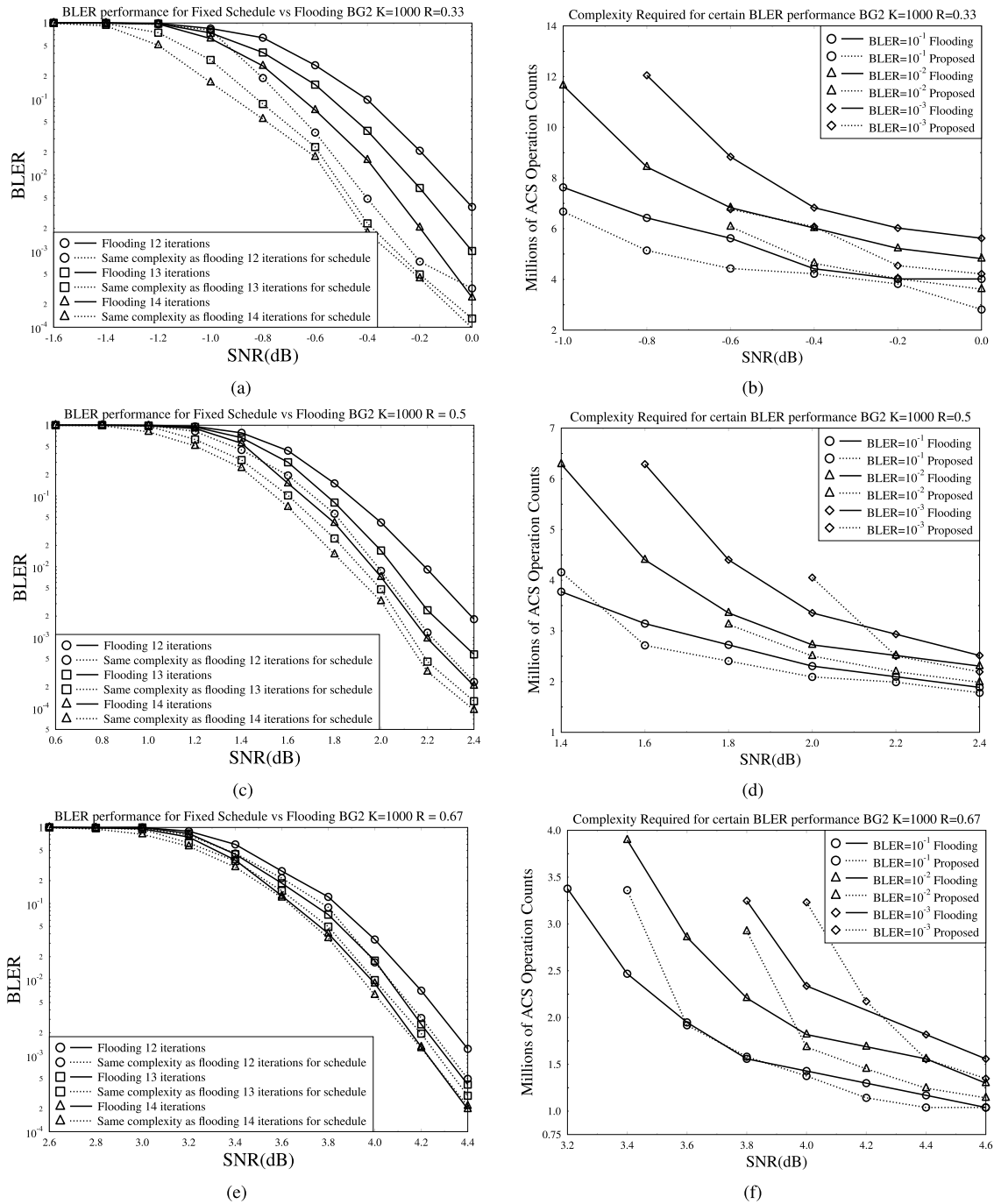


FIGURE 11. Pairs of simulation results to characterize the error correction performance of the proposed LDPC decoder in AWGN channel, as functions of channel SNR and decoding complexity. All plots are obtained using BG2 and an information block length of $K' = 1000$ bits. Plots (a) and (b) are obtained with 1/3 coding rate. Plots (c) and (d) are simulated with 1/2 coding rate. Finally plots (e) and (f) are using 2/3 coding rate. The schematic of Fig. 5 and flow chart of Fig. 7 is used.

of $R = 1/3$ in Figure 11(a) and (b); $R = 1/2$ is employed for the medium coding rate simulation of Figure 11(c) and (d); $R = 2/3$ is used for the high coding rate simulation of Figure 11 (e) and (f).

In this section, we consider two different scenarios. In the first scenario of Figure 11 (a), (c), (e), we characterize the BLER performance of the flooding based decoder using 12, 13, 14 iterations [23]–[25]. Then we compare these

to the BLER performance of the proposed decoder having the same complexity. While the flooding decoder performs a fixed number of iterations and has a fixed complexity regardless of the SNR, the complexity of proposed decoder varies with the SNR, as discussed in Section IV-A. Therefore, in different SNR environments, a constant number of flooding iterations will correspond to different numbers of iterations for the proposed decoder. In the second scenario

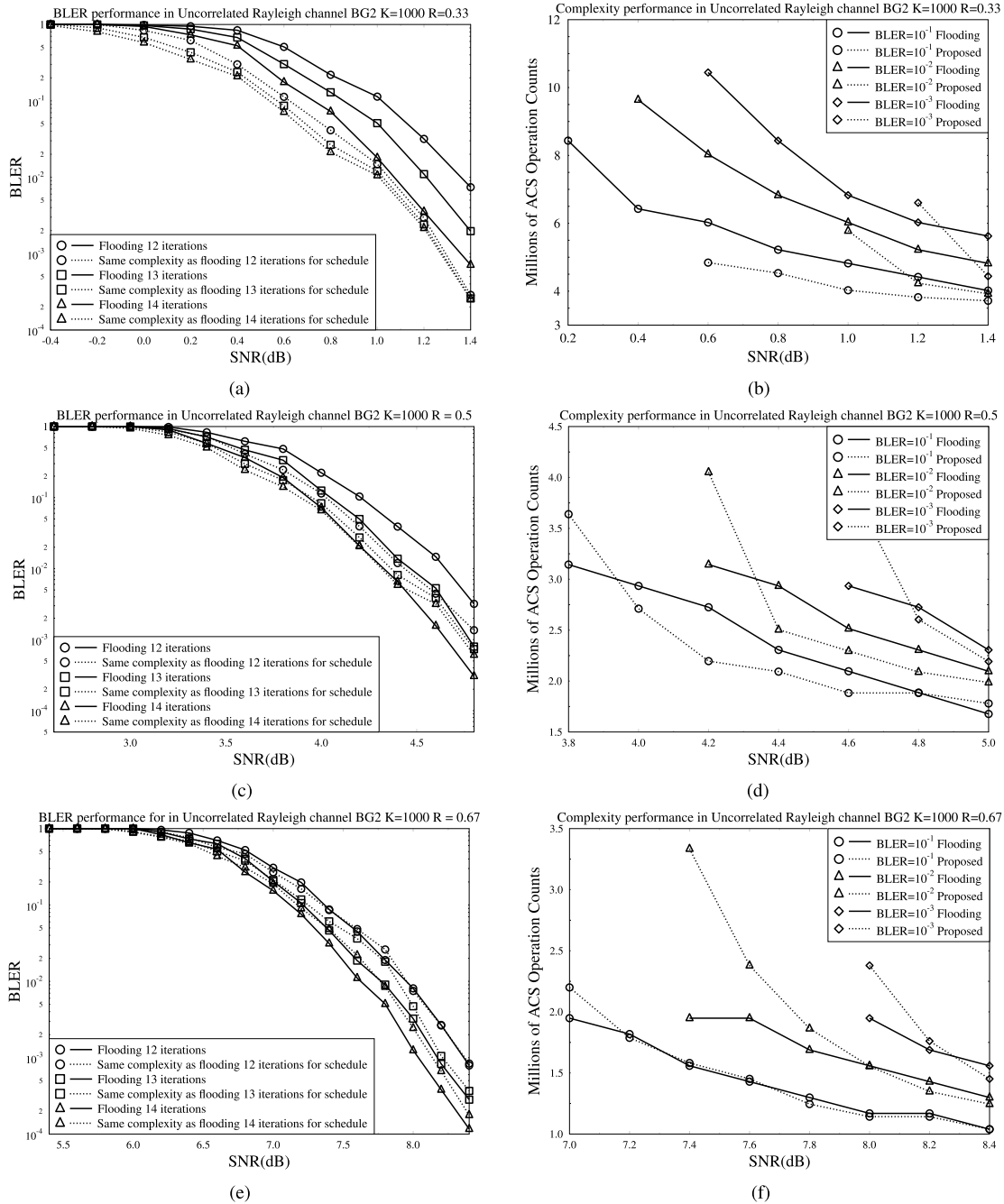


FIGURE 12. Pairs of simulation results to characterize the error correction performance of the proposed LDPC decoder in uncorrelated Rayleigh fading channel, as functions of channel SNR and decoding complexity. All plots are obtained using BG2 and an information block length of $K' = 1000$ bits. Plots (a) and (b) are obtained with 1/3 coding rate. Plots (c) and (d) are simulated with 1/2 coding rate. Finally plots (e) and (f) are using 2/3 coding rate. The schematic of Fig. 5 and flow chart of Fig. 7 is used.

of Figure 11 (b), (d) and (f), we characterize the complexity required by each decoder to achieve BLERs of 10^{-1} , 10^{-2} and 10^{-3} , respectively. Here, the complexity is quantified by the number of Add Compare Select (ACS) arithmetic operations performed, as commonly used in hardware design evaluation [26].

Figure 11 (a) considers a coding rate of 1/3 and shows that the proposed decoder offers an average of approximately 0.3 dB improvement over the flooding decoder at the

same BLER performance and the same complexity. In the corresponding complexity plot of Figure 11 (b), the proposed decoder is shown to offer around 23% complexity reduction compared to the flooding based decoder. When the coding rate is increased to 1/2, as presented in Figure 11 (c), the proposed scheme having the same complexity as 12 flooding iterations achieves the BLER performance of 14 flooding iterations. In the complexity comparison of Figure 11 (d), the corresponding complexity reduction observed is 14%.

Finally, Figure 11 (e) and (f) provide the corresponding simulation results for a high coding rate of $2/3$. Here, the BLER results show that the proposed scheme no longer maintains its error-correction capability advantage for a high number of iterations, but it still outperforms the benchmarker for a relatively low number of iterations. Furthermore, the same 14% complexity reduction is attained over the benchmarker.

As shown in the complexity versus SNR plots of Figure 11 (b), (d) and (e), the proposed decoder is unable to achieve the targeted BLER performance in some low-SNR scenario. Hence at low SNRs the proposed scheme would suffer from an error floor, unless increased the number of iterations above that of the benchmarker. However, we observed that this may be mitigated by increasing the convergence threshold beyond the 99.99% value recommended in Section IV-A. This increased convergence threshold of selecting the switching point beyond which the extension CNs are neglected, and will achieve an improved BLER at the cost of reducing its complexity advantage. Nonetheless, we recommend 99.99% since the number of flooding decoder iterations required to observe this effect is high.

2) PERFORMANCE OF THE PROPOSED DECODER IN UNCORRELATED RAYLEIGH FADING CHANNELS

In this section, we compare the flooding and proposed LDPC decoder in the case of an uncorrelated Rayleigh fading channel. In order to have a comprehensive comparison, Figure 12 uses the same parameters as Figure 11 for all simulations. As shown in Figure 12 (a) and (b), for the low coding rate of $R = 1/3$, the proposed decoder has superior BLER versus complexity performance. When the complexity is fixed for both decoders, the proposed decoder achieves the same BLER at an SNR reduction of 0.3 dB. However, observed in the Figure 12 (c) and (e) for the higher coding rates that the proposed decoder no longer maintains its BLER performance gain for a high number of iterations. As for its complexity, Figure 12 (b) and (d) shows that the proposed decoder still offers approximately 14% improvement, but in Figure 12 (f), the proposed decoder no longer offers any complexity advantage for high coding rates, owing to its reduced error correction capability.

V. CONCLUSION

In this article, we have characterized the MI exchange of the 5G NR LDPC code using EXIT charts. We have shown that conventional 2D EXIT chart analysis is unable to accurately characterize the MI exchange behaviour of the decoder, hence failing to reliably distinguish whether the EXIT tunnel is open or closed. As a remedy, we reconstituted its factor graph by partitioning the decoder into four elements, namely the core VNs, core CNs, extension VNs and extension CNs of Fig. 2. In order to suit this new factor graph, we suitably adapted the MI equations of [4] and developed a novel 3D EXIT chart representation of the 5G NR LDPC decoder. We demonstrated that our 3D EXIT chart is eminently capable of characterising both the MI exchange amongst the decoder components,

as well as the open/closed state of EXIT chart's tunnel. Furthermore, we also conceived a novel 2D EXIT projection of the proposed 3D EXIT chart for the convenient visualization of whether the EXIT tunnel is open or closed.

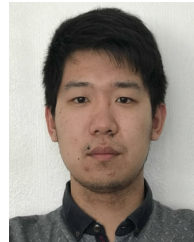
Drawing upon the unique insights offered by our EXIT chart analysis, we proposed a novel LDPC decoder activation order. More specifically, we observed that the NR LDPC decoder will typically achieve prompt MI convergence towards that of the extension CNs during the first few iterations, with the extension CNs offering little further benefit during the last few iterations. Therefore, we arranged deactivating for the extension CN decoding when the corresponding MI convergence accelerated by the extension CNs reaches the 99.99% margin of its fully converged value. By comparing the conventional flooding based and the proposed LDPC decoder, we found that the proposed decoder offers an approximately 0.2 dB gain at the same complexity and BLER performance. Viewing these benefits from a different perspective, at a specific BLER and SNR, about 14% to 19% average complexity reduction is attained compared to the flooding based decoder.

In a nutshell, we proposed a new EXIT chart analysis method and used it for reducing the decoder's complexity. This method is also eminently suitable for other sophisticated decoders combined with Hybrid Automatic Repeat reQuest (HARQ), as described in [27], since we have the knowledge whether any particular re-transmission contains sufficient information for creating an open EXIT chart tunnel and successfully decoding the transmitted bits. We can directly dispense with any futile decoding attempts and ask for the next incremental redundancy transmission for the sake of reducing the decoding delay and complexity. Furthermore, the introduction of the proposed 2D EXIT projection creates an opportunity for improving the design of the NR LDPC code. As narrated in [28], the area properties and the match between the EXIT curves of a 2D EXIT chart can be exploited for minimizing the 'capacity-loss' by finding the most appropriate coding rate. The proposed NR LDPC decoder activation order may still be further improved from a practical implementation perspective in our future research. Firstly, an activation order based on layered belief propagation can be developed, which will reduce both the complexity and memory requirement of a practical implementation. Additionally, rather than using the Sum-Product Algorithm (SPA), a computational complexity reduction can be achieved by using a bespoke variant of the fixed-point Min-Sum Algorithm (MSA) instead, which uses only binary logical and integer operations in its hardware implementation [29]. In conclusion, unveiling this novel EXIT chart analysis for the NR LDPC decoder may be expected to offer significant further development of the NR LDPC code and its practical implementation.

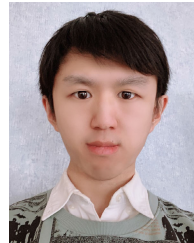
REFERENCES

- [1] *NR Multiplexing and channel coding V15.1.0*. Accessed: Apr. 2018. [Online]. Available: http://3gpp.org/ftp/Specs/archive/38_series/38.212/

- [2] P. Hailes, L. Xu, R. G. Maunder, B. M. Al-Hashimi, and L. Hanzo, "A survey of FPGA-based LDPC decoders," *IEEE Commun. Surveys Tuts.*, vol. 18, no. 2, pp. 1098–1122, 2nd Quart., 2016.
- [3] T. Richardson and S. Kudekar, "Design of low-density parity check codes for 5G new radio," *IEEE Commun. Mag.*, vol. 56, no. 3, pp. 28–34, Mar. 2018.
- [4] S. ten Brink, G. Kramer, and A. Ashikhmin, "Design of low-density parity-check codes for modulation and detection," *IEEE Trans. Commun.*, vol. 52, no. 4, pp. 670–678, Apr. 2004.
- [5] M. El-Hajjar and L. Hanzo, "EXIT charts for system design and analysis," *IEEE Commun. Surveys Tuts.*, vol. 16, no. 1, pp. 127–153, 1st Quart., 2014.
- [6] L. Kong, Y. L. Guan, J. Zheng, G. Han, K. Cai, and K.-S. Chan, "EXIT-Chart-Based LDPC code design for 2D ISI channels," *IEEE Trans. Magn.*, vol. 49, no. 6, pp. 2823–2826, Jun. 2013.
- [7] F.-M. Li, C.-H. Lin, and A.-Y. Wu, "A new early termination scheme of iterative turbo decoding using decoding threshold," in *Proc. IEEE Workshop Signal Process. Syst. Design Implement.*, Oct. 2006, pp. 89–94.
- [8] A. Ashikhmin, G. Kramer, and S. ten Brink, "Code rate and the area under extrinsic information transfer curves," in *Proc. IEEE Int. Symp. Inf. Theory*, Jun. 2002, p. 115.
- [9] A. Kraskov, H. Stögbauer, and P. Grassberger, "Estimating mutual information," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 69, no. 6, Jun. 2004, Art. no. 066138. [Online]. Available: <https://link.aps.org/doi/10.1103/PhysRevE.69.066138>
- [10] S. ten Brink, "Convergence behavior of iteratively decoded parallel concatenated codes," *IEEE Trans. Commun.*, vol. 49, no. 10, pp. 1727–1737, Oct. 2001.
- [11] T. L. Narasimhan and A. Chockalingam, "EXIT chart based design of irregular LDPC codes for large-MIMO systems," *IEEE Commun. Lett.*, vol. 17, no. 1, pp. 115–118, Jan. 2013.
- [12] A. Elkelesh, M. Ebada, S. Cammerer, L. Schmalen, and S. ten Brink, "Decoder-in-the-loop: Genetic optimization-based LDPC code design," *IEEE Access*, vol. 7, pp. 141161–141170, 2019.
- [13] H. Wu and H. Wang, "A high throughput implementation of QC-LDPC codes for 5G NR," *IEEE Access*, vol. 7, pp. 185373–185384, 2019.
- [14] Y. Zhang, K. Peng, X. Wang, and J. Song, "Performance analysis and code optimization of IDMA with 5G new radio LDPC code," *IEEE Commun. Lett.*, vol. 22, no. 8, pp. 1552–1555, Aug. 2018.
- [15] Y. Julian, R. P. Astuti, and K. Anwar, "EXIT analysis for decoding behaviour and performances of 5G NR QC-LDPC codes," in *Proc. 21st Int. Symp. Wireless Pers. Multimedia Commun. (WPMC)*, Nov. 2018, pp. 437–442.
- [16] Y. Zhang, K. Peng, Z. Chen, and J. Song, "Construction of rate-compatible raptor-like quasi-cyclic LDPC code with edge classification for IDMA based random access," *IEEE Access*, vol. 7, pp. 30818–30830, 2019.
- [17] B. Wang, Y. Zhu, and J. Kang, "Two effective scheduling schemes for layered belief propagation of 5G LDPC codes," *IEEE Commun. Lett.*, vol. 24, no. 8, pp. 1683–1686, Aug. 2020.
- [18] R. Tanner, "A recursive approach to low complexity codes," *IEEE Trans. Inf. Theory*, vol. 27, no. 5, pp. 533–547, Sep. 1981.
- [19] X.-Y. Hu, E. Eleftheriou, D.-M. Arnold, and A. Dholakia, "Efficient implementations of the sum-product algorithm for decoding LDPC codes," in *Proc. IEEE Global Telecommun. Conf. (GLOBECOM)*, vol. 2, Nov. 2001, p. 1036.
- [20] M. Franceschini, G. Ferrari, and R. Raheli, "Does the performance of LDPC codes depend on the channel?" *IEEE Trans. Commun.*, vol. 54, no. 12, pp. 2129–2132, Dec. 2006.
- [21] D. Divsalar, "Ensemble weight enumerators for protograph LDPC codes," in *Proc. IEEE Int. Symp. Inf. Theory*, Jul. 2006, pp. 1554–1558.
- [22] A. I. V. Casado, M. Griot, and R. D. Wesel, "LDPC decoders with informed dynamic scheduling," *IEEE Trans. Commun.*, vol. 58, no. 12, pp. 3470–3479, Dec. 2010.
- [23] A. Amaricai, O. Boncalo, and I. Mot, "Memory efficient FPGA implementation for flooded LDPC decoder," in *Proc. 23rd Telecommun. Forum Telfor (TELFOR)*, Nov. 2015, pp. 500–503.
- [24] E. Pisek, D. Rajan, and J. Cleveland, "Gigabit rate low-power LDPC decoder," in *Proc. IEEE Inf. Theory Workshop*, Oct. 2011, pp. 518–522.
- [25] B. Le Gal, C. Jego, and J. Crenne, "A high throughput efficient approach for decoding LDPC codes onto GPU devices," *IEEE Embedded Syst. Lett.*, vol. 6, no. 2, pp. 29–32, Jun. 2014.
- [26] K. K. Parhi, "An improved pipelined MSB-first add-compare select unit structure for Viterbi decoders," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 3, pp. 504–511, Mar. 2004.
- [27] F. Hamidi-Sepehr, A. Nimbalkar, and G. Ermolaev, "Analysis of 5G LDPC codes rate-matching design," in *Proc. IEEE 87th Veh. Technol. Conf. (VTC Spring)*, Jun. 2018, pp. 1–5.
- [28] A. Ashikhmin, G. Kramer, and S. ten Brink, "Extrinsic information transfer functions: Model and erasure channel properties," *IEEE Trans. Inf. Theory*, vol. 50, no. 11, pp. 2657–2673, Nov. 2004.
- [29] H. Chen, K. Zhang, X. Ma, and B. Bai, "Comparisons between reliability-based iterative min-sum and majority-logic decoding algorithms for LDPC codes," *IEEE Trans. Commun.*, vol. 59, no. 7, pp. 1766–1771, Jul. 2011.



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