IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received October 1, 2020, accepted October 5, 2020, date of publication October 12, 2020, date of current version October 30, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3030390

Coordinated Two-Stage Operation and Control for Minimizing Energy Storage Capacitors in Cascaded Boost-Buck PFC Converters

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This work was supported by the Chinese National Natural Science Foundation under Project 51977068.

ABSTRACT Cascaded boost-buck PFC (CBBPFC) converters offer a wide voltage conversion ratio and a near-unity power factor but require a large output electrolytic capacitor, leading to poor reliability and power density. In this paper, a coordinated two-stage operation and control strategy is proposed to significantly minimize the capacitor requirement without any other hardware changes. In a conventional CBBPFC converter, the boost and buck stages either operate independently nor complementally. In contrast, the proposed method operates the two stages in a concerted manner, so it is possible to use the dc-link capacitor with certain voltage fluctuation to buffer the power imbalance between the AC input and DC output. A new coordinated control strategy and a fluctuation-ratio based design consideration are developed to coordinate the operation of the two stages, further complement the system design. A 200W CBBPFC prototype based on the design concept exhibits a maximum reduction of the output capacitor by 83%, a peak efficiency of 95.8%, and a power factor of 0.99.

INDEX TERMS Power factor correction (PFC), cascaded boost-buck (CBB), LED driver, voltage ripple.

I. INTRODUCTION

Light-Emitting Diodes (LEDs) are becoming increasingly ubiquitous due to their advantages in reliability, lifetime, energy efficiency, and maintenance requirements [1]–[3]. As a result, there is a growing demand for single phase power factor correction (PFC) converters with high power density, near-unity power factor, wide voltage conversion ratio, and high reliability in LED lighting applications [4]–[6]. In universal output voltage LED driver applications, it is important to provide both step-up and step-down conversion so the output dc voltage becomes adjustable. Conventional single-switch buck-boost topologies, including the buck-boost, flyback, SEPIC, and Cuk converters, suffer from increases in component stress and component size [7]–[9]. In contrast, the two-switch buck-boost (TSBB) topologies are suitable candidates for a wide output range of converter operations [10]. The TSBB is usually composed of boost, buck, or buck-boost cascade combination, which offers step-up and step-down operations with much-reduced voltage stress on the components, and is widely adopted in PV [11], [12], wireless power transfer systems [13], and PFC applications [14]–[16]. Among them, the combinations with buck stage in front, such as cascaded buck-boost [17] and interleaved-cascaded buck-boost converters [18], are not efficient in economic and efficiency. A key issue with those converters is that when the buck switch at the input is turned off, an additional input *LC* filter is required to operate the converter in continuous conduction mode (CCM), which greatly limits the application range, especially in PFC application. Oppositely, the cascaded boost-buck inherently contains an inductor at the input to provide a high power factor in PFC applications. Fig. 1 shows the topology of the cascaded boost-buck PFC (CBBPFC) converter, in which the boost and buck stages are cascaded with a common dc-link capacitor in between. The CBBPFC topology offers not only a wide

The associate editor coordinating the review of this manuscript and approving it for publication was Sze Sing Lee.

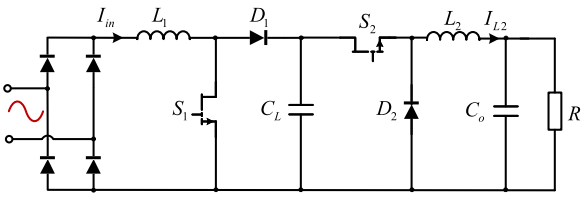


FIGURE 1. Cascaded boost-buck PFC (CBBPFC) topology.

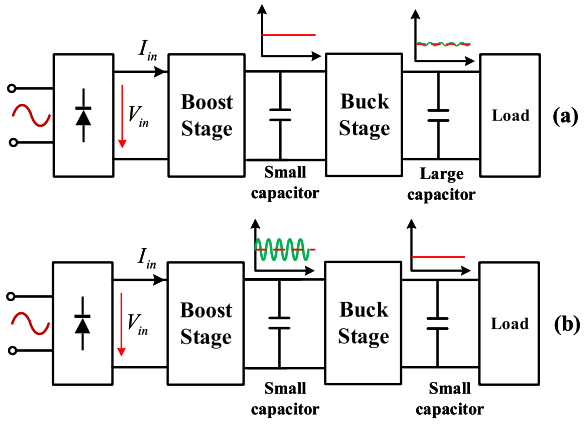


FIGURE 2. Different operation methods. (a) Previous complimentary or separate modes, where only the bulky electrolytic output capacitors can buffer the imbalance power due to the strict output voltage ripple requirements. (b) Proposed coordinated two-stage operation mode, where the dc-link ports with a larger amplitude fluctuation voltage use the smaller film capacitor to buffer the imbalance power.

voltage conversion ratio but also a near-unity power factor even without a pre-stage filter as well as continuous input and output currents benefiting from the two inductors used. However, the CBBPFC topology has the disadvantages of increase in components (two capacitors and two inductors used), cost and size. Furthermore, substantial energy storage is required in any ac-dc converters to buffer the power imbalance between the ac input and dc output [19]. In the previously reported CBBPFC converters, the boost and buck stages operate in a complementary mode [20] or independently [21], [22], entirely relying on the output capacitor to buffer the power imbalance between the ac input and dc output, shown in Fig. 2(a). Presently, only electrolytic capacitors can meet the large capacitance requirement to reduce the output voltage ripple, but they suffer from relatively short lifetime and large volume in a long lifetime and high power density LED applications [23].

Several approaches were proposed to reduce the output capacitance requirement and eliminate the use of electrolytic capacitors in PFC converters to improve product lifetime and compactness. References [24]–[26] suggested to insert an active filter to eliminate the electrolytic capacitor but require additional power electronic components and undermine the goal of system downsizing. References [27]–[30] proposed an integrated solution to share the use of the active switches between the PFC rectifier and the active dc filter without requiring extra active switches. References [31]–[33] reported several flying capacitor multilevel topologies in the buck and buck-boost stages to reduce capacitance requirement with reduced switch stress. Unfortunately, those solutions do not maintain a continuous input current flow, leading to a poorer power factor and a more complex filter design challenge. Recently, reference [34] made a high-level review of the second harmonic current reduction control schemes for a two-stage single-phase converter from the dc-bus port-impedance perspective. However, the two-stage in the CBBPFC converter essentially DC/DC with step-up and step-down ability, instead of the two converters with different functions in [34], which makes the control methods mentioned in [34] may not be suitable for the CBBPFC converter. Furthermore, different topologies have specific operations and characteristics, it is still necessary to establish corresponding control strategies and design considerations based on specific characteristics and operation.

Based on the CBBPFC topology and operation characteristics, this paper proposes a coordinated two-stage operation and control method to minimize energy storage requirements. The proposed solution enables the CBBPFC converters to simultaneously achieve a wide conversion ratio, high power factor, high reliability in meeting the demands of next-generation LED drivers. The main contributions of this paper are listed as follows.

(a). A coordinated two-stage operation is proposed for the first time to prevent the imbalance power from flowing into the load side, which makes it possible to use dc-link capacitors to buffer the imbalance power.

(b). The dc-link capacitors voltage is designed to fluctuate with a larger amplitude to buffer the imbalance power, resulting in a large reduction of energy storage capacitors without adding extra components, shown in Fig. 2(b).

(c). A coordinated control strategy is proposed to coordinate the two-stage operation and realize system stability control.

(d). A design consideration from the new perspective of fluctuation-ratio is developed to minimize the energy storage capacitors and complement the system design.

The remainder of the paper is organized as follows. Section II introduces the operating principle and steady-state analysis of the proposed CBBPFC concept. Section III discusses a new coordinated control strategy to allow the dc-link capacitor for energy buffering. The detailed design considerations based on fractional ratio are provided in Section IV. In Section V, a hardware prototype is presented along with experimental results to validated the proposed concept. Finally, the conclusions are provided in Section VI.

II. PRINCIPLE OF OPERATION

The basic operation principle and steady-state analysis of the proposed CBBPFC converter are discussed in this section.

A. CIRCUIT CONFIGURATION AND OPERATING PRINCIPLE

As shown in Fig. 1, the CBBPFC converter consists of a boost stage and a buck stage, where the two stages are cascaded

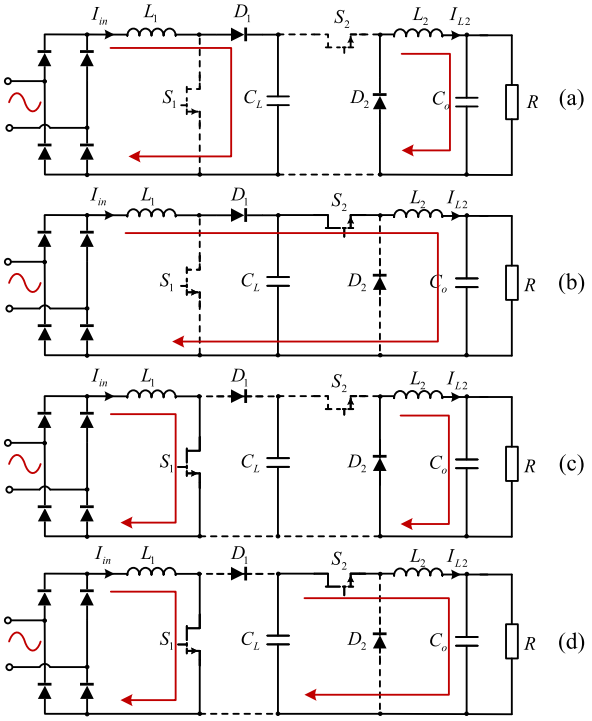


FIGURE 3. Operation states of CBBPFC converter. (a) State I: both S_1 and S_2 are turned off; (b) State II: S_1 is turned off and S_2 is turned on; (c) State III: S_1 is turned on and S_2 are turned off; and (d) State IV: both S_1 and S_2 are turned on.

together with a common dc-link capacitor. The choice of this topology is motivated by the following factors.

a. Wide conversion ratio. It can operate as a boost (for voltage step-up) or as a buck (for voltage step-down) converter offering a wide conversion ratio.

b. High power factor and smaller filter. The input and output current remains continuous due to its two inductors, which makes the high power factor can be easily achieved even without pre-stage filter.

c. Reduced system energy storage requirements and high power density. With proposed coordinated operation and control, the dc-link capacitors can be controlled to buffer the imbalance power with much-reduced capacity, offering high power density. Meanwhile, the development of wide bandgap (WBG) devices permits the converters to operate at higher frequencies, which can significantly reduce the inductor volume to further improve the power density.

Assuming the continuous-conduction mode (CCM) of operation, the CBBPFC converter has two power switches, thus the system contains four different operation states, shown in Fig. 3. And The operating waveforms of the converter for different states are shown in Fig. 4, which are briefly described as follows.

State I: both S_1 and S_2 are turned off, in which I_{in}, I_{L2} and V_o decreased, the dc-link capacitor voltage V_{CL} increased. This state is used to transfer the energy from the input side to the dc-link capacitor C_L.

State II: S_1 is turned off and S_2 is turned on, in which I_{L2}, V_o increased and I_{in} decreased. Depending on the current

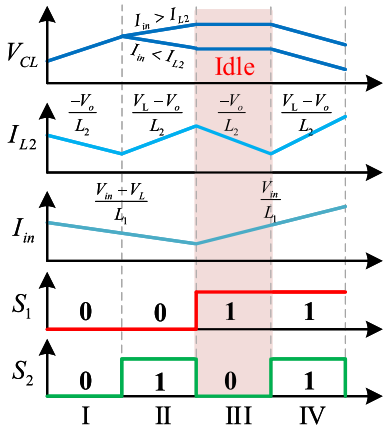


FIGURE 4. The operating waveforms of the CBBPFC converter for different states. Note that the idle state (State III) can prevent the imbalance power from flowing into the load side.

magnitude relationship between I_{in} and I_{L2}, there will be two trends for dc-link capacitor voltage V_{CL}. If $I_{in} > I_{L2}$, V_{CL} increased, in which the energy transfer from sources into the dc-link capacitor C_L and load side. Conversely, If $I_{in} < I_{L2}$, V_{CL} decreased, and the energy transfer from sources and the dc-link capacitor C_L into the load side.

State III: S_1 is turned on and S_2 is turned off, in which the input current I_{in} increases, while the output inductor current I_{L2} decreases. Of note that the C_L is in the idle state with no current flowing through it. This state can prevent the imbalance power from flowing into the load side, which has not been used in the reported complementary or separate control methods.

State IV: both S_1 and S_2 are turned on, in which I_{in}, I_{L2}, V_o increased and V_{CL} decreased. This state is used to transfer the energy from capacitor C_L to the loads, and store the input energy into the inductor for step-up.

According to the operating states, the power transferred to the load is controllable thanks to the added State III. Then, if the power transferred to the load is equal to the load power, the bulky electrolytic capacitor will be not required anymore. The proposed operation coordinates two parts and exploits all operations states (especially state III) to prevent the imbalance power from flowing into the load side and ensure the dc-link capacitors buffer the imbalance power. As a result, the output port does not require buffer the imbalance power, and only a small film capacitor can maintain the reference output voltage without any double-line frequency ripple.

B. STEADY-STATE CIRCUIT ANALYSIS

Considering a general PFC converter structure, the input voltage V_{in} is a sinusoidal waveform with an angular velocity of ω, and the current I_{in} is a sine variable with in-phase variation, shown in Fig. 5(a).

$$\begin{cases} V_{in} = V_m \sin(\omega t) \\ I_{in} = I_m \sin(\omega t) \end{cases} \tag{1}$$

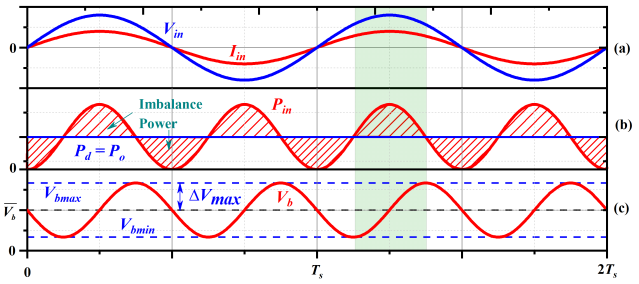


FIGURE 5. Single phase ac-dc converter operation waveforms. (a) the input voltage and current operation waveforms; (b) the input and output power; and (c) the voltage for the capacitors which buffer the imbalance power.

where V_m and I_m are the amplitude of V_{in} and I_{in}, respectively, and ω is the angular frequency of the ac mains.

The instantaneous power on the input side can be expressed as:

$$P_{in}(t) = V_{in}(t)I_{in}(t) = \underbrace{\frac{V_m I_m}{2}}_{P_d} - \underbrace{\frac{V_m I_m}{2}\cos(2\omega t)}_{P_r} \tag{2}$$

The input power consists a steady-state component P_d and a double-line frequency imbalance component P_r shown in the Fig. 5(b). P_d provides the energy for the loads, i.e. $P_d = P_o = V_m I_m/2$, and P_r is fully buffered by the capacitors in the circuit. A voltage increase will be generated on the buffer capacitors C_b, shown in the shadow part in Fig. 5(c), and the maximum value ΔV_{max} satisfies the formula.

$$\begin{cases} \frac{1}{2}C_b V_{b\max}^2 - \frac{1}{2}C_b V_{b\min}^2 = \int_{-\frac{\pi}{4\omega}}^{\frac{\pi}{4\omega}} P_r(t)dt = \frac{P_o}{\omega} \\ V_{b\max} = \overline{V_b} + \Delta V_{\max} \\ V_{b\min} = \overline{V_b} - \Delta V_{\max} \end{cases} \tag{3}$$

where $\overline{V_b}$ stands for the average voltage component on the buffer capacitors and C_b is the capacitance, which can be obtained by:

$$\begin{cases} \overline{V_b} = \dfrac{P_o}{2\omega C_b \Delta V_{\max}} \\ C_b = \dfrac{P_o}{2\omega \overline{V_b} \Delta V_{\max}} \end{cases} \tag{4}$$

We define the fluctuation ratio α to indicate the magnitude of the voltage fluctuation shown in the Fig. 5 (c), i.e. $\alpha = \Delta V_{max}/\overline{V_b}$. Therefore, the capacitance C_b, the voltage of the buffer capacitors V_b and the required minimum capacity energy E_{bmin} can be expressed as:

$$\begin{cases} C_b = \dfrac{P_o}{2\omega \overline{V_b}^2} \times \dfrac{1}{\alpha} \\ V_b = \overline{V_b} - \alpha \overline{V_b}\sin(2\omega t) = (1 - \alpha \sin(2\omega t))\overline{V_b} \\ E_{b\min} = \dfrac{C_b V_{b\max}^2}{2} = \dfrac{P_o(1+\alpha)^2}{4\omega\alpha} \end{cases} \tag{5}$$

where V_{bmax} stands for the maximum value of the buffer capacitors voltage.

In previous CBBPFC converters, only the output capacitors can be used for energy with a complimentary or separate mode. However, extremely strict ripple requirements are imposed on the output voltage, the voltage swing is usually limited [35], [36]. Assuming that $f = 50$ Hz, $\alpha = 3\%$, for a PFC converter with $P_o = 200$ W, $V_o = 100$-200 V, the required capacitance will be up to 1.06 mH. So, a bulky electrolytic capacitor bank is required to be configured on the output side, maintaining small voltage fluctuations for the loads. In this case, the lifetime, the power density and the reliability are reduced.

As can be seen in (5), the minimum system storage energy requirement, which is approximately proportional to the capacitors volume, is decrease inversely as the α is increased. And if the upper limit of the fluctuation ratio is increase, the required minimum capacity energy can be greatly reduced and it became possible to replace the electrolytic capacitors with longer life film and ceramic capacitors. Based on the topology of CBBPFC converter, this paper proposes a coordinated operation and control to allow the dc-link capacitors instead of the output capacitors to buffer the imbalance power. The dc-link capacitors will be greatly reduced by increasing its voltage fluctuation ratio without any disturbances for the output voltage. This will solve the bulky, low-reliability and low power density problem of CBBPFC converter.

III. CONTROL STRATEGY

Previous control methods (complimentary operating mode in literature [20] and independent operating mode in [21], [22]) generally maintain a constant dc-link capacitor voltage. It cannot prevent the imbalance power from flowing into the load side and making it difficult for dc-link capacitors to buffer imbalance input power. This paper proposes a new coordinated control strategy based on average current mode control. In addition to controlling the input current and output voltage like a conventional PFC converter, there is another control target: the dc-link capacitor voltage V_L, which must be controlled to fluctuate with a larger amplitude to buffer the imbalance power, resulting in a large reduction of the volume the capacitors. Fig. 6 shows the system control block diagram of the CBBPFC converter. There are two controllers: the voltage regulator and the coordinated current controller.

A. VOLTAGE REGULATOR

The outer voltage regulator is to generate the reference values for the inductor currents, shown in the red block of Fig. 6. The input current reference value is quite like conventional ACMC, except that the dc-link capacitors average voltage $\overline{V_L}$ instead of the output voltage is used as feedback. Here the reference average voltage of the dc-link capacitors can be calculated with the output reference value voltage and output power, the detailed discussion will be introduced in Section IV-C. And the low-pass filter (LPF) is used for the extraction of the dc-link capacitors average voltage, and the proportion-integral (PI) controller ensures zero steady-state tracking error due to its infinite gain for dc signal. Meanwhile,

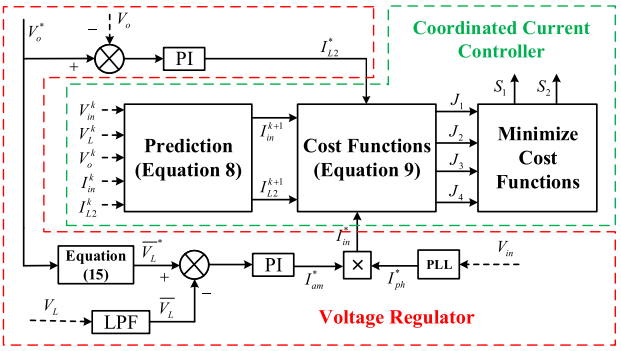


FIGURE 6. The system control block diagram of the CBBPFC converter. The red box is the voltage regulator to generate the inductor current reference value, the green box is the coordinated current controller to choose the desired operation state in a coordinated manner.

with the phase lock loop (PLL), the frequency and phase of the input voltage can be achieved. We take the output voltage feedback loop to generate the output inductor reference value. Similarly, the PI controller is used to release the zero steady-state tracking error for the output voltage.

B. COORDINATED CURRENT CONTROLLER

The dc-link capacitor is designed to buffer the imbalance power, which requires the boost and buck part work in a coordinated manner to prevent the imbalance power from flowing into the load side. Meanwhile, fluctuating dc-link capacitor voltage makes the boost and buck stage both run in the non-steady-state process in real-time. Due to the nonlinearity, it is difficult to achieve the control requirements by using a conventional PI controller. This paper considers the system operation in terms of states and proposes a coordinated current controller directly chooses the desired operation state in a coordinated manner. The detailed discussions of the specific implementation method are as follows.

Based on the Kirchhoff's current law, the system model can be expressed as:

$$\begin{cases} L_1 \dfrac{dI_{in}}{dt} = (V_{in} - (1 - S_1) V_L) \\ L_2 \dfrac{dI_{L2}}{dt} = (S_2 V_L - V_o) \end{cases} \tag{6}$$

where S_i $(i = 1, 2)$ stands for the switch function, S_i is 1 for the on state, and 0 for the off state. To get a discrete-time model, the current derivative dI/dt is replaced by a forward Euler approximation. That is, the derivative is approximated as follows:

$$\frac{dI}{dt} \approx \frac{I(k+1) - I(k)}{T} \tag{7}$$

where T stand for the sampling period, $I(k+1)$ stand for the prediction value at time $(k+1)$, and $I(k)$ stand for the sample value at time k.

Substituting (7) into (6), the general discrete mathematical model for the CBBPFC converters can be expressed as:

$$\begin{cases} I_{in}^{k+1} = \dfrac{\left(V_{in}^k - (1 - S_1) V_L^k\right) T}{L_1} + I_{in}^k \\ I_{L2}^{k+1} = \dfrac{\left(S_2 V_L^k - V_o^k\right) T}{L_2} + I_{L2}^k \end{cases} \tag{8}$$

where V_{in}^k, V_o^k, V_L^k, I_{in}^k, I_{L2}^k represent the sample values at time k for input voltage, output voltage, dc-link capacitors voltage, input inductor current and output inductor current, respectively. And I_{in}^{k+1} and I_{L2}^{k+1} are the prediction values at time $(k+1)$ for input and output inductor current, respectively. Equations (8) can be used to predict the inductor current at time $(k+1)$ by using the system state at time k.

In the actual implementation, parameters T/L_1 and T/L_2 can be used as the constant once the system components are selected. Therefore, the calculation burden of the prediction function (Eq. 8) can be greatly reduced, and only 2 additions, 2 subtractions, and 4 multiplications can complete the prediction of all four states. Furthermore, if the $L_1 = L_2$, the calculation burden can be further released by reusing some internal calculation results.

The current controller directly chooses the system state by minimizing a cost function in each sampling cycle. There are two control variables in this controller: the input and output inductor current. Thus, the cost function measures the error between the references and the predicted currents, which can be expressed as:

$$J = \left|I_{in}^* - I_{in}^{k+1}\right| + \left|I_{L2}^* - I_{L2}^{k+1}\right| \tag{9}$$

where I_{in}^* and I_{L2}^* stand for the reference values for the input current and output current, which can be obtained by the outer voltage regulator. After evaluating the cost function for each state, one can obtain the optimal operation state which is corresponding to the minimum cost function to control the various switches in a coordinated manner. Since the proposed method directly chooses the desired operation state, the limiters and PWM modules in conventional PI controllers are no longer not needed, and some logic judgment operations can be omitted in the actual implementation.

IV. DESIGN CONSIDERATIONS

The dc-link capacitor can buffer the imbalance power and its voltage has the freedom to fluctuate with a larger amplitude, the key issue is how to choose the system parameters, such as the α_L, C_L and $\overline{V_L}$. This section will discuss a fluctuate-ratio-based design consideration for proposed coordinated method.

A. DESIGN CONSTRAINT OF α_L

Due to the boost and buck topological structure, the minimum voltage for dc-link capacitors must higher than both input peak voltage and output voltage, which can be expressed as:

$$V_{L\min} = (1 - \alpha_L)\,\overline{V_L} = K_1 \max\left(V_m, V_o^*\right) \tag{10}$$

where K_1 stand for the stable margin, which must bigger than 1 to enable the stable operation for both parts. Usually,

TABLE 1. The voltage stress for different switch devices under different operation states.

Operation State	S_1	D_1	S_2	D_2
State I	V_L	0	V_L	0
State II	V_L	0	0	V_L
State III	0	V_L	V_L	0
State IV	0	V_L	0	V_L
Minimum Stress	V_{Lmax}	V_{Lmax}	V_{Lmax}	V_{Lmax}

the operating duty cycle is limited to 0.1-0.9 to ensure that the switching device is not affected by the narrow pulse. Thus, the value of K_1 is in the range of $[1/D_{max}, 1/D_{min}]$, that is, [1.1, 10]. To minimize the voltage stress on the device, the $K_1 = 1.1$ is selected for this design. Thus, the average and maximum value for dc-link capacitor voltage can be obtained by:

$$\begin{cases} \overline{V_L} = \dfrac{K_1 \max\left(V_m, V_o^*\right)}{1-\alpha_L} \\ V_{L\max} = \dfrac{K_1\left(1+\alpha_L\right)\max\left(V_m, V_o^*\right)}{1-\alpha_L} \end{cases} \tag{11}$$

Table 1 summarizes the voltages across the power devices of the CBBPFC converter during State I - State IV, based on which their minimum voltage ratings are also calculated. It is evident that the minimum voltage ratings for all the switch devices are the maximum voltage of the dc-link capacitors. Considering a safety margin for switch devices, the voltage rating of all the devices can be expressed as:

$$V_{ds} = \frac{K_1\left(1+\alpha_L\right)\max\left(V_m, V_o^*\right)}{K_2\left(1-\alpha_L\right)} \tag{12}$$

where the K_2 stands for the safety margin for the power devices, which always chosen to 0.6 in the actual implemental stage. The required energy decreased significantly with the increase of α_L, while the voltage ratings for the devices increase as shown in equation (12). These contradictions prompt us to seek a reasonable value for the α_L.

Based on the equation (12), we can get another formula for α_L, which can be expressed as:

$$\alpha_L = \frac{V_{ds} - K_1 \max\left(V_m, V_o^*\right)/K_2}{V_{ds} + K_1 \max\left(V_m, V_o^*\right)/K_2} \tag{13}$$

At present, the voltage ratings of commercial devices used for LED applications are 450V and 600V [37]. To avoid increasing extra cost on the devices, the 450V and 600V commercial devices are considered in this design. Fig. 7 shows the maximum fluctuation ratio α_L under the different output voltages where the V_{ds} is fixed at 400V or 650V. Given V_{in} = RMS 110 V, $K_1 = 1.1$, $K_2 = 0.6$ and V_o = 100-200V. Note that as the output voltage increases, the maximum value of α_L decreases to avoid the breakdown of the devices, which is the most important design constraint for the CBBPFC converter.

B. SELECTION OF DC-LINK CAPACITORS C_L

Smaller C_L offers higher power density but suffer from significantly increased voltage stress. The design of C_L is

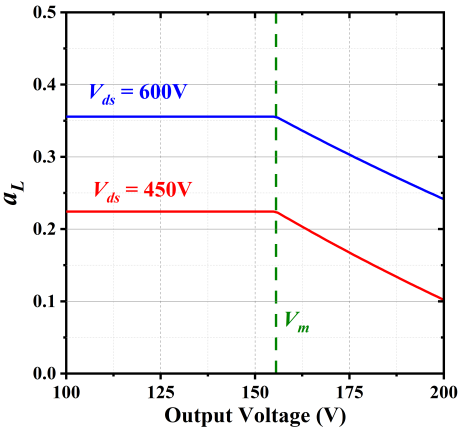


FIGURE 7. The maximum α_L in different output voltage when the V_{ds} is fixed at 450 V and 600 V. Note that as the output voltage increases, the maximum value of α_L decreases to avoid the breakdown of the devices.

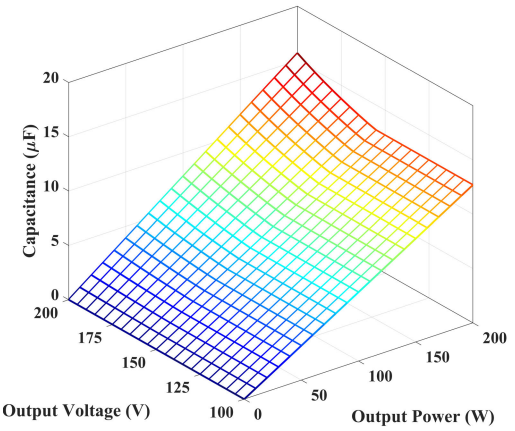


FIGURE 8. The function between the capacitance, output voltage and power. Given V_o = 100-200 V, P_o = 0-200 W, f = 50 Hz, V_{in} = RMS 110 V, $K_1 = 1.1$, $K_2 = 0.6$, V_{ds} = 600 V. Note that $C_L = 20$ μF is selected in this design to satisfy all the operation conditions.

essentially a compromise between power density and the operating constraints. Substituting (13), (11) into (5), we can obtain a function to calculate C_L, which can be expressed as:

$$C_L = \frac{2P_o}{\omega\left(K_2 V_{ds} + A\right)^2} \times \frac{V_{ds} + A/K_2}{V_{ds} - A/K_2} \tag{14}$$

where $A = K_1 \max\left(V_m, V_o^*\right)$, which stands for the minimum dc-link capacitor voltage $V_{L\min}$.

Fig. 8 shows the capacitance under different working conditions. Given V_o = 100-200 V, P_o = 0-200 W, f = 50 Hz, V_{in} = RMS 110 V, $K_1 = 1.1$, $K_2 = 0.6$, V_{ds} = 600 V. To satisfy all the operation conditions, the $C_L = 20$ μF is selected in this design.

C. SELECTION OF $\overline{V_L}$ AND α_L

After $C_L = 20$ μF is selected, the fluctuation ratio α_L and average voltage $\overline{V_L}$ are determined, which can be calculated

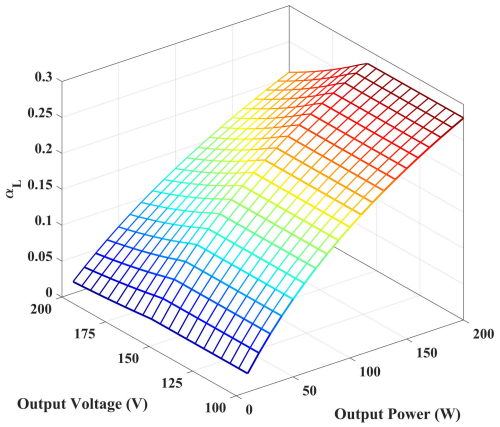


FIGURE 9. α_L under different output power and output voltage, where C_L is selected to the 20 μF.

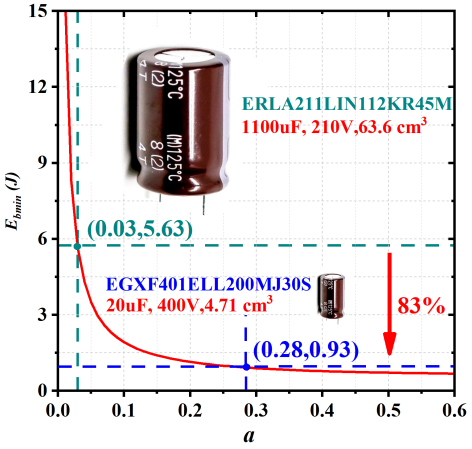


FIGURE 10. The function between α and the required minimum capacity energy E_{bmin}, where P_o is fixed at 200 W, f is fixed at 50 Hz. Note that the proposed method uses dc-link capacitor to buffer the energy and raises α to 0.28. Compared to the conventional method with $\alpha = 0.03$, the system energy storage requirements decreased 83%.

as follows.

$$\begin{cases} \overline{V_L} = \dfrac{A + \sqrt{A^2 + \frac{2P_o}{\omega C_L}}}{2} \\ \alpha_L = \dfrac{B - \sqrt{B^2 - 4P_o^2}}{2P_o} \end{cases} \tag{15}$$

where $B = 2P_o + 2\omega A^2 C_L$.

Fig. 9 shows the α_L under different working conditions when C_L is selected to 20 μF. Note that when the PFC is working at the step-down applications, the α_L is only determined by the output power, whereas in the step-up applications, which is determined by both output voltage and power. Meanwhile, α_L in all the operation conditions satisfy the limitations in Fig. 7. The maximum α_L occurs at $V_o = 100$ V, $P_o = 200$ W, which is 0.28, which can greatly reduce the energy storage capacitors. To clearly illustrate this trend, the E_{bmin} is plotted as function of α according to Eq. (5), as shown in Fig. 10. And compared to the conventional method with $\alpha = 0.03$, the system energy storage requirements decreased 83%. Meanwhile, the same series of capacitors with different parameters are selected for volume comparison according to the design requirements of the conventional and proposed methods. The conventional method requires a volume of 63.6 cm^3 for capacitors, while the proposed method only requires 4.71 cm^3. Furthermore, the smaller energy storage requirements make it possible to replace the electrolytic capacitors with longer life film and ceramic capacitors.

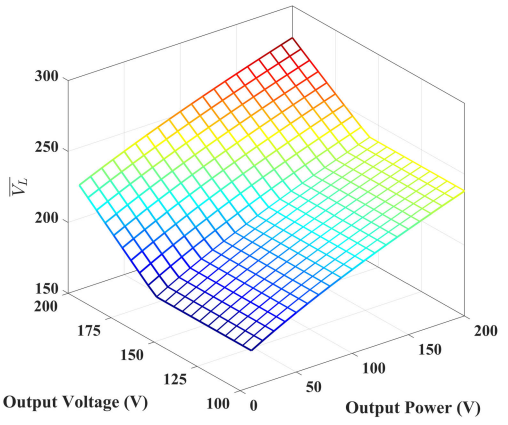


FIGURE 11. $\overline{V_L}$ under different output power and output voltage, where C_L is selected to the 20 μF.

TABLE 2. Normalized comparisons with previous TSBB PFC reports.

	Method	P_o / f	C_b	$\overline{V_{bmax}}$	Results
Ref. [10]	Passive	1 kW / 60 Hz	950 μF	450 V	72.52
Ref. [14]	Passive	0.1 kW / 60 Hz	150 μF	200 V	22.62
Ref. [15]	Passive	2 kW / 60 Hz	1680μF	350 V	38.79
Ref. [30]	Active	0.1 kW / 60 Hz	20 μF	300 V	6.79
Proposed	Active	0.2 kW / 50 Hz	20 μF	277 V	2.41

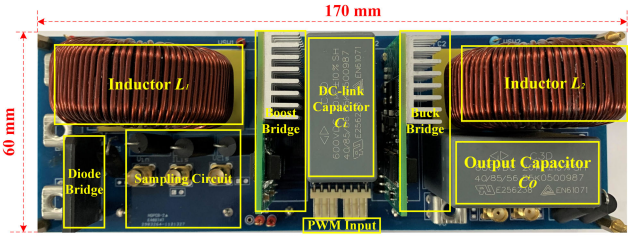
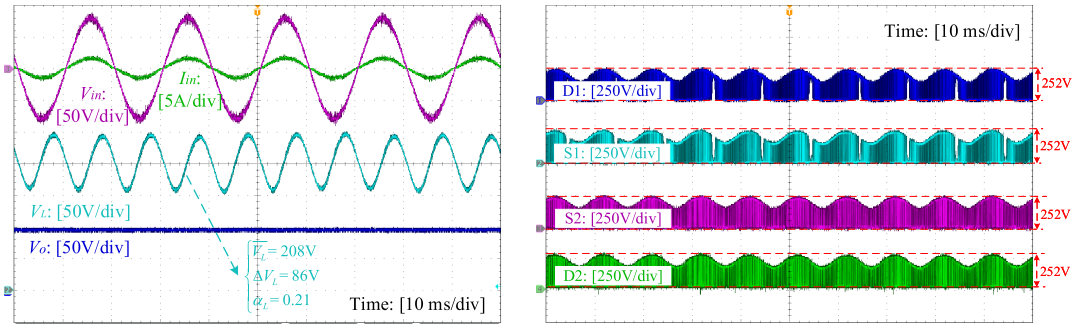


FIGURE 12. GaN-based CBBPFC converter prototype.

Fig. 11 shows the dc-link capacitors average voltage $\overline{V_L}$ under different operation conditions. Similarly, where $\overline{V_L}$ is only determined by the output power in the step-down applications, whereas in the step-up applications, $\overline{V_L}$ is affected both by output power and voltage. And this formula can be used to calculate dc-link capacitors voltage reference value $\overline{V_L}^*$ under different working conditions.

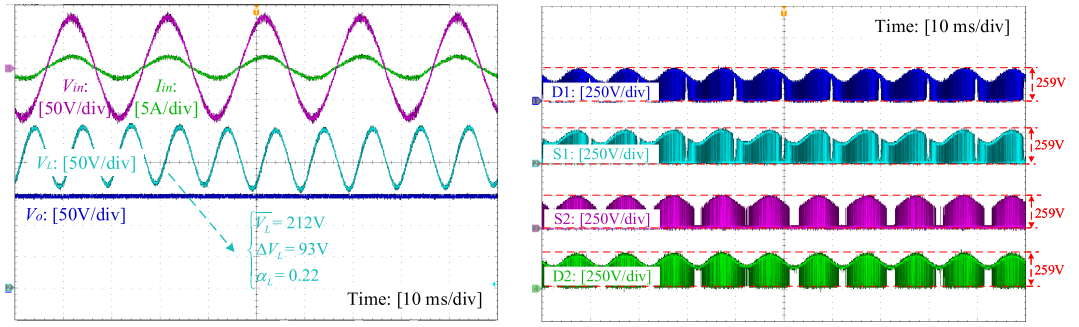
D. COMPARISONS WITH PREVIOUS WORKS

To highlight the effectiveness of the proposed methods in capacitance reduction, a normalized capacitance comparison



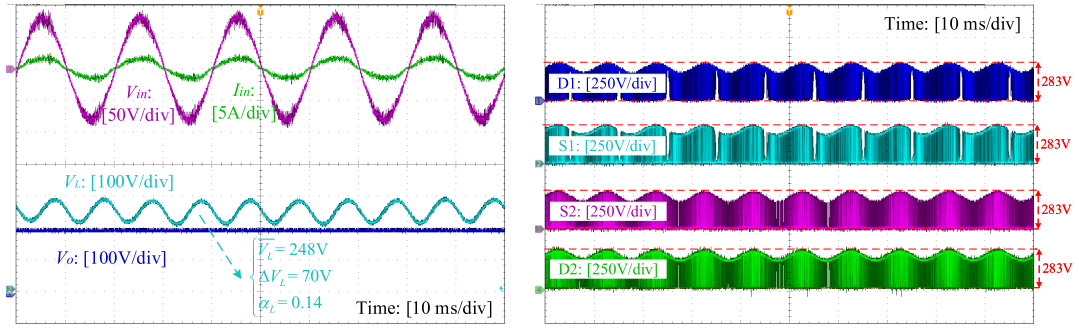
(a)Measured steady-state waveforms; (b) Corresponding waveforms of all devices

FIGURE 13. Measured steady-state waveforms of the CBBPFC converter at V_o = 100 V, P_o = 110 W. Note that unity power factor is achieved and that V_o is well regulated at 100 V without double-line frequency ripple benefit from dc-link capacitors that buffer imbalance power with a large α_L, and all the voltage stresses are depend on the dc-link capacitors voltage.



(a)Measured steady-state waveforms; (b) Corresponding waveforms of all devices

FIGURE 14. Measured steady-state waveforms of the CBBPFC converter at V_o = 150 V, P_o = 125 W. Note that unity power factor is achieved and that V_o is well regulated at 150 V without double-line frequency ripple benefit from dc-link capacitors that buffer imbalance power with a large α_L, and all the voltage stresses are depend on the dc-link capacitors voltage.



(a)Measured steady-state waveforms; (b) Corresponding waveforms of all devices

FIGURE 15. Measured steady-state waveforms of the CBBPFC converter at V_o = 200 V, P_o = 110 W. Note that unity power factor is achieved and that V_o is well regulated at 200 V without double-line frequency ripple benefit from dc-link capacitors that buffer imbalance power with a large α_L, and all the voltage stresses are depend on the dc-link capacitors voltage.

between the proposed work and the previous two-switch buck-boost PFC reports is discussed in this section, including the passive and active solution for buffer the imbalance power.

Since there are differences between the voltage, line frequency, and power rating in our work and the previous related literature reports, all works should be normalized for objective and accurate comparison. From Eq. (5), a normalization factor $K_{p.u.}$ is introduced to strip off the impact of different operating conditions on the comparison results, which can be expressed as

$$K_{p.u.} = \frac{\omega \overline{V_b}^2}{P_o} = \frac{2\pi f \overline{V_b}^2}{P_o} \tag{16}$$

The normalized comparison results can be calculated by $C_b K_{p.u.}$, which are summarized in Table 2. Smaller $C_b K_{p.u.}$, better performance. The results show that the proposed

TABLE 3. System hardware and software parameters.

Parameters	Value	Parameters	Value
Input Voltage	AC 110 V / 50 Hz	L_1	500 μH
Output Voltage	DC 100-200 V	L_2	500 μH
Switching Devices	LMG3410R070	C_L	20 μF
Diodes	RFV8BM6STL	C_o	20 μF
Voltage Controller	20 kHz	Current Controller	100 kHz

coordinated solution and design considerations are more effective than the previous two-switch buck-boost PFC reports in reducing capacitance.

V. EXPERIMENTAL RESULTS

A proof-of-concept 200 W GaN based CBBPFC converter prototype is constructed and tested as shown in the Fig. 12. We use Texas Instruments LMG3410R070 (600 V, 70 mΩ) as the switching devices and Rohm RFV8BM6STL (600 V, 8 A) diodes. And an FPGA (Artix-7 100T AX7102) is used as controller. Table 3 summarizes the circuit hardware parameters. The design of the converter strictly follows that described in Section IV. The calculation frequency of the current controller is higher than the voltage regulators. Here the calculation frequency for the coordinated current controller is equal to the sampling frequency, i.e. 100kHz, whereas the voltage controller is only set to 20kHz to reduce the calculation cost. Benefits from the proposed coordinated two-stage operation, the system energy storage requirements are greatly reduced, here the dc-link capacitors and output capacitors are all 20 μF. The high-reliability film capacitors are used in this prototype design, and the smaller ceramic capacitors in parallel will be a better choice for high power density applications. Meanwhile, the pre-stage filter is eliminated thanks to the two inductors in the structure.

Fig. 13-15(a) shows the steady-state waveforms of the CBBPFC converter with a fixed input AC voltage of RMS 110 V, an output voltage of 100, 150, and 200 V, an output power of 110, 125, and 110 W, respectively. In all the three scenarios, the input current follows the input voltage without phase difference and near unity power factor is achieved. The voltage across the dc-link capacitor C_L is pulsating significantly at a double-line frequency, indicating that C_L is buffering the imbalanced power. Furthermore, the peak-to-peak voltage variations ΔV_L are 86, 93, and 70 V, the average voltages $\overline{V_L}$ are 208 (theoretical: 212 V), 212 (theoretical: 215 V) and 248 V (theoretical: 254 V), the fluctuation ratios α_L are 0.21 (theoretical: 0.19), 0.22 (theoretical: 0.21) and 0.14 (theoretical: 0.13), respectively, which match well with the design specifications in Fig. 9-11 with some allowable errors. Since the imbalanced power is fully buffered by the dc-link capacitor, the output voltage V_o is well regulated to maintain the reference value without double-line frequency ripple. On the other hand, the corresponding voltage waveforms of all devices are shown in the Fig. 13-15(b). Note that the voltage stresses of all devices depend on the voltage of the dc-link capacitor and within the safe operating voltage of the device. Besides that, these waveforms also confirm that the

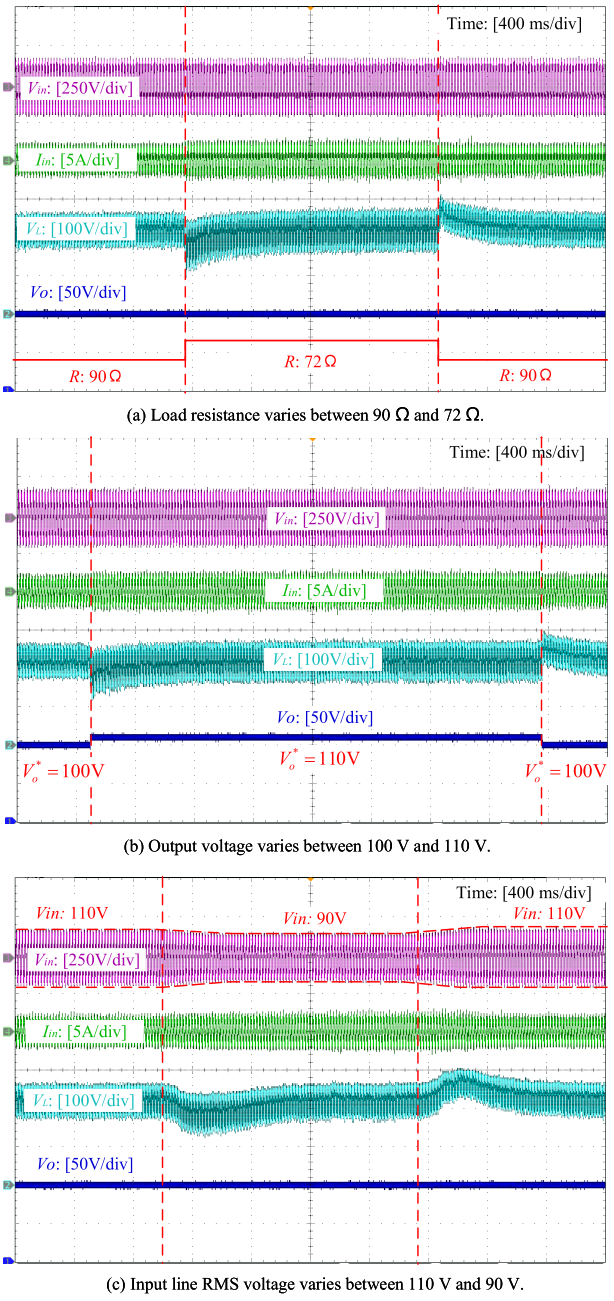


FIGURE 16. Dynamic waveforms of the CBBPFC converter. Note that the dc-link capacitors buffered all the transient imbalance power with instant voltage variations, V_o is almost immune to all the disturbances and retains tight dc voltage regulation during those transient processes.

CBBPFC has both voltage step-down (AC 110 V - DC 100 V) and step-up (AC 110 V - DC 200 V) capabilities and a wide output voltage range is attainable.

Fig. 16 shows the dynamic waveforms of the CBBPFC converter in response to (a) a step change of output power, (b) a step change of output voltage and (c) a step change of input line voltage. In Fig. 16 (a), the step change of the output power will produce a sudden change of the imbalance power, resulting in instant voltage variations for V_L. Thanks

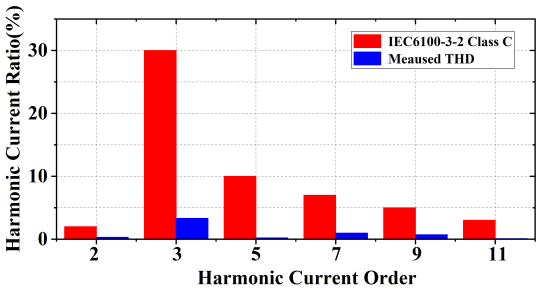


FIGURE 17. Measured input current harmonics in comparison with IEC 61000-3-2 class C.

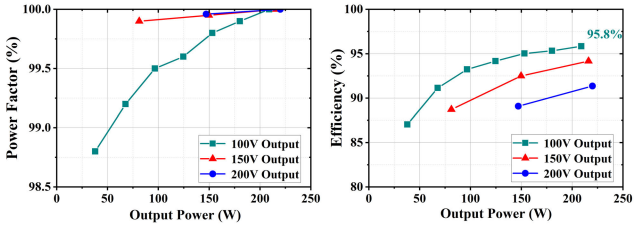


FIGURE 18. Measured power factor and efficiency across the entire load range and different output voltage.

for the dc-link capacitors buffer all the imbalance power, the output voltage is well regulated by the coordinated controller to maintain the reference without any disturbances. Fig. 16(b) shows the dynamic waveforms for V_o^* varies between 100 V and 110 V. Note that all the transient imbalance power is fully buffered by the dc-link capacitors, the output voltage can rapidly track the reference value without any fluctuation. Fig. 16(c) shows the waveforms for the input line voltage varies between 110 V and 90 V. Similar to the Fig. 16(a), all the transient imbalance power are fully buffered by the dc-link capacitors with instant voltage variations, V_o is almost immune to all the disturbances and the controller retains tight dc voltage regulation during those transient process.

Fig. 17 records the input current spectrum of the input current at 200 V, 220 W. The results show that the CBBPFC converter meets IEC 61000-3-2 Class C standards while achieving a power factor of 0.99 and a total harmonics distortion of 5.3% even without the pre-stage filter.

The efficiency and power factor performance across the entire load range and different output voltage are plotted in Fig. 18. Benefits from the two inductors, high power factor ($\geq$0.99) can be easily achieved for a wide load range even without the front-stage filter. The power factor lower than 0.99 only occurs at 100V, 38W, mainly caused by the quantization errors of the ADCs.

The peak efficiency occurs at the 210W, 100V output voltage, which is 95.8%. In low-power PFC applications, a drop in efficiency is inevitable as the output voltage increased. It is caused by the increase in device stress. Several methods can improve this condition. One solution is to replace the diodes D_1 and D_2 with active switches, which can not only reduce losses but also enable the ability of bidirectional operation. Similar operations are widely used in totem pole bridgeless PFC [38]. Another way is to use some optimization algorithms (such as particle swarm optimizer, grey wolf optimizer) to optimize the operation state to find the best performance point in real-time. Especially for the dc-link capacitor voltage, it directly determines the voltage stress of all devices, thereby affecting the efficiency of the entire converter. This paper focuses on the coordinated operation and control strategy for minimizing energy storage capacitors in CBBPFC converters, the efficiency improvement methods will be discussed in future publications.

VI. CONCLUSION

In this paper, a coordinated two-stage operation and control method for the CBBPFC converter to minimize energy storage capacitors is proposed. By fully exploiting all operations states, the dc-link capacitors can be used to buffer double-line frequency imbalance power with a large dc-link voltage fluctuation. The proposed solution makes it possible to replace the bulky electrolytic capacitors with longer life film and ceramic capacitors, enabling the CBBPFC converters to achieve simultaneously high power density, wide conversion ratio, high power factor and high reliability. A coordinated control scheme and a fluctuation-ratio based design consideration are detailed to complement the system design. A 200W CBBPFC prototype with maximum 83%-reduced energy storage requirements exhibits a peak efficiency of 95.8% and a near-unity power factor.

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