IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received September 29, 2020, accepted October 8, 2020, date of publication October 12, 2020, date of current version October 23, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3030269

Measurement of Power Dissipation Due to Parasitic Capacitances of Power MOSFETs

UTKARSH JADLI, (Student Member, IEEE), FAISAL MOHD-YASIN, (Senior Member, IEEE), HAMID AMINI MOGHADAM, PEYUSH PANDE, (Member, IEEE), JORDAN R. NICHOLLS, AND SIMA DIMITRIJEV, (Senior Member, IEEE)

Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, QLD 4111, Australia
School of Engineering and Built Environment, Griffith University, Brisbane, QLD 4111, Australia

Corresponding author: Utkarsh Jadli (utkarsh.jadli@griffithuni.edu.au)

This work was supported in part by the Innovative Manufacturing Cooperative Research Centre (IMCRC), in part by the BlueGlass as the Industry Partner under Grant 220132, in part by the Queensland Node of the Australian National Fabrication Facility, a company established through the National Collaborative Research Infrastructure Strategy to provide nano- and microfabrication facilities for Australia's researchers, and in part by the School of Engineering and Built Environment (EBE), Griffith University.

ABSTRACT Analysis of the switching losses in a power MOSFET is crucial for the design of efficient power electronic systems. Currently, the state-of-the-art technique is based on measured drain current and drain-to-source voltage during the switching intervals. However, this technique does not separate the switching power due to the resistance of the MOSFET channel and due to the parasitic capacitances. In this paper, we propose a measurement method to extract the power dissipation due to the parasitic capacitances of a MOSFET, providing useful information for device selection and for the design of efficient power electronic systems. The proposed method is demonstrated on a basic boost converter. The proposed method shows that the existing method underestimates the turn-On losses by 41% and overestimates the turn-Off losses by 35%.

INDEX TERMS Channel current, current diversion phenomenon, C_{OSS} losses, efficiency, power losses, power MOSFET, switching losses.

I. INTRODUCTION

With the increase in demands for electricity and the explosion in renewable energy technologies, power electronics is playing a vital role in benefiting society. The progress of power electronic systems is being driven by advancements in power semiconductor devices [1]. As the market for power devices continues to grow, it is becoming increasingly important to select the appropriate power device for a given application. One of the most important parameters for selection of a power device is its power dissipation, and so an understanding of the power losses is crucial.

The most commonly used power switching device, the power MOSFET, exhibits two types of losses: switching losses and conduction losses. Operation at high frequencies is desirable to reduce the overall converter size but, on the other hand, it also results in an increase in the MOSFET switching losses. Therefore, to obtain a high efficiency design, it is necessary to accurately determine the switching losses of the power MOSFET.

The associate editor coordinating the review of this manuscript and approving it for publication was Alexander Micallef.

The current state-of-the-art technique for measuring switching loss of a power MOSFET is performed by integrating the product of the drain-to-source voltage (v_{DS}) and drain current (i_D). However, the dynamic characteristics of a power MOSFET are affected by the various parasitic capacitances in the device [2]. These are not considered when applying the standard technique, which leads to underestimation and an overestimation of the power losses during the turn-On and turn-Off intervals, respectively. In order to account for these capacitances, we need to know the difference between the total current through the drain terminal (i_D) and the current flowing through the channel (i_{CH}).

The ability to separate i_{CH} from i_D enables proper analysis of charging and discharging of the effective output capacitance (C_{OSS}) and its corresponding power dissipation. This knowledge aids in the selection of the appropriate MOSFET for a particular application. In response to this need, various modeling and simulation techniques have been used to analyze the difference between i_{CH} from i_D and the impact of this difference on the switching power losses [3]–[9]. Although simulation-based analyses provide useful insights, measurements with real MOSFETs and in real circuits are necessary to obtain the ultimate results. Unlike simulation

and modeling, the only current that can be measured in a packaged MOSFET is the current flowing through the drain terminal. It appears that this has been seen as an unavoidable limit and, consequently, no measurement results separating i_{CH} from i_D have been reported. In this paper, we show how to avoid this perceived limit by employing a combination of static and dynamic measurements, which results in a novel experimental method for extracting i_{CH} of a power MOSFET. With this technique, measured switching losses can be split into contributions due to the parasitic capacitances and due to the channel resistance. We demonstrate our technique by applying it to the practical measurements of a boost converter.

This paper is divided into the following sections: Section II will discuss the limitations of the current existing technique for measuring power losses. Section III will give a detailed description of the experimental setup and the measuring instruments. Proposed methodology for extracting i_{CH} is presented in Section IV. The results and discussions are presented in Section V. Section VI will conclude and foreshadow potential future work.

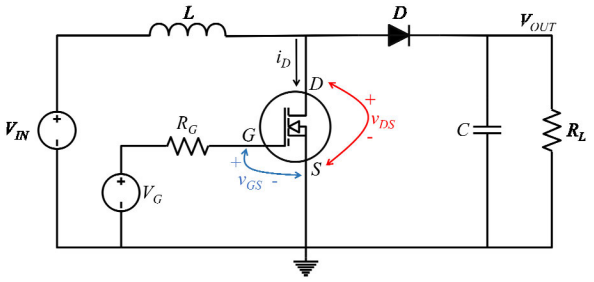


FIGURE 1. Typical boost converter.

II. LIMITATIONS OF THE EXISTING POWER ANALYSIS TECHNIQUES

In order to show the limitations of the existing technique for analysis of switching power loss, a typical boost converter utilizing a power MOSFET is selected and shown in Fig. 1. Fig. 2 shows the experimental switching waveforms measured across the power MOSFET for a single period.

According to the existing method, the power dissipated in a power MOSFET during switching intervals (P_{SW}) is obtained by integrating the product of the measured voltage (v_{DS}) and the measured current (i_D) [10]:

$$P_{SW} = f \int v_{DS}(t) \times i_D(t) dt \tag{1}$$

Here, f represents the switching frequency and the integration is performed during the switching intervals, t_{ON} and t_{OFF}. The turn-On losses (P_{ON}), and turn-Off losses (P_{OFF}) are shown in Fig. 3. Together, these constitute the switching losses (P_{SW}). Note that the P_{OFF} losses are higher than P_{ON} losses due to the charging of the inductor during the conduction period. Similarly, the conduction losses (P_{CON}) in a MOSFET (as depicted in Fig. 3) can also be calculated by (1) using t_{CON} as the integration interval.

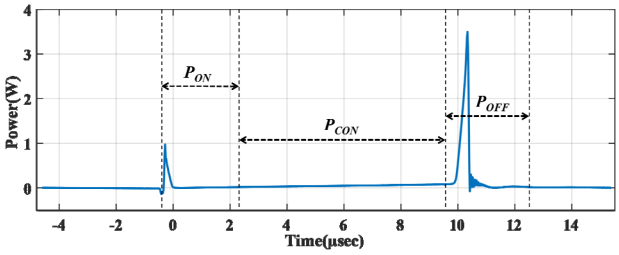


FIGURE 3. Power losses corresponding to the switching waveforms depicted in Fig. 2 for a single period.

Estimation of the switching losses in a power MOSFET using (1) is widely performed by many researchers and manufacturers [10]–[14]. However, with the advancement in MOSFETs for high voltage applications, it was realized that the effective output capacitance (C_{OSS}), which is defined as the sum of the gate-to-drain capacitance (C_{GD}) and the drain-

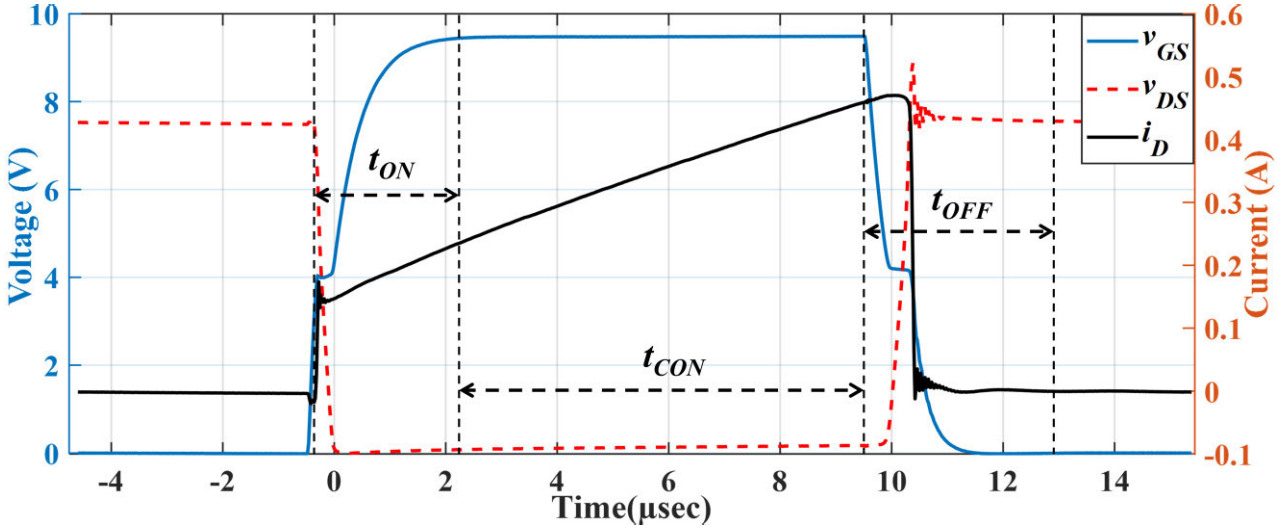


FIGURE 2. Measured switching waveforms of a power MOSFET while operating as the switch in the boost converter shown in Fig. 1; v_{DS} is the measured drain-to-source voltage, v_{GS} is the measured gate-to-source voltage, i_D is the measured drain current flowing into the power MOSFET, t_{ON}, t_{OFF}, and t_{CON} are the turn-On, turn-Off, and conduction intervals, respectively.

to-source capacitance (C_{DS}), also plays a significant role in MOSFET power losses during the switching intervals [2], [3]. During the turn-Off interval, C_{OSS} stores some energy, and then dissipates it in the channel of the MOSFET during the turn-On interval. Initial attempts to include the losses due to C_{OSS} added an additional term to (1) [2], [15]–[18]:

$$P_{SW} = f \int v_{DS}(t) \times i_D(t)dt + \frac{1}{2} C_{OSS} v_{DS}^2 f \tag{2}$$

Here, the newly added term in (2) is generally known as the output capacitance loss term. The inclusion of the C_{OSS} loss term was very controversial for many years, until the discrepancy was cleared by Xiong *et.al.* [3]. Using a mixed device modelling approach, they simulated the channel current (i_{CH}) and demonstrated its effect during the transition period. It was revealed that the first term of (2) underestimates P_{ON} and overestimates P_{OFF}. They showed that the net difference in the power losses during switching intervals does not justify the addition of the C_{OSS} loss term [the second term in (2)]. In other words, it was found to be specious and redundant. Also, by careful analysis of the results shown in [3], it is clear that the estimation of switching losses using (1) is erroneous, as the current that flows through the channel of the MOSFET (i_{CH}) is not equal to i_D during the switching intervals. It is also worthwhile to note that the switching loss, as depicted in Fig. 3, is comprised of two losses: a loss due to the channel resistance and a loss due to C_{OSS} charging and discharging. These cannot be separated by using (1).

Recently published papers, have shown the impact of displacement currents due to C_{OSS} during turn-On and turn-Off intervals, and how they directly affect the calculation of switching losses [4]–[7]. The equivalent circuit of the power MOSFET, as shown in Fig. 4, can be used to elucidate this current displacement phenomenon during switching intervals.

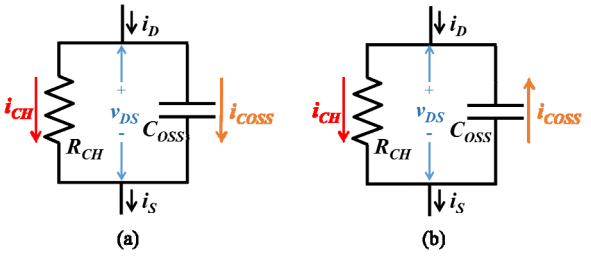


FIGURE 4. MOSFET equivalent circuit while charging and discharging of C_{OSS} during (a) turn-Off and (b) turn-On interval.

Referring to Fig. 4(a), when the MOSFET is turning off, i_D gets divided into two components: one component of the i_D flows through the channel of the MOSFET (i_{CH}), and the other component of i_D, which is i_{COSS}, charges the C_{OSS} up to the maximum of v_{DS}. Similarly, when the MOSFET is turning on, as illustrated in Fig. 4(b), the stored energy in the C_{OSS} is being discharged in the channel of the MOSFET. Hence, it is obvious that, during switching intervals depicted in Fig. 2, the measured drain current i_D is not equal to i_{CH}.

Castro *et al.* [5] demonstrated the current displacement phenomenon in superjunction MOSFETs using a mixed-mode simulation approach. They developed an analytical model to obtain i_{CH} and used this current to determine the switching power losses:

$$P_{SW} = f \int v_{DS}(t) \times i_{CH}(t)dt \tag{3}$$

Using (3), Castro *et al.* [5] found that the modification does not affect the total switching loss, but it redistributes the losses between P_{ON} and P_{OFF}. They also showed that without the current displacement phenomenon, the P_{ON} and P_{OFF} losses were underestimated and overestimated by 25% and 200%, respectively [5]. Hence, it is quite evident from their results that the switching losses in a MOSFET should be obtained with i_{CH} rather than i_D.

Two other groups [8], [9], have also estimated the switching loss by modeling i_{CH} for specific power MOSFETs and SiC transistors. However, in a real life scenario, i_{CH} flows inside a packaged MOSFET and cannot be directly measured, while calculating it by analytical modeling is time consuming and device-specific [5]–[9]. In Section IV, we aim to address these limitations by proposing a measurement method to extract i_{CH} for all types of transistors.

III. EXPERIMENTAL SETUP

We have used the typical boost converter, shown in Fig. 1, to explain the new measurement method using real experimental data. The components we used for this boost converter are listed in Table 1. The converter is operated at a switching frequency of 50 kHz using an AFG1022 function generator. In order to measure the voltages $v_{GS}(t_s)$ and $v_{DS}(t_s)$ and the current $i_D(t_s)$ with sufficient accuracy, probes and oscilloscopes of sufficient bandwidth must be used [19]. For this reason, a careful selection of the measurement setup was required, and is listed in Table 2. Note that the effect of parasitic capacitance of the probes on the measurements is negligible due to low operating switching frequency. Furthermore, MATLAB is used for processing the measured data.

TABLE 1. Components of the boost converter.

No.	Circuit Element	Value/Model
1.	L	90.7 µH
2.	C	220 µF
3.	*MOSFET*	IRF540
4.	*Diode*	SR310
5.	R_G	10 Ω
6.	R_L	50 Ω

The static *I-V* characteristics for the power MOSFET *IRF540* were measured with Agilent Power Device Analyzer

TABLE 2. Description of the measurement system.

Part No.	Manufacturer	Description	Bandwidth	Measured Signal
DPO7104	Tektronix	Digital Phosphor Oscilloscope	1 GHz	-
THDP0200	Tektronix	Differential Probe	200 MHz	v_{DS} & v_{GS}
TCP0030	Tektronix	Current Probe	120 MHz	i_D

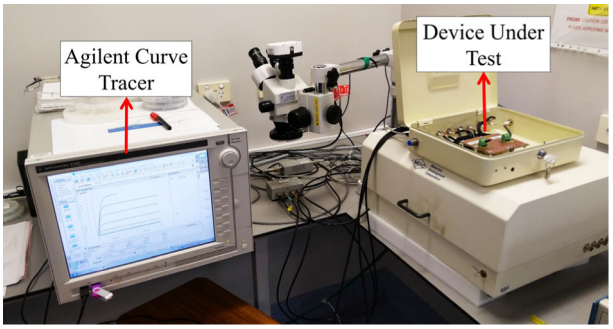


FIGURE 5. Measurement setup for measuring static *I-V* characteristics.

(B1505A) using four-point probe measurement. The setup to measure static *I-V* characteristics is shown in Fig. 5 and will be explained in detail in the next section.

IV. PROPOSED METHOD

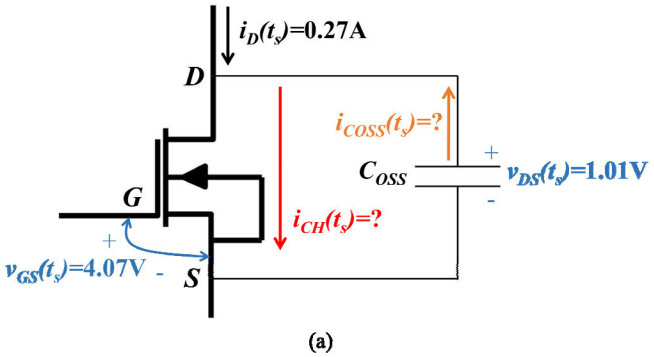
A. EXTRACTING i_{CH} FOR TURN-ON INTERVAL

The MOSFET is operating as a switch in the boost converter and is in the turn-On mode when v_{GS} is larger than the threshold voltage. As discussed in Section II, during the turn-On interval, C_{OSS} discharges its energy into the channel of the MOSFET and is shown by the equivalent circuit in Fig. 6(a).

During the MOSFET turn-On operation, the instantaneous value of rising gate-to-source voltage, $v_{GS}(t_s)$, and falling drain-to-source voltage, $v_{DS}(t_s)$, can be measured by the setup described in the previous section. The measured results are shown in Fig. 6(b) where t_s is the sample time at which the measurement is performed.

To explain the method of extracting the channel current $i_{CH}(t_s)$ from the measured drain current $i_D(t_s)$, we will focus on the specific sampling time $t_s = 0.46\ \mu$s. At that instant of time, the measured voltage between the drain and the source is $v_{DS}(t_s) = 1.01$ V, the measured voltage between the gate and the source is $v_{GS}(t_s) = 4.07$ V, and the measured drain current is $i_D(t_s) = 0.27$ A, as shown in Fig. 6. Now we need to determine how much current $i_{COSS}(t_s)$ is supplied by C_{OSS} and is discharged into the channel of the MOSFET at $t_s = 0.46\ \mu$sec. Due to the nonlinear voltage dependency of both C_{DS} and C_{GD}, calculating the current flowing through the equivalent capacitance $C_{OSS} = C_{DS} + C_{GD}$ is quite challenging and unreliable. Hence, much better option is to determine the channel current $i_{CH}(t_s)$.

In order to extract i_{CH} at the sample time $t_s = 0.46\ \mu$s, the same MOSFET is taken out of the boost circuit and is measured at static condition using instruments described in Section III. While measuring the MOSFET in static conditions, the same bias voltages are applied to the MOSFET, which are $V_{DS} = v_{DS}(t_s) = 1.01$ V and $V_{GS} = v_{GS}(t_s) = 4.07$ V, as shown in Fig. 7(a). Traditionally, *I–V* characteristics are measured by sweeping V_{DS} from 0 to the required value, for set values of V_{GS}. However, device heating due to the continuous power dissipation could increase the temperature and impact the measured results. To avoid this issue, high grade instruments such as the Agilent Power Device Analyzer provide the option of pulsed *I–V* measurements. An important feature for measuring static *I–V* characteristics is that the measuring instrument takes some finite amount of time



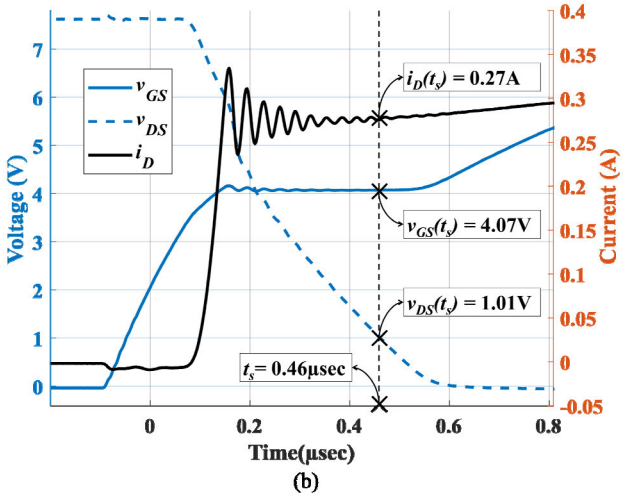


FIGURE 6. (a) Equivalent circuit of a MOSFET operating in the boost circuit during the turn-On interval, showing that $C_{OSS} = C_{DS} + C_{GD}$ discharge their currents ($i_{COSS} = i_{DS} + i_{GD}$) into the MOSFET channel. The numerical values of the voltages and the current are shown at the sample time of 0.46 μs. (b) Switching waveforms of the MOSFET operating in the boost configuration during the turn-On interval (t_{ON}).

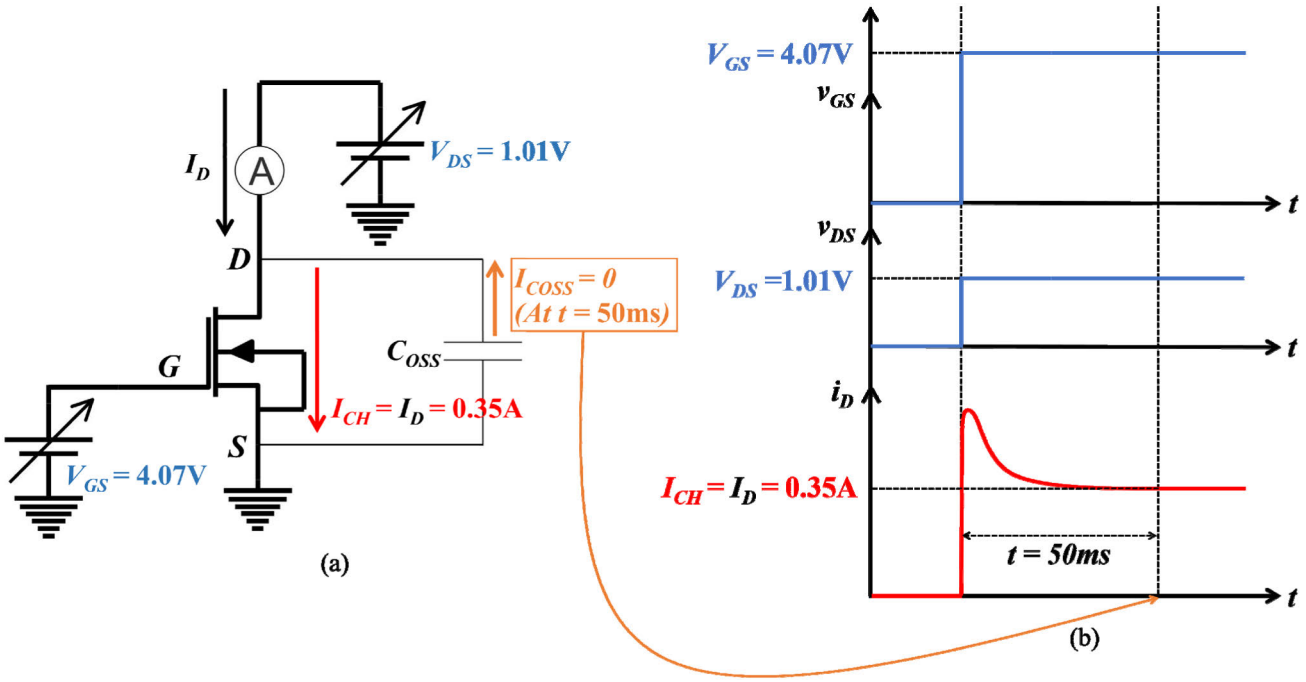


FIGURE 7. (a) MOSFET is set at static (DC) voltages $v_{GS}(t_s) = V_{GS} = 4.07$ V and $v_{DS}(t_s) = V_{DS} = 1.01$ V to measure the corresponding static (DC) current $I_{CH} = I_D$. (b) Pulsed I-V measurement using Agilent Power Device Analyzer with the transient settling time of 50 ms.

to settle down the transients, as illustrated in Fig. 7(b). In our example, when the bias voltages are pulsed to $V_{GS} = 4.07$ V and $V_{DS} = 1.01$ V, the Agilent Power Device Analyzer takes approximately 50 ms to settle down the transients before the drain current is measured.

In principle, I_{CH} can be calculated by using a suitable model for the static current–voltage characteristics of the MOSFET. To illustrate this point, we can use the simple equation for a MOSFET in triode region [20]:

$$I_D = I_{CH} = \beta[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \tag{4}$$

To use this equation, we need to know the values of the threshold voltage (V_T) and the transconductance parameter (β) for the specific MOSFET that is used in the practical circuit. To enable circuit simulation, many manufacturers provide complex MOSFET models with extracted parameter values, but these models may not provide sufficiently precise match to the experimental I–V characteristics of specific MOSFETs. Therefore, static measurements of I_{CH} are much more simple and reliable.

A MOSFET operating in a circuit has continuously changing voltages and currents, which results in a large number of sampling points. Therefore, it is quite impractical to manually measure the MOSFET static behavior at each of these sample points. In order to solve this issue the I–V characteristics of the power MOSFET IRF540 are measured with a small step size. In our example, the power MOSFET IRF540 was measured with the step size of 50 mV for V_{GS} and V_{DS}. The points between the measured values were interpolated using spline interpolation in MATLAB, which did not cause errors because the measurements were performed with sufficiently small step size of 50 mV. Hence, the data collected from the measured I–V characteristics with such great resolution served as a lookup table to extract $i_{CH}(t_s)$ for corresponding $v_{GS}(t_s)$ and $v_{DS}(t_s)$ values during the entire turn-On interval. The obtained current $i_{CH}(t_s)$ is shown in Fig. 8. The difference $i_{CH}(t_s) - i_D(t_s)$ is equal to the current from the discharging capacitance C_{OSS}.

B. EXTRACTING i_{CH} FOR TURN-OFF INTERVAL

As discussed in Section II and illustrated by the equivalent circuit in Fig. 9(a), C_{OSS} is charged during the turn-Off interval. Again, the instantaneous value of the falling

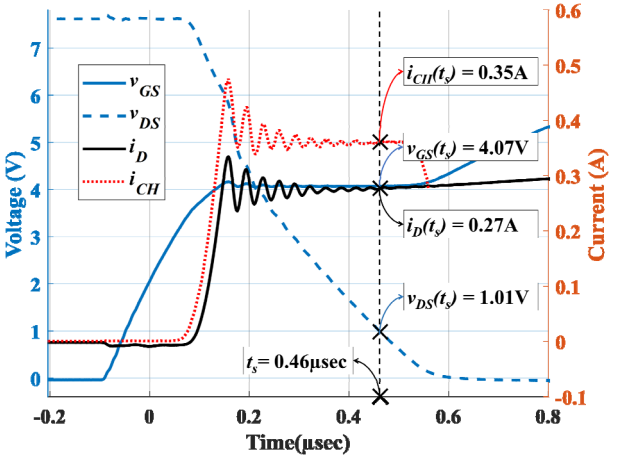


FIGURE 8. The extracted i_{CH} during turn-On interval is plotted alongside v_{GS}, v_{DS}, and i_D.

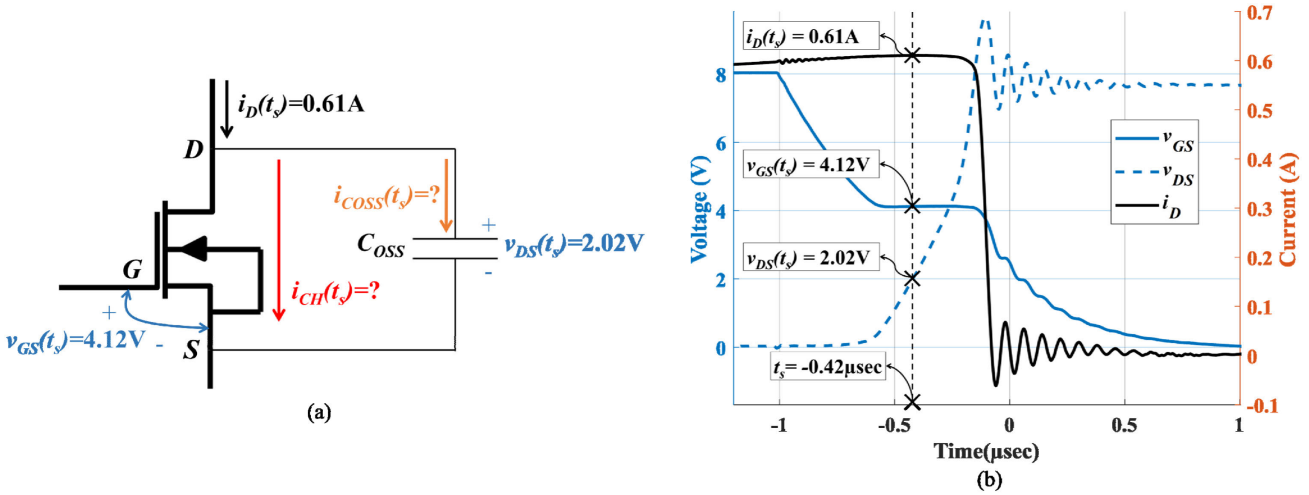


FIGURE 9. (a) Equivalent circuit of the MOSFET operating in the boost circuit during the turn-Off interval, showing that i_D splits into i_{CH} and i_{COSS}. The values of the voltages and the current correspond to the sample time of −0.42 μs. (b) Switching waveforms of the MOSFET operating in the boost converter during the turn-Off interval (t_{OFF}).

gate-to-source voltage, $v_{GS}(t_s)$, and the rising drain-to-source voltage, $v_{DS}(t_s)$, can be directly measured by the setup described in Section III and the results are shown in Fig. 9(b), where t_s is the sample time at which the measurement is performed.

Taking as an example $t_s = -0.42$ μs, the measured voltage between the drain and the source is $v_{DS}(t_s) = 2.02$ V, the measured voltage between the gate and the source is $v_{GS}(t_s) = 4.12$ V, and the measured drain current is $i_D(t_s) = 0.61$ A, as shown in the Fig. 9. Analogously to the turn-On interval, we need to determine how much current $i_{CH}(t_s)$ is flowing through the channel of the MOSFET at that instant of time. Just like it was done for the turn-On interval, we use the measured I–V characteristics of the MOSFET to obtain the current for the bias voltages of $V_{DS} = v_{DS}(t_s) = 2.02$ V and $V_{GS} = v_{GS}(t_s) = 4.12$ V and the result is $I_D = i_{CH}(t_s = 0.42\ \mu s) = 0.42$ A. Repeating this procedure, $i_{CH}(t_s)$ can be obtained for the entire turn-Off interval, and the result is shown in Fig. 10.

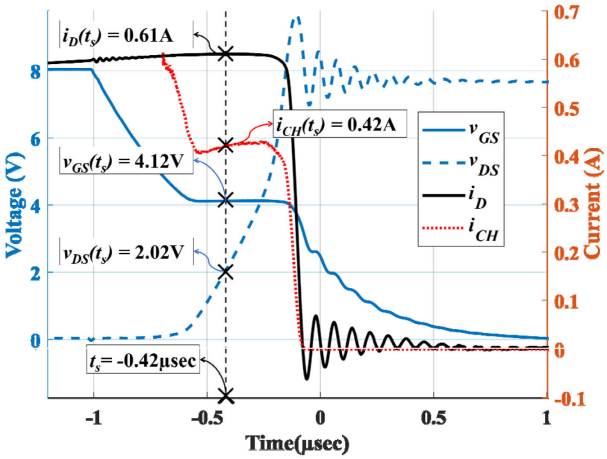


FIGURE 10. The extracted i_{CH} during turn-Off interval is plotted alongside v_{GS}, v_{DS}, and i_D.

The obtained results for both turn-On and turn-Off intervals are discussed in detail in the next section.

V. RESULTS AND DISCUSSION

The previous section clearly shows the effectiveness of the proposed method to extract i_{CH} during switching intervals. During turn-On interval, the extracted i_{CH} is larger than i_D because C_{OSS} is discharging into the channel of the MOSFET. During the turn-Off interval, the extracted i_{CH} was smaller than the i_D, reflecting the fact that i_D is divided between i_{CH} and the current charging C_{OSS}, i.e. i_{COSS}. This is consistent with the current displacement phenomenon discussed in Section II.

A. VALIDATION OF THE PROPOSED METHOD

To further validate the proposed method, we use the energy conservation principle. According to this principle, the estimation of energy loss by the MOSFET using the extracted i_{CH} should match the estimation by the prevailing calculation using i_D. The only difference between these two approaches will be the distribution of power during the turn-On and turn-Off intervals. The turn-On (E_{ON}) and turn-Off (E_{OFF}) energy losses obtained by both methods are shown in TABLE 3. Both equations, (1) and (3), use the same integration limits. For E_{ON}, the integration limits are defined from the start to the end of the falling v_{DS} waveform, as shown

TABLE 3. Calculation of energy losses.

Energy Losses	Calculated by $\int v_{DS}(t) \times i_D(t) dt$	Calculated by $\int v_{DS}(t) \times i_{CH}(t) dt$
E_{ON}	0.30 µJ	0.51 µJ
E_{OFF}	1.00 µJ	0.74 µJ
$E_{SW} = E_{ON} + E_{OFF}$	1.30 µJ	1.25 µJ

in Fig. 8. For E_{OFF}, the integration interval is from the start to the end of the rising v_{DS} waveform, as shown in Fig. 10. It is clear from TABLE 3 that the total switching energy loss (E_{SW}) from both methods is quite similar. In other words, our method of using extracted i_{CH} adheres to the energy conservation principle. There is a slight discrepancy, which is due to limited measurement accuracy.

We would like to provide further insight on the power distribution within MOSFET by plotting P_{ON} and P_{OFF} of IRF540 using both methods. The results are shown in Fig. 11. It is clear from this figure and the data in TABLE 3 that the existing method using i_D underestimates the turn-On losses by 41.2% and overestimates the turn-Off losses by 35.1%. Castro *et al.* [5] documented similar finding on superjunction MOSFETs using analytical modeling. This percentage of energy loss distribution depends on both the voltage and the MOSFETs used. The usage of different MOSFETs will change C_{OSS} and, hence, will change the energy loss distribution. Furthermore, C_{OSS} of each MOSFET depends on the voltage across the MOSFET, which means the energy loss distribution for turn-On and turn-Off will be different for different voltages.

It is also worthwhile to note that the energy conservation principle holds only if the energy stored in the C_{OSS} during turn–Off interval is being dissipated during the turn-On interval. At a particular voltage, using the fixed value of C_{OSS} from the datasheet for calculating the stored energy can result in a huge error [21]. Hence, with the help of the extracted i_{CH}, it is quite easy to obtain the current i_{COSS} flowing through the C_{OSS} during the switching intervals, which is given as:

$$i_{COSS}(t) = |i_{CH}(t) - i_D(t)| \tag{5}$$

Here, the absolute sign in (5) is used to simplify the C_{OSS} energy calculation. Using (5), the energy stored/dissipated by the C_{OSS} can be calculated as:

$$E_{stored/dissipated} = \int v_{DS}(t) \times i_{COSS}(t)dt \tag{6}$$

TABLE 4 shows the energy that is stored and dissipated by C_{OSS} of IRF540. We use the same integration limits to calculate the energy losses. It is evident from TABLE 4 that the conservation of energy is preserved and therefore supports the justification for removing the C_{OSS} loss term from (2) as described by Xiong *et al.* [3]. A slight difference is credited to the limited measurement accuracy. The empirical results that are shown in TABLES 3 and 4 validate the proposed method.

TABLE 4. Calculation of C_{OSS} energy.

Energy	Value
Stored in the C_{OSS}	0.26 µJ
Dissipated by the C_{OSS}	0.22 µJ

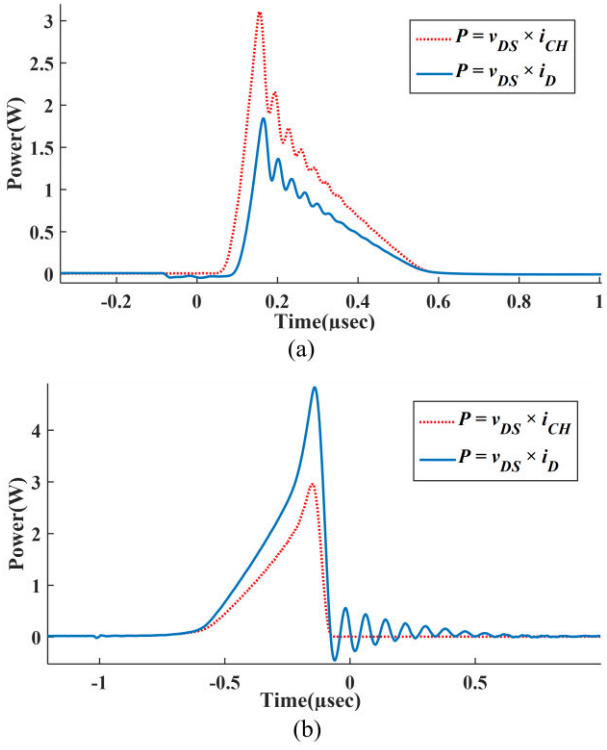


FIGURE 11. Plots of (a) P_{ON} and (b) P_{OFF} for IRF540. The red dotted line represents the switching loss calculation using extracted i_{CH}, while the solid blue line represent the commonly used switching loss calculation using i_D. The latter method underestimate the power loss during turn-On interval and overestimate the power loss during turn-Off interval.

B. ENERGY DISSIPATION DURING THE CONDUCTION INTERVAL

To obtain the total energy loss during the complete switching period $T = t_{ON} + t_{OFF} + t_{CON}$, we need to add the energy losses during the conduction interval. During the conduction interval the channel current is equal to the drain current flowing though the MOSFET. Hence, the conduction loss can be obtained using either current and is given by:

$$E_{CON} = \int v_{DS}(t) \times i_{CH}(t)dt = R_{DS(ON)} \int i_{CH}(t)^2 dt \tag{7}$$

Here, $R_{DS(ON)}$ is the drain to source on-state resistance, which is generally provided by the manufacturers in the datasheets. For better power-conversion efficiency, the device manufacturers keep $R_{DS(ON)}$ to minimum so that the conduction losses of the MOSFET can be minimized.

As can be seen from (7), there are two options to estimate conduction losses. One from the measured v_{DS} and i_{CH} and another from the datasheet $R_{DS(ON)}$ and the measured i_{CH}. However, referring to Fig. 8 and Fig. 10, it is clearly noticeable that the extraction of i_{CH} is only performed during t_{ON} and t_{OFF}, and not during the t_{CON}. This is due to the low $R_{DS(ON)}$ of the IRF540 whose value is given in the datasheet as 77 mΩ. Lower $R_{DS(ON)}$ results in very small drain to source voltage in the conduction region—in order of millivolts. Since the values of v_{DS} are so small, the extraction of i_{CH} is quite challenging due to the limited sensitivity of the differential probes. Moreover, if the measurement error of small v_{DS} is large, it will eventually result in a large error in the extracted i_{CH}. Therefore, instead of measuring v_{DS},

$R_{DS(ON)}$ from the datasheet can be easily used to estimate conduction losses.

C. IMPACT OF THE SWITCHING FREQUENCY ON THE ENERGY DISTRIBUTION

From (1) and (3), it is clear that the switching loss in the switch is directly proportional to the switching frequency. Using the same boost configuration, we varied the operating frequency and the resulting distribution of energy losses by the MOSFET during turn-On and turn-Off intervals is shown in Fig. 12. It is evident that the error in estimating the distribution of energy losses during switching intervals is significant if the energy loss is calculated by $\int v_{DS} \times i_D dt$. Although the total switching losses are the same, there are implications for the design of the control circuitry in terms of minimizing the

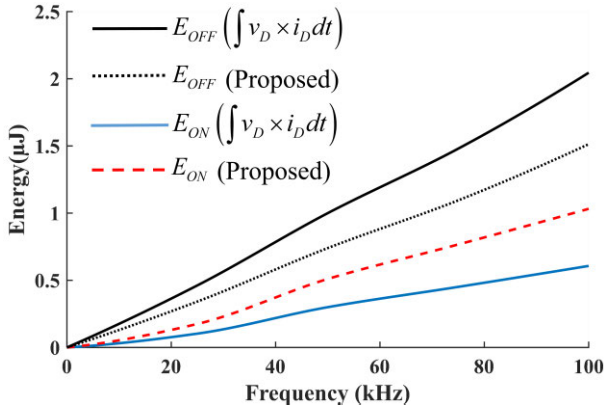


FIGURE 12. Energy losses distribution with increasing frequency.

switching losses. Furthermore, different switching strategies critically rely on the accurate estimation of the switching losses. Hence, the proposed method can be very helpful when designing converters with high efficiency.

VI. CONCLUSION

The proposed experimental method to extract i_{CH} inside MOSFETs is successfully demonstrated in order to calculate switching power loss due to the parasitic capacitances. The power dissipation measured by the proposed method is not affected by the voltage dependence of the parasitic capacitances. Hence, this versatile and facile method can be applied to any device, either in simulation or experiments. In this paper, we test it on IRF540 that is employed as a switch in a basic boost converter. For comparison, the energy losses in the device during switching were calculated using both the new and the existing method. This comparison demonstrated that the new method can accurately measure the distribution of energy loss during turn-On and turn-Off intervals. Furthermore, the new method can be used to determine accurately the energy stored in the MOSFET's output capacitances. The results obtained by the proposed method are also compared to the existing method for different switching frequencies. The difference between the distributions of energy losses shows the importance of the proposed method when designing more efficient power circuits. Another implications of this finding is that circuit designers can use it to select the most suitable transistor for converter configurations at specific voltage and frequency.

REFERENCES

[1] H. Alan Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor Devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015.

[2] J. Wang, H. S.-H. Chung, and R. T.-H. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[3] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. John Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009.

[4] V. Hoch, J. Petzoldt, H. Jacobs, A. Schlogl, and G. Deboy, "Determination of transient transistor capacitances of high voltage MOSFETs from dynamic measurements," in *Proc. 21st Int. Symp. Power Semiconductor Devices IC's*, Jun. 2009, pp. 148–151.

[5] I. Castro, J. Roig, R. Gelagaev, B. Vlachakis, F. Bauwens, and D. G. Lamar, "Analytical switching loss model for superjunction MOSFET with capacitive nonlinearities and displacement currents for DC–DC power converters," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2485–2495, Mar. 2016.

[6] D. Cittanti, F. Iannuzzo, E. Hoene, and K. Klein, "Role of parasitic capacitances in power MOSFET turn-on switching speed limits: A SiC case study," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2017, pp. 1387–1394.

[7] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019.

[8] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power MOSFETs: An improved analytical losses model," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1626–1640, Jun. 2010.

[9] M. Liang, T. Q. Zheng, and Y. Li, "An improved analytical model for predicting the switching performance of SiC MOSFETs," *J. Power Electron.*, vol. 16, no. 1, pp. 374–387, Jan. 2016.

[10] R. W. Erickson, "Switch realization," in *Fundamentals of Power Electronics*. New York, NY, USA: Chapman Hall, 1997, pp. 94–104.

[11] Z. Ivanovic, B. Blanusa, and M. Knezic, "Analytical power losses model of boost rectifier," *IET Power Electron.*, vol. 7, no. 8, pp. 2093–2102, Aug. 2014.

[12] W. Eberle, Z. Zhang, Y.-F. Liu, and P. C. Sen, "A practical switching loss model for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 700–713, Mar. 2009.

[13] D. Graovac, M. Pürschel, and A. Kiep, "MOSFET Power Losses calculation using the datasheet parameters," Infineon, Neubiberg, Germany, Appl. Note. [Online]. Available: https://application-notes.digchip.com/070/70-41484.pdf

[14] G. Lakkas, "MOSFET power losses and how they affect power-supply efficiency," *Analog Appl. J.*, to be published. [Online]. Available: http://www.ti.com/lit/an/slyt664/slyt664.pdf

[15] R. Sodhi, S. Brown, and D. Kinzer, "Integrated design environment for DC/DC converter FET optimization," in *Proc. 11th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, vol. 28, May 1999, pp. 241–244.

[16] M. Melito and G. Beverde, "STripFET TM III and optimal choice of MOSFETs in high current VRMs," STMicroelectronics, Geneva, Switzerland, Appl. Note AN1730, Jul. 2003.

[17] H. C. Sartori, F. Beltrame, H. H. Figueira, J. E. Baggio, and J. R. Pinheiro, "Power density comparative analysis concerning to three transistor technologies applied to a CCM PFC BOOST converter using optimization techniques," in *Proc. Brazilian Power Electron. Conf.*, Oct. 2013, pp. 1317–1323.

[18] K.-H. Chen, T.-J. Liang, and B.-K. Huang, "A new adaptive output voltage controller for fast battery charger," in *Proc. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, Mar. 2017, pp. 3345–3351.

[19] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9307–9318, Dec. 2017.

[20] S. Dimitrijev, "MOSFET," in *Principles of Semiconductor Devices*. New York, NY, USA: Oxford Univ. Press, 2012, pp. 312–316.
[21] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 985–995, Feb. 2015.

UTKARSH JADLI (Student Member, IEEE) was born in Pauri, Pauri Garhwal, Uttarakhand, India, in 1994. He received the B.Tech. degree in electrical and electronics engineering and the M.Tech. degree in control system from Graphic Era University, Dehradun, India, in 2015 and 2017, respectively. He is currently pursuing the Ph.D. degree with the Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Australia.

FAISAL MOHD-YASIN (Senior Member, IEEE) received the B.Sc. degree in electrical engineering, the M.Sc. degree in telecommunications engineering, and the M.Sc. degree in computer engineering from The George Washington University, USA, in 1999, 2002, and 2005, respectively, the Ph.D. degrees in integrated circuit design from Ibaraki University, Japan, in 2009, and the Ph.D. degree in MEMS from Multimedia University, Malaysia, in 2014. He is currently a Senior Lecturer with the School of Engineering and Built Environment, and a member of the Queensland Micro- and Nanotechnology Centre at Griffith University, Brisbane, Australia.

HAMID AMINI MOGHADAM received the B.Eng. degree from Azad University, Bojnord, Iran, in 2005, the M.Eng. degree in electronic engineering from Semnan University, Semnan, Iran, in 2011, and the Ph.D. degree from Griffith University, Australia, in 2016. He is currently a Lecturer with the Griffith School of Engineering and Built Environment. His current research interests include design, fabrication, and electrical characterization of wide bandgap power semiconductor (4H-SiC, AlGaN/GaN) devices.

PEYUSH PANDE (Member, IEEE) received the B.Eng. degree in electronics and telecommunication engineering from Amravati University, Amravati, India, in 2002, the M. Eng. degree in VLSI system design from Griffith University, Australia, in 2004, and the Ph.D. degree from the Queensland Micro- and Nanotechnology Centre, Griffith University, Australia, in 2020. He is currently working as an Associate Professor with Graphic Era University, Dehradun, India. His current research interest includes the physics and engineering of metal–oxide–SiC device structures, design, and electrical characterization of wide bandgap power semiconductor (SiC and GaN) devices.

JORDAN R. NICHOLLS received the B.Eng. degree (Hons.) in microelectronic engineering from Griffith University, Brisbane, Australia, in 2017, where he is currently pursuing the Ph.D. degree with the Queensland Micro- and Nanotechnology Centre.

His current research interests include the physics, modeling and characterization of metal–SiC and metal–oxide–SiC structures and the engineering of silicon carbide power devices.

SIMA DIMITRIJEV (Senior Member, IEEE) received the B.Eng., M.Sc., and Ph.D. degrees in electronic engineering from the University of Nis, Nis, Yugoslavia, in 1982, 1985, and 1989, respectively.

He is currently a Professor with the Griffith School of Engineering and the Deputy Director of the Queensland Micro- and Nanotechnology Centre at Griffith University, Brisbane, Australia. He is the author of *Principles of Semiconductor Devices*, 2^{nd} Ed. (New York: Oxford University Press, 2011).