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A 1.0 V, 5.4 pJ/bit GFSK Demodulator Based on an Injection Locked Ring Oscillator for Low-IF Receivers

SOONYOUNG HONG[1], (Graduate Student Member, IEEE), ARUP K. GEORGE[1], (Member, IEEE), DONGGU IM[2], (Member, IEEE), MINKYU JE[3], (Senior Member, IEEE), AND JUNGHYUP LEE[1], (Member, IEEE)

[1]Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science and Technology (DGIST), Daegu 42988, South Korea
[2]Department of Electronic Engineering, Jeonbuk National University, Jeonju-si 54896, South Korea
[3]School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 34141, South Korea

Corresponding author: Junghyup Lee (jhlee1@dgist.ac.kr)

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ABSTRACT This paper presents an ultra-low power, low cost demodulator for gaussian frequency shift keying (GFSK) receivers that use low intermediate frequencies (IF). The demodulator employs a direct IF to digital data conversion scheme by using an injection-locked ring oscillator (ILRO) with a 1-bit flip-flop. It consumes 2.7 μW from a 1.0 V supply at a data rate of 500 kbps achieving an energy efficiency of 5.4 pJ/bit which is 30 times better than that of the recently presented works. The demodulator also achieves 17.5 dB SNR at 0.1 % BER while operating at the same date rate. The demodulator is implemented in a 0.18 μm standard CMOS process and occupies an active area of 0.012 mm^2.

INDEX TERMS Demodulator, GFSK, low power, injection locked ring oscillator, low-IF, CMOS.

I. INTRODUCTION

Gaussian frequency shift keying (GFSK) is a popular modulation scheme for short-range, multi-channel communication standards such as Bluetooth and WPAN due to its high sensitivity and superior spectral efficiency [1]. Several GFSK transceivers have been actively developed in order to implement a physical layer for wireless networks [2]. The demand for GFSK transceivers having small feature sizes and lower power consumption has increased in recent Internet-of-Things (IoT) and Medical Implanted Communication Service (MICS) applications. Consequently, research efforts have been focused on reducing the feature size as well as the power consumption of such transceivers [3]–[4]. GFSK transmitters can be power-efficient, as the constant envelope characteristics of the GFSK modulation allow the use of energy-efficient nonlinear power amplifiers, enabling a low-power operation without any data distortion caused by spectral regrowth [5]. However, conventionally, GFSK receivers have a complicated structure and consume larger power. Secondly, they tend to have a large size, limiting their suitability for such size-constrained and low-power applications. To address these problems, the zero-IF and low-IF architectural flavors that integrate all filter components to a single chip are commonly used in the GFSK receivers [6]. However, the zero-IF has intrinsic issues caused by flicker noise and DC offset as well as local oscillator leakage. As a result, the low-IF is a more preferred option for enhanced signal-to-noise ratio (SNR) performance. Nevertheless, the low-IF receivers still suffer from relatively low energy efficiency due to the high frequency operation needed in detecting two different IF frequencies during the demodulation process. Therefore, in this paper, we present an ultra-low power, low cost demodulator for the GFSK receivers with a low IF that can improve the energy efficiency by more than 30 times than those of the recently presented works [7]–[10].

Several GFSK demodulators employing techniques such as delay line discrimination [7], zero-crossing detection [8], phase domain analog-to-digital conversion [9], and FM discrimination [10] have been reported in prior literature. The delay line discrimination approach of [7] is complex and consumes large power of about 200 μW as it uses two

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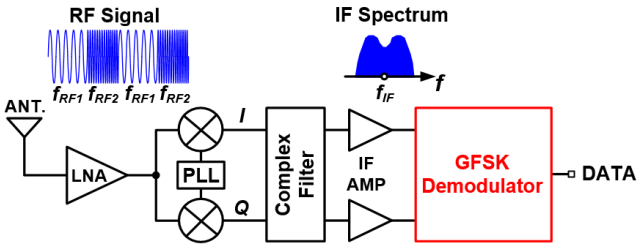


FIGURE 1. Overall structure of a GFSK receiver with a low IF.

voltage-controlled delay loops for its operation. Similarly, the zero-crossing technique used in [8] also has a limited suitability for low power operation as it uses a Sallen-Key filter and a differentiator whose power consumptions are 270 μW and 180 μW respectively. The demodulator based on the phase domain analog-to-digital converter in [9] needs several current mirrors and comparators and thus inevitably consumes over 500 μW. The last structure with the FM discriminator [10] still consumes large power of 170 μW due to the high sampling frequency of 32 MHz. Thus, the recent demodulators for the GFSK receivers are less suitable to be employed in low power sensor nodes or in bio-medical applications.

To solve the above-mentioned problems regarding area and power consumption, we propose an injection locked ring oscillator (ILRO) based GFSK demodulator. The GFSK demodulator for low-IF receivers presented in this paper dissipates only 2.7 μW from a 1 V supply, equivalent to an energy efficiency of 5.4 pJ/bit at a data rate 500 kbps. The rest of this paper is organized as follows: Section II presents the proposed demodulator architecture employing an ILRO. Section III discusses the detailed ILRO operation in the demodulator for direct IF to data conversion. Section IV presents the simulation and chip measurement results before concluding this article in Section V.

II. PROPOSED GFSK DEMODULATOR

The architecture of GFSK receivers using a low IF scheme is shown in Fig. 1. It comprises a low noise amplifier, mixers, a local oscillator, a complex filter, IF amplifiers as well as a demodulator. The RF front-end amplifies and down converts the RF input to the IF signal. The image components from the IF signal are filtered out by the complex filter, and the digital data is recovered by the demodulator. Among the various blocks of a GFSK receiver, the demodulator is one of the components that dissipate significant power and hence, minimizing it is essential in improving the overall power efficiency [8]. This paper proposes an ultra-low power, low cost GFSK demodulator using an ILRO towards achieving this end.

The proposed GFSK demodulator based on an ILRO is shown in Fig. 2. The input signal is down-converted to IF signal (A). The frequency f_{IF1} represents a data bit '1' while the frequency f_{IF2} represents a data bit '0'. The signal A is passed through a limiter to obtain B, which has a constant voltage swing. The pulse slicer generates an approximately

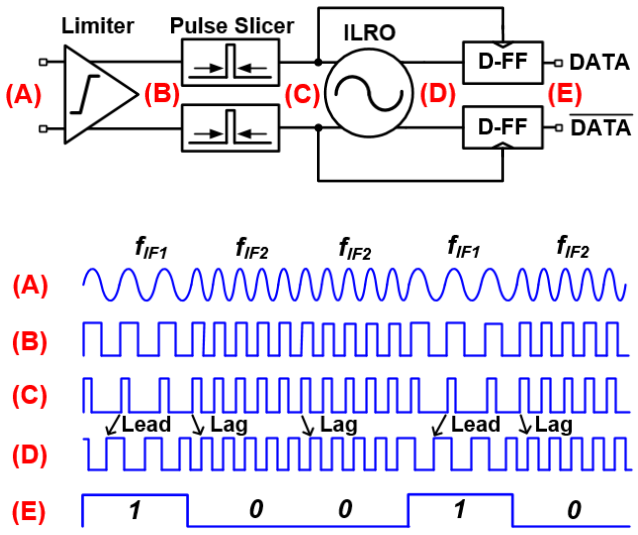
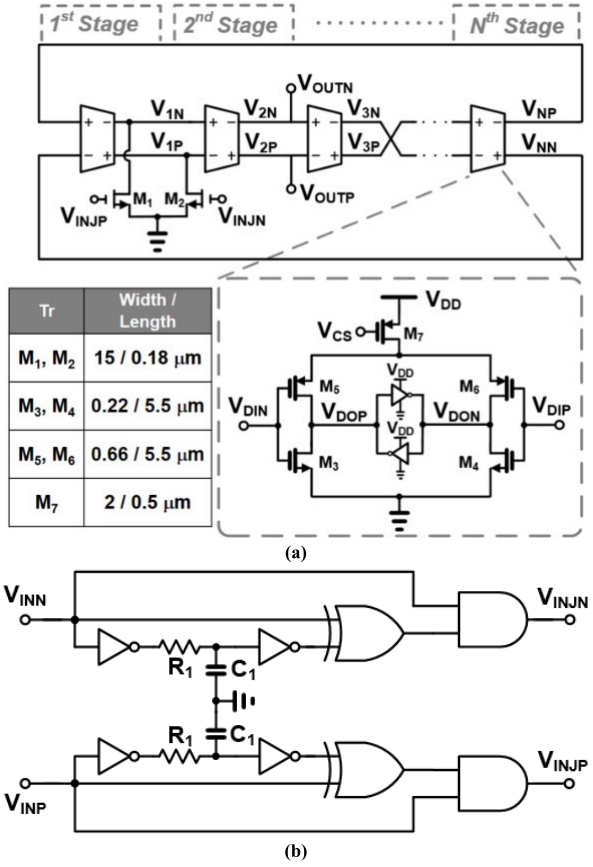


FIGURE 2. Block diagram and timing waveforms of the proposed ILRO based GFSK demodulator.

25%-width pulse output C that serves as the injection signal to the ILRO from its input B. The ILRO, once locked, maintains the phase differences between the injection input C and its output D such that C will always lead or lag D when the modulator input frequencies are f_{IF1} and f_{IF2} respectively.

The flip-flop (DFF) serves as a 1-bit time-to-digital converter that samples the ILRO output D during the rising edge of the injection pulse C. Given the fixed lead/lag relationships between C and D established by the ILRO, the input data can be reliably demodulated by this approach as D will sample a logic high from the signal C when the input frequency is f_{IF1} and a logic low when the input frequency is f_{IF2}. In comparison to conventional demodulators, the proposed architecture is simple and digital-intensive while the overall power consumption is significantly lower than conventional approaches that uses analog methods.

Fig. 3(a) shows the schematic of the differential N-stage ILRO used in the proposed GFSK demodulator. Note that we use a 4-stage ILRO ($N = 4$) in this implementation. The injection signals V_{INJN} and V_{INJP} are complementally injected into the first nodes V_{1N} and V_{1P} by using NMOS switches. The phase-shifted outputs V_{OUTN} and V_{OUTP} are obtained from the nodes V_{2N} and V_{2P} respectively. The free running frequency of the ILRO is determined by the delay cell's PMOS current source bias V_{CS} as shown in Fig. 3 (a). In addition, a latch circuit formed by cross-coupled inverters are added to the delay cells to minimize the rise/fall times of the ILRO node signals. The schematic of the pulse slicer used in the GFSK demodulator is shown in Fig. 3 (b). The pulse slicer makes the pulse-width of the ILRO injection signal approximately equal to the time constant R_1C_1, designed such that the pulse slicer output width is ~25 % of that of the free-running ILRO output. The reason for using the 25% duty-cycle will be explained in Section IV. The pulse slicer input and a delayed version of the same are passed through an XOR gate to generate pulses on both the rising and falling



Tr	Width / Length
M_1, M_2	15 / 0.18 μm
M_3, M_4	0.22 / 5.5 μm
M_5, M_6	0.66 / 5.5 μm
M_7	2 / 0.5 μm

FIGURE 3. Schematics of the differential ILRO and its delay cell (a), and the pulse slicer (b).

edges of the input. Only the pulse generated on the rising edge of the input goes to the output due to the AND operation.

III. DIRECT IF TO DATA CONVERSION BASED ON AN ILRO

An ILRO, as discussed in the previous section, can enable a simple and energy efficient conversion of IF to data and is hence a key building block in the proposed GFSK demodulator. In this section, we discuss the detailed operation of the ILRO, and in particular, the transient response of the injection locking process depending on whether the injection signal is higher or lower than the free-running frequency of the VCO. We will also discuss, how this can be used for a direct conversion of the IF to its equivalent digital data. Primarily, the ILRO comprises a chain of interconnected delay cells as shown in Fig. 3 (a). As mentioned in the earlier section, the NMOS switch with the input V_{INJN} pulls down V_{1P} to GND when V_{INJN} is high. Given that V_{INJN} and V_{INJP} are complimentary to each other, V_{1N} remains floating as the V_{INJP} switch gets turned off. However, since V_{1P} and V_{1N} are interconnected by a latch as shown in Fig. 3 (a), V_{1N} is pulled high. The overall effect of the nodes V_{1P} and V_{1N} being pulled down and up is that the phase-delay contribution of the individual delay stages changes in response to the relative frequency of the injection signal to that of the free-running frequency, taking the ILRO to be locked to a frequency equivalent as that of the injection signal. To explain this,

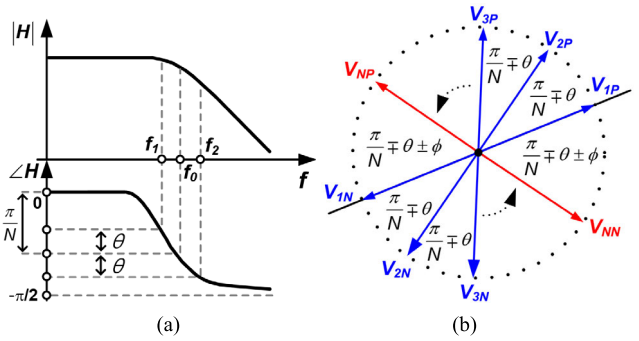


FIGURE 4. Frequency response of the delay cell (a) and a phase diagram for injection locking (b).

we consider the phase response of an individual delay stage when the ILRO is free-running and also when it is injection locked.

A. PHASE-SHIFT OF DELAY-CELLS IN AN ILRO

A delay cell in the N-stage ILRO can be modeled as a single pole amplifier, whose amplitude response rolls off at −20 dB/dec after the dominant pole and the phase difference between the input and output reaches $-\pi/2$ radians at frequencies significantly higher the dominant pole as shown by the frequency response in Fig. 4 (a). In the ILRO, for the oscillation to sustain, the total phase shift of the loop must be a multiple of 2π so as to meet the Barkhausen criteria [11]. To meet this, an ILRO having even number of stages, has to cross couple the inputs to one of the stages from the previous stage's outputs. In this implementation 4th delay-cell inputs are cross coupled to 3rd delay-cell outputs. In the absence of an injection signal, each non-cross-coupled delay cells of the ILRO adds a phase of $(\pi + \pi/N)$, while the cross coupled delay cell adds a phase of π/N making sure that the Barkhausen criteria is met. Note, that this phase delay responses are valid only for ILROs with even number of stages. A given delay-cell introduces an intrinsic phase reversal equivalent to π radians to its input signal. In addition, a variable component equal to π/N that depends on the number of delay stages is also added. Note that the cross-coupled stage does not add the intrinsic phase reversal to its input. Since the intrinsic phase reversal of the delay remains constant irrespective of whether the injection signal is present, it can be omitted from the rest of the analysis and is not included in the frequency response shown in Fig. 4 (a). The effect of injection locking is that the variable phase-delay of each of the delay cells changes in response to the injection signal to move the ILRO frequency to a locked state. It can be shown that once the ILRO is locked to the injection frequencies of $f_0 \mp \Delta f$ (f_1 and f_2), the phase shift of the delay cell changes to $\pi/N \mp \theta$. The overall phase-shift can be expressed as:

$$\begin{cases} (N-1)\,\pi + N\left(\dfrac{\pi}{N} - \theta\right) + \phi = 2m\pi, & for\ f_{INJ} < f_0 \\ (N-1)\,\pi + N\left(\dfrac{\pi}{N} + \theta\right) - \phi = 2m\pi, & for\ f_{INJ} > f_0 \end{cases} \tag{1}$$

where, θ represents the amount of phase shift caused by the change in oscillation frequency as shown by the frequency response of the delay cell (Fig. 4 (a)), and ϕ represents the additional amount of phase shift generated by first delay cell due to the signal injection. The factor (N-1)π is the sum of the intrinsic phase-shift introduced by all the delay cells in the ILRO and remains a constant. However, when injection locking occurs at a different frequency from the free-running frequency, for satisfying (1), the value of $\mp N\theta$ must be canceled by $\pm\phi$ so that the overall phase shift of the oscillator loop becomes $2m\pi$ ($m = 1, 2\ldots$) to maintain oscillation at the input injection frequency. As shown in Fig. 4 (b), therefore, the phase shift of delay cell D_1, ζ', and the phase shift of other delay cells, ζ, when f_{INJ} is less than f_0, can be described as follows:

$$\begin{cases} \zeta = \dfrac{\pi}{N} - \theta, \\ \zeta' = \dfrac{\pi}{N} - \theta + \phi = \dfrac{\pi}{N} - \theta + N\theta \end{cases} \tag{2}$$

Similarly, the phase shift of delay cell D_1, ψ', and the phase shift of other delay cells, ψ, when f_{INJ} is greater than f_0, can be described as follows:

$$\begin{cases} \psi = \dfrac{\pi}{N} + \theta, \\ \psi' = \dfrac{\pi}{N} + \theta - \phi = \dfrac{\pi}{N} + \theta - N\theta \end{cases} \tag{3}$$

where, θ according to the oscillation frequency in the lock state can be expressed as [12]:

$$\theta = \left| tan^{-1}\left[tan\left(\frac{\pi}{N}\right)\frac{f_{INJ}}{f_0}\right] - \frac{\pi}{N}\right| \tag{4}$$

B. TRANSIENT RESPONSE OF THE ILRO

To understand the concept of the injection locking process in the ILRO, we can consider the transient response of the output nodes of each of the ILRO delay cells. Several possible scenarios that show the relative alignment of an injection signal to the free-running VCO clock frequency (f_0) and how it modifies the phase-response of the ILRO clock outputs are shown Fig. 5. The illustration only shows the effect of a single injection signal pulse. As discussed earlier, in the absence of an injection signal, each of the delay cells introduce a variable phase-delay equivalent to π/N. We assume that the equivalent time-delay corresponding to a phase-delay of π/N is represented by Δt_{DEL}. The effect of the injection signals V_{INJP} or V_{INJN} are that it pulls down the nodes V_{1N} or V_{1P} to GND when one of them goes high. If either V_{1N} or V_{1P} are already at the GND level, the injection signal does not alter that node at all. Thus, the injection signal can affect the ILRO when both V_{1N} and V_{INJP} are high or when V_{1P} and V_{INJN} are high. The relative alignment of the injection signal and the free-running clock pulse can be summarized into four different scenarios:

- **Scenario 1:** The injection pulse V_{INJP} overlapping the rising edge of the free-running clock V_{1N} as shown in Fig. 5 (a). The overlap interval between V_{INJP} and V_{1N} is denoted as Δt_{INJR}.

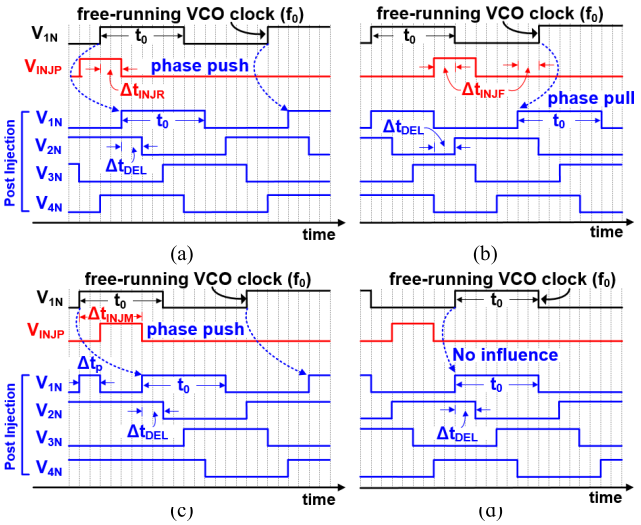


FIGURE 5. Change of 4-stage ILRO output according to injection position rising edge (a), falling edge (b), high state (c) and low state (d).

- **Scenario 2:** V_{INJP} overlapping the falling edge of the V_{1N} as shown in Fig. 5 (b). The overlap interval in this case is denoted as Δt_{INJF}.
- **Scenario 3:** V_{INJP} overlapping the high-state of V_{1N} as shown in Fig. 5 (c), where the time-interval between the rising edge of V_{1N} and the falling edge of the injection signal is Δt_{INJM}.
- **Scenario 4:** V_{INJP} overlapping the low-state of V_{1N} as shown in Fig. 5 (d).

When the injection signal V_{INJP} overlaps the rising edge of the free-running signal V_{1N}, (Fig. 5 (a)), the low state of the V_{1N}, is retained for an additional Δt_{INJR} time. The result of this is that the V_{1N} pulse is delayed by Δt_{INJR}. In contrast, when V_{INJP} overlaps the falling edge of V_{1N}, (Fig. 5 (b)), the injection signal pulls down V_{1N} earlier by Δt_{INJF}, causing the V_{1N} to advance by the same time-interval. When V_{INJP} overlaps with the high-state of V_{1N}, (Fig. 5 (c)), the effect on V_{1N} is similar to that of the case shown in Fig. 5 (a), where the rising edge is delayed. However, in this case, the delay time is equivalent to the time-interval between the rising edge of V_{1N} and the falling edge of the injection signal, Δt_{INJM}. Effectively, this scenario is equivalent to resetting V_{1N} by the V_{INJP}. Note that the reset operation causes a glitch in the V_{1N} waveform, whose width is shown as Δt_p. If Δt_p is lower than the default delay time of the subsequent stages, it will not affect them as shown in Fig. 5 (c). However, if Δt_p is larger, this glitch would manifest in V_{2N}, V_{3N} and also V_{4N}. Irrespective of the magnitude of Δt_p, the fact that the rising edge would be delayed remains the same. Finally, the V_{INJP} has no effect on V_{1N} when it overlaps with its low-state as shown in Fig. 5 (d). In a practical operating scenario, a sequence of the above four cases lead the ILRO to be locked to a frequency equal to the injection signal.

To illustrate the locking mechanism further, the transition process from a free-running state to a locked state when the injection signal is applied to the middle of high state of

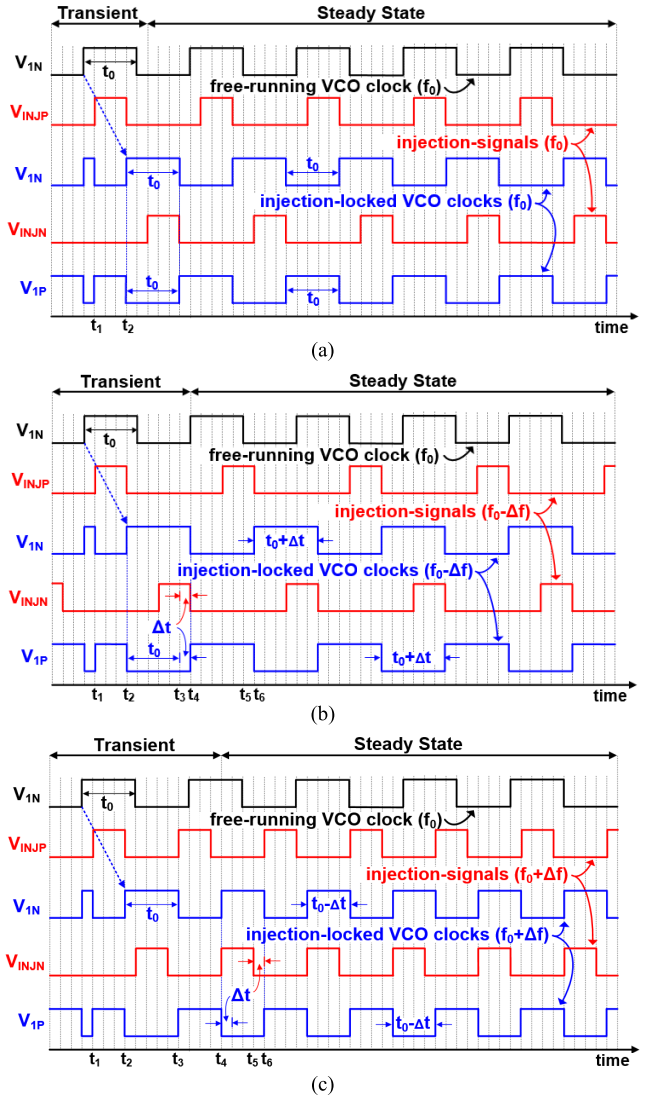


FIGURE 6. Injection-locking transient responses at $f_{INJ} = f_0$ (a), $f_{INJ} < f_0$ (b) and $f_{INJ} > f_0$ (c).

free-running signal (shown in Fig. 5 (c)), is shown in Fig. 6. In practice, the relative alignment of the injection signal could possibly be any one of the scenarios mentioned in Fig. 5. However, this scenario is chosen for illustration as it involves the events shown in the other cases of Fig. 5 as will be discussed later.

The transient operation is discussed for cases when the injection signal frequency is equal to, lower and higher than the free-running frequency of the ILRO. Fig. 6 (a) shows the transient operation when the frequency of V_{INJP} is equal to the free-running frequency of the ILRO, V_{1N}. The V_{INJP} signal resets the node voltage V_{1N} to GND at the instant t_1. As the V_{INJP} goes low, the V_{1N} node rises to a high-state at t_2, thereby delaying the rising edge of the free-running VCO clock. This is the scenario 3 of the locking process. Thereafter, the V_{INJP} or the V_{INJN} signals will not affect the ILRO operation, as they would overlap with the low-state of the V_{1N} and V_{1P}, which is the scenario 4 of the locking process. Thus, despite the phase-push introduced by $V_{INJP}$and V_{INJN}, the ILRO frequency remains the same. Fig. 6 (b) shows the transient operation when the frequency of V_{INJP} is lower than the free-running frequency the ILRO, V_{1N}. At the instant t_1, the V_{INJP} goes high, pulling down the V_{1N} to GND. At t_2, the V_{INJP} goes low, leaving V_{1N} floating. As a result, the rising edge of V_{1N} is delayed to the instant t_2, causing a phase-push (scenario 3). In the absence of the injection signal at V_{INJN}, the V_{1P} should have gone to a high-state at the instant t_3. However, as V_{1P} is pulled down by V_{INJN} until, t_4 the signal V_{1P} stays low for an extended period of Δt, thereby locking the ILRO to the lower injection frequency (scenario 1). Between t_5 and t_6, the V_{INJP} holds V_{1N} down to GND for an additional Δt (scenario 1). Once a lock is achieved, the scenario 1 repeats alternatively in V_{1N} and V_{1P}. When the injection signal frequency is higher than the free running frequency of the ILRO (Fig. 6 (c)), a phase-push happens and delays the rising edge of the V_{1N} to t_2(scenario 3). Between t_2 and t_4, V_{INJN} and V_{INJP} go high without influencing the current state of V_{1P} and V_{1N} respectively as they are already at GND (scenario 4). However, at t_4, V_{INJN} pulls down V_{1P} to GND, causing the V_{1N} to rise to a high-state instantaneously (scenario 2). The overall effect of this is that the period is reduced by Δt, thereby locking the ILRO to the injection frequency that is higher than the free-running frequency. Once locked, the scenario 2 repeats alternatively in V_{1N} and V_{1P}. In summary, the complimentary injection signals V_{INJP} and V_{INJN} introduces a phase-push/pull along with the widening or shortening of the ILRO outputs leading it to be locked with a frequency lower or higher than the nominal ILRO operating frequency.

C. PHASE RELATIONSHIPS OF THE ILRO

Fig. 7 shows the output waveform of each node of N-stage ILRO in the steady state after injection locking. When the ILRO is locked to an injection signal frequency that was originally lower its free-running frequency as shown Fig. 7 (a), the phase-delay between the successive edges between V_{NN} and V_{1N} becomes equal to $\zeta' = \pi/N - \theta + \phi$ as shown by equation (2). However, the delay between the successive edges of the other stages such as between V_{1N} and V_{2N}, V_{2N} and V_{3N} and so on remains at $\zeta = \pi/N - \theta$. The output is obtained by sampling one of the ILRO outputs using the injection locking clock. The fixed relative-phase relationship between the injection signal and the locked ILRO outputs enable latching one of the outputs at the sampling edge such that the output is registered as logic-high or logic-low. To explain this and to develop a closed form expression, the phase difference (PD) between the sampling edge of the input signal V_{INJP} and the successive rising edges of ILRO delay cell outputs V_{kN} can obtained as follows:

$$PD_k = \alpha + (k-1)\cdot\left(\pi + \frac{\pi}{N} - \theta\right) \quad for\ f_{INJ} < f_0, \qquad (5)$$

where k denotes the index of the stage from which the output is taken. In (5), α denotes a phase equivalent to a duty-cycle of $T_d \times 2\pi$ / T_{inj}. Similar to this, a definite phase-relationship exists between V_{INJP} and V_{NN}, when the injection signal

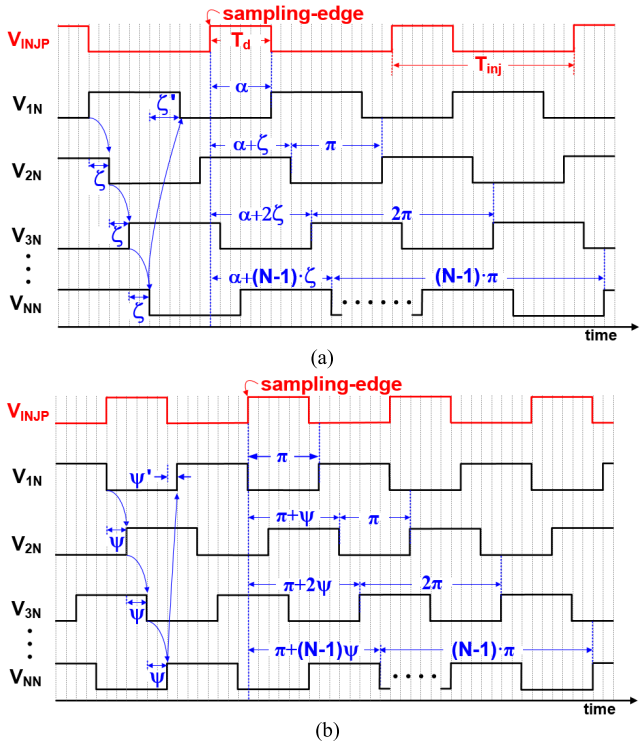


FIGURE 7. Phase-relationships with the sampling edge at $f_{INJ} < f_0$ (a) and $f_{INJ} > f_0$ (b).

frequency is higher than the free-running ILRO frequency as shown in Fig. 7 (b). The phase-delay between the successive edges between V_{NN} and V_{1N} becomes equal to $\psi = \pi/N + \theta - \phi$ from equation (3). However, the delay between the successive edges of the other stages such as between V_{1N} and V_{2N}, V_{2N} and V_{3N} and so on becomes at $\psi = \pi/N + \theta$. In this case, however, the PD between the sampling edge of the input signal V_{INJP} and the successive rising edges of ILRO delay cell of outputs V_{kN} can be shown as:

$$PD_k = \pi + (k-1)\cdot\left(\pi + \frac{\pi}{N} + \theta\right) \quad for\ f_{INJ} > f_0 \qquad (6)$$

Using the relationships (5) and (6), an appropriate ILRO output can be sampled as the demodulator output as shown in Table 1. Due to the injection locking, a well-defined phase-relationship is established between V_{INJP} and the ILRO outputs V_{kN} and V_{kP}, where k refers to the state from which the outputs are taken. As shown in Table 1, for an even stage, $(k = 2, 4\ldots)$ if the total phase difference between the sampling edge and the rising edge of k^{th} delay cell output is greater than $k\pi$, the output will be sampled as active low. On the contrary, if the phase difference is less than $k\pi$, the output will be sampled as active high. If the outputs are taken from the odd numbered stages $(k = 1, 3\ldots)$ and the overall phase difference between the sampling edge and the rising edge of k^{th} delay cell output is higher than $k\pi$, the output will be sampled as active high. If the phase difference is lower than $k\pi$, the output will be sampled as active low.

Finally, as observed from (5) and (6), the sampled output state in the cases when f_{INJ} is greater or lower than $f_0$depends on the duty-cycle of injection signal. As shown in Table 1 and using N = 4 and k = 2 (values used by this design as discussed later), the DFF samples the low-state when the duty-cycle is over 38 % and the high-state when the duty-cycle is less than 38 % when f_{INJ} is lower than f_0. However, when f_{INJ} is higher than f_0, the DFF is always sampled as a logic-low as shown by (6) and Table 1. Therefore, in this paper, a duty-cycle of 25 % is used so as to provide a margin of 13 % from the maximum allowable duty cycle where the sampled outputs remain complimentary to each other.

TABLE 1. Sampling state according to the phase difference.

Output Stage	$f_{INJ} < f_0$ or $f_{INJ} > f_0$	
Even	$PD_k > k\pi$	Low
	$PD_k < k\pi$	High
Odd	$PD_k > k\pi$	High
	$PD_k < k\pi$	Low

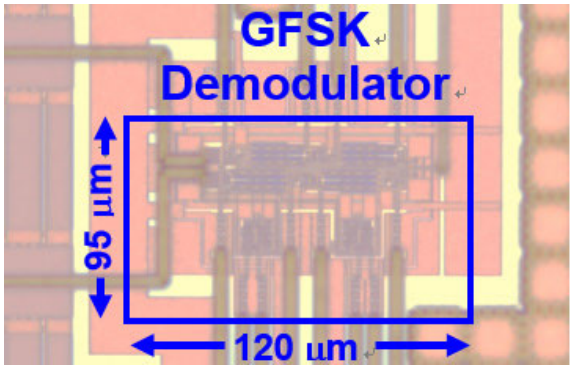


FIGURE 8. Chip micrograph.

IV. SIMULATION AND MEASUREMENT RESULTS

Fig. 8 shows the chip micrograph of the proposed GFSK demodulator. The demodulator is implemented in a 0.18 μm standard CMOS process and occupies an active area of 95 × 120 μm^2. The proposed demodulator consumes an average current of 2.7 μA from a 1.0 V supply. The power breakdown of the receiver is shown in Table 2. The most of power is consumed by the ILRO. The demodulator frequency has to be chosen to strike a balance between power consumption and the transient settling time of the ILRO to get to a locked state. For this reason, 2 MHz was selected for the design goal of power consumption under 3 μW and 500 kbps data-rate. The ILRO used in the demodulator has 1.4 MHz (1.3 ∼ 2.7 MHz) lock range.

The proposed demodulator is vulnerable to PVT variation due to the open-loop operation of the ILRO. Deviation of the free-running frequency from the IF frequency of the receiver degrades the BER performance of the demodulator. Such effects can be minimized by using an external reference clock and a frequency locked loop (FLL) using a replica VCO [13]. This implementation, however, does not include an on-line calibration circuit to mitigate the PVT effects. The free-running frequency of ILRO is tuned to the IF frequency used in the receiver by adjusting V_{CS}. Fig. 9 shows the change

TABLE 2. Power breakdown of the demodulator.

Limiter	220 nA
Pulse Slicer	560 nA
ILRO	1.5 μA
Latch	270 nA
DFF	150 nA
Total Power	**2.7 μW**

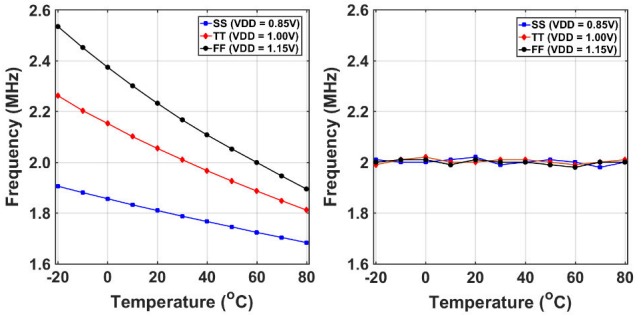
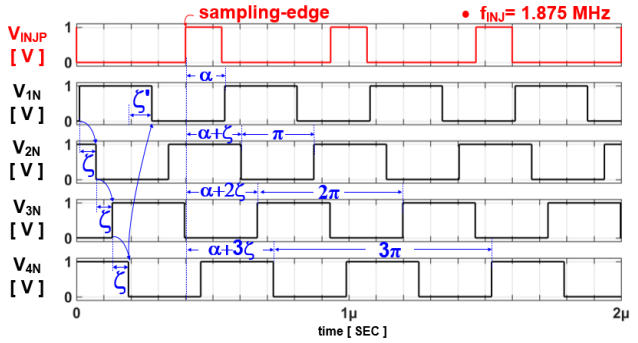


FIGURE 9. Change of free-running frequency of ILRO according to PVT (a) before calibration (b) after calibration.

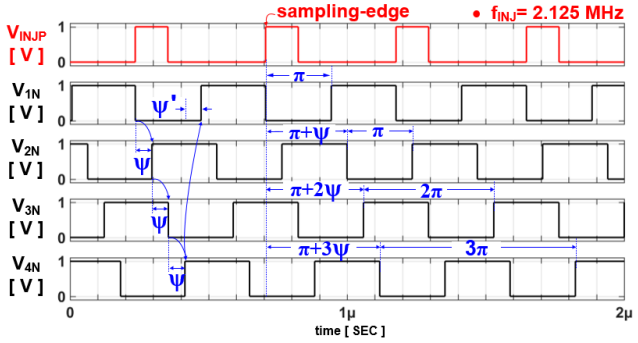
of ILRO's free-running frequency due to PVT variations and results of calibration. The free-running frequency of ILRO in proposed demodulator is changed from 1.7 to 2.55 MHz over a temperature and supply ranges of −20° C to 80° C and 0.85 V to 1.15 V respectively along with three different process corners, as shown in Fig. 9 (a). However, by adjusting V_{CS}, the free oscillation frequency can be moved closer to 2 MHz for various process corners such as FF (V_{DD} = 1.15 V), TT (V_{DD} = 1.0 V), SS (V_{DD} = 0.85 V) as shown in Fig. 9 (b).

Fig. 10 shows the Cadence Spectre simulation results that plot the phase differences between injection signal and the output signal of each of the delay stages. The free-running frequency of ILRO is designed at 2 MHz and an approximately 25 % duty cycled injection signal is used. Fig. 10 (a) shows the output signal of each node in the injection locked state with the 1.875 MHz injection signal. From simulation, it can be seen that the phase shift of the delay cell has a phase shift ζ is 43.2° and ζ' is 50.4°. Thus, the values θ and ϕ can be evaluated as 1.8° and 7.2° respectively. When ILRO is locked to the 2.125 MHz signal as shown in Fig. 10 (b), the phase shift ψ is 46.8° and ψ' is 39.6°. In this case also, the values θ and ϕ can be evaluated as 1.8° and 7.2° respectively as expected from (2), (3) and (4). In this implementation, the outputs are taken from the second stage delay cells. When the injection frequency is lower than the free-running frequency, based on the simulation results, the phase difference of the second delay cell output and the injection signal is 313.2° from (5). In other words, the rising edge of second stage delay cell output is 46.8° ahead of the sampling edge of V_{INJP}.



Parameter	ζ	ζ'	θ	ϕ	PD_2	Sampling state
Phase [°]	43.2	50.4	1.8	7.2	313.2	High

(a)



Parameter	ψ	ψ'	θ	ϕ	PD_2	Sampling state
Phase [°]	46.8	39.6	1.8	7.2	406.8	Low

(b)

FIGURE 10. Simulation results of 4-stage differential ILRO at $f_{INJ} < f_0$ (a) and $f_{INJ} > f_0$ (b).

Since PD_2 is lower than 360° (or 2π), the output is sampled as logic-high. When the injection frequency is higher than free-running frequency, the phase difference PD_2 is 406.8° from (6). The rising edge of second stage delay cell output is 46.8° lag to V_{INJP}. Since PD_2 is higher than 360° (or 2π), the output is sampled as logic-low.

Fig. 11 shows the measured input and output waveforms of the ILRO in the proposed demodulator and the data waveform demodulated through the D-flip flop using and injection signal of 25 % duty cycle. It can be seen that when the injection frequency is 2.125 MHz, the output is sampled as a logic-low. Similarly, when the injection frequency is 1.875 MHz, the output is sampled as a logic-high. In order to measure the BER performance, GFSK signal with AWGN (Additive White Gaussian Noise) and frequency deviation of ±125 kHz is applied to the demodulator by using signal generator, SMW200A of ROHDE & SCHWARZ. As shown in Fig. 12, the demodulator achieves an input SNR of 17.5 dB equivalent to a BER of 0.1 % at a data rate of 500 kbps. At 200 kbps, the SNR improves to 16.9 dB.

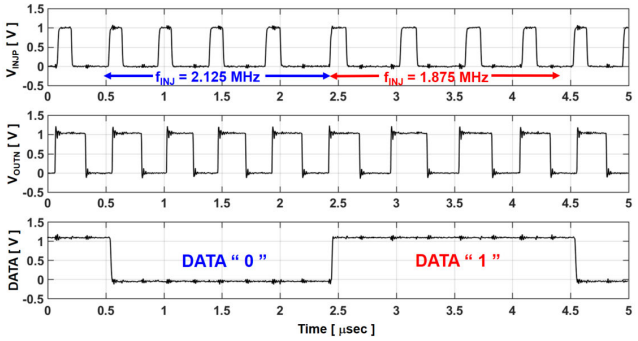


FIGURE 11. Measured GFSK demodulator responses.

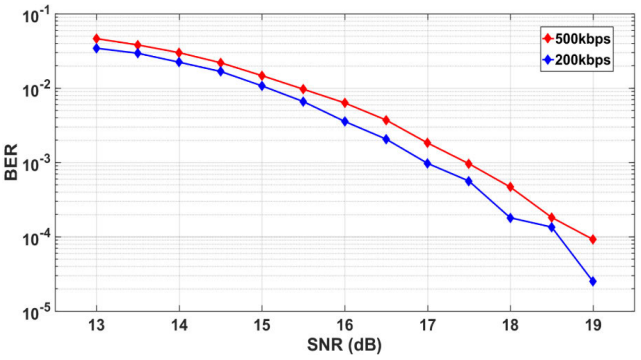


FIGURE 12. Measured BER performances of the GFSK demodulator.

TABLE 3. Performance comparison.

	[7]	[8]	[9]	[10]	This work
Tech [μm]	0.18	0.18	0.18	0.13	0.18
Supply [V]	0.5	1.8	1.8	1.2	1.0
Max. Data-rate [Mbps]	1	1	0.25	1	0.5
IF [MHz]	3	3	2	1	2
SNR [dB]	18.7	16.5	16.7	14.4	17.5 @ 0.5 kbps 16.9 @ 0.2 kbps
Power [μW]	200	918	630	170	2.7
Energy Efficiency [pJ/bit]	200	918	2520	170	5.4
Area [mm^2]	0.36	0.08	0.14	0.05	0.012

Table 3 compares the performance of recently proposed GFSK demodulators with the proposed architecture. In comparison to [4]–[7] the proposed demodulator consumes significantly lesser power achieving energy efficiency at least 30 times better. The overall silicon area is 4 times smaller, thanks to its simple structure arising from the ILRO based approach. The energy efficiency and the area can be further improved by implementing the proposed modulator in a more advanced process node due to its digital intensive nature.

V. CONCLUSION

In this paper, a novel GFSK demodulator based on an injection ring oscillator suitable for low-IF receiver architecture is presented. The proposed approach is digital-intensive enabling ultra-low power operation. The measured results show that the proposed demodulator can accurately demodulate GFSK signals with a simple structure. Furthermore, ultra-low power consumption and small active area of the architecture enables its use in many low power low cost wireless communication systems for IoT and MICS applications.

ACKNOWLEDGMENT

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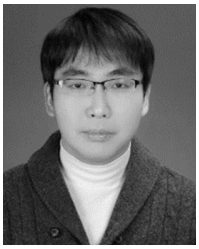
SOONYOUNG HONG (Graduate Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Chungnam National University, Daejeon, South Korea, in 2006 and 2008, respectively. He is currently pursuing the Ph.D. degree in information and communication engineering with the Daegu Gyeongbuk Institute of Science and Technology (DGIST).

His current research interests include wireless transceiver design for ultra-low power applications using CMOS technologies and sensor interface circuits for wireless sensor network (WSN).

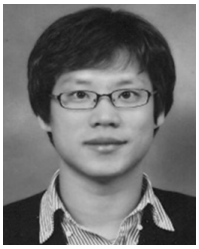
ARUP K. GEORGE (Member, IEEE) received the B.Tech. degree in electronics and communication engineering from the Cochin University of Science and Technology, India, in 2003, the M.Sc. degree (Hons.) in electronics and communication engineering from the University of Glasgow, Glasgow, U.K., in 2010, and the Ph.D. degree in electrical and electronic engineering from Nanyang Technological University, Singapore. He was a Senior Staff Engineer with Nvidia Graphics India, developing image and video firmware for their mobile platform SoCs. He is currently a Research Professor with the Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science and Technology, Daegu, South Korea. His research interests include sensor interface circuits for ultra-low-power biomedical and sensor node applications.



DONGGU IM (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2004, 2006, and 2012, respectively. From 2006 to 2009, he was an Associate Research Engineer with LG Electronics, Seoul, South Korea, where he was involved in the development of universal analog and digital TV receiver ICs. From 2012 to 2013, he was a Postdoctoral Researcher with KAIST, where he was involved in the development of the first RF SOI CMOS technology in Korea with SOI Business Team, National NanoFab Center (NNFC), Daejeon, where he was responsible for the design of antenna switch, digitally tunable capacitor, power MOSFETs, and ESD devices. He joined the Texas Analog Center of Excellence (TxACE), Department of Electrical Engineering, University of Texas at Dallas, as a Research Associate, in 2013, where he developed ultra-low-power CMOS radios with adaptive impedance tuning circuits. He joined the Division of Electronics Engineering, Chonbuk National University, Jeollabuk-do, South Korea, in 2014, where he is currently an Associate Professor. His research interests include CMOS RF/mm-wave ICs and system design for wireless communications.

MINKYU JE (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1998 and 2003, respectively.

He joined Samsung Electronics, Giheung, South Korea, as a Senior Engineer, in 2003, where he worked on multi-mode multi-band RF transceiver SoCs for GSM/GPRS/EDGE/WCDMA standards. From 2006 to 2013, he was with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A∗STAR), Singapore. He worked as a Senior Research Engineer, from 2006 to 2007, a Member of Technical Staff, from 2008 to 2011, a Senior Scientist, in 2012, and a Deputy Director, in 2013. From 2011 to 2013, he led the Integrated Circuits and Systems Laboratory, IME, as a Department Head. In IME, he led various projects developing low-power 3D accelerometer ASICs for high-end medical motion sensing applications, readout ASICs for nanowire biosensor arrays detecting DNA/RNA and protein biomarkers for point-of-care diagnostics, ultra-low-power sensor node SoCs for continuous real-time wireless health monitoring, and wireless implantable sensor ASICs for medical devices, as well as low-power radio SoCs and MEMS interface/control SoCs for consumer electronics and industrial applications. He was also a Program Director of NeuroDevices Program under A∗STAR Science and Engineering Research Council (SERC), from 2011 to 2013, and an Adjunct Assistant Professor with the Department of Electrical and Computer Engineering, National University of Singapore (NUS), from 2010 to 2013. From 2014 to 2015, he was an Associate Professor with the Department of Information and Communication Engineering, Daegu Gyenogbuk Institute of Science and Technology (DGIST), South Korea. Since 2016, he has been an Associate Professor with the School of Electrical Engineering, KAIST. He is the author of five book chapters and has more than 290 peer-reviewed international conference and journal publications in the areas of sensor interface IC, wireless IC, biomedical microsystem, 3D IC, device modeling and nanoelectronics. He also has more than 50 patents issued or filed. His main research interests include advanced IC platform development, including smart sensor interface ICs and ultra-low-power wireless communication ICs, as well as microsystem integration leveraging the advanced IC platform for emerging applications, such as intelligent miniature biomedical devices, ubiquitous wireless sensor nodes, and future mobile devices. He has served on the Technical Program Committee and Organizing Committee for various international conferences, symposiums, and workshops, including the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE Asian Solid-State Circuits Conference (A-SSCC), and the IEEE Symposium on VLSI Circuits (SOVC). He is currently working as a Distinguished Lecturer of the IEEE Circuits and Systems Society.



JUNGHYUP LEE (Member, IEEE) received the B.S. degree in electrical and electronics engineering from Kyungpook National University, Daegu, South Korea, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2005 and 2011, respectively.

He joined the Institute of Microelectronics, Agency for Science, Technology, and Research (A∗STAR), Singapore, in 2011, where he was engaged in the development of high-speed wireless transceivers for biomedical applications and reference clock generators. Since 2016, he has been an Assistant Professor with the Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science and Technology (DGIST), Daegu. His research interests include mixed-signal and analog circuits for low-power biomedical devices and PVT tolerant circuits. He has served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC).