Design of Compact Dual-Band RF Rectifiers for Wireless Power Transfer and Energy Harvesting

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ABSTRACT In this paper, we propose a compact dual-band impedance matching network (DBIMN) for radio frequency (RF) rectifiers. The DBIMN is achieved with a single-stage T-type network, with only three segments of the transmission line. We investigate the closed-form design equations, as a design guideline of the DBIMN. In addition, we propose the design methodology of the rectifier using the DBIMN. For validation, we design two dual-band rectifiers (0.915 and 2.45 GHz), for different input power levels. The rectifier with high input power level, is designed for a wireless power transmission (WPT) system. With a 12 dBm input power, the measured power conversion efficiencies (PCEs) are 81.7 and 73.1% at the working frequencies. The PCEs becomes 69.2 and 64.1% (at -1 dBm input power) for the low-power input rectifier that can be used in an RF energy harvesting (RF-EH) system. The simulated and measured results match each other well. Compared with previous designs, the proposed designs have advantages in compactness and high efficiency.

INDEX TERMS Rectifiers, dual-band, impedance matching, wireless power transfer, energy harvesting.

I. INTRODUCTION

Wireless power transmission (WPT) and radio-frequency (RF) energy harvesting (RF-EH) techniques have attracted much more attention in recent years, because of their potential in powering electrical vehicles, mobile devices [1], Internet of Thing (IoT) nodes [2], and biomedical implanted devices [3], etc.. In both WPT and RF-EH systems, rectifier is a key component to convert the RF power to the direct current (DC) power [4].

RF-to-DC power conversion efficiency (PCE for short) is a pivotal parameter to evaluate the performance of the rectifier. To realize a high PCE, different rectifier topologies have been investigated recently. In general, there are four basic rectifier topologies: single-series [5], single-shunt [6], [7], voltage doubler [8], [9] and bridge type [10]. According to the operating frequency, rectifiers can be classified into three categories, single-band [11]–[13], multi-band [14], [15] and broadband [8], [16]. Generally, single-band rectifier is conductive to achieve a high PCE, but the amount of the collected DC output power is limited. Broad-band rectifier

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aims at harvesting energy from all available frequency spectrums, but inevitably sacrifices the quality-factor (Q) value of the input matching network, and thus the maximum PCE. Therefore, multi-band rectifier, selectively harvesting energy from certain bands, may be a good solution as a tradeoff between the output power and maximum PCE.

In recent years, dual-band and multi-band rectifier design have been intensively explored. A dual-band impedance matching network, consisting of six segments of the transmission line (two-stage T-type networks), was proposed in [17] for a rectifier working at 1.84 and 2.14 GHz. Yet, this matching network complicates the design. In [18], a dual-band rectifier working at 0.915 and 2.45 GHz was introduced. The dual-band matching network is realized by an L-type network cascaded with a PI-type network, increasing the design complexity. A rectifier working at 2.45 and 5.8 GHz for a low input power system was reported in [19]. However, the input matching will be degraded when the two operating frequencies are close to each other. [20] designed the dual-band matching network with a cross-shaped stub cascaded by a T-shaped stub. Reference [21] proposed to employ lumped elements (inductors, capacitors) as a dual-band matching network. However, the lumped elements are lossy

at high frequency, which may undermine the PCE. In [22]–[25], multi-band (dual-band or triple-band) rectifiers were reported. In these designs, each multi-band IMN was realized by multiple (≥6) transmission line stubs.

In this paper, we propose a compact dual-band impedance matching network (DBIMN), consisting of a single-stage, T-type network with only three segments of transmission line. This significantly reduces the design complexity, insertion loss and physical size of the matching network. This paper is organized as follows. We derive its closed-form design equations, and propose a design methodology of the rectifier using this network in Section II. For verification, we design two dual-band rectifiers, aiming at a high and low input power, based on this methodology. The simulated and measured results are given in Section III. Section IV concludes this paper.

II. DUAL-BAND RECTIFIER DESIGN

Fig. 1 shows the basic configuration of the proposed dual-band rectifier, which consists of a DC-block capacitor (C_{in}), a DBIMN, two Schottky diodes, a DC-pass filter (C_{out}) and a resistive load (R_L). Here, we use the voltage doubler configuration for a high output voltage. Z_L represents the load impedance of the impedance matching network, which is frequency-dependent due to the parasitic components and the nonlinearity of the rectifying diode. And $Z_0 = 50\ \Omega$ is the characteristic impedance of the RF signal source. The targeted working frequencies are f_1 (0.915 GHz) and f_2 (2.45 GHz).
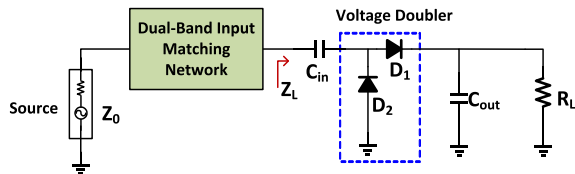

FIGURE 1. Schematic of the proposed dual-band rectifier.

The optimum R_L and the input power level (P_{in}) should be first found for the selected rectifying devices, achieving with a source-pull simulation [26]. Fig. 2 shows the test-bench. After R_L and P_{in} are determined, we obtain Z_L (at f_1 and f_2) through a harmonic balance (HB) simulation [27]. Then, we design a dual-band impedance matching network, to transform Z_L to Z_0 at f_1 and f_2 simultaneously, as discussed below.
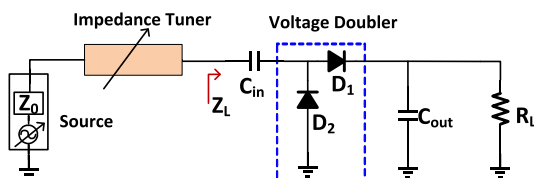

FIGURE 2. Source-pull simulation test-bench.

A. DUAL-BAND IMPEDANCE MATCHING NETWORK DESIGN

Fig. 3 gives the schematic of the proposed DBIMN, consisting of a single-stage T-type network. This network consists of three segments of transmission line denoted as TL_1, TL_2 and TL_3. The common node of TL_1, TL_2 and TL_3 is denoted as point a. Fig. 4 intuitively shows the working principle of the transmission lines.
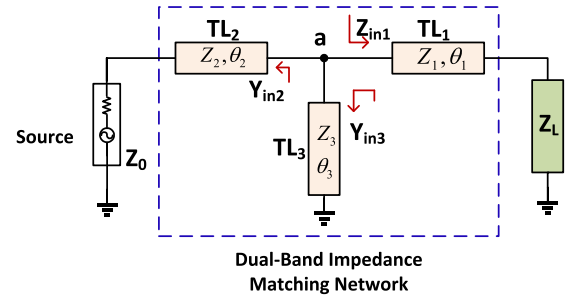

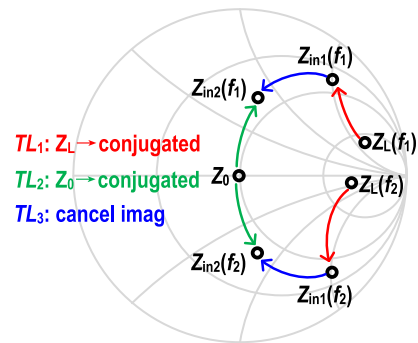**FIGURE 3.** Schematic of the proposed dual-band impedance matching network.

FIGURE 4. Intuitive working principle of the transmission lines.

1) TL_1: CONJUGATED IMPEDANCE TRANSFORMATION FROM Z_L TO Z_{IN1}

TL_1 is employed to transform two frequency-dependent input impedances to a pair of conjugated impedances. TL_1's characteristic impedance and electrical length at f_1 are denoted as Z_1 and θ_1. The frequency ratio $k = f_2/f_1$, which is 2.67 for the targeted two working frequencies. Z_L is denoted as $R_{L1}+jX_{L1}$ and $R_{L2}+jX_{L2}$ at f_1 and f_2. Then after TL_1 transformation, $Z_L(f_1)$ and $Z_L(f_2)$ become $Z_{in1}(f_1)$ and $Z_{in1}(f_2)$:

$$Z_{in1}(f_1) = Z_1 \times \frac{R_{L1}+j(X_{L1}+Z_1\tan\theta_1)}{Z_1-X_{L1}\tan(\theta_1)+jR_{L1}\tan(\theta_1)} \quad (1)$$

$$Z_{in1}(f_2) = Z_1 \times \frac{R_{L2}+j(X_{L2}+Z_1\tan(k\theta_1))}{Z_1-X_{L2}\tan(k\theta_1)+jR_{L2}\tan(k\theta_1)}. \quad (2)$$

$Z_{in1}(f_1)$ and $Z_{in1}(f_2)$ are a conjugated pair:

$$Z_{in1}(f_1) = Z_{in1}^*(f_2) \quad (3)$$

Combining (1) - (3), we have:

$$\tan[(1+k)\theta_1] = \frac{Z_1(R_{L2}-R_{L1})}{R_{L2}X_{L1}-R_{L1}X_{L2}} \quad (4)$$

$$\tan[(1+k)\theta_1] = \frac{Z_1(X_{L1}+X_{L2})}{R_{L1}R_{L2}+X_{L1}X_{L2}-Z_1^2}. \quad (5)$$

Subsequently, we derive Z_1 and θ_1 as:

$$Z_1 = \sqrt{R_{L1}R_{L2} + X_{L1}X_{L2} + \frac{X_{L1} + X_{L2}}{R_{L2} - R_{L1}}(R_{L1}X_{L2} - R_{L2}X_{L1})}$$

$$(6)$$

$$\theta_1 = \frac{1}{k+1}\left\{\arctan\left[\frac{Z_1(R_{L1} - R_{L2})}{R_{L2}X_{L1} - X_{L2}R_{L1}}\right] + n\pi\right\}. \quad (7)$$

where n is an arbitrary integer. To ease the fabrication and reduce the physical size, the value of n should be minimum. Mathematically, the expression under the square root of (6) could possibly be negative. But this is less likely to take place after taking numerical calculations or simulations with multiple frequently used diodes at targeted frequency bands.

2) TL_2: CONJUGATED ADMITTANCE TRANSFORMATION FROM Z_0 TO Y_{IN2}

Here, TL_2 is utilized to make the input admittance Y_{in2} at f_1 and f_2 conjugated. Thus, the input impedances Z_{in2} (f_1) and Z_{in2} (f_2) are also a pair of conjugated impedances, as given in Fig. 4. TL_2's characteristic impedance and electrical length at f_1 are denoted as Z_2 and θ_2. Then the electrical length of TL_2 at f_2 is equal to $k\theta_2$, and Y_{in2} at f_1 and f_2 are:

$$Y_{in2}(f_1) = \frac{1}{Z_2} \times \frac{Z_2 + jZ_0\tan(\theta_2)}{Z_0 + jZ_2\tan(\theta_2)} \quad (8)$$

$$Y_{in2}(f_2) = \frac{1}{Z_2} \times \frac{Z_2 + jZ_0\tan(k\theta_2)}{Z_0 + jZ_2\tan(k\theta_2)}. \quad (9)$$

As observed, $Y_{in2}(f_1) = Y_{in2}^*(f_2)$ can only be met with $\tan(\theta_2) = -\tan(k\theta_2)$. Thus, θ_2 is designed as:

$$\theta_2 = \frac{\pi}{1+k}. \quad (10)$$

As stated before, TL_1 has made the input admittance looking from the common node (point a) towards right at f_1 and f_2 are also a pair of conjugated admittance. That is, the real parts of Y_{in1} at f_1 and f_2 are equal and the imaginary parts are opposite in sign. Since the input impedance of an open or shorted stub does not have any real part, to satisfy the conjugate matching condition at the common node, the real part of Y_{in2} should be equal to the real part of Y_{in1} at the two operating frequencies. Thus, we have

$$G_{in2} = G_{in1} \quad (11)$$

where G_{in1} and G_{in2} are the real part of Y_{in1} and Y_{in2}, respectively.

Combining (8), (9) and (11), we obtain

$$\frac{Z_0 + Z_0\tan^2(\theta_2)}{Z_0^2 + Z_2^2\tan^2(\theta_2)} = G_{in1}. \quad (12)$$

From (12), we derive the characteristic impedance Z_2 as:

$$Z_2 = \sqrt{\frac{Z_0 + Z_0\tan^2(\theta_2) - Z_0^2 G_{in1}}{\tan^2(\theta_2)G_{in1}}}. \quad (13)$$

Similar to (6), the expression under the square root of (13) could be negative in mathematics, but it is always positive with the frequently used diodes.

3) TL_3: CANCEL OUT ALL THE IMAGINARY PARTS AT POINT A

We employ TL_3, possibly either a shorted or open stub, to cancel out all imaginary impedances at the common node. The characteristic impedance and electrical length of TL_3 at f_1 are denoted as Z_3 and θ_3, respectively. The input admittance of Y_{in3} can be written as:

$$\begin{cases} Y_{in3} = -j\cot(\theta_3)/Z_3 & \text{(shorted stub)} \\ Y_{in3} = +j\tan(\theta_3)/Z_3 & \text{(open stub)} \end{cases} \quad (14)$$

To cancel out all imaginary impedances at the common node, Y_{in3} should meet:

$$Y_{in3} = -j(B_1 + B_2) \quad (15)$$

where B_1 and B_2 are the imaginary parts of Y_{in1} and Y_{in2}, respectively. If $(B_1 + B_2) < 0$, then $Y_{in3} > 0$ and we should use an open stub. Otherwise, we use a shorted stub. Besides, the input admittances Y_{in3} at f_1 and f_2 also have a conjugated relationship:

$$Y_{in3}(f_1) = Y_{in3}^*(f_2) \quad (16)$$

Thus, regardless of which type the stub is, its electrical length at f_1 is

$$\theta_3 = \frac{\pi}{1+k}. \quad (17)$$

Combining (14) and (15), Z_3 becomes:

$$Z_3 = \begin{cases} \dfrac{-\tan(\theta_3)}{B_1 + B_3} & \text{(open stub)} \\ \dfrac{\cot(\theta_3)}{B_1 + B_3} & \text{(shorted stub)}. \end{cases} \quad (18)$$

So far, the characteristic impedances and the electrical lengths of TL_1, TL_2 and TL_3 are determined. Fig. 5 summarizes a flowchart for the design procedure of the proposed DBIMN.
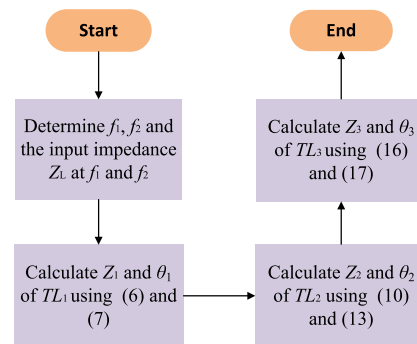

FIGURE 5. The flowchart for the DBIMN design.

B. DESIGN GUIDELINE FOR THE PROPOSED DUAL-BAND RECTIFIER

Incorporating the previous analysis, a design guideline for the proposed dual-band rectifiers is summarized below for a quick design.
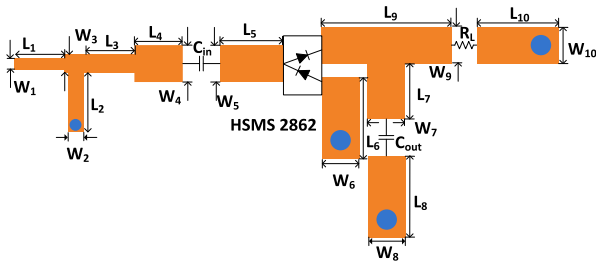
FIGURE 6. Layout of rectifier-I.

FIGURE 7. Fabricated prototype of rectifier-I.

TABLE 1. Dimensions of the microstrip line.

Parameters	Width/Length (mm)	Parameters	Width/Length (mm)
TL_1	0.4/33.2	TL_6	2.1/3.0
TL_2	0.8/29.6	TL_7	2.1/3.0
TL_3	0.9/16.6	TL_8	2.1/3.0
TL_4	2.1/3.0	TL_9	2.1/8.1
TL_5	2.1/3.0	TL_{10}	2.1/3.0

1. According to the application, determine the two desired operating frequencies (f_1 and f_2) and choose appropriate Schottky diodes.
2. Take out the source-pull simulation to determine the optimum load (R_L), input power (P_{in}), the values of C_{in} and C_{out}.
3. Take out the harmonic balance (HB) simulation in ADS to determine the load impedance (Z_L) of the matching network at f_1 and f_2.
4. Design the proposed dual-band matching network from Fig. 5.
5. Fine-tune the parameters for an optimum performance.

III. SIMULATION AND MEASUREMENT RESULTS

To verify the proposed DBIMN methodology, we designed, fabricated and measured two dual-band rectifiers, both working at 0.915 and 2.45 GHz. Rectifier-I is designed for a WPT application under a high input power level (P_{in}), whereas Rectifier-II is for RF-EH under a low P_{in}. These two rectifiers are simulated in ADS software and fabricated on a 0.762 mm thick Arlon AD 255 substrate, with a relative permittivity of 2.55 and loss tangent of 0.0018.

A. RECTIFIER I

We choose Schottky diode Avago HSMS 2862 as the rectifying device, for its superior performance in high input power scenarios. The diode has a series resistance (R_s) of 5 Ω, breakdown voltage (V_{br}) of 7 V, and zero-bias junction capacitor (C_{j0}) of 0.18 pF. In addition, a 15-pF capacitor is used as the DC-pass filter. After performing source-pull simulation, the load $R_L = 2500$ Ω is found to provide the optimum efficiency for both operation frequencies. Based on the theoretical analysis of the DBIMN, the initial characteristic impedance and electrical length of TL_1, TL_2 and TL_3 can be obtained. Here, $Z_1 = 85.7$ Ω, $\theta_1 = 91°$, $Z_2 = 129.1$ Ω, $\theta_2 = 48.946°$, $Z_3 = 94$ Ω, $\theta_3 = 48.946°$.

The layout and fabricated prototype of rectifier I are shown in Figs. 6 and 7, occupying 74.1×35.3 mm^2. Table 1 lists the microstrip line dimensions. The PCE is defined as the rectified DC output power (P_{dc}) over the RF incident power P_{in}:

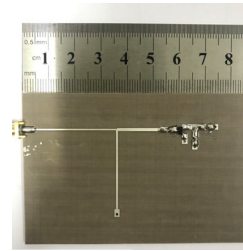$$PCE = \frac{P_{dc}}{P_{in}} \times 100\% = \frac{V_{out}^2}{R_L} \times \frac{1}{P_{in}} \times 100\% \quad (19)$$

where V_{out} is the output DC voltage. Here, the RF incident power is provided by the signal generator Keysight N5172 B.

Fig. 8 displays the simulated and measured PCEs versus the frequency at 12 dBm P_{in}. As observed, the maximum measured PCEs are 81.7 % and 73.1 % at 0.93 and 2.44 GHz, respectively. There is a small difference between the measurement and simulation results, due to the inaccuracy of the diode model and the fabrication tolerance. The efficiency could be possibly further improved by adding a harmonic rejection network to the DBIMN.
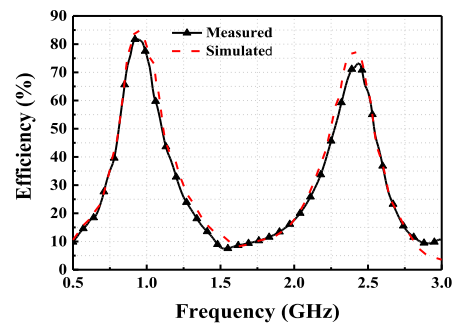

FIGURE 8. Simulated and measured efficiency versus frequency at the input power of 12dBm.

Fig. 9 shows the insertion loss of the DBIMN in rectifier I. As can be seen, the insertion losses at 0.915 and 2.45 GHz are 0.055 and 0.1 dB, respectively. Fig. 10 plots the simulated and measured S_{11}, showing consistency. At the input power of 10 dBm, the measured S_{11} are −24.4 dB at 0.93 GHz and −27.5 dB at 2.44 GHz. The $S_{11} < −10$ dB in the low and high frequency bands are from 860 to 1035 MHz and from 2345 to 2490 MHz, respectively. Thus, the bandwidth of the rectifier-I is 175 and 145 MHz for the low and high band.

Fig. 11 presents the simulated and measured PCEs and output voltages of rectifier I versus P_{in} at 0.93 GHz. As can
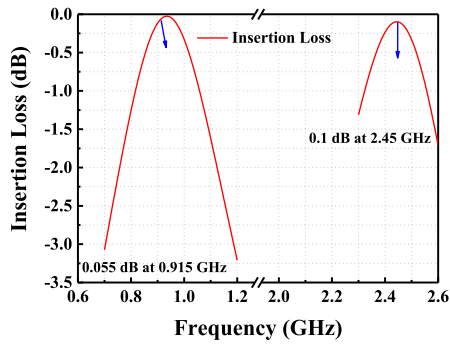
FIGURE 9. Simulated insertion loss of the dual-band impedance matching network in rectifier I.
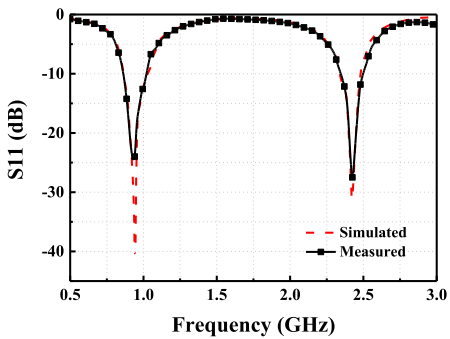

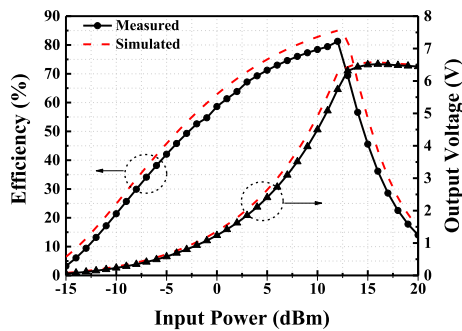**FIGURE 10.** Simulated and measured S_{11} of rectifier-I.

FIGURE 11. Simulated and measured efficiency and output voltages of rectifier-I, versus input power at 0.93 GHz.

FIGURE 12. Simulated and measured efficiency and output voltages of rectifier-I, versus input power at 2.44 GHz.

and substrate were utilized in this design. The DC-pass filter is realized by a 100 pF capacitor, which is used to suppress the harmonics generated by the diodes. Moreover, the input low-pass filter is achieved by a 75 pF capacitor. The overall size of rectifier II is 80.3 × 23.4mm². The measurement setup of rectifier II is presented in Fig. 13. Table 2 gives the optimized parameters of the microstrip lines.
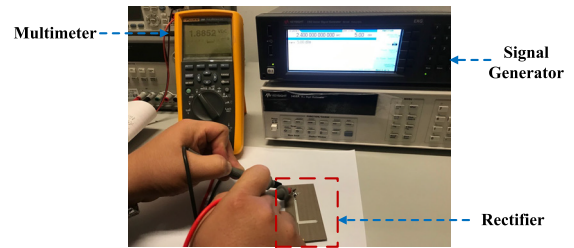
FIGURE 13. Photograph of the measurement setup of rectifier-II.

TABLE 2. Dimensions of the microstrip line.

Parameters	Width/Length （mm）	Parameters	Width/Length (mm)
TL_1	0.4/18.3	TL_6	2.1/3.0
TL_2	3.8/18.9	TL_7	2.1/3.0
TL_3	2.8/32.7	TL_8	2.1/3.0
TL_4	2.1/3.0	TL_9	2.1/8.1
TL_5	2.1/3.0	TL_{10}	2.1/3.0

be seen, the maximum measured PCE is 81.7 % with a 5.7 V V_{out} at the input power of 12 dBm. The measured input power range for PCE higher than 50% is from −4.8 to 14.7 dBm. Fig. 12 displays the results of 2.44 GHz, where the maximum measured PCE is 73.1 % with a 5.4 V V_{out}. The input power range is from 2.4 to 14.6 dBm for PCE > 50%. Simulation results almost match the measured ones.

B. RECTIFIER II

The second rectifier is designed for an RF-EH application. In this design, we select the Schottky diode SMS7630 due to its low biasing voltage requirement for a weak input signal [28]. Similar to rectifier I, the same rectifying structure
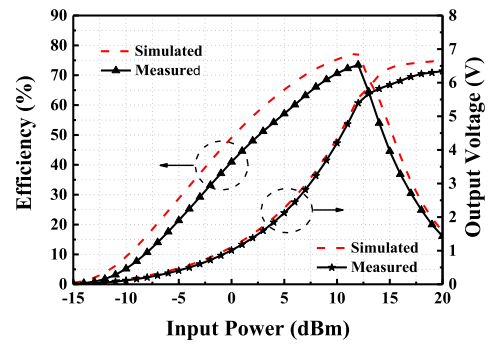
Fig. 14 shows the simulated and measured PCEs of the rectifier II with an optimum 1500 ΩR_L at −1 dBm P_{in}. As can be seen, the maximum measured PCEs at 0.9 and 2.4 GHz are 69.2 and 64.1%, respectively. The slight frequency shift between the simulated and measured results may result from the variation of the chip capacitor values and fabrication tolerance. Fig. 15 displays the simulated and measured S_{11}, which are −18.7 and −30.6 dB at 0.9 and 2.4 GHz, respectively. The S_{11} lower than −10 dB in the low and high frequency bands are from 885 to 935 MHz and from 2405 to 2495 MHz. Therefore, the bandwidths of rectifier II in the low and high frequency bands are 50 and 90 MHz, respectively.

TABLE 3. Comparison of the proposed rectifiers and related designs.

Ref.	Input power (dBm)	Frequency (GHz)	Type of Schottky diode	Maximum efficiency (%)	Electrical size	Number of the transmission line segments of the impedance matching network
[17]	−18	1.84 & 2.14	HSMS2852	37.5 & 34	0.452λg×0.082λg	6
[18]	14.6	0.915 & 2.45	HSMS2862	77.2 & 73.5	0.181λg×0.099λg	5
[19]	10	2.45 & 5.8	HSMS2860	66.8 & 51.5	0.285λg×0.212λg	6
[20]	0	2.45 & 5.8	HSMS2850	57.6 & 33.62	0.383λg×0.109λg	6
[21]	−15	0.915 & 2.14	SMS7630	23 & 18	NA	NA
[23]	5	0.915 & 1.8	HSMS2850	NA	1.128λg×0.701λg	6
This work	12	0.915 & 2.45	HSMS2862	81.7 & 73.1	0.226λg×0.107λg	3
	−1	0.915 & 2.45	SMS7630	69.2 & 64.1	0.244λg×0.071λg	3

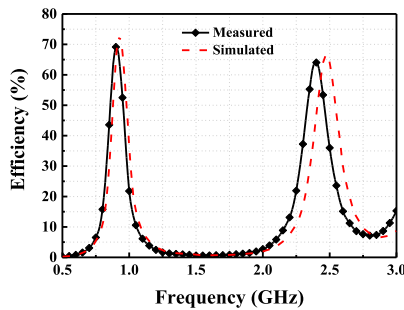* λg is the wave-length at the lowest operating frequency.

FIGURE 14. Simulated and measured efficiency of rectifier-I, versus frequency at the input power of −1dBm.
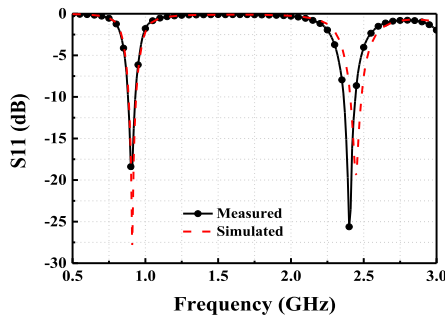

FIGURE 15. Simulated and measured S_{11} of rectifier-II.

FIGURE 16. Simulated and measured efficiency and output voltages of rectifier-II, versus input power at 0.9 GHz.
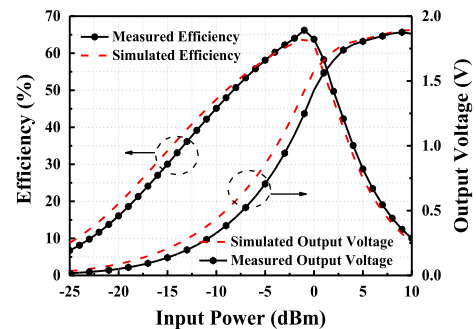
FIGURE 17. Simulated and measured efficiency and output voltages of rectifier-II, versus input power at 2.4 GHz.

Figs. 16 and 17 show the simulated and measured PCEs and output voltages versus the input power at 0.9 and 2.4 GHz. Reasonable agreement between the simulation and measurement can be observed. Under a −1 dBm P_{in}, the maximum measured PCEs are 69.2 % and 64.1 % for 0.9 and 2.4 GHz. For the lower band, the measured PCE is higher

than 50 % over the input power range from −11.8 to 2.5 dBm (14.3 dB), while it is −8.6 to 1.7 dBm for the upper band.

Table 3 compares the proposed two rectifiers with other related designs. It can be seen that our designs feature a high conversion efficiency at both bands. Furthermore, the dimensions of our designs are smaller than most of the previous

ones, due to the proposed DBIMN has only a single-stage T-type network, which consists of three segments of transmission line. Yet the proposed scheme has a lower design freedom than [17]–[21] that have multiple transmission lines, since adding a transmission line provides two extra degrees of design freedom (width and length of transmission line segment).

IV. CONCLUSION

In this paper, we present a simple dual-band impedance matching methodology. In such matching network, we employ a single-stage, T-type network that has only three transmission-line segments. Its closed-form design equations are derived. With the proposed matching methodology, a compact circuit structure was achieved, leading to a reduction in the complexity of matching network, the insertion loss and the physical size. For validation, two dual-band rectifiers working at 0.915 and 2.45 GHz have been implemented and tested. The measurement results are in good agreement with the simulation ones. Compared with some other reported dual-band rectifiers, the proposed works advance the previous ones in PCE and physical size.

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