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Analytical Solution of Amplifier-Antenna System's Impedance Matching Requirement for Reliable Microwave Transmitter

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ABSTRACT In this paper, the integration of push-pull class B amplifier and antenna module have been proposed. The high efficiency and low distortion of push-pull class B due to its differential feeding technique makes it a viable candidate as a power amplifier. The aperture-coupled antenna structure is used in this work as it offers the designer various methods to effectively adjust the variables thereby making way for more efficient configuration which can be fabricated on system-on-chip. Moreover, this enables a wide range of values that can be chosen on the Smith Chart thus allowing the conditions needed for odd-mode matching to be satisfied. This matching requirement is specific for only a given transistor and in this work by incorporating bandstop filters made of resonant stubs it has been possible to filter harmonic power up to 3rd harmonic. The frequency of operation of the integrated push-pull transmitting amplifier during simulation is at 2.06 GHz. The Wilkinson power divider, power coupler, phase shifter and bias decoupling circuits have been employed so as to efficiently integrate the push-pull class B power amplifier with the differentially fed aperture coupled antenna. Two types of antenna were studied whereby one was designed with the conventional 50 Ω environment while the other makes use of the complex value impedance. Parametric study was also performed on both types of antennas so as to investigate the effects it has on the impedance matching requirements. Finally, the prototype was realized through fabrication and measurements were performed at fundamental frequencies and up to 3rd harmonics to show gain at fundamental component and filtering of 2nd and 3rd harmonic.

INDEX TERMS Aperture coupled antenna, class B, complex termination, differential feed, gallium nitride (GaN), harmonic suppression, monolithic microwave integrated circuit (MMIC), push-pull amplifier, power amplifier, system-on-chip, Wilkinson power divider (WPD).

I. INTRODUCTION

The exponential growth in the communication engineering industry mainly in the wireless communication systems is due to the massive demand from consumers and the media. This has created competitive industry which aims to achieve the challenging requirements for implementing 4G LTE and the newly anticipated 5G network aimed for radio frequency (RF) and microwave spectrum. The change from 4G to 5G systems means that there should be major improvement in terms of wider bandwidth, lower power consumptions, and better coverage of signals. The introduction of integrated circuit (IC) in the field of RF and microwave communication systems has paved the way for creating smaller sized transceivers at much lower cost and increased bandwidth which is implemented in system of chip (SoC) [1]. This technology has enable the integration of multiple components within a single chip block such as the combination of balun, switches with active devices such as low noise amplifier (LNA) and power amplifier (PA) with the exception of the antenna onto a single

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system on chip module. Nevertheless, despite the use of IC which enabled considerable reduced size and cost for fabrication of the RF and wireless systems, one major flaw that has to be accounted for is an increase in insertion loss [2].

Numerous semiconductor technologies have been explored which would offer the possibility to incorporate the whole wireless communication system onto a single package. These technologies include Indium Phosphide (InP), Silicon Germanium (SiGe), Gallium Nitride (GaN) and Gallium Arsenide (GaAs) [3]–[6]. It is imperative to know the technologies used for power transistors and their range of frequencies of operation as well as a perspective on their power usage. In order to compare power transistors we need to analyze the data published based on power added efficiency (PAE) and power attainable by using those technologies [7]. This will enable RF designers to have an overview of which transistors to choose for their design. The power transistor being adapted into this work is made from the GaN fabrication technology and the reason for this choice is its ability to work up to 100 GHz and high output power as it is already relevant based on its superior power and PAE as shown in Figure 1 [7], [8].

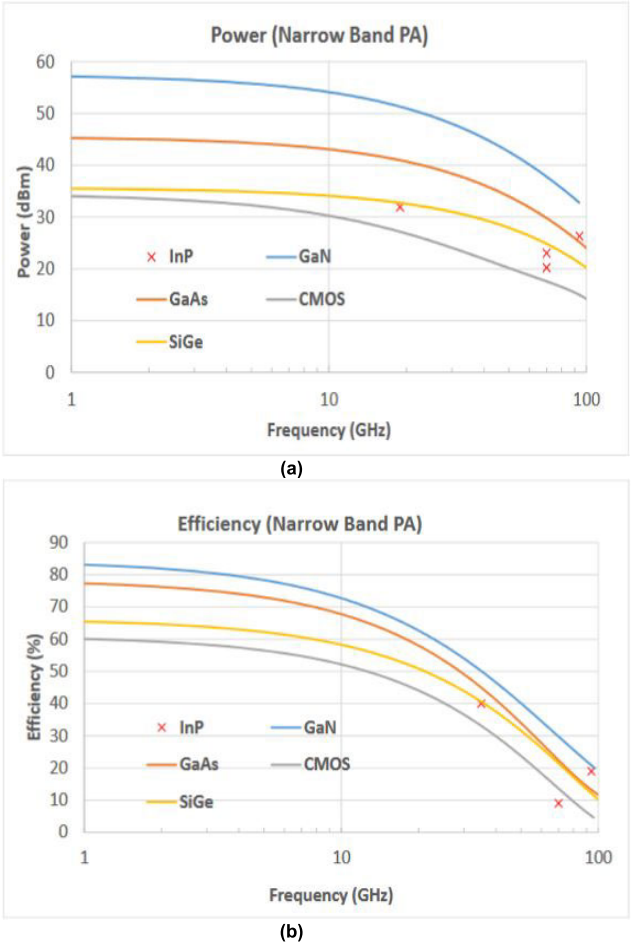


FIGURE 1. Relative merits and comparison of power transistors technologies based on power and efficiency [7].

The size of the antenna plays a major role and the RF and microwave engineer are keen to make the antenna as small as possible so as to be able to be implemented in portable handheld wireless devices. One method used to achieve this was by using a single dielectric slab of semiconductor to produce modern integrated circuit (IC) devices which is known as Monolithic Microwave Integrated Circuits (MMIC) [9], [10]. A major advantage of using MMIC is found when cascading sub-circuits and this alleviates the problem of design an external matching network. However, it possesses some drawbacks as it involves a high level integration at a higher cost and there will always a trade-off for the overall system performance such as a narrower bandwidth, lower gain and efficiency. The reason for this is the compactness of the small electrical antenna and thereby having a small radiation aperture size which will cause those aforementioned problems [11].

Some possible solutions to such problems include having the antenna built externally from the MMIC module and the electrical feed needs to have no direct electrical connection to the MMIC which is by using bond wires or vias [12]. Another method was to electromagnetically couple the energy from the chip through the parasitic patch to the antenna. The problem with this method was that at low frequencies the system would have an inferior performance since the chip size is quite small and the chip carrier where the antenna was to be situated also had to fit inside it [13]. In order to tackle on this scenario, a differential feeding technique is employed whereby the two-port networks made up of exactly similar parts facing each other are electrically fed to generate two signals. The benefits of using two port feeding technique compared to the regular one port for the antenna is that it will be unaffected by the common mode interference as the two signals flowing in opposite direction along the differential lines and this also negates the crosstalk occurring across the common bias lines [14].

On the other hand, the balun implementation into the front end architecture for a differentially fed antenna design such as the hybrid coupler and impedance transformer will be invalid as ICs can be fed by differential signals which are more preferred compared to the usage of balun [2]. This allows the antenna to behave as a perfect coupler and good matching circuit while maintaining its capability to radiate signals [15]–[17]. It should be noted that the symmetry of the antenna should be maintained when using the IC technologies. The balun incorporation into a one-port antenna is to act like a matching circuit thereby making the unbalanced signal to transform into a balanced signal before being fed into the IC module [18]–[20]. However, balun will not be employed in this work as it is not suitable for IC realization since it does not satisfy the requirements of fully integrated solutions. Moreover, balun has imperfections as balanced signal from a balun will not be perfectly differential in practical. This balun's imbalance will add to the total system loss since the symmetrical balanced ports will be imbalanced and hence making it irrelevant to a push-pull amplifier configuration.

Meaning that if the balun is still being implemented to circuit configuration to the amplifiers the efficiency of the device will be severely affected [21].

Considering efficiency in power amplifiers, RF power amplifiers are classified into multiples classes which are based upon their efficiency, linearity and their conduction angles. There are many classes of RF power amplifiers and the most commonly used ones in the applications of wireless communication systems are the Class A, Class B, Class AB and Class C. The simplest class of amplifiers is the Class A amplifiers and is often used as a benchmark for the other amplifier classes. The maximum achievable efficiency of a class A amplifier is 50% and is considered to have high linearity when compared to the other classes. Class B amplifiers operate when the transistors are biased at the pinch-off region so as to negate the drain to source current which accounts for a higher maximum efficiency of 78.5% compared to class A albeit having a drawback of being non-linear. In order to find a compromise between the high linearity of class A and high efficiency of Class B, the class AB power amplifier have been made as a hybrid of both classes. The class C power amplifier conducts in reduced conduction angle mode and a lower gate bias voltage than the pinch off voltage. This means the class C amplifier will have high efficiency but with drawbacks of being highly nonlinear. The main attributes of the different classes of power amplifiers are summarized in Table 2 [22].

TABLE 1. Classification of different classes of operation for conventional RF power amplifier.

Classification	A	AB	B	C
Conduction angle, θ (radians)	2π	$\pi < \theta < 2\pi$	π	$\theta < \pi$
Peak Achievable Efficiency (%)	50	50 – 78.5	78.5	≈ 100
Maximum Peak-to-Peak Output (V)	≫ Vcc	≈ Vcc	< Vcc	≪ Vcc
Distortion	Small	Small to moderate	Moderate	Large
Linearity	Most linear	Slightly non-linear	Non-linear	Highly non-linear

Impedance matching for amplifiers with antennas are to be considered to achieve better efficiency [17]. The use of the 50Ω impedance interface is very popular in the RF and microwave field whereby the front-end systems have had their design to comply with the standard 50Ω environment without significant mismatches. Such a systems have drawbacks, consider an example using an amplifier with an optimum impedance of 20Ω, we have to transform it into 50Ω in order to get them matched. As a consequence, losses in the transforming circuit and limitations on the achievable bandwidth are unavoidable. This scenario is going to be repeated using a complex value of impedance (the load will consist of real value for the resistance and imaginary value for the reactance, $Z = R + jX$) instead of the 50Ω, the efficiency of the overall system would change. If the system is working at low frequencies the reactance X may be negligible so that the impedance Z can be considered as purely resistive which is expressed in real value R. Meanwhile, operating at higher frequencies, the complex value of Z has to be accounted since it becomes significant in determining the overall system performance.

The aim of this work is mainly to make a search and systematic inquiry into whether replacing the unbalanced 50Ω interface could be advantageous compared to that regularly used design procedure when designing an amplifier-antenna system. As represented in Figure 2, it is obvious physically as well as electrically that the proposed design approach would produce a less complex front-end system than the conventional way. Ultimately, the design of a novel system for direct integration of power amplifier and antenna was undertaken. The EM structure is design based on a two-port aperture coupled microstrip antenna as the push-pull amplifier configuration makes use of differential feeding technique. Therefore, the EM structure will be differentially fed at two ports so that the push-pull amplifier design can be incorporated.

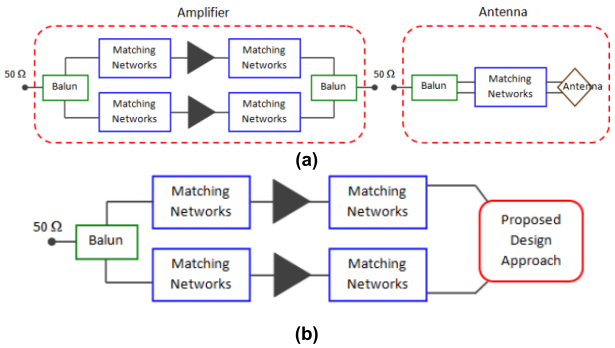


FIGURE 2. (a) Conventional amplifier-antenna front-end system (b) The potential advantages of integrating an amplifier-antenna system.

II. DESIGN ARCHITECTURE OF A PUSH-PULL AMPLIFIER

The class of amplifier implemented in this paper is based on the class B mode of operations. The simulations carried out in this paper has been performed on the nonlinear transistor NEC NE722S01 which the device model was provided by the Modelithics. However, as for practical implementation, this model could not be used as it was no longer produced by the manufacturer. Alternatively, the power amplifier was built based on the nonlinear transistor from NITRONEX NPTB00004. The procedure being carried out in this work can be applied to both transistors hence the simulations performed on transistor model NEC NE722S01 is also suitable to be used on model NITRONEX NPTB00004. A brief comparison has been summarized in Table 2 which gives a basic idea on the operational capability of these devices.

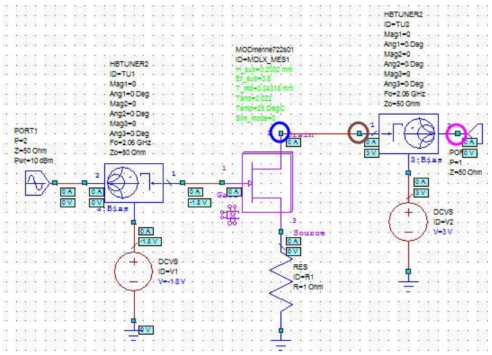
A. INPUT MATCHING SETTING

The matching approach used for the input matching network design is approximately equivalent to a conjugate impedance matching problem, maximizing the gate voltage swing on the input terminal of the transistor. The approximation is because

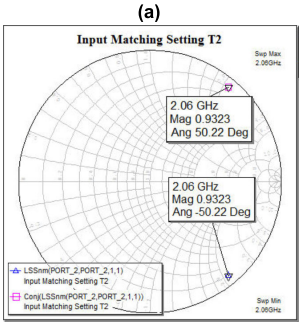
TABLE 2. Difference between two proposed devices.

	NEC NE722S01	NITRONEX NPTB00004
Device Technologies	GaAs	GaN
Operating Frequency (Ghz)	C to X band 4 - 12	DC to 6
Output Power At 1dB Gain Compression Point, P1dB (dBm)	15	34.6
Power Gain, G (dBm)	V_{DS} =3V I_{DS} = 10 mA T= 25 °C F = 4 GHz G = 12	V_{DS} =28V I_{DS} = 50 mA T= 25 °C F = 2.5 GHz G = 15.5

the transistor input impedance is power dependent, so the appropriate drive level must be used in the simulation. Thus, a fixed drive level input power and exact bias conditions has been specified when the simulation and measurement was conducted. The settings for the input power and bias conditions are only applicable to this device NEC NE722S01 at resonant frequency 2.06 GHz. The input power of 10 *dBm* is applied meanwhile the gate bias voltage and drain bias voltage have been set to -1.8 *V* and 3 *V* respectively. These settings are done purposely to ensure that the amplifier will be working efficiently at Class B. Figure 3(a) shows the circuit configuration for getting appropriate input impedance with its conjugate impedance match, giving simulated result shown in Figure 3(b).



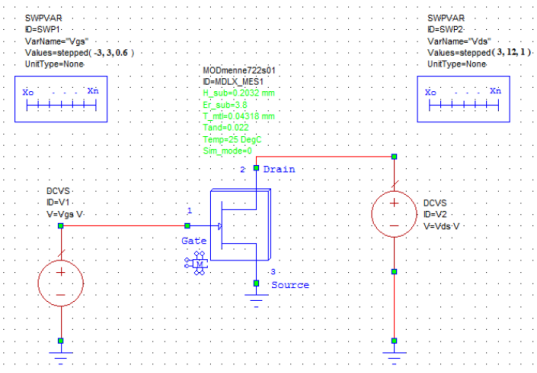
(a)



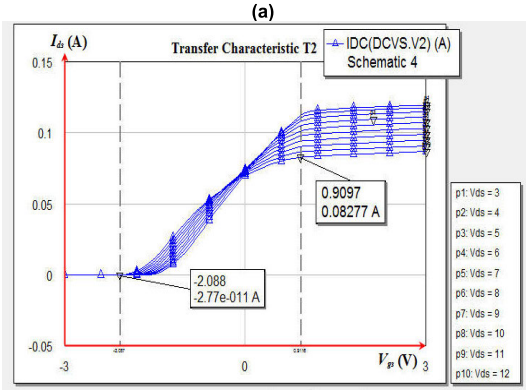
(b)

FIGURE 3. The input matching configuration using AWR software showing (a) biasing circuit (b) simulated results.

The objective here is to make the push pull amplifier to work in Class B mode therefore the drain current should be near to zero. This means that the gate-to-drain voltage V_{GS} should lies in between the threshold voltage V_{th} and the maximum gate voltage V_{MAX} ($V_{TH} < V_{GS} < V_{MAX}$) whose values are -2.09 V and 0.9 V respectively which is found by plotting the transfer characteristic of the transistor i.e. I_{DS} versus V_{GS}. The circuit used to simulate the transfer characteristic is shown in Fig 4(a) while the simulation results are shown in Figure 4(b) and it should be noted that the drain voltage is kept constant at 3 V. Since the drain quiescent current has to be near to zero for Class B operation, hence the bias gate voltage is chosen to be at -1.8 V.



(a)

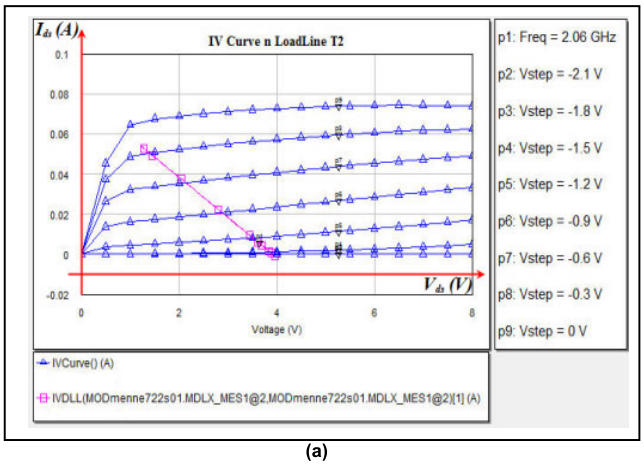


(b)

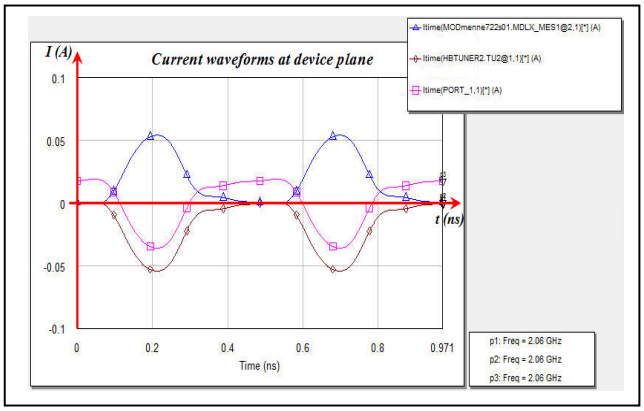
FIGURE 4. The transfer characteristic of transistor NEC NE722S01 showing (a) the biasing circuit (b) simulated results.

On the other hand, the circuit schematic as in Figure 3(a) is also used to compute the I-V curve and I-V Dynamic Load Line (IVDLL) as shown in Figure 5(a). Note that the parameter of the DC Voltage Source (DCVS) of both tuners have been set up for Class B operation. Plus, as seen in Figure 3(a), there is no current flowing in the drain to source of the device ($I_{ds} = 0\ A$) which means that the amplifier is already in the Class B mode.

Figure 5(b) shows the Class B half-rectified current waveforms at three different reference device planes (reference circuit is shown in Figure 3(a)). Ideally, we need to look at the waveform on the package model. Due to limitation, the waveform at the device plane also gives an indication of working in Class B. It would be more clearly if we could do all impedance synthesis within the package model by looking at their intrinsic waveforms.



(a)



(b)

FIGURE 5. Simulation results of device NEC NE722S01 showing (a) the DC-IV plot (b) Class B current waveforms at three different reference device planes.

B. OPTIMUM LOAD IMPEDANCE

In non-linear RF circuit simulation, harmonic balance or frequency domain analyses are widely used mainly for two reasons. First, time domain or transient analyses, in the case where there are harmonics or closely-spaced frequencies, the simulation must be run for long enough to observe one full period of the lowest frequency present since the minimum time step must be compatible with the highest frequency present. Secondly, the harmonic balance method is a powerful technique for the analysis of high-frequency nonlinear circuits such as power amplifiers, mixers and oscillators. It is well-suited for simulating analogue RF and microwave circuits, since these are naturally handled in the frequency domain. In this work, the harmonic balance method is used to perform power amplifier load-pull contour analyses. Figure 6 shows the circuit schematic used in obtaining the optimum load impedance. The reflection coefficient that is looking into the Gate of the transistor has been configured only at fundamental frequency according to simulated input impedance matching as shown in Fig. 3.6. Besides, the reflection coefficients that are looking into the Drain of the transistor will be configured only at the 2nd harmonic and 3rd harmonic frequencies. Note that device NEC NE722S01 will be used in this load-pull analysis and the same sequence of procedures applies on the analysis for Nitronex NPTB00004 but it is not shown in this paper.

The next step is to optimize load impedance Z_{load} for maximum output power. The maximum output power here is actually referring to simulated measurements of Total Power (PT) delivered at the output port and Power Added Efficiency (PAE). A lossless network incorporating a Bias Tee is used, which transforms the impedance at its Port 2 into a user-defined impedance at its Port 1. As a Class B amplifier, it requires harmonic short at the output up to the third harmonic. Therefore, the second and third harmonic reflection coefficients are set to be as $\Gamma_{2f_0} = \Gamma_{3f_0} = 0.99\angle 180°$. Since the output reflection coefficient at the fundamental frequency Γ_{f_0} is going to be swept, the start value for the reflection coefficient in the schematic can be anything, as seen in the example shown in Figure 6; it is set to be default which is $\Gamma_{f_0} = 0\angle 0°$. Note that all user-defined parameters mentioned above are specified for the lossless HBTUNER2 TU2.

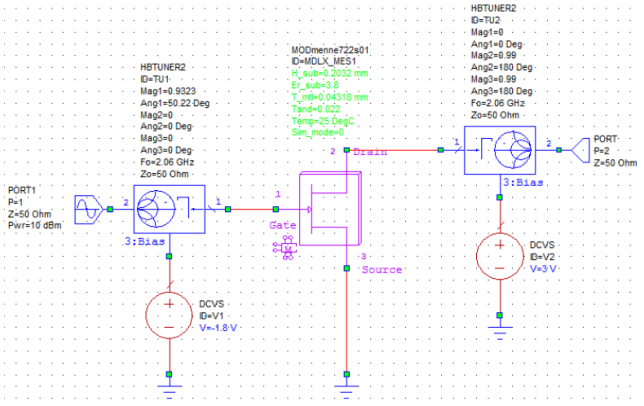


FIGURE 6. Load-pull circuit configuration.

Note that the simulation sometimes will fail to converge at certain output impedance points. This is due to non-linearity of the transistor becomes severe as the fundamental input impedance $\Gamma_{f_0} = 0.9323\angle 50.22°$ has been set in the first place to cause the maximum Gate voltage swings, hence making the Drain current reach its maximum. Generally, a convergence failure happens in highly non-linear transistor simulation due to converged impedances point density. In order to avoid the convergence failure, the converged impedance point density needs to be reduced. As a result, a rough contour at first attempt load-pull analysis which indicates the optimum load impedance can be plotted as shown in Figure 7.

Based on the coarse contour shown in Figure 7, impedance at p22 might be able to deliver about 8.8 dBm total power for the system. In order to get more accurate estimation of the load impedances for the maximum achievable PAE and PT, another load pull analysis is performed with a refined converged impedance points that focus at where the optimum load impedances of maximum PAE and PT might be.

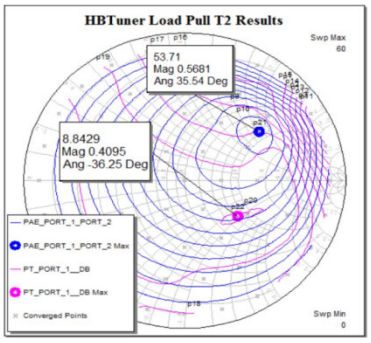
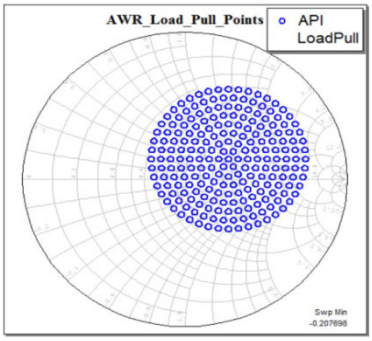
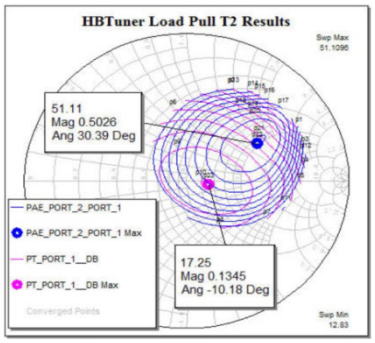


FIGURE 7. Rough contour on the Smith chart at first attempt load-pull analysis.



(a)



(b)

FIGURE 8. (a) Shrunk sweeping region of converged impedance points (b) Second attempt load-pull analysis with shrunk sweeping region.

Figure 8(a) shows a refined sweeping region of the converged impedance points and the result for this load pull analysis is shown in Figure 8(b). As can be seen in Figure 8(b), a much smaller contour indicates p23 to deliver 17.25 dBm which is 8.4 dB more output power than the first attempt of load-pull analysis. At this stage, any point on the contour could be chosen as the optimum load impedance which is able to give high PT, PAE or good compromise between PT and PAE depending on design specification.

C. SIMULATION OF CLASS B PUSH-PULL AMPLIFIER

The design of the circuit for a fully functional push pull amplifier aimed for class B can be implemented in two main parts. The first one is the implementation of the matching network in the power amplifier and the second part is the combination of sub circuits to form the whole push pull power amplifier. The availability of components and design variables are parameters that greatly limits the selection of matching networks. A point has been chosen for optimum load impedance and so one possible configuration of an integrated biasing and matching networks based on ideal components has been used to configure a single ended Class B power amplifier shown in Figure 9. In order to prevent DC current from flowing into the source and load, a capacitor placed in series configuration should be included at the Gate and Drain terminal respectively [23]. Meanwhile, the harmonic trap lies at the load side of the transistor which present an open circuit at design frequency 2.06 GHz, and a short circuit at certain harmonics. Therefore, it would be only the fundamental frequency power is transmitted. All the parameters mentioned above which include the input matching impedance at the fundamental ($\Gamma_{f_0} = 0.9323\angle 50.22°$), harmonics termination ($\Gamma_{2f_0} = \Gamma_{3f_0} = 0.99\angle 180°$) and load impedance ($\Gamma_{f_0} = 0.1345\angle -10.18°$) that capable of delivering highest total power were represented as being incorporated into the HBTUNER2. Note that this configuration is only valid for a constant input power which maintained at 10 dBm. Besides, the implied bias decoupling networks used here are ideal. In any real circuit implementation, it would be necessary to simulate the effect of bias decoupling networks on the stability.

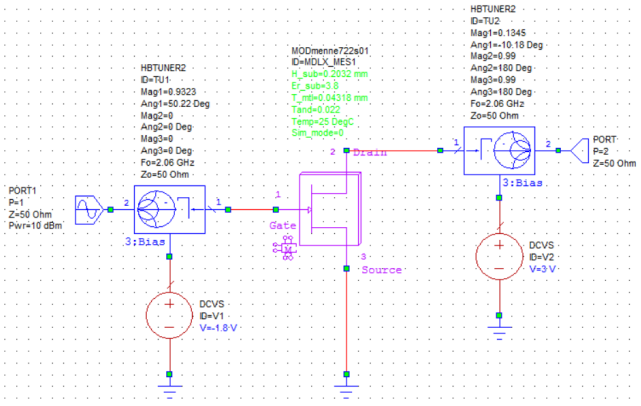


FIGURE 9. Configuration of single-ended Class B power amplifier.

Figure 10(a) shows the ideal configuration of push-pull transmitting amplifier while Figure 10(b) shows the circuit of single-ended power amplifier without harmonic terminations forming part of the sub circuit in Figure 10(a). The push pull power amplifier contains two 180° hybrids where one of them is used as a power splitter at the input side while the other one at the output is used as power combiner. The red dotted line in Figure 10(a) is where the current waveform of a Class B pushpull transmitting power amplifier with harmonic filtering up to 3rd harmonic is verifiable by observation through simulation and the results are shown in Figure 10(c). The harmonics higher than the 3rd order are causing the multiple ripples in the current waveform of Figure 10(c). Normally, to test

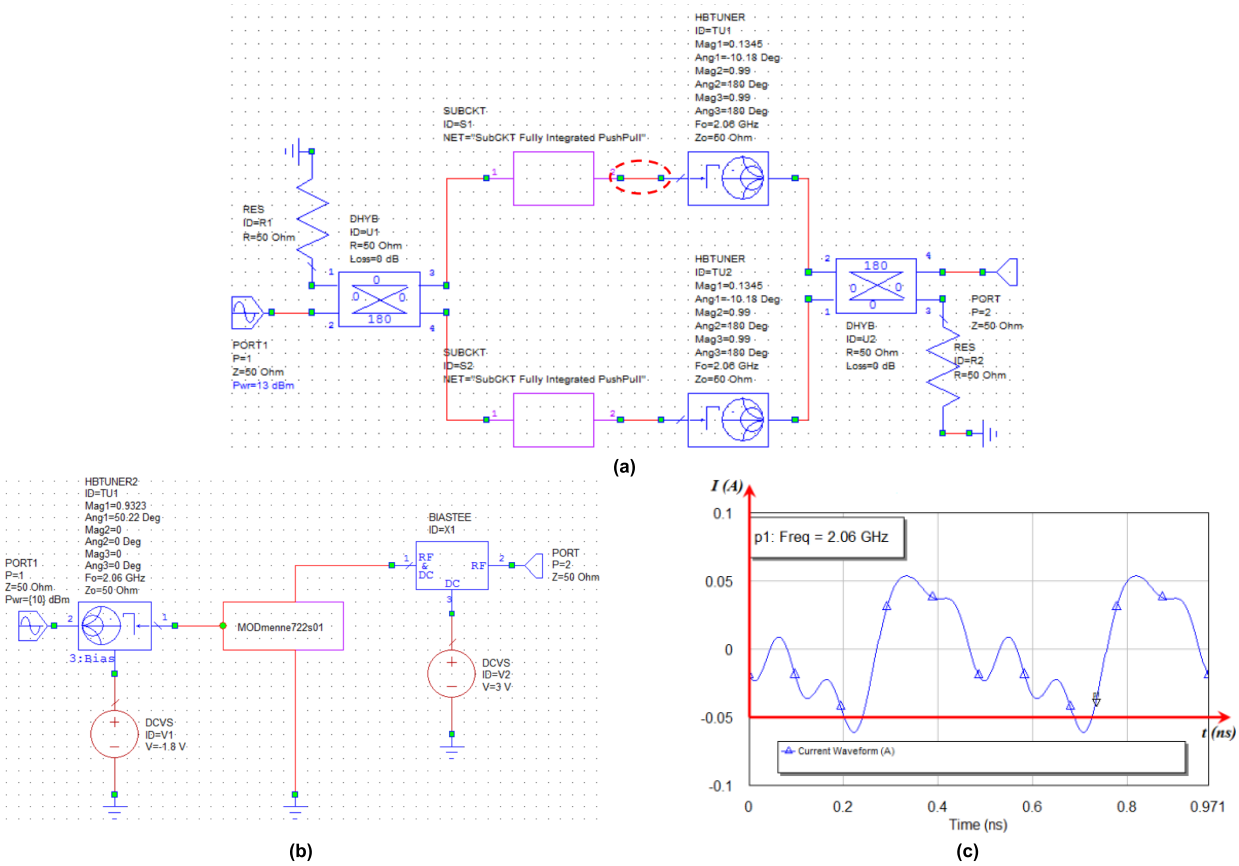


FIGURE 10. Fully integrated push pull amplifier showing (a) Ideal configuration of push-pull transmitting power amplifier with harmonic filtering up to 3rd order (b) Single-ended power amplifier without harmonic terminations (c) Waveform of a Class B power amplifier with up to 3rd order harmonic suppressed.

if the device is working under the principles of the Class B power amplifier, the current and voltage waveform analysis should be performed at the device plane by de-embedding a full package model. Nevertheless, it is still possible to know if device is operating at Class B by analyzing current waveform at the output plane but it will contain additional ripple due to the harmonics displacement current caused by the drain to source capacitance of the transistor (C_{DS}).

In order to ascertain whether it is the harmonics that is the origin of the ripples formation in the current waveform in Figure 10(c), higher harmonic traps are employed which will filter out the higher order harmonics during simulation. The circuit shown in Figure 11(a) shows the configuration for push pull amplifier embedded with harmonic traps that filters harmonic frequencies up to the 7th order. The harmonic traps sub circuits for the 4th and 5th order harmonics are shown in Figure 11(b) while the 6th and 7th order are shown in Figure 11(c). Then the new current waveform obtained by applying the harmonic traps up to the 7th order is shown in Figure 11(d) and it can be observed that the waveform contains fewer ripple therefore proving the aforementioned statement that harmonics are the cause for the occurrence of ripples in the current waveform.

III. DIFFERENTIAL APERTURE COUPLING TECHNIQUE FOR PUSH-PULL TRANSMITTING AMPLIFIER

Two types of differentially fed aperture coupled passive antennas was designed in this work and they were labelled as Structure A and Structure B. The designs were simulated with a finite ground plane using CST Microwave Studio (CST MWS) alongside the AWR Microwave Office software and the realization of the prototypes were completed to perform measurements. The main difference between the two structures is that Structure A was designed for 50 Ω odd mode impedance while Structure B gives the freedom to choose arbitrary odd mode impedance. Finally, one of the design is chosen to be realized whereby it is integrated along with the double-ended Class B power amplifier in order to create a push-pull transmitting amplifier configuration. The circuit in Figure 12 gives a bird's eye view on where the push-pull transmitting amplifier is going to be integrated with the antenna whereby the red dashed-line on the circuit is going to be replaced by the proposed structure A and B.

Pozar explained that the single fed aperture coupled antenna uses an extended microstrip line with approximate length of λ/4 beyond the edge of slot/aperture and terminated

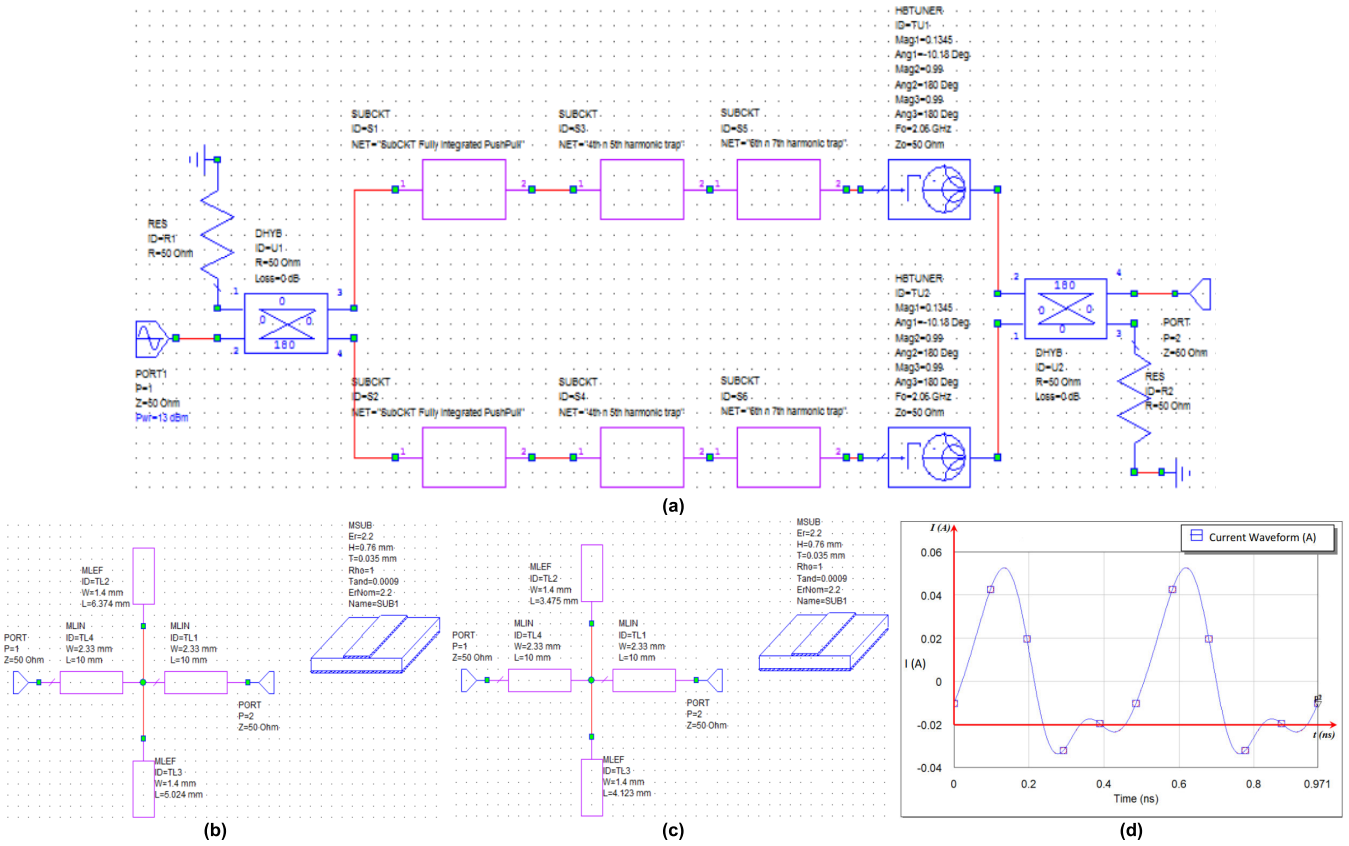


FIGURE 11. Higher order filtering showing (a) Push-pull power amplifier with integrated higher order harmonic traps (b) 4th and 5th harmonic sub circuit traps (c) 6th and 7th harmonic sub circuit traps (d) Waveform of a Class B power amplifier with up to 7th order harmonic suppressed.

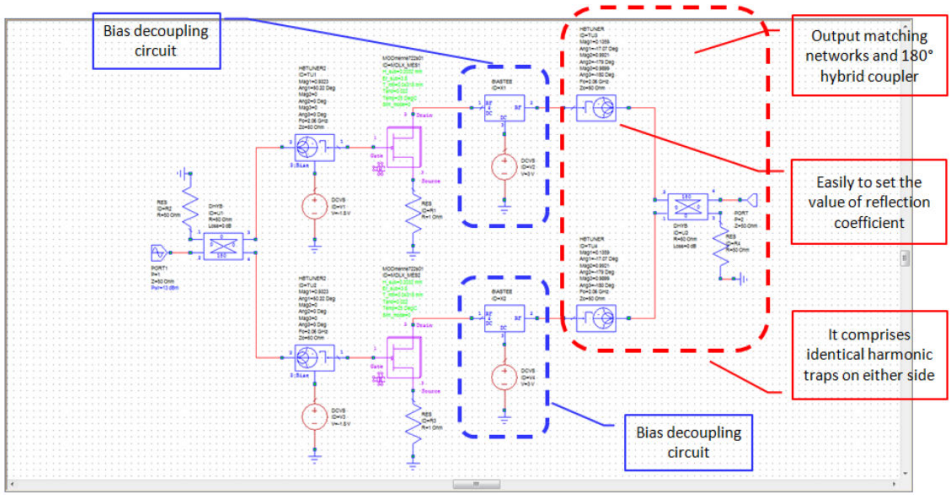


FIGURE 12. Ideal configuration of push-pull transmitting power amplifier.

in an open-circuit [24]. This technique has helped in the making of an effective virtual short-circuit in the middle of the slot/aperture where the current is at its peak value. This makes the microstrip patch antenna to be electromagnetically coupled with the maximum current. This method of antenna feeding technique is based upon the open-short circuit transmission line theory [25] and is demonstrated in Figure 13. Whereby the distance d = l having load impedance Z_L and this gives us the input impedance Z_{IN} as

$$Z_{IN}(\ell) = Z_0 \frac{Z_L + jZ_0 \tan(\beta\ell)}{Z_L + jZ_L \tan(\beta\ell)} \quad (1)$$

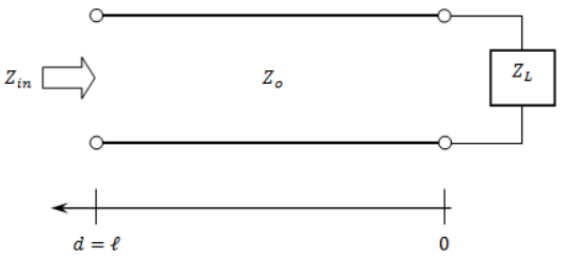


FIGURE 13. A lossless transmission line terminated in the impedance Z_L.

Let the load impedance $Z_L = \infty$ (open circuit condition) then equation (1) becomes

$$Z_{IN}(\ell) = -jZ_0 + \cot(\beta\ell) \tag{2}$$

When a distance from the load, $\ell = \frac{\lambda}{4}$, then

$$Z_{IN}\left(\frac{\pi}{2}\right) = -jZ_0 \cot\left(\frac{\pi}{2}\right) \tag{3}$$

Therefore, it is seen that by leaving a distance of λ/4 between the microstrip line end (open-circuit), the input impedance $Z_{IN} = 0$ thereby showing that the current formed at this point is at its highest which creates a virtual circuit making sure that there is strong coupling between the electromagnetic energy to the patch antenna via the aperture and this is illustrated in Figure 14. The single fed aperture coupled microstrip antenna having open-circuit stub is shown in Figure 14 as separate layers comprising its whole structure.

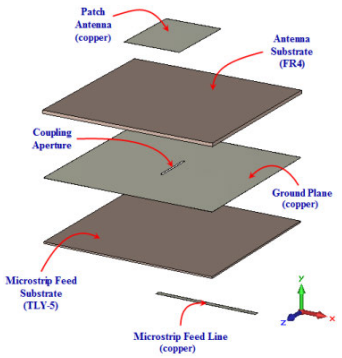


FIGURE 14. Separated layers of a single fed aperture coupled microstrip antenna.

A. 50Ω DIFFERENTIAL INPUT VERSION (STRUCTURE A)

The design of the differential fed aperture coupled half wavelength patch was done at resonant frequency of 2.062 GHz with the top layer shown in Figure 15(a) and is made of FR-4 substrate having dielectric constant $\varepsilon_{r1} = 4.4$ whereby the antenna patch is etched on it. The bottom layer shown in Figure 15(b) which is made of another substrate namely the Taconic TLY-5 having dielectric constant $\varepsilon_{r2} = 2.2$ and it is supporting the ground plane (copper) having a slot within it and is sandwiched between the two substrates and finally the microstrip feed line is etched on the bottom layer as shown

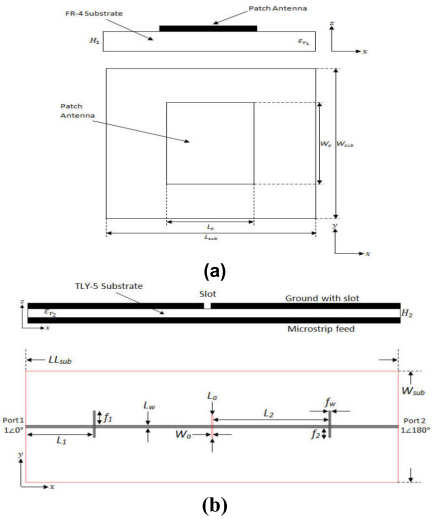


FIGURE 15. Structure A containing (a) Top layer (b) Bottom Layer.

previously in Figure 14. The dimension of for the Structure A is tabulated in Table 3.

TABLE 3. Dimensions for structure A.

LAYER	DIMENSIONS
ANTENNA PATCH	W_p x L_p = 37 x 28 mm
FR-4 (ε_{r1} = 4.4) ANTENNA SUBSTRATE	H_1 = 1.6 mm W_{sub} = L_{sub} = 100 mm
GROUND PLANE (COPPER) SLOT	W_a = 1 mm L_a = 20 mm
TACONIC TLY-5 (ε_{r2} = 2.2)	H_2 = 0.8 mm W_{sub} = 100 mm LL_{sub} = 285.4 mm
MICROSTRIP FEED (WITH BANDSTOP FILTERS ACTING AS HARMONIC TRAPS)	L_1 = 51.925 mm L_2 = 89.375 mm L_w = 2.33 mm f_1 = 12.975 mm (λ/4 at $2f_0$) f_2 = 8.595 mm (λ/4 at $3f_0$) f_w = 1.4 mm

The work done in this paper uses a methodology that was described in [26] whereby the external Class B (NEC NE3210S01 PHEMT) push-pull power amplifier was used to generate the differential signals which would then be fed to the aperture couple antenna. Theoretically, in order to obtain maximum current (I_{MAX}) or virtual short circuit ($V = 0\ V$), out-of-phase signals have to be fed into the two ends of the microstrip feed line. This ensures that electromagnetic energy is efficiently coupled from the microstrip feed line to the patch antenna via single aperture (slot) [27]. Therefore, differential feeding technique for push-pull Class B amplifier is used to demonstrate the usage of a new proposed power combiner which was adapted from the previous aperture-coupled differential antenna structure published in [26], [27]. The advantages by using such a concept is that there is a higher efficiency and greater battery life. This structure differs from the previous aperture-coupled technique in that it comprises identical harmonic traps on either side of the aperture, using resonant stubs to form bandstop filters (BSF).

Since the amplifiers are integrated, harmonic terminations should be taken into consideration. Hence, bandstop filters were designed in order to control the harmonics. In this study, only 2nd ($2f_o$) and 3rd ($3f_o$) harmonics were taken into account. The bandstop filters (BSF) employed in the configuration as shown in Figure 15, will cause a further mismatch at fundamental (f_o). Therefore, the 50 Ω lines which are connected to the both ends of microstrip feed line need to be optimized and neatly tuned by adjusting their electrical length in order to use the filter's susceptance to match the antenna.

The line length L_1 should provide 180° phase compensation in the electrical length so that the reflection coefficient at the respective harmonics will be seen like a short circuit (Magnitude = 1, Angle = 180°). The line length L_2 is an optimised 50 Ω line length to ensure the fundamental (f_o) at its best state whereas for this case, the lowest possible reflection magnitude is close to zero (Magnitude = 0) is desired to be achieved. This is unlike the previous differentially fed aperture coupled active antenna whereby no harmonic trap was integrated within the circuit configuration. It was just active devices were simply integrated with the aperture coupled antenna without taking into consideration the harmonic impedances presented to the non-linear devices. As can be seen in Figure 16(a), at fundamental frequency ($f_0 = 2.062$ GHz) the reflection magnitude is not even close to zero (mismatched). Although it was mentioned in [16] that the aperture-coupled antenna structure is like a matching network and 0 *dB* power combiner, but still the reflection coefficient at the fundamental is considered very poor. Also from Figure 16(a), the reflection coefficient at harmonics ($2f_0 = 4.124$ *GHz* and $3f_0 = 6.186$ *GHz*) does not show any signs of perfectly suppressed (0.99∠180°).

In Figure 16(b), a good match at fundamental is achieved where the reflection coefficient magnitude is almost equal to zero. The 2nd($2f_0$) and 3rd ($3f_0$) harmonics were suppressed perfectly as they were seen like a short circuit where both the magnitude and angle were close to unity and almost equal to 180° (≈0.99∠180°) respectively. The improvement at fundamental frequency is achieved by adjusting L_2 while harmonic suppression is done by adjusting the line length L_1.

On the other hand, Figure 17 shows the comparison between measured and simulated return loss of the structure with 50 Ω differential input. A 2-port S-parameter measurement was conducted using Agilent 8720ES network analyzer and the odd-mode return loss, S_{Odd} was obtained using Eqn. (4).

$$S_{Odd} = S_{1,1} - S_{2,2} \tag{4}$$

The measured result shows the resonant frequency is shifted up to 2.111 GHz, a 2.5% frequency shift from the simulated resonance. This frequency shift is due to the tolerances of dielectric constant from both substrates which are FR-4 and Taconic TLY-5. Other possible explanations are:

- During the etching process there may be errors over the length and width of the patch such as if there is a minor over-etching it will cause the distributed capacitance to be reduced thereby causing the frequency to be shifted at higher value.
- Misalignment between the layers cold reduce interlayer capacitance thereby shifting the frequency upwards.
- There may also be small air gaps between the layers causing the overall effective dielectric constant to be reduced and therefore increasing the frequency.

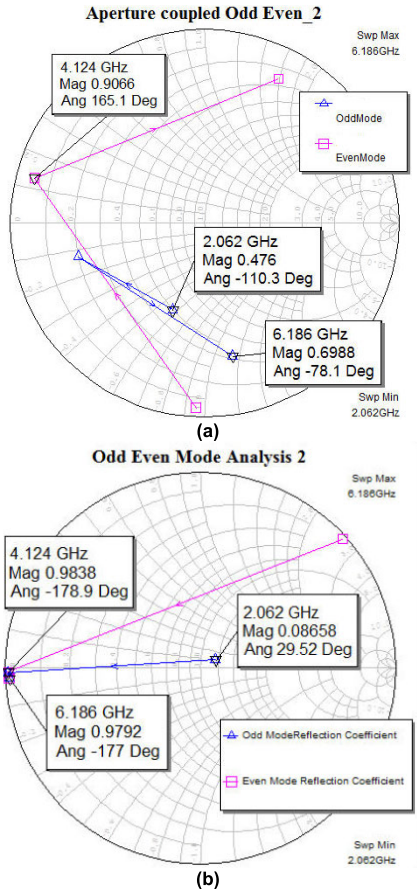


FIGURE 16. Simulation of aperture-coupled technique (a) without harmonic termination (b) new proposed structure with built-in harmonic termination.

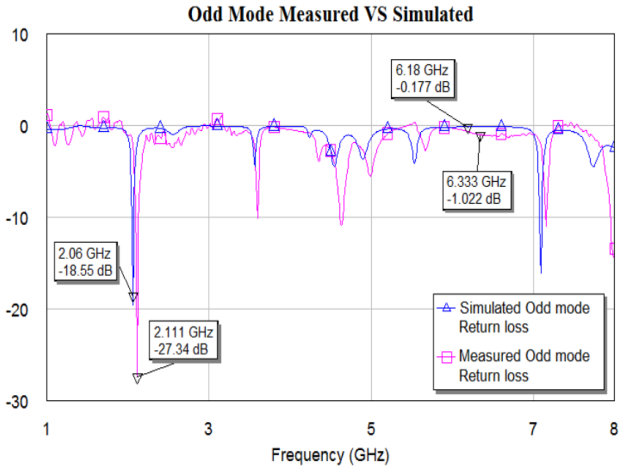


FIGURE 17. Comparison of the odd mode return loss for Structure A.

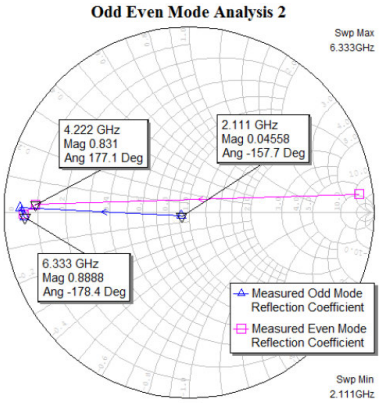


FIGURE 18. Measured odd mode reflection coefficient of Structure A.

Measurements for the odd and even mode reflection coefficients for fundamental frequency at 2.111 GHz as well as for 2nd harmonics and 3rd harmonic frequencies were performed and the results shown in Figure 18. There is a good match at fundamental frequency as the reflection coefficient is close to zero with impedance around 45.9 Ω by deformalizing to 50 Ω. Now for the 2nd and 3rd harmonic frequencies (which is 4.222 GHz and 6.333 GHz for the 2nd and 3rd harmonics respectively) the measurements shows that they have been well negated since the reflection coefficient magnitude and their angle respectively are $0.831\angle 177.1°$ and $0.8888\angle -178.4°$ which is close to unity and 180°.

B. COMPLEX ARBITRARY INPUT IMPEDANCE VERSION (STRUCTURE B)

The previous Structure A was purposely designed particularly to comply with the standard 50 Ω environment. However, this unique advantage of universal connectability also has some drawbacks and it has been highlighted and explained earlier in the previous section. This section will present another design of a differentially fed aperture coupled microstrip antenna that involves a complex impedance requirement. This new proposed structure can be used to set the odd-mode fundamental frequency impedance to a value required for the class B load-line of a given transistor which is effectively incorporating the output matching circuit into the combined filters and power combiner.

Similar to Structure A, the design of Structure B used the same substrate material with the same properties such as thickness and dielectric constant for both top and bottom layers. The difference in Structure B is that it is a reduced-size version of Structure A, in which the optimized 50 Ω line length L_1 and L_2 in Structure B are λ/2 shorter than that of Structure A where the line length $L_1 = 27.175$ mm and $L_2 = 13.875$ mm respectively. Besides, while keeping the original slot length, L_a as well as slot width, W_a in Structure A, the straight line slot is replaced by a new slot shape with added two slots ($LL_a = 6$ mm each), forming a cross shape.

TABLE 4. Dimensions for structure B.

LAYER	DIMENSIONS
ANTENNA PATCH	W_p x L_p = 37 x 28 mm
FR-4 ($\varepsilon_{r1} = 4.4$) ANTENNA SUBSTRATE	$H_1 = 1.6$ mm $W_{sub} = 80$ mm $L_{sub} = 85.9$ mm
GROUND PLANE (COPPER) SLOT	$W_a = 1$ mm $L_a = 20$ mm $LL_a = 6$ mm
TACONIC TLY-5 ($\varepsilon_{r2} = 2.2$)	$H_2 = 0.8$ mm $W_{sub} = 80$ mm $L_{sub} = 85.9$ mm
MICROSTRIP FEED (WITH BANDSTOP FILTERS ACTING AS HARMONIC TRAPS)	$L_1 = 27.175$ mm $L_2 = 13.875$ mm $L_w = 2.33$ mm $f_1 = 12.975$ mm (λ/4 at $2f_0$) $f_2 = 8.595$ mm (λ/4 at $3f_0$) $f_w = 1.4$ mm

As summarized in Table 4, the top layer consists of an FR-4 substrate ($H_1 = 1.6$ mm, $\varepsilon_{r1} = 4.4$, $W_{sub} = 80$ mm, $L_{sub} = 85.9$ mm) with the rectangular patch antenna ($W_p \times L_p = 37 \times 28$ mm) etched on it whereby the configuration is exactly as shown in Figure 15(a) except with the dimensions mentioned above. The bottom layer as shown in Figure 19 is another substrate from Taconic TLY-5 ($H_2 = 0.8$mm, $\varepsilon_{r2} = 2.2$, $W_{sub} = 80$ mm, $L_{sub} = 85.9$ mm) supporting the ground plane with a new cross shaped slot ($W_a = 1$ mm, $L_a = 20$ mm) sandwiched between those two substrates. The microstrip feed line is etched on the bottom layer. Again, note that as a Class B amplifier, it requires a harmonic short or Band Stop Filter (BSF) at the output side. These harmonic shorts are generated by the two open-circuit stubs with dimensions similar to those used in Structure A.

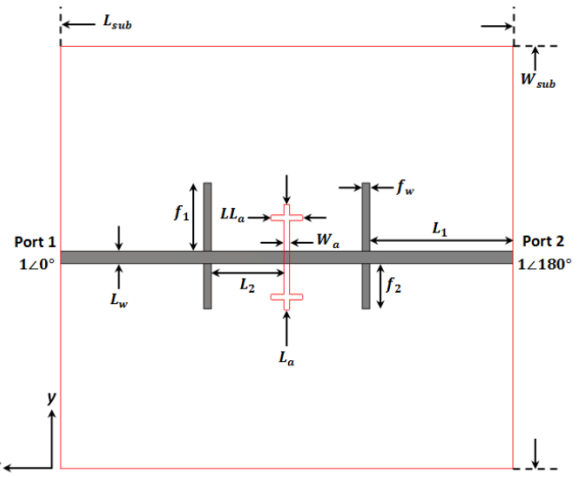


FIGURE 19. Layout of Structure B (bottom layer).

The susceptance of the BSF elements is used in the fundamental frequency matching network by optimizing the lengths of the 50 Ω lines between the slot and the stubs. This new technique makes use of the odd-mode fundamental signal to generate maximum current under the antenna and efficiently couple the electromagnetic energy from a

microstrip feed line to the antenna via an aperture or slot. The proposed design suppresses harmonic voltages at $2f_o$ and $3f_o$, whilst also optimizing the load line impedance seen by the two amplifiers at the fundamental frequency in odd mode at f_o (2.06 GHz).

As can be seen in Figure 19, the line length L_1 is a non-zero value in order to establish a proper microstrip mode before the junctions with the harmonics stubs. In order to provide a short circuit at the harmonics, the L_1 is either made 180° long or its effect is de-embedded in order to give impedance at the junction with the stubs. The line length L_2 is a variable that can be used to tune the reflection coefficient at the fundamental (f_0) to the required value of odd mode impedance requirement for the amplifier performance.

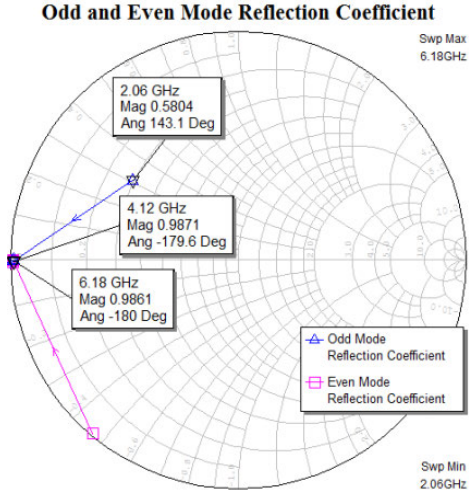


FIGURE 20. Simulated results of odd and even mode reflection coefficients.

Figure 20 shows the simulated results of odd and even mode reflection coefficients at fundamental frequency, 2nd harmonic and 3rd harmonic for the proposed design shown in Figure 19. This Structure B has been specifically designed to meet the impedance requirement of a given transistor (NPTB00004) at fundamental frequency with simultaneously suppressed harmonics.

In order to demonstrate how the new proposed structure is used to set the odd mode fundamental frequency impedance by simulation, the line length L_2 in Structure B has been varied and specifically tuned so that it will comply with the impedance requirements imposed by NPTB00004 RF Power GaN HEMT. In this case, a good compromise between achievable maximum Power Added Efficiency (PAE) and Total Power (PT) is concerned. Figure 21 shows a simulated load-pull contour of shrunk sweeping range for that particular transistor which indicates where desired optimum load impedance might be for PT at the output and PAE respectively.

Figure 22 shows a trajectory of the odd mode reflection coefficient for the proposed structure on a Smith chart. There are nineteen red squares on the Smith chart resulting

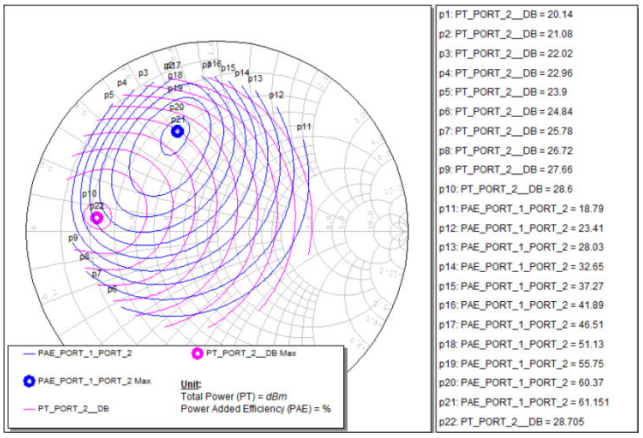


FIGURE 21. Load-pull contour of NPTB00004 RF Power GaN HEMT.

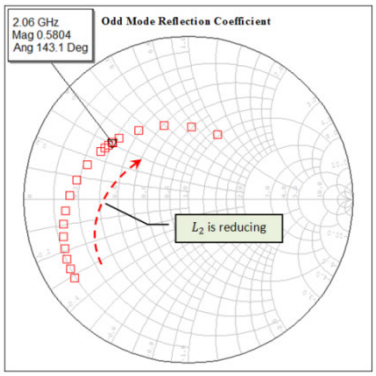


FIGURE 22. Trajectory of the odd mode reflection coefficient.

from nineteen different L_2 values moving towards the slotted ground plane whilst keeping all other parameters constant. This is what we would expect when we move a fixed capacitance (the stub reactance) up and down a fixed length of transmission line. Based on Figure 21 and Figure 22, we can see there is at least one point which falls onto the requirement of optimum load impedance for getting a very good compromise between PT and PAE. More generally, the trajectory suggests that the design variables available here including the size and shape of the aperture and the 50 Ω line length, allow good coverage of the Smith so that a wide range of matching requirements could be met particularly for different devices and bias conditions. As for our proposed design of Structure B shown in Figure 19, the reflection coefficient at 2.06 GHz is chosen to be at $0.5804\angle 143.1°$ which will give a considerably good PAE as well as reasonably high PT.

Generally, the Structure B shown in Figure 19 is designed using CST software and hence, it is not showing any other devices attached on the Structure B in the simulation. This is because of the integration of push-pull amplifier using two identical transistors (NPTB00004 RF Power GaN HEMT) and Structure B will be made and done in AWR MWO software. Basically, the line length L_1 of Structure B is purposely made 180° before the junctions with the harmonic

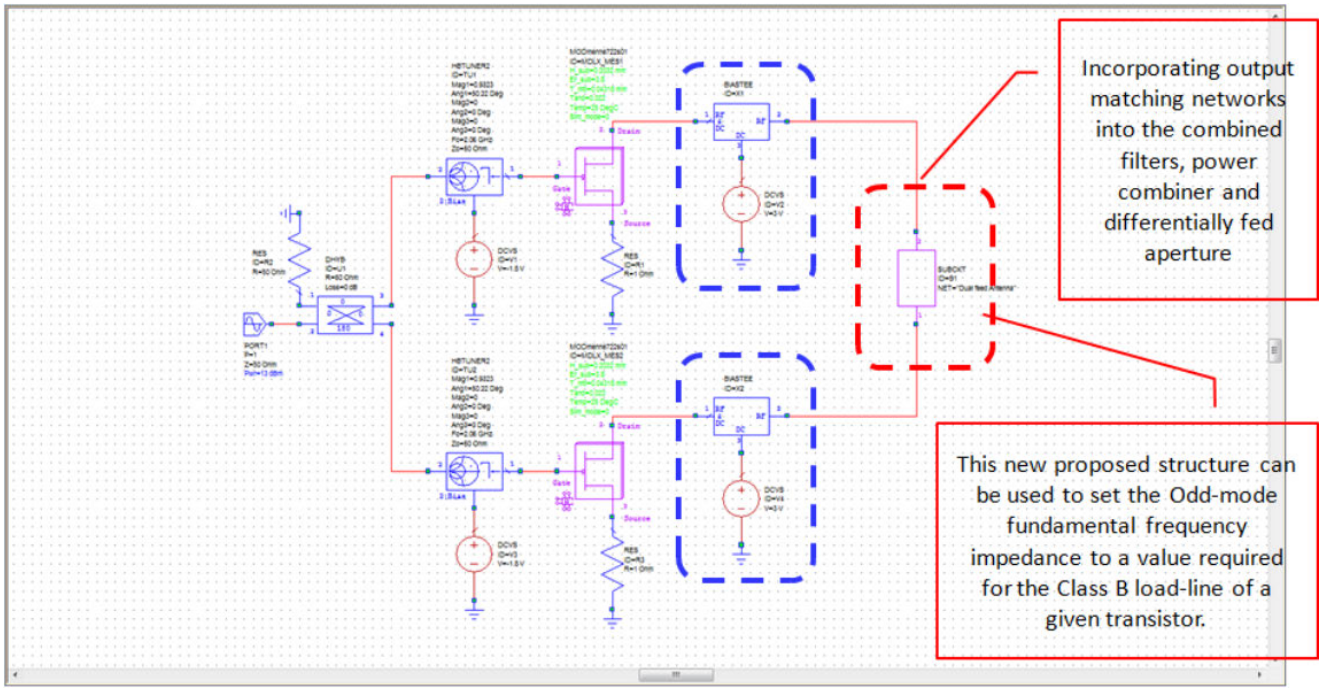


FIGURE 23. Representation of new proposed push-pull transmitting power amplifier.

stubs in order to establish a proper microstrip mode and thus, providing harmonics short effects. The simulated reflection coefficients for the odd- and even-mode shown in the previous Figure 20 are the resulting of the line length L_1 effects is de-embedded in order to give impedance at the junction with the harmonic stubs. As a result, the 2nd (4.12 GHz) and 3rd (6.18 GHz) harmonics are seen as a short circuit and considered as perfectly suppressed since the reflection coefficient is 0.9871∠179.6° and 0.9861∠-180° respectively.

Simultaneously, the reflection coefficient or impedance at the fundamental (2.06 GHz) is tuned at 0.5804∠143.1° in which it complies with the impedance requirements imposed by the transistor NPTB00004 RF Power GaN HEMT based on the simulated load-pull shown in Figure 21. In other words, a point at where the junctions with the harmonic stubs will present impedance matching or reflection coefficients as mentioned above. Since both amplifiers have been specifically designed to be working in Class B where harmonics should be seen as short circuit 0.99∠180° and based on the transistor's simulated load-pull at the fundamental frequency, the differential signals generated by these amplifiers can be directly injected at the aforementioned point. This whole configuration has the potential to form a new push-pull transmitting amplifier and it is shown in Figure 23. This could be best if compared with the conventional push-pull amplifier's version shown in Figure 12 using ideal user-defined HBTUNER at the output stage.

The comparison has been made through simulation between an ideal push-pull transmitting amplifier (Figure 12) and this new representation of a push-pull amplifier as seen in Figure 23. The current waveforms have been captured and compared at the node before entering a red dashed-line sub circuit block. Figure 24 shows the comparison of those current waveforms, which have a good agreement. They differ slightly in the ripples due to the effects from higher order harmonics such as 5th and 7th. The reasonable agreement between the waveforms in Figure 24 gives a verification of the proposed new structure. Noted that we are aware this is all observational and empirical as ideally, the current and voltage waveforms should be measured at the full package model to be able to properly use their intrinsic waveforms within the device package as a means of determining Class B mode of operation. Due to the limitation, this is not possible

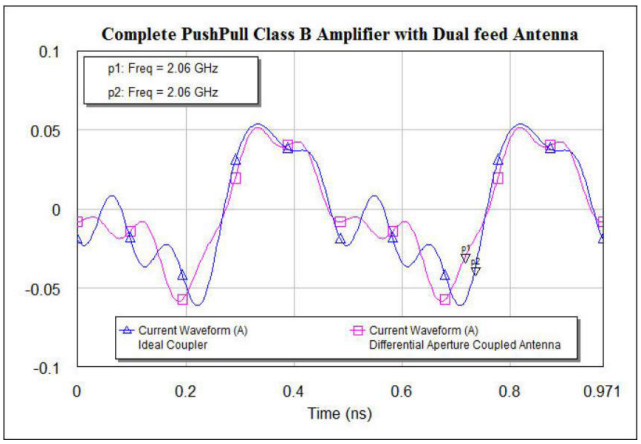


FIGURE 24. Comparison of the current waveforms.

without a full package of an equivalent circuit model. At least, the current waveform at the device plane gives an indication of working in Class B.

C. PARAMETRIC STUDY ON DESIGN SLOT A

The main objective of this parametric study was to investigate and characterize the basic proposed design of a differentially fed aperture coupled microstrip antenna so as to grasp and analyze the effect on the range of values obtained for odd mode impedance or the reflection coefficient at fundamental frequency, 2nd harmonics and 3rd harmonics when one of the parameters is varied on. There are four parameters namely the filter width (f_w), slot width (W_a), slot length (L_a) and lastly adjusting the filter position as shown in Figure 25, that have been varied each one at a time. Do note that the design of slot A was inspired from the slot design of Structure A and all the dimensions in this primary design is similar to Structure B with exception of the slot's shape.

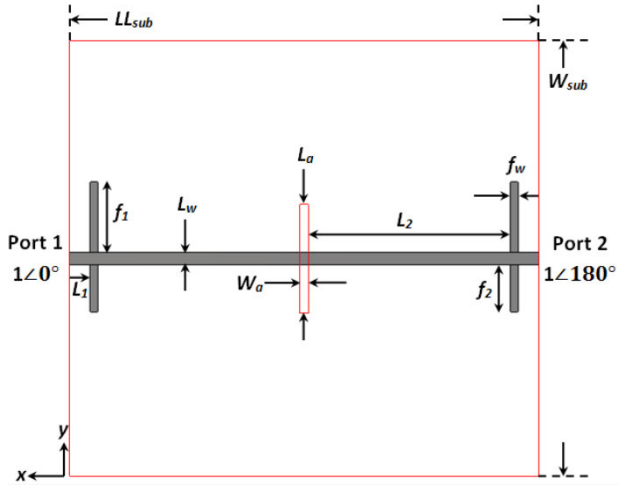


FIGURE 25. Primary design for parametric study (bottom layer).

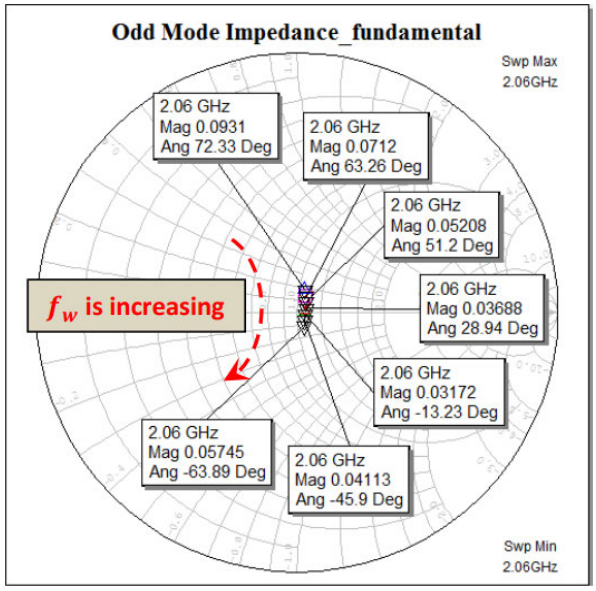


FIGURE 26. Variation of the odd mode reflection coefficient at fundamental f_0.

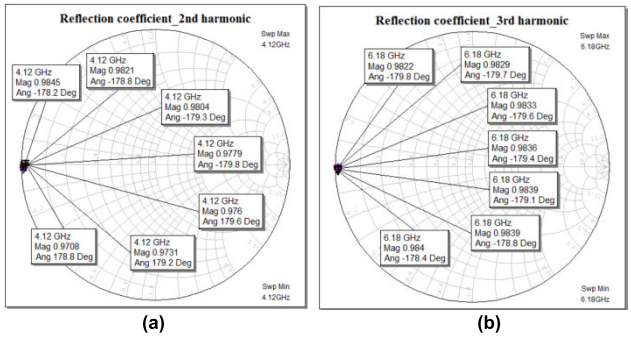


FIGURE 27. (a) Variation of the even mode reflection coefficient at 2nd harmonic. (b) Variation of the odd mode reflection coefficient at 3rd harmonic.

The filter width f_w is varied beginning from 1.1 mm to 1.7 mm in variation of 0.1 mm whereas there should be seven different values of the odd mode reflection coefficient displayed on the Smith chart which is shown in Figure 26. It can be seen from Figure 26 that the variation of the filter width f_w produces only a small effect on the odd mode reflection coefficient simulated at fundamental frequency This means that varying the width alters the susceptance of the stub in such a way that the variation produces a conductance arc, showing the plot of the odd mode reflection coefficient on the Smith chart. Here the primary filter width is taken at 1.4mm which produces and odd mode reflection coefficient of $0.03688\angle 28.94°$.

As mentioned before, the parametric study will also be performed on the harmonics. Therefore, the Figure 27(a) and Figure 27(b) shows the effect of the variation of the filter width at 2nd harmonic and 3rd harmonic respectively. It can be seen that the variations have very little effect at the 2nd and 3rd harmonic frequency because they are in short circuit i.e. the line impedance has no effect here meaning the stub's length is barely changed thereby not affecting the short circuit operations needed to terminate the harmonics.

Another factor which was varied is the slot width dimension whereby it is taken in the range of 0.5 mm to 1.5 mm having steps of 0.1 mm. It can be seen from Figure 28 that for a small increment in slot width (W_a) values there is quite a big gap between the odd mode reflection coefficients obtained at fundamental frequency. The reason for such a coarse trajectory is because of the varying radiation resistance and the coupling capacitance being also changed by the line L_2 and the stub capacitance. There will be wide coverage of the Smith chart therefore meaning that a wide range of impedance requirements can be realized.

The variation of the slot width at 2nd and 3rd harmonics produces no effect on the reflection coefficient since the harmonics are still short circuited and this is shown in Figure 29.

The slot length L_a is varied in steps of 1 mm with the primary slot length taken at $L_a = 20$ mm which mean variation

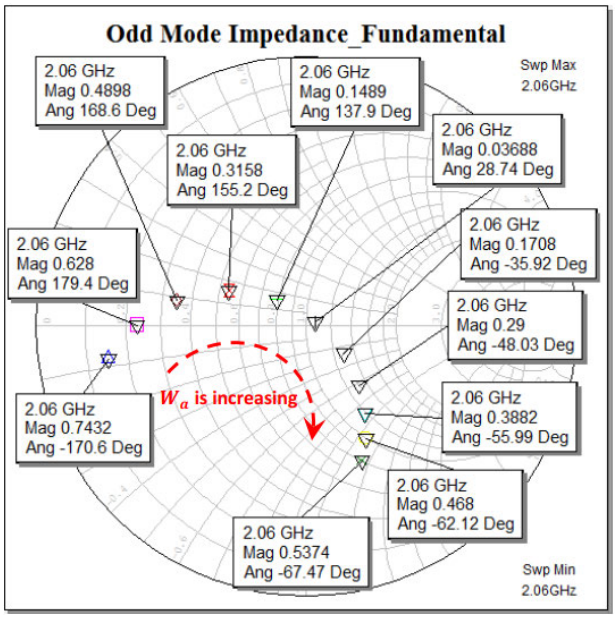


FIGURE 28. Variation of the odd mode reflection coefficient at fundamental, f_0.

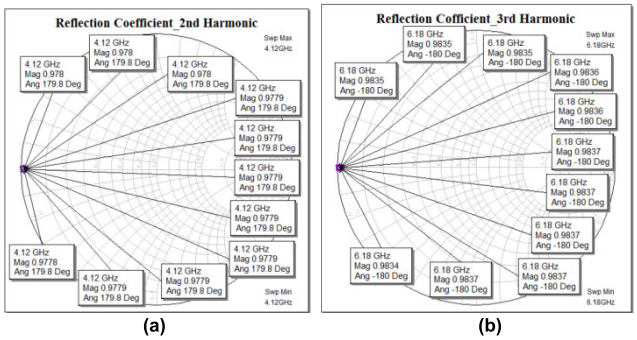


FIGURE 29. (a) Variation of the even mode reflection coefficient at 2nd harmonic. (b) Variation of the odd mode reflection coefficient at 3rd harmonic.

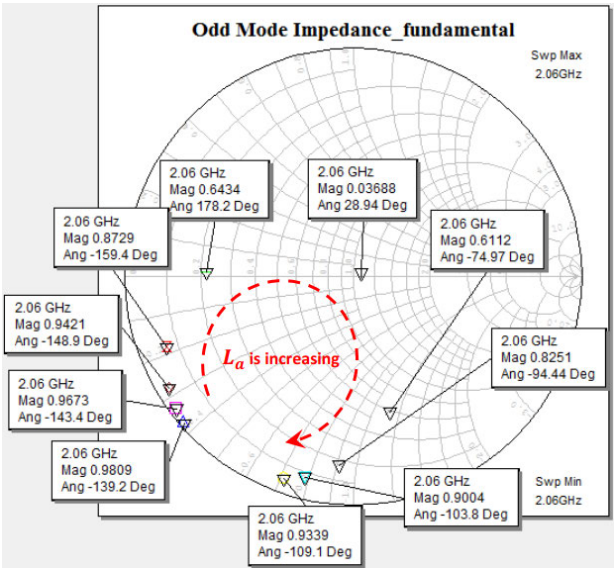


FIGURE 30. Variation of the odd mode reflection coefficient at fundamental, f_0.

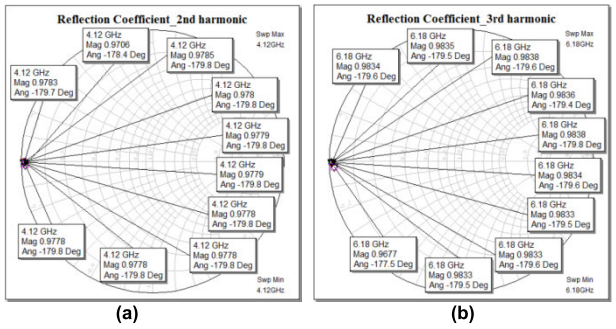


FIGURE 31. (a) Variation of the even mode reflection coefficient at 2nd harmonic. (b)Variation of the odd mode reflection coefficient at 3rd harmonic.

is ranging from smallest length at 15mm to the longest length at 24 mm. It is seen in Figure 30 that by varying the slot length, the odd mode reflection coefficient at fundamental frequency changes nonlinearly and plotting its values forms a near complete circle. The circle is somehow comparable to the trajectory of the arc in Figure 28 with the difference here that the plotted values nearly reaches the circumference of the Smith chart since the resonance of the transmission line is linked with the slot. The trajectory here offers an adequate amount of coverage meaning there is a large variety of choices for satisfying the impedance matching requirement.

It is also observed from the simulation results obtained shown in Figure 31, whereby the slot length variation performed at harmonic frequencies shows inadequate changes to the reflection coefficient values.

The last part of this parametric analysis for design slot A is to observe the effect it has on reflection coefficient. Therefore, here two parameters were varied, firstly three different values of slot width W_a (i.e. 0.5 mm, 1 mm and 1.5 mm) are chosen. Then, for each of these specific width the simulation is performed for 35 different values of L_2 which ranges from $L_2 = 38.45$ mm to $L_2 = 4.45$ mm with steps of 1 mm. The results are shown in Figure 32 whereby there are three different trajectories for the different filter width and they have peculiar characteristics. These trajectories depict the reflection coefficient values needed for satisfying the impedance matching requirement for any devices and bias conditions. Such a result is to be expected as having the transmission line connected to an impedance other than 50 Ω and varying its length and changing filter width would yield different trajectories. The reason behind this is that by changing the slot width, the coupling capacitance at transmission line joining the filter is altered hence the simulation result yield different arc for different slot width values.

D. PARAMETRIC STUDY ON DESIGN SLOT B

In the previous parametric study, most of the odd mode impedances have covered the lower region on the Smith chart.

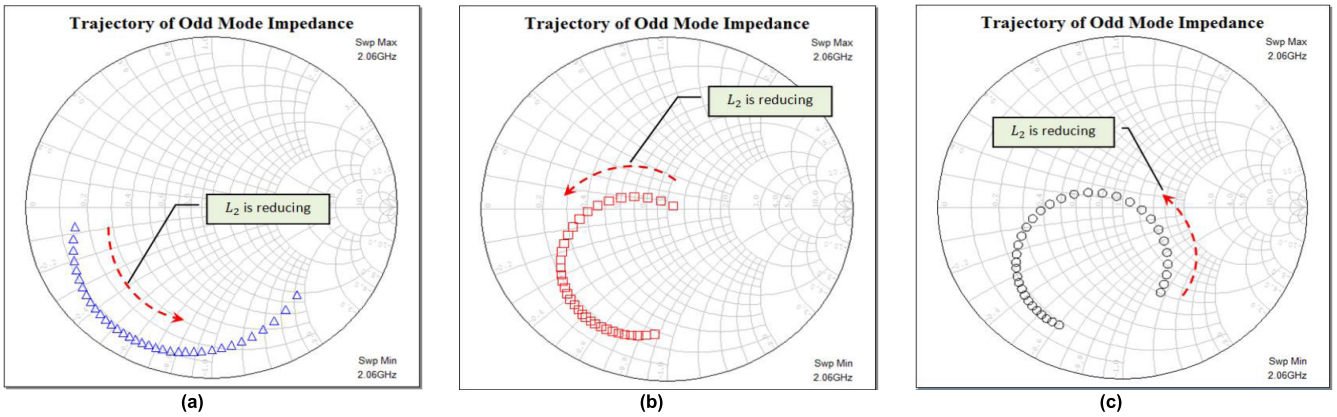


FIGURE 32. (a) Trajectory of the odd mode impedance when changing L_2 and maintaining the slot width $W_a = 0.5$ mm (b) Trajectory of the odd mode impedance when changing L_2 and maintaining the slot width $W_a = 1.0$ mm (c) Trajectory of the odd mode impedance when changing L_2 and maintaining the slot width $W_a = 1.5$ mm.

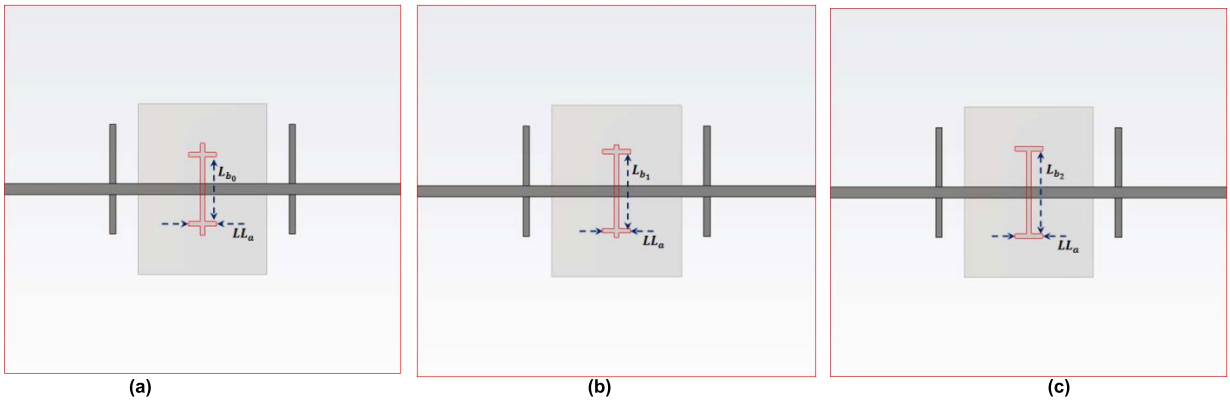


FIGURE 33. Different design of slotted ground planes.

In this section, another set of novel techniques will be investigated, aimed at covering the upper region of Smith chart with every possible point of the odd mode impedance matching requirement. The parameter variables involved in this study is based on the primary design of Structure B shown in Figure 19. The effects of moving filter point towards designated slot are considered. There are three different design of slotted ground planes involved in this study. They are shown in Figure 33.

Based on Figure 33, for three different values of L_b ($L_{b0} = 14$ mm, $L_{b1} = 16$ mm and $L_{b2} = 18$ mm), variation of the odd mode reflection coefficient has been determined by simulation for 16 different values of L_2 which is started from $L_2 = 38.45$ mm until $L_2 = 23.45$ mm in 1 mm step. Figure 34 shows the effect on a trajectory of the odd mode impedance based on the moving filter points towards different designated slotted ground plane. It seems the trajectory of the odd mode reflection coefficient has good coverage on the Smith chart especially the upper region.

This novel technique allows the power combiner and matching network functions to be integrated into the two-port antenna structure. It has sufficient degree of freedom so that

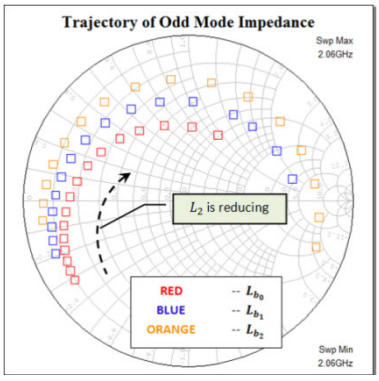


FIGURE 34. Trajectories of odd mode impedance at fundamental, f_0.

we can simply and systematically vary the available parameters to fit with the requirement of the design specification for any given devices and bias conditions. Therefore, it can offer advantages of neat and tight integration of a push-pull transmitting amplifier. Furthermore, controlling other higher harmonic impedances using open-circuit stubs will produce less-distorted output waveforms at a cost of rising in complexity.

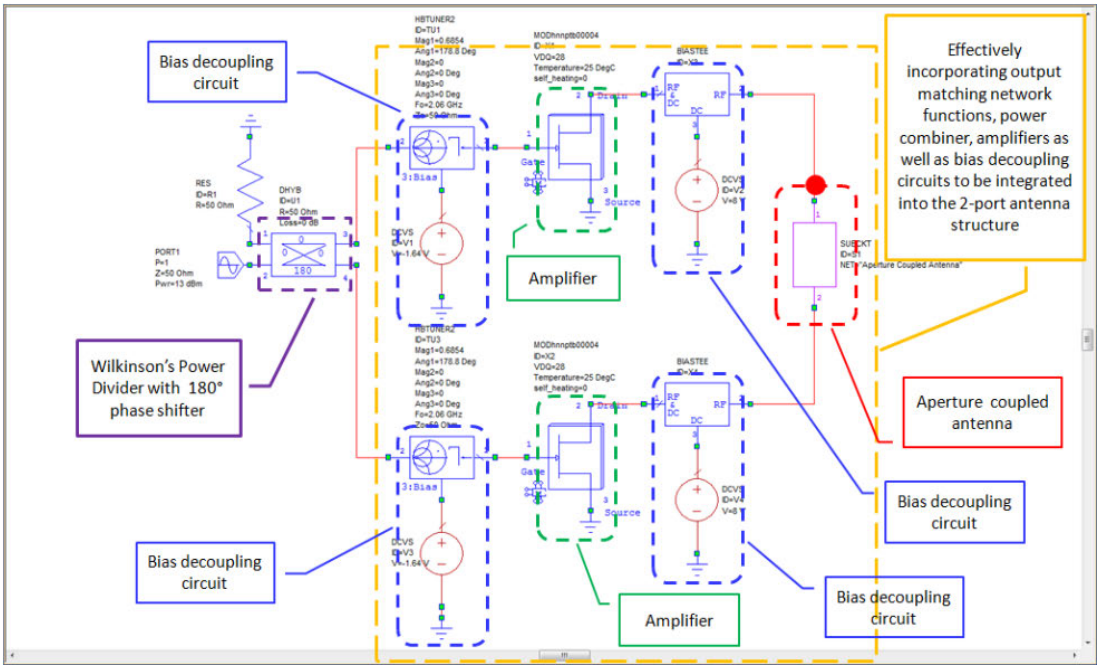


FIGURE 35. Proposed push-pull transmitting amplifier front-end.

IV. FULLY INTEGRATED ANTENNA-AMPLIFIER SIMULATIONS AND MEASUREMENTS

This section presents the direct integration of a push-pull amplifier and an aperture coupled antenna. It starts with the simulation of push-pull transmitting amplifier followed by its transformation into a fully integrated version using realistic lossy components such as optimized biasing decoupling circuits and a power divider with a phase shifter. Comparison between those two versions has been made through simulation.

A. PUSH-PULL TRANSMITTING AMPLIFIER

Previously in Figure 12, an ideal configuration of push-pull transmitting amplifier is shown purposely to express the idea of replacing the output matching networks, 180° hybrid coupler and harmonic traps that reside within the red dashed-line block with a proposed design of Structure A or Structure B. One example design was shown in Figure 23 where Structure B is incorporated within the ideal push-pull amplifier. It is only Structure B which will be discussed further for direct integration with other sub circuit blocks such as transistors, input and output bias decoupling circuits. This is a challenging task to accommodate those mentioned three sub circuit blocks within the limited size of Structure B. Hence, the Wilkinson power divider with 180° phase shifter will be a separate entity. Therefore, this push-pull transmitting amplifier is formed by two main blocks comprising a Wilkinson power divider with phase shifter and another block that effectively incorporates the output matching network functions, power combiner, bias decoupling circuits, antenna and amplifiers. Figure 35 shows the array of sub circuit blocks which is neatly transformed into a push-pull transmitting amplifier front-end.

B. WILKINSON POWER DIVIDER/SPLITTER

The Wilkinson divider is an ideal form of power splitter / divider that is often used in many RF and microwave applications. It uses quarter-wave transformers which are easily fabricated on printed circuit boards and hence, it is a very cheap and simple power divider while still providing high levels of performance. The advantages of Wilkinson power divider include simplicity, reasonably low cost, considerably low loss and a high degree of isolation between the "output" ports.

Although the Wilkinson power divider concept can be used for an N-way system, it is easiest to see how it operates as a 2-way system. The Wilkinson power divider uses quarter-wave transformers to split the input signal in order to provide two output signals that are in-phase with each other. In this work, as the two legs of the splitter / divider are not identical in that they have different electrical length about 180°, the signals appearing at the outputs will have 180° phase difference with the same magnitude. Besides, theoretically the Wilkinson power divider can be considered as lossless since there is no current flow in the resistor which means the resistor does not dissipate any power. However, in practice there are some losses introduced but these are relatively low and can be neglected. Figure 36(a) shows a two way Wilkinson power splitter / divider with 180° phase difference at the outputs while Figure 36(b) shows the simulated results, showing very good return loss at Port 1, equally divided and transmitted power to the outputs at Port 2 and Port 3 as

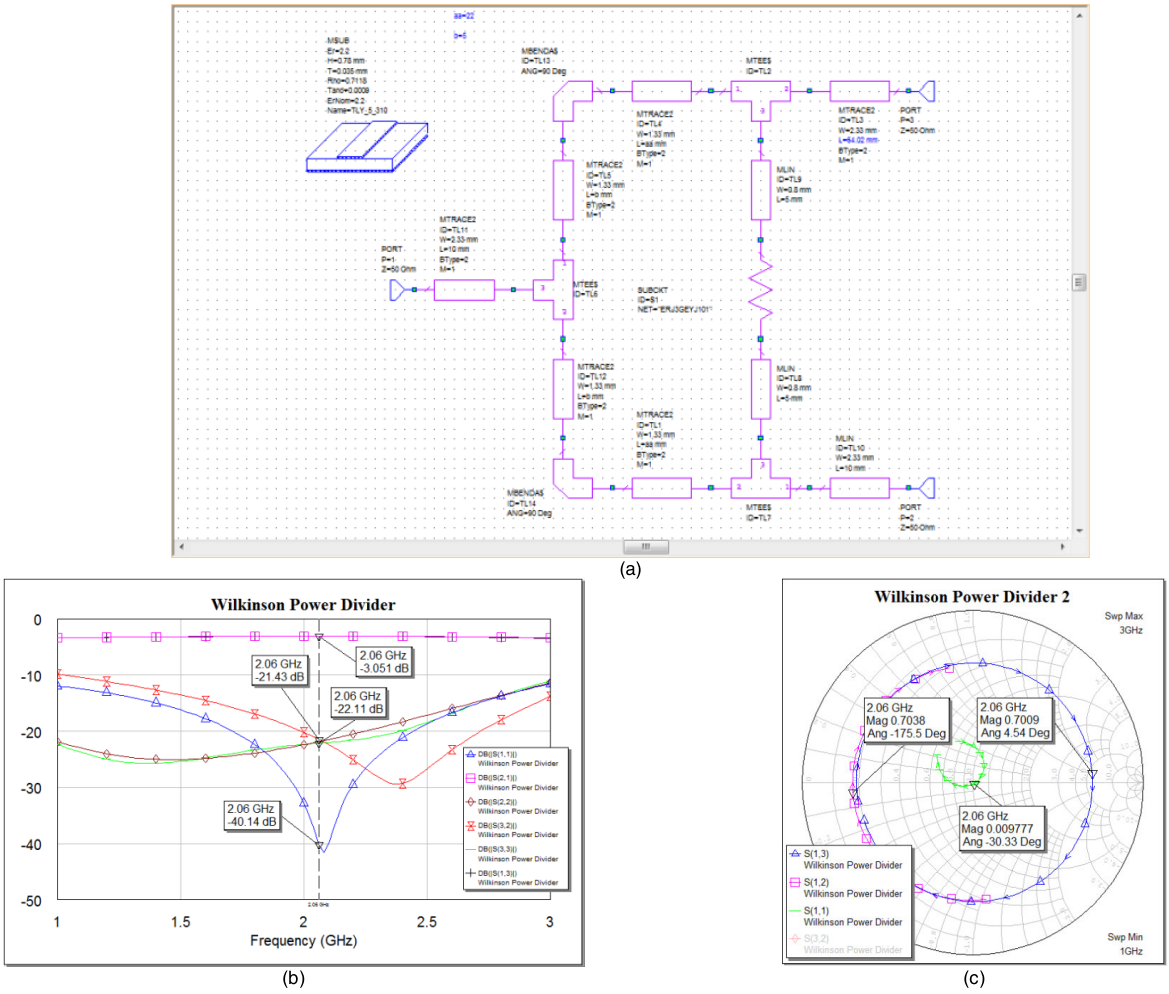


FIGURE 36. **(a) Two way Wilkinson power splitter / divider (b) S-parameter results of Wilkinson power divider (c) Phase difference at the outputs of Wilkinson power divider.**

well as providing considerably good isolation between those two ports. Meanwhile, Figure 36(c) shows the outputs of Wilkinson power divider that have the same magnitude with 180° phase difference.

C. BIAS DECOUPLING CIRCUIT

The design of bias decoupling circuit plays an important role in establishing stable operation and it is a fundamental and absolutely necessary in any RF power amplifiers design since at lower frequencies the impedance presented to the transistor is mainly determined by the bias circuitry. There are several versions which vary from other forms of bias decoupling circuit. Figure 37 shows the complete push-pull transmitting amplifier prototype with standard configuration of input and output bias decoupling circuits where all elements are from real lossy material. As mentioned in the previous chapter, there is a series capacitor on both sides of the transistor to block the DC current from flowing into the source and the load.

Also at the load side, there is an EM Structure represented by a sub circuit block incorporating the output matching network functions, power combiner, antenna and harmonic traps that lies at the load side of the transistor which present an open circuit at design frequency 2.06 GHz, and a short circuit for up to 3rd order harmonics. Therefore, only the fundamental frequency power is transmitted through the patch antenna via aperture.

As seen in Figure 37, there is a large capacitor at the edge end of the biasing line which is mainly to provide a short circuit at that connection point. With a quarter-wavelength ($\lambda/4$ at f_0) of the biasing line, the other end of that biasing line will be seen like an open circuit which will prevent fundamental frequency signal from flowing into the voltage source. Furthermore, an optimum inductor which is connected in series with the DC voltage source is purposely for backing up the imperfection of the capacitor. This precaution step is required and necessary to ensure the point where the connection of the biasing line with capacitor still remains as a perfect short circuit. So, the fundamental signal will see the

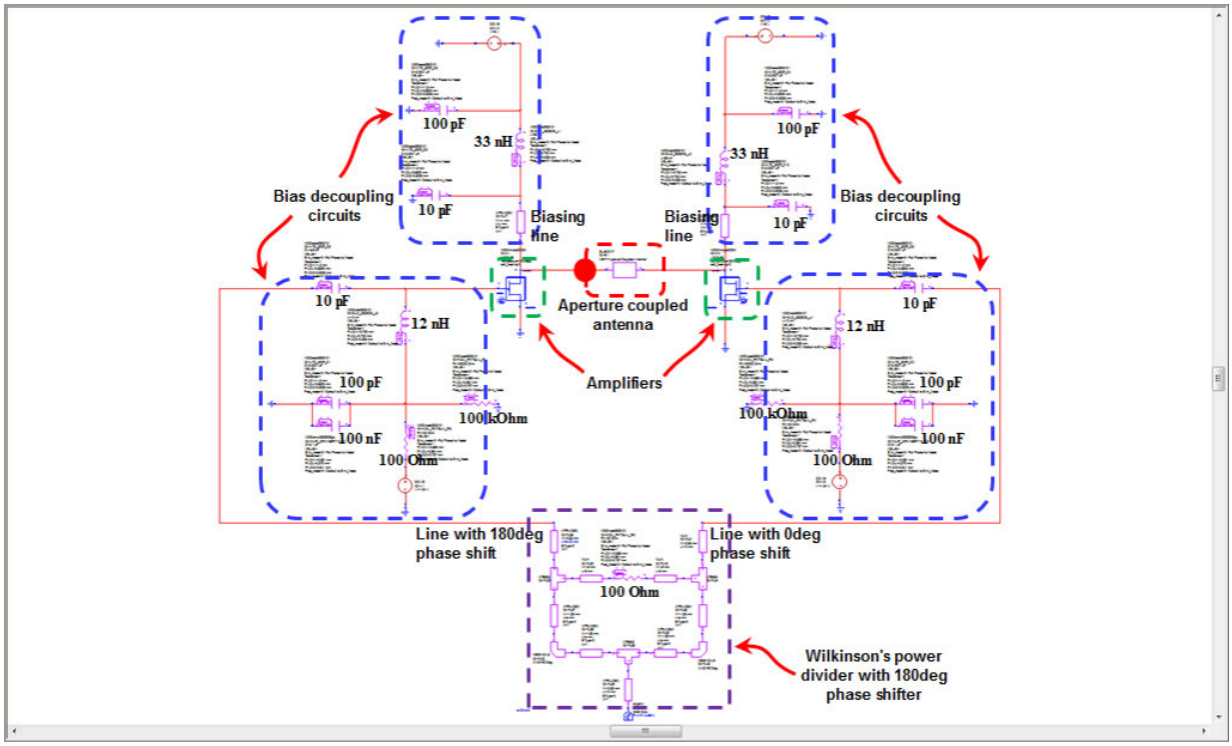


FIGURE 37. New push-pull transmitting amplifier prototype.

impedance at the junction with that biasing line as an open circuit and thus, it can flow through the line length L_2 of the aperture coupled antenna. According to Tian He in [23], there should be inductors at the input side of the transistors which will be working as RF Choke. Besides, both voltage sources are connected to large capacitor in parallel to prevent a sudden change of the voltage supply while the 100 Ω and 100 kΩ resistors to ground for safety precaution steps in case the parallel capacitors do not behave well, avoiding the transistors from burning out.

D. COMPARISON OF PUSH-PULL AMPLIFIER TOPOLOGIES

Before any further characterization of the embedded amplifiers in an aperture coupled antenna, it is necessary to verify the prototype. This confirmation is very important because it is not possible to measure the output power and PAE of the amplifiers directly since they are physically connected to the antenna with no detachable interface. Therefore, a comparison is made between two different push-pull amplifier topologies in terms of waveform at a selected node on the circuitry, by simulation. This could at least ensure the embedded amplifiers will work and behave in Class B mode and are not adversely affected by the proposed EM Structure B during a real in-house test.

The comparison made is based on Figure 35 and Figure 37. All components used in Figure 37 are from real lossy materials including substrate, capacitors, inductors, resistors and

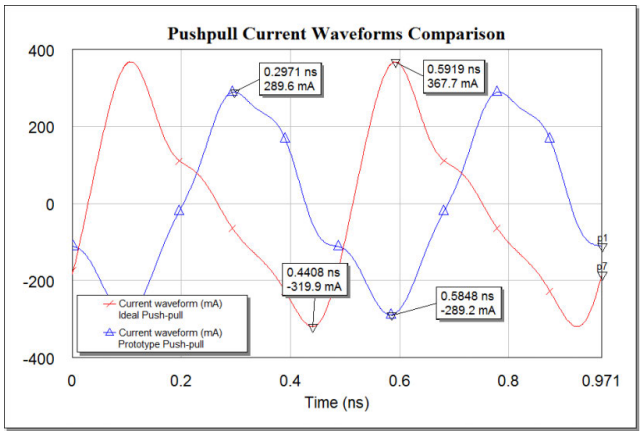


FIGURE 38. Comparison of the current waveforms between ideal push-pull and new prototype.

transistors. In other words, all components that reside within the sub circuit blocks shown in Figure 35 are replaced by the realizable structures. There is one selected node on ideal circuitry as seen in Figure 35 to observe the current waveform flowing into the Structure B. The same nodes applied to the prototype shown in Figure 37 so that the consistency for both ideal push-pull amplifier and the new prototype could be assessed. The simulations have been carried out for both circuits and the results are shown in Figure 38. Comparing those two waveforms, it is obvious that the prototype has retained a similar trend of waveform characteristic to that of

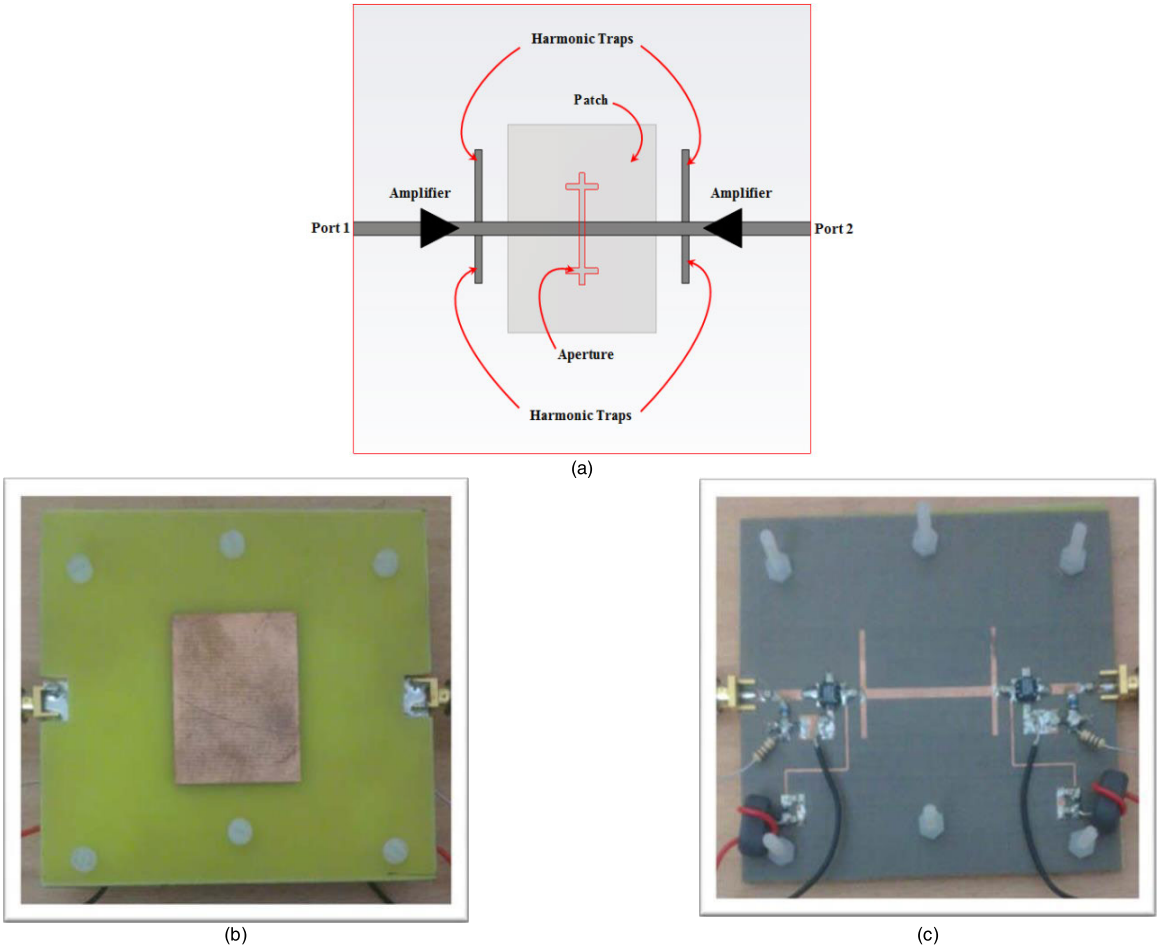


FIGURE 39. (a) Layout of amplifiers embedded on antenna Structure B (b) Fabricated push-pull transmitting amplifier showing top layer (c) Fabricated push-pull transmitting amplifier showing bottom layer.

its ideal form. It is then confirmed that the prototype worked well in Class B mode.

E. FULLY INTEGRATED TRANSMITTING PUSH-PULL AMPLIFIER

Apart from establishing a novel technique for direct integration of power amplifiers and antennas, it is of interest to demonstrate the feasibility of applying it to a fully integrated antenna–amplifier front-end. This also has a potential to realize a fully integrated push-pull amplifier for microwave transmitters.

In this work, a passive version of the antenna is adapted from aperture coupled microstrip antenna. As for the active version of this novel antenna, it is constructed by mounting an opposed pair of Class B amplifiers into the line with the harmonic traps, 50 Ω line length, aperture and radiating patch forming the output load and matching networks as seen in Figure 39(a). Two transistors from Nitronex NPTB00004 are used with Class B operation in a push-pull amplifier configuration. They are placed in such a way that the amplifiers' outputs are facing each other as shown in Figure 39(a).

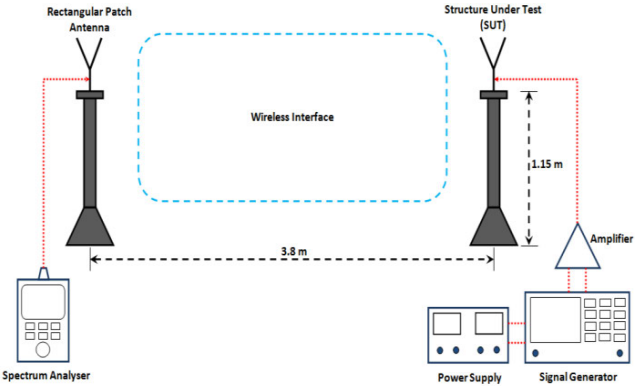


FIGURE 40. Measurement setup for small signal power gain.

Meanwhile, Figure (b) and (c) show a real fabricated prototype of embedded push-pull amplifier based on antenna Structure B shown in Section III. During odd mode excitation, the amplifiers will be in a differential configuration and create maximum current at the center point where two signals meet and interact between the circuits and patch antenna.

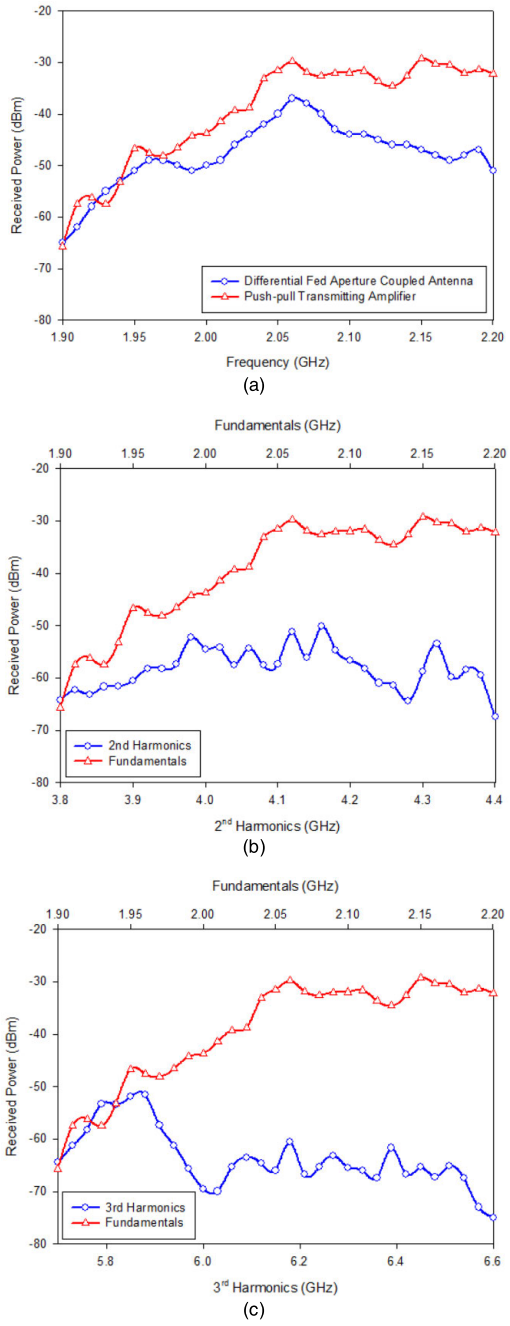


FIGURE 41. (a) Received power from the passive and active integrated antenna (b) Radiated power from the fundamentals and 2nd harmonics (c) Radiated power from the fundamentals and 3rd harmonics.

F. MEASUREMENT

In order to validate this fully integrated push-pull transmitting amplifier, a systematic measurement procedure is required. A block diagram which is illustrating the measurement setup can be seen in Figure 40. Firstly, the structure under test (SUT) should be in transmitting mode. There are two types of SUT involved in this measurement, the passive antenna and an active integrated antenna as known as push-pull transmitting amplifier. Note that the passive antenna structure has no embedded amplifiers and hence, no harmonic traps are required.

In this case, a single rectangular patch antenna which is printed on FR-4 board is used at the receiving side. This receiving antenna has been specifically designed to have resonance at 2.06 GHz. Secondly, the measurement starts with measuring the received power from both SUTs over a range of frequencies. Finally, the difference in received power between both measurements is the power gain of the integrated push-pull amplifier. Generally, the experimental works are divided into two parts which are stated as follows:

i. Measurement of received power between Rectangular Patch Antenna (receiving mode) and Differential Fed Aperture Coupled Antenna (transmitting mode).
ii. Measurement of received power between Rectangular Patch Antenna (receiving mode) and Pushpull Transmitting Amplifier (transmitting mode).

The received power measurement was successfully carried out in an open lab environment using available equipment and facilities. As seen in Figure 40, the transmitting and receiving antenna are separated by a distance which is sufficient to be in the farfield zone. This is to ensure a rectangular patch antenna is illuminated by a plane wave from the transmitting SUTs during measurement. With step frequency 10 MHz which is started from 1.9 GHz to 2.2 GHz, the received power was measured. Figure 41(a) shows a comparison of received power from two different structures which are passive and active respectively. As seen in Figure 41(a), the push-pull transmitting amplifier is capable of providing an additional power gain about 6 *dB* at designed frequency 2.06 GHz.

Since the harmonic terminations are incorporated with Structure B, it is one of our concerns to observe the response of the received power due to 2nd and 3rd harmonics. The same measurement setup and procedure is used to measure the received power and their differences compared to the fundamentals were observed. The measured results have been plotted in separate graphs shown in Figure 41(b) and Figure 41(c) respectively. Those two figures show that the harmonics have been well suppressed.

V. CONCLUSION

During the design of active components for front-end systems operating at microwave frequencies it is of cardinal importance that the consideration of complex values in impedance matching is taken into account. This means that the resistance and reactance components have to be considered when directly integrating power amplifier and antennas together into the front-end system. By doing so will eliminate the need of extra components such as transformers, baluns and hybrid coupler in the two sub-circuit systems thereby avoiding additional losses. After all it could be a viable method for future technologies in microwave and RF field to realize a fully integrated push-pull transmitting amplifier. The usual design of a push-pull power amplifier makes use of hybrid coupler and baluns at the input and output stage functioning as power splitter as well as combiner. In this work though, by apply the odd-mode concept, the antenna structure for a two-port feed was designed. Then impedance matching between the two has

to be perform in order to efficiently integrate the push-pull amplifier and the two-port antenna. Based on the impedance matching requirement as well as biasing condition imposed by the push-pull amplifier, a novel design of differentially fed aperture coupled antenna was achieved. This new structure was realized through fabrication and experimented upon in order to prove the theory.

Overall this concept has alleviated the use of lossy components and output baluns by making use of output matching impedances and power combiner within the two-port antenna structure. Furthermore, the efficiency of the entire system concerning wireless communication is ameliorated since there is a reduction in total loss for direct integration of amplifiers and antennas. Lastly, this system could be fitted on a MMIC while not using bond wires for electrical connection.

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