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Low-Voltage Capacitive-Based Step-Up DC-DC Converters for RF Energy Harvesting System: A Review

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ABSTRACT Bulky off-chip inductors are predominantly adopted for inductive-based step-up DC-DC converter in RF energy harvesting (RFEH) systems, which impose a restriction in physical form factor for miniaturized device. This article review and explores the capacitive-based step-up DC-DC converters (charge-pump) as voltage boosting element for low-voltage RFEH systems. An overview of RFEH is established and a comprehensive review of CMOS charge-pump is followed along with the complementary frequency generation circuit used as a clocking element. Key design considerations of charge-pump circuits are included here along with recommendations to circumvent its bottlenecks for future development in RFEH systems.

INDEX TERMS RF energy harvesting (RFEH), charge-pump, capacitive-based converters, dc-dc converter, CMOS.

I. INTRODUCTION

In the recent decade, the demand for miniaturized ultra-low-power (ULP) wireless sensor nodes (WSNs) [1], [2], medical implants [3], and wearable devices [4] for the Internet of Things (IoT) [5] are gaining momentum in academic and industrial research. Power consumption of ULP analog-front-end (AFE) and transceivers are ever decreasing, prompting the use of energy harvesting (EH) as an alternative solution to batteries where their replacement is a constraint and impractical for implantable devices. Research works are keen on harvesting ambient energy from solar [6], [7], thermal [8], vibration [9], or electromagnetic/RF [10] to power up ULP devices.

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Solar or piezoelectric (PZ) energy has significant power density compared to thermal and RF energy [9], however, limitations due to weather dependency and irregularity of the energy source is unattractive for applications that require a constant power source; i.e: biomedical sensor nodes (BSNs) [1], [3], [4]. Alternatively, is it a challenge to design an effective and efficient start-up circuit for thermoelectric generators (TEG) harvesting in complementary-metal-oxide-semiconductor (CMOS) due to the low-voltage generated [3], [8]. On the other hand, RF energy harvesting (RFEH) is an attractive solution for powering ULP circuits despite its low power density. High reliability of the energy source (in far-field RFEH) and small physical form factor of the transducer (antenna) are key advantages of adopting RFEH.

The block diagram of an RFEH system is shown in Fig.1(a). Till date, prior-art CMOS RFEH systems have predominantly been adopted inductive-based step-up DC-DC

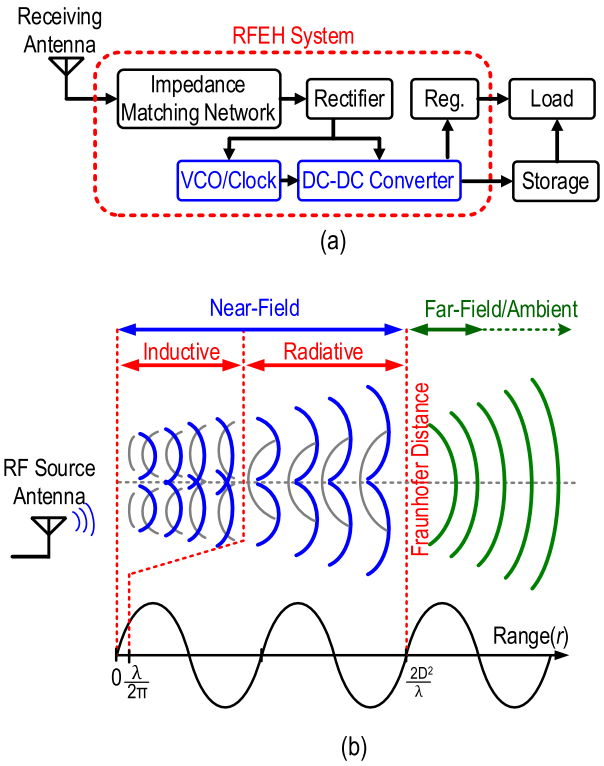

FIGURE 1. RF energy harvesting. (a) Block diagram (b) Propagation of energy through space.

converters [10]. This is due to the effectiveness in design for low start-up and promotes high power conversion efficiency (PCE) compared to the capacitive-based counterpart (charge-pump). Recently, it has been demonstrated that capacitive-based step-up DC-DC converters are becoming competitive in effective start-up and improved PCE performance for EH applications [5], [6]. However, there are only limited development of capacitive-based CMOS step-up DC-DC converters implemented in RFEH systems [11]–[15]. This prompts the need to investigate and explore design considerations, limitations, and future development goals of capacitive-based CMOS step-up DC-DC converters for RFEH systems to achieve reduction in the physical form factor of the overall miniaturized IoT device.

Therefore, this article investigates the constraints of implementing a capacitive-based step-up DC-DC converter for RFEH systems. First, an overview of RFEH system is presented in section II. Section III covers a comprehensive review of charge-pump circuits and the corresponding frequency generation circuit as a clock element. A discussion on the findings are made in section IV to review design considerations, limitations, and future development goals of implementing capacitive-based CMOS step-up DC-DC converters for RFEH systems. Section V concludes the paper.

II. RF ENERGY HARVESTING (RFEH)

RFEH systems can be classified into two types: Near-field and Far-field RFEH. The depiction in operation of each RFEH type is shown in Fig. 1(b). Its classification is typically determined based on power density, frequency, and range of transmission of the RF energy being harvested. Near-field RFEH operates through magnetic coupling where the transmitter and receiver are placed in proximity within the Fraunhofer distance ($2D^2/\lambda$) where D is the diameter of the antenna and λ is the wavelength of the RF signal. Also, the power density of near-field RFEH is significantly larger compared to far-field RFEH. Furthermore, near-field RFEH can be subclassified into the reactive/inductive region and radiative/Fresnel region according to the transmission range or the RF wavelength. Electromagnetic (EM) radiation consists of electrical (E) and magnetic (H) fields which characterize the freely propagated wave. The relation between E and H in near-field RFEH is highly complex in predicting the power density where either E or H may dominate at a given time.

When the transmission range of the propagated RF energy is beyond the Fraunhofer's distance, the system is classified as dedicated far-field or ambient RFEH. The E and H fields in far-field RFEH have equal magnitude at different points in space. Hence, the received power of the antenna is predictable through Friis transmission equation[16] expressed as,

$$P_{RX} = \frac{P_{TX} G_{TX} G_{RX} \lambda^2}{(4\pi R)^2} \tag{1}$$

P_{TX} is the transmitted power, G_{TX} is the gain of the transmitting antenna, P_{RX} is the received power, G_{RX} is the gain of the receiving antenna and R is the distance between transmitting and receiving antenna. Alternatively, the peak input voltage amplitude, V_{Ant} received at the antenna can be calculated by [17],

$$V_{Ant} = \sqrt{8 \times R_{Ant} \times P_{RX}} \tag{2}$$

where R_{Ant} is the radiation resistance of the antenna. The efficiency of the RFEH system can be calculated based on the efficiency of each block in the system by,

$$\eta_{System} = \eta_{IMN} \cdot \eta_{Rectifier} \cdot \eta_{PMU} \tag{3}$$

in which η_{IMN}, $\eta_{Rectifier}$ and η_{PMU} corresponds to the efficiency of the impedance matching network (IMN), rectifier, and power management unit (PMU), respectively.

A. RECTIFIER

The rectifier block is considered as the core circuit in an RFEH system. It converts the input RF power in alternating current (AC) to usable direct current(DC) for powering up ULP circuits [18]–[20]. Previously, rectifiers in RF identification (RFID) are constructed using Schottky diodes due to its low turn-on voltage characteristic [21]. The exponential growth of integrated circuit (IC) has delivered the MOSFET, particularly CMOS technology in which diode-connected transistors have replaced the Schottky diode. The equivalent diode configuration of MOSFET is shown in Fig. 2(a). However, the threshold voltage (V_{th}) of diode-connected transistors are higher than the Schottky diodes. To overcome this issue, static-V_{th} compensation schemes have been introduced to reduce the forward loss as well as to reduce its

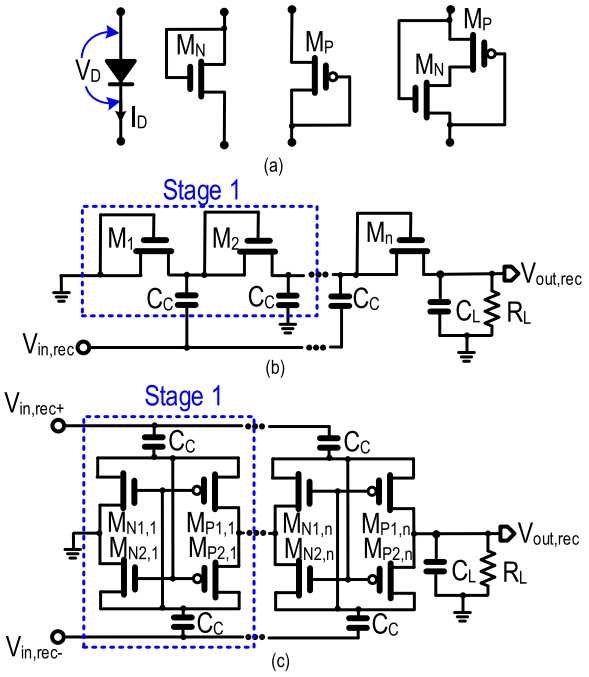

FIGURE 2. (a) Equivalent diode configuration of MOSFET RF rectifier topology (b) Dickson (c) Cross-Coupled Differential-Drive (CCDR).

on-resistance to attain better forward-biasing. The penalty of the trade-off is in the increase of the reverse leakage current due to higher gate bias voltage in reverse bias mode. To overcome this effect, the active compensation technique is introduced [22]. This technique reduces the V_{th} during forward-bias mode and increases the V_{th} during reverse bias mode.

Conventional rectifier topologies in CMOS are the Dickson and Cross-Coupled Differential Drive (CCDR) shown in Fig. 2(b) and Fig. 2(c), respectively. The CMOS rectifiers were initially adopted in ultra-high frequency (UHF) RFID application with the circuit structure and performance features being the same for RFEH application. The operation of CCDR is described in two operation cycles, which are the positive and negative RF input cycles. During the positive cycle, $M_{\text{P1,1}}$ and $M_{\text{N2,1}}$ of Fig. 2(c) are operated in a linear mode as switches and $M_{\text{P2,1}}$ and $M_{\text{N1,1}}$ are in cut-off mode. The current flows to the next stage through M_{P1} and flows back to the negative terminal of the input source through M_{N2}. A similar operation occurs during the negative cycle where M_{P2} and M_{N1} operates in linear mode and M_{P1} and M_{N2}, in cut-off mode. This operation is the same for all succeeding stages in a multi-stage rectifier.

The peak amplitude of the rectifier's input voltage, $V_{\text{in,rec}}$ can be quantified with the expression given by [23],

$$V_{\text{in,rec}} = \frac{V_{\text{Ant}}}{2}\sqrt{1+Q^2} \tag{4}$$

where Q is the quality factor of the inductor in the IMN. The expression to compute the rectifier's input power, $P_{\text{in,rec}}$ excluding the IMN interface is given by,

$$P_{\text{in,rec}} = P_S\left(1 - |S_{11\text{rec}}|^2\right) \tag{5}$$

where $S_{11\text{rec}}$ denotes the input reflection coefficient of the rectifier and P_S represents the input power source. An accurate formulation for the CCDR to determine the input power is given as:

$$P_{\text{in,rec}} = P_S(1 - |S_{\text{dd11,rec}}|^2 - |S_{\text{cd11,rec}}|^2) \tag{6}$$

where $S_{\text{dd11,rec,}}$ and $S_{\text{cd11,rec}}$ is the rectifier reflection coefficient of differential-to-differential mode and differential-to-common mode respectively.

The power conversion efficiency (PCE) primarily depends on the input RF frequency, V_{Ant}, $V_{\text{in,rec}}$, and the output load resistor (R_{L}), with the general formula,

$$\text{PCE} = \frac{P_{\text{out,rec}}}{P_{\text{in,rec}}} = \frac{V_{\text{out,rec}}^2/R_{\text{L}}}{P_{\text{in,rec}}} \tag{7}$$

$P_{\text{out,rec}}$ is the output power delivered to the load, calculated by the rectified output voltage, $V_{\text{out,rec}}$ divided by R_{L}.

In summary, Schottky diodes were primarily integrated as rectifier on an IC for RFID to overcome the limitation of forward voltage drop and reverse leakage current. However, a complete CMOS implementation is still preferred due to cost, form factor, and technology integration compatibility. CMOS implementation of the rectifier has focused solely towards reducing the forward voltage drop and reducing the reverse-leakage current. These are the primarily consideration needs to taken into account when designing the rectifier for ambient RFEH.

B. IMPEDANCE MATCHING NETWORK (IMN)

The IMN is an interface between the antenna and the rectifier as shown in the equivalent circuit model in Fig.4. R_{L} and C_{L} are the load resistor and capacitor, respectively. Alternatively, $R_{\text{in,rec,}}$ and $C_{\text{in,rec}}$ are the rectifier's equivalent resistor and capacitor, respectively. L_{M1}, $L_{\text{M2,}}$ and C_{M1} forms the IMN where L_{P1}, L_{P2}, R_{P1}, R_{P2}, C_{P1}, and C_{P2} represent the parasitic components [24]–[26]. Parasitics exist from various sources such as substrate capacitance, bond wires, and printed circuit board (PCB). The IMN entails a combination of capacitive and inductive elements which acts as a bridge between the receiver antenna to the rectifier for maximum power transfer by reducing impedance mismatch at the desired frequency. Besides achieving maximum power transfer, various work on ambient RFEH has looked upon IMN as a voltage boosting element to increase the sensitivity of the RFEH system [27]. Fig.3 summaries various IMN configurations that are suitable for RFEH systems [26], [28]–[35].

The performance of the IMN is quantified through the input reflection coefficient, S_{11} given by,

$$\text{S}_{11}\ (\text{dB}) = \Gamma = \frac{Z_{\text{in,rec}} - Z_{\text{Ant}}^*}{Z_{\text{in,rec}} + Z_{\text{Ant}}^*} \tag{8}$$

$Z_{\text{in,rec}} = R_{\text{in,rec}} + X_{\text{in,rec}}$ is the impedance of the rectifier and Z_{Ant}^* is the complex conjugate of Z_{Ant} and $Z_{\text{Ant}} = R_{\text{Ant}} + X_{\text{Ant}}$ is the impedance of the antenna (typically 50-Ω). Equation (9)

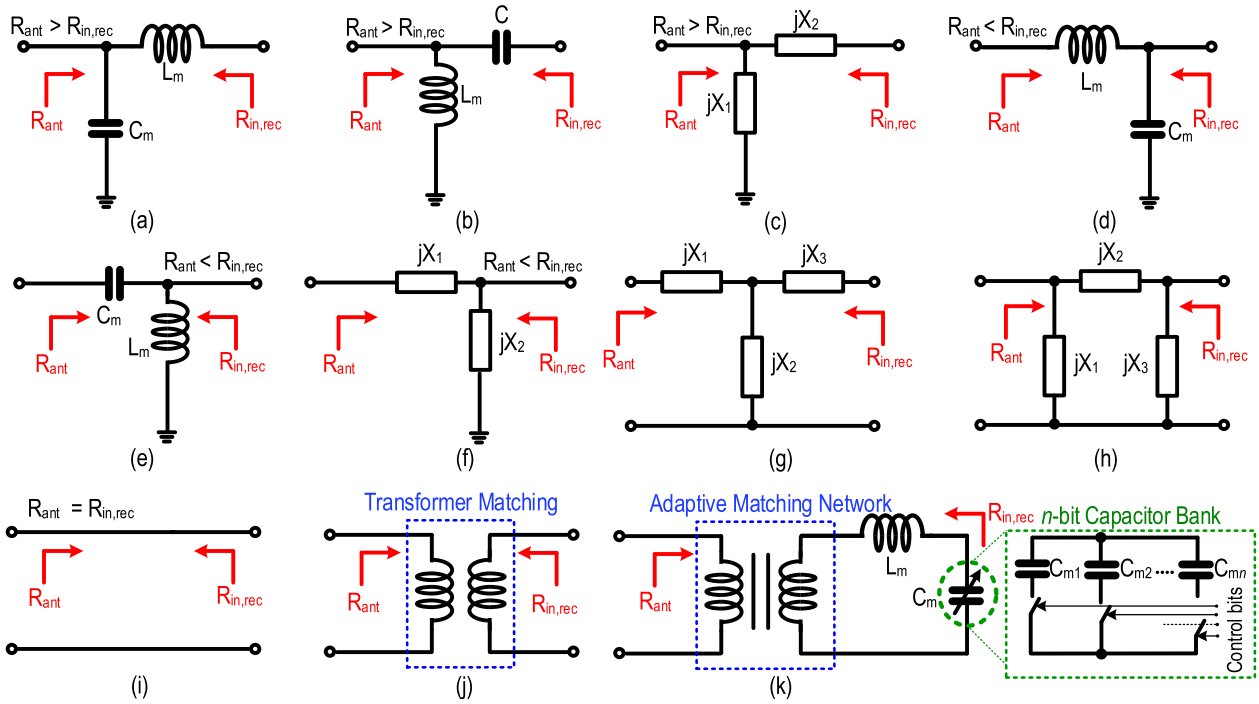

FIGURE 3. Various types of impedance matching networks. (a)-(f) LC networks [27]. (g) T-network. (h) π-network (i) Co-design [28]–[31] (j) Transformer Matching [32]–[34] (k) Reconfigurable Matching [25].

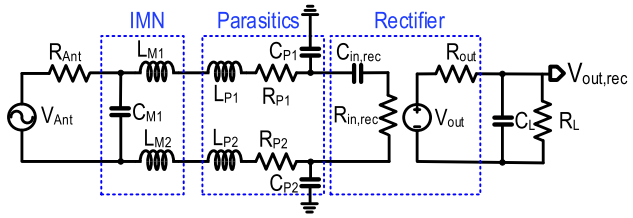

FIGURE 4. Equivalent circuit of RFEH front-end.

refers to the amount of power reflected which is the square of the reflection coefficient in (8).

$$|\Gamma|^2 = \left|\frac{Z_{\text{in,rec}} - Z^*_{\text{Ant}}}{Z_{\text{in,rec}} + Z^*_{\text{Ant}}}\right|^2 \tag{9}$$

To attain a maximum power transfer and minimize losses, the real term of the antenna and rectifier has to be equal. Also, the imaginary term has to be cancelled out through the conjugate term respective to each other.

As demonstrated in [27], the IMN can also act as a passive voltage booster where the V_{Ant} from the antenna is boosted. This technique could improve the operation of the rectifier by boosting the input voltage signal beyond the V_{th} of the transistors. The voltage gain, A_{v} is directly proportional to the quality factor of inductor [21], [36] evaluated by,

$$A_{\text{V}} = \frac{1}{2}\sqrt{1 + Q_{\text{L}}^2} \tag{10}$$

As can be described in (10), the level of voltage boosting is highly dependent on the inductor's quality(Q)-factor. Generally, off-chip inductors have larger Q-factor compared to on-chip inductors. As an example, with an off-chip inductor with a Q-factor that is four times higher compared to an on-chip inductor, the voltage gain is increased by a factor of two in comparison to its on-chip counterpart [37]. Hence, the Q-factor of the IMN inductor plays a significant role in enhancing the sensitivity performance of the RFEH system by boosting V_{Ant} to drive the transistors of the rectifier in improving the operation. The Q-factor [21] of an inductor is given by,

$$Q_{\text{L}} = \frac{X_{\text{L}}}{R_{\text{Ls}}} = \frac{\omega_{\text{o}} L}{R_{\text{Ls}}} \tag{11}$$

where ω_0 is the resonance frequency in radians per second, L is the inductance, X_{L} is the inductive reactance, and R_{Ls} is the series resistance of the inductor. Alternatively, the Q-factor of the capacitor is given by,

$$Q_{\text{C}} = -\frac{X_{\text{C}}}{R_{\text{C}}} = \frac{1}{\omega_{\text{o}} C R_{\text{C}}} \tag{12}$$

Xc is the capacitive reactance, R_{C} is the series resistance of capacitor and C is the lumped capacitance. Together, the Q-factor of the RLC circuit is given by,

$$Q = 2\pi \times \frac{\text{Maximum Energy Stored}}{\text{Energy dissipated per cycle}} \tag{13}$$

where R_{L} and X_{L} of the IMN represent the input of the rectifier. It is worth noting that the rectifier is a non-linear circuit, where the input impedance changes respective to the level of $V_{\text{in,rec}}$. A diligent design methodology is essential when designing the IMN to ensure maximum power transfer and effective voltage boosting across a wide range of RF input power. The Q factor of an on-chip inductor is dependant on parasitics which is proportional to the technology

TABLE 1. *Q*-factor of inductor type/model.

Ref.	Q-factor	Inductor Model/Type
[10]	120	Co-design antenna
[27]	80	Off-chip (MURATA-LQW18AN)
[28]	10	On-chip
[28]	50	Off-chip
[38]	12	On-chip
[41]	130	Co-design antenna

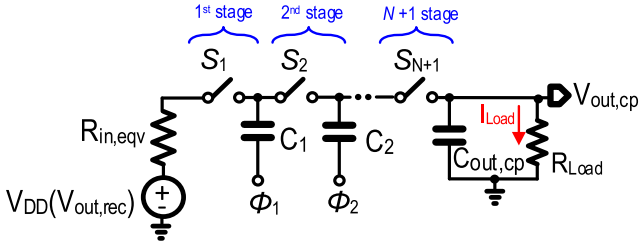

FIGURE 5. A simple scheme of a charge pump.

node [38]. Nevertheless, there are various techniques reported in improving the *Q*-factor through the physical design innovation of on-chip inductors [37], [39], [40] and high-*Q* co-design antenna [10], [41] to attain superior performance in sensitivity. Table I summarizes the *Q*-factor of various inductors.

III. CAPACITIVE-BASED STEP-UP DC-DC CONVERTER

A. CHARGE-PUMP

A charge-pump circuit boosts a low DC voltage to a higher DC voltage to a load. The charge-pump is an alternative to the inductive-based step-up DC-DC converter [42] which typically requires a bulky off-chip inductor [27], [43]. In the current era of IC design, switch-capacitor (SC) or charge-pump circuits has gained interest in miniaturized devices to achieve a reduction in physical form factor and to promote system-on-chip(SoC) solution [44].

Fig.5. shows a simplified schematic of a charge-pump circuit. It is comprised of switches, $S_{\rm i}$ (where $i = 1, 2..N$, $N + 1$), pumping capacitors $C_{\rm pump}$(pump $= 1, 2, N$), a load capacitor ($C_{\rm out,cp}$), and a load resistor ($R_{\rm Load}$). $R_{\rm Load}$ represents the circuit element to be powered by the charge-pump. In a capacitive-based step-up DC-DC converter, charge is transferred from a supply voltage ($V_{\rm DD}$) or the output DC voltage of a rectifier ($V_{\rm out,rec}$) to $R_{\rm Load}$ through $C_{\rm pump}$ which are activated by $S_{\rm i}$ using two alternating clock signals, Φ_1, and Φ_2. The clock signals alternate sequentially to activate the switches to avoid short circuit losses or latch-up [45].

The operations of an N-stage charge-pump are described as follow. During the first half cycle, Φ_1 is low and Φ_2 is high. Odd-numbered $S_{\rm i}$ are activated to allow charges from the prior stage to be transferred to the next immediate $C_{\rm pump}$ stage. Alternatively, during the next half-cycle where Φ_1 is high and Φ_2 is low, the odd-numbered switches are open and even-numbered switches are activated. The charge stored in the odd-numbered pumping capacitors are transferred to the next immediate $C_{\rm pump}$. The output voltage of the charge pump, $V_{\rm out,cp}$ rises steadily as the cycles repeats and reaches a steady-state value. The steady-state value of $V_{\rm out,cp}$ can be mathematically expressed as,

$$V_{\rm out,cp} = V_{\rm clk}.N_{\rm cp} + V_{\rm DD} - N_{\rm cp}\frac{I_{\rm Load}T}{C_{\rm pump}} \tag{14}$$

$N_{\rm cp}$ is the number of charge-pump stages, T is the period of the clock, and $I_{\rm Load}$ is the output current. Alternative, the output voltage at no-load condition can be written as,

$$V_{\rm out,cp(n.l.)} = V_{\rm clk}.N_{\rm cp} + V_{\rm DD} \tag{15}$$

The total current consumption of the charge-pump is the sum of the ideal current and parasitic current which is expressed in (16).

$$I_{\rm in} = \left[(N+1)+\alpha\frac{N^2}{\left(N_{\rm cp}.V_{\rm clk} + V_{\rm DD} - V_{\rm out,cp}\right)}.V_{\rm DD}\right]\cdot I_{\rm Load} \tag{16}$$

$I_{\rm in}$ is the input current into the charge-pump and α is a factor of the pumping capacitor at the bottom plate parasitic capacitance.

The power loss in a charge-pump and its peripheral circuit has to be kept minimal to attain high PCE and voltage conversion efficiency (VCE) performances which are expressed by (17) and (18), respectively.

$$\text{Power Conversion Efficiency} = \frac{P_{\rm out,cp}}{\rm P_{in,cp} + P_{peri}} \tag{17}$$

$$\text{Voltage Conversion Efficiency} = \frac{V_{\rm out,cp(actual)}}{V_{\rm out,cp(ideal)}} \tag{18}$$

$P_{\rm out,cp}$ is the output power, $P_{\rm in,cp}$ is the input power, and $P_{\rm peri}$ is the power consumed by the peripheral circuit(s) like voltage-controlled oscillator(VCO), buffer, Non-overlap clock generator(NOC), and level shifter circuit(s) of the charge-pump. Alternatively, $V_{\rm out,cp(ideal)}$ is the ideal output voltage whereas $V_{\rm out,cp(actual)}$ is the actual output voltage of the charge-pump. The power losses in a charge-pump are contributed by the following factors:

1) REDISTRIBUTION LOSS

A non-negligible loss in between $C_{\rm out,cp,}$ and the $N_{\rm th}$ stage of the charge-pump which causes the last node voltage swing to be higher than $V_{\rm out,cp}$ [46]. Therefore, the output voltage for no-load condition is usually lesser than (15).

2) CONDUCTION LOSS

Conduction loss occurs in the channels when the transistor is turned-on with an *on*-resistance ($R_{\rm on}$) expressed through [47]–[49],

$$R_{\rm on} = \frac{1}{\mu C_{\rm ox}\frac{W}{L}(V_{\rm gs} - V_{\rm th})} \tag{19}$$

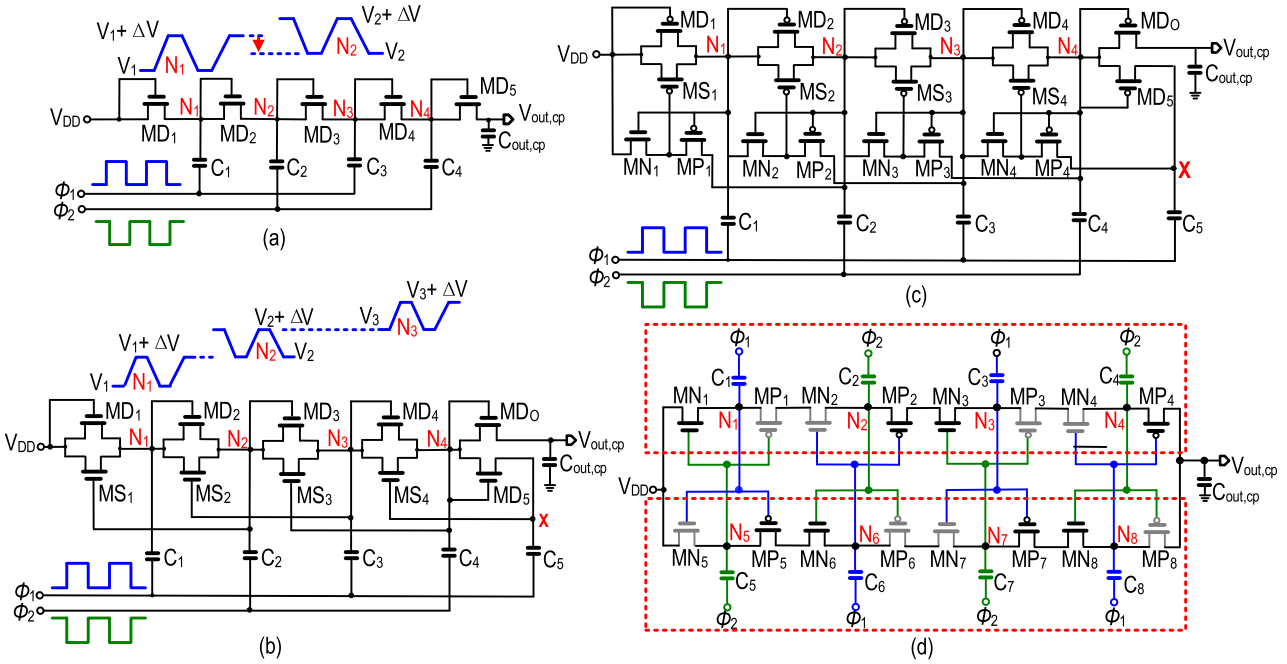

FIGURE 6. Charge-pump topologies. (a) Conventional [54]. (b) Charge transfer switch: *Type*-I [56]. (c) Charge transfer switch: *Type*-II [56]. (d) Two-branch latch charge-pump [57].

where μ is the mobility of the electron/holes and C_{ox} is the oxide capacitance which is a technology dependent parameters. Conduction loss can be reduced by increasing the gate-to-source voltage (V_{gs}) and width (W) of the transistor. However, increasing the width of the transistor leads to an increase in absolute V_{th}. Thus, adopting mature CMOS technology (>100 nm) might not be well suited for low-voltage operation due to higher V_{th} [50].

3) REVERSE CHARGE SHARING AND LEAKAGE

As an antithetical to the aforementioned losses, reverse charge leakage are significant in advanced CMOS technology which is attributed to shorter device length. The reverse sharing phenomenon causes current to flow from the $N_{th,cp}$ node to $(N\text{-}1)_{th,cp}$ by indecorous switching effects through V_{th} variation, lack of gate-to-source voltage (V_{gs}) drive, and short circuit dissipation [51]–[53].

4) SHORT CIRCUIT LOSS

When $V_{DD} > V_{tn} + |V_{tp}|$, the NMOS and PMOS are shorted for a brief period. This leads to short circuit loss, shoot-through current loss, or shoot through loss [53]. These phenomena can be avoided with non-overlap clock signal and various body-biasing techniques for the charge-pump.

5) SWITCHING LOSSES OR DYNAMIC LOSSES

Switching loss of a transistor is proportional to the switching frequency, parasitic capacitance, and transistor size [47]. Also, switching loss is inversely proportionally to the conduction loss.

$$\text{Conduction loss } \alpha \ \frac{1}{\text{Switching loss}} \tag{20}$$

Proper transistor sizing and aspect ratio of the PMOS: NMOS transistors (2:1 or 2.5:1) is maintained for a compromised trade-off in the switching loss and conduction loss.

B. REVIEW OF CHARGE-PUMP

The first monolithic integrated charge-pump using MOS diodes with the pumping capacitor was introduced in [54] with the schematic shown in Fig.6(a). The Dickson charge-pump was invented for high voltage applications whereas today's state-of-the-art charge-pumps cater for low-voltage EH applications. The Dickson charge-pump operates in two modes; saturation and cut-off. Efficient voltage multiplication relies on the size of the pumping capacitors with its value greater than the stray capacitor of the charge-pump expressed in (21-23).

$$\Delta V = V_{\emptyset} \cdot \frac{C_{\text{pump}}}{C_{\text{pump}} + C_s} - \frac{I_{\text{Load}}}{f\left(C_{\text{pump}} + C_s\right)} \tag{21}$$

$$2\Delta V > V_{\text{tn}}\,(V_2) \tag{22}$$

$$2\Delta V < V_{\text{tn}}\,(V_1) \tag{23}$$

C_s is the node parasitic capacitance or stray capacitance of the node, f is the frequency of clock signals, V_{Φ} represents the supply voltage (V_{DD} or $V_{out,rec}$), and ΔV is the change in voltage at each node. The peak output voltage is limited by N_{cp} as the output impedance increases to limit the allowable $V_{out,cp}$. Body effect in charge-pumps can be eliminated through floating well technique to increase the maximum allowable $V_{out,cp}$ [55], but this creates an increase in substrate current and reduces the pumping efficiency due to V_{th}.

As an example, to ensure the MOSFET switch MS_2 in Fig.6(a) is fully turned off, the V_{gs} ($2\Delta V$) has to be less than

the change in V_{th} denoted in (23). However, this condition is not attained in a *Type*-I charge transfer switch (CTS1) shown in Fig.6(b), indicating MS_2 will not be completely switched off [56]. Due to this, reverse charge flowing from node 3 (V_3) to node 1 (V_1) is inevitable. Therefore, the pumping efficiency of the charge-pump is retained by attaining ΔV according to (21) until it satisfies (22).

The *Type*-2 charge transfer switch (CTS2) in Fig. 6(c) is introduced to eliminate the reverse charge phenomenon by adding two pass transistors and creating a dynamically controlled charge-pump circuit [56]. This allows for MS_2 to be completely turned off/on by the pass transistor through a backward control technique. However, both CTS types can suffer from high voltage stress on its gate oxide due to maximum change in voltage of each stage; usually $\sim 2V_{DD}$ which can cause reliability issues. Besides, a dynamic controlling switch is limited at the last stage of the charge-pump. Hence, diode-connected configuration is typically adopted for the last stage in a CTS-*type* charge-pump. Transistor MD_O shown in Fig.6(b) is added to push charges to the output. MD_5 is connected to C_5 as well to provide a control signal to MS_4.

Voltage fluctuation at node X (ΔV_x) can be large due to the absence of output load (open-circuit). This limits the minimum input voltage as well as the maximum output voltage. Body effect also occurs in the diode-connected MOSFET at the last stage of a CTS charge-pump. To overcome this effect, cross-coupled bootstrap technique is applied to boost the input clock amplitude of the last stage [56]. However, a $\sim 3\times$ increase in parasitics capacitance at nodes 1 to 4 of the charge-pump is evident. Hence, C_s is non-negligible and can reduce the pumping efficiency of the charge-pump according to (21). Therefore, larger pumping capacitor is needed to suppress the effect of C_s to attain higher efficiency performance.

Two branch latch charge-pump shown in Fig.6(d) gives a complete solution for reliability issue occurs due to gate oxide stress by ensuring the non-overlap clock, drain-to-source voltage (V_{ds}) and V_{gs}, does not exceed V_{DD} [57]. This was demonstrated through two power-efficient charge-pumps in 3 stage and 5 stage configuration in a triple-well CMOS technology [50], [58], [59]. Optimal frequency is maintained to attain peak current and pumping efficiency. By integrating larger capacitors, higher efficiency can be attained with a trade-off in chip area through large on-chip capacitors which can incur additional cost. Hence, adopting large capacitors is not an optimal solution. Increasing the oscillating frequency can be adopted to reduce the size of capacitors while retaining PCE performance [60].

Clock boosting techniques can be explored to overcome the limitations of prior-art charge-pump circuits. There are 4 clock schemes for a clock boosting technique for charge-pump which delivers better PCE at low output current (65% at 40 μA). However, PCE is impinged at high output current ($\sim$20% at 200 μA)[60]. Boosted charge transistors have to withstand the voltage drop twice the value of V_{DD}. Therefore, high voltage transistors are used to prevent breakdown. Higher V_{th} and increase parasitics are evident in high voltage transistors which leads to deteriorating switching efficiency. Also, the voltage doubler cannot be cascaded due to their breakdown limit. To overcome this limitation, a triple-well process is used where the bulk of the NMOS can be shorted to any terminal point in the circuit so that the voltage drop across the transistors never exceeds V_{DD}.

In [61], an NMOS based CTS is replaced by PMOS with lower charge mobility, improving the efficiency of prior-art CTS by reducing reverse charge sharing phenomena. The size of a PMOS has less impact on the absolute V_{th} than the NMOS counterpart [62] where wider devices are able to reduce conduction loss. Therefore, there is no need of a diode-connected MOS as the last transistor in a charge-pump circuit [61] where the gate control of the last PMOS stage is connected with the gate of the prior stage for effective switching.

However, in a linear charge-pump (LCP), effective switching efficiency is limited when the input voltage is lesser than the V_{th}. The Meindl limits [63] sets the permissible supply voltage according to,

$$V_{DD,min} = 2\ln 2\left(\frac{kT}{q}\right) \tag{24}$$

where k is Boltzmann's constant, T is the absolute temperature and q is the electron charge. This is less than the V_{th} of the transistor. Hence $V_{DD,min}$is depended on the subthreshold swing (S_s) of CMOS technology described by [63],

$$V_{DD,min} = 52\ \text{mV}.\ln\left(1 + \frac{S_s}{60\text{mV}}\right) \tag{25}$$

at a temperature of 300K. In standard CMOS technology, the range of subthreshold slope is between 70 to 100 mV/decade. State-of-art charge-pumps are able to operate as low as 120 mV to 150 mV [64]–[66]. However, these charge-pumps are not operating in vicinity to Meindl limits due to parasitics effect which causes conduction losses and dead time during switching [67]. Therefore, advanced CMOS technology can be beneficial for achieving an operation approximating to Meindl limit.

Charge-pump improvement techniques for EH application can be classified into their operational techniques: gate-biasing, bulk-biasing, reconfigurable, clock boosting, pre-charging node, and adiabatic. The performances of recent published charge-pumps for EH are compiled in Table II. Gate-biasing can be subclassified into internal gate-biasing and external gate-biasing. The effective switching of the transistors relies on V_{gs}. The transistor has to be driven in the triode region for effective charge transfer. Current state-of-the-art charge-pumps has achieved a minimum input/start-up voltage of $\sim$150 mV. This input voltage is lower than V_{th} which is typically between 300 to 500 mV. This implies that the transistors are operating in weak inversion which dwindles the conduction of the MOSFETs. The various operational techniques in charge-pump for EH application aims to circumvent this drawback.

TABLE 2. Comparison of state-of-the-art energy harvesting CMOS charge-pump.

Ref.	Tech. (nm)	Topology	Input Voltage (V)	No. of Stage	Pumping Cap. (pF)	Load Cap. (pF)	Load (µA)	VCE (%)	PCE (%)	Clock Freq. (MHz)	Area (mm^2)
[6]	130	Switched four-branches Bootstrap based CP	0.5	5	10x4x14.56 + 20x4x0.097	800	30	93 @ 500 mV	78.6	0.8-2.5	0.98
[7]	180	CC-CP: MVG and HVG	0.35	2 (MVG) 2 (HVG)	4x480 (MVG) 4x360 (HVG)	1300 (MVG) 200 (HVG)	114/ 396	79.7 @ 0.59 V (MVG) 60.5 @ 2.5 V (HVG)	49.1/ 75.8	-	1.75
[42]	130	Bootstrap	0.27 - no reg. 0.4 - reg.	3	50 x 3	500	5	65 @ 450 mV	58	0.8 [nominal] 0.6-1 [tunable]	0.42
[45]	65	CC-CP: low-leakage drivers	0.1-0.6	3	50 x 6	100	0.032/ 1000	90.5@100 mV / 99 @ 600 mV	12.7/ 70.3	-	-
[64]	65	CC-CP: clock boosting to 3 x V_{DD} and 6-phase frequency generation	0.15	3	2.5 x 9	30	1.74	80 @ 150 mV	38.8	15.2	0.032
[65]	65	CC-CP: FBB start-up technique	0.18	3	12.3 x 6 + 0.4 x 2	12.30	8.75	69 @ 180 mV	-	10	0.296
[66]	65	Dickson: dual mode [startup/ operation]	0.12	10	28.6 x 10	-	3.9	58 @ 120 mV	38.8	1 [startup] 20 [op.]	0.78
[70]	180	CC-CP: D(G/B)B	0.32	6	24 x 12	50.7	-	89 @ 320 mV	-	0.45	0.14
[71]	65	Dickson: DGB	0.55	4	40 x 4	400	10	98 @ 700 mV	66	0.5-1.8	0.17
[72]	65	Charge Transfer Switch	0.4/0.2	4	4 x 20	160	20/50	94.3/ 99.4	72.7/ 78.2	25	0.019
[73]	65	Bootstrap CP: DGB	0.1	10	100 x 10 + 0.1 x 10	100	6.6	76 @ 100 mV	33	1	1.32
[81]	130	Cross-doubler: DBB	0.15	3	10000 x 6 (off-chip)	10000 (off chip)	21	86 @ 180 mV	34	0.25	0.066 w/o cap
[83]	180	Reconfigurable CP	0.45	4	62.7 x 4	2050	-	89 @ 0.45V	-	0.286-1	4.00
[85]	65	CC-CP	0.4	4	8 x 10	160	0.1	99.2	87.8	4	0.021
[86]	130	2-Branches Diode-PMOS with DGB to implement two-step clock signal.	0.125	3/7	16 x 6, 16x14	100	0.1	80 @ 125 mV, 70 @ 125 mV	65/ 59	0.36	0.10, 0.15

In gate-control (biasing) [67]–[71], the gate voltage of the $N_{th,cp}$ stage is provided through a voltage potential generated internally from a higher node in the charge-pump. As the pumping efficiency of the charge-pump degrades due to the off-state of the device, a CMOS inverter is adopted to dynamically control the gate by providing a higher voltage potential from the subsequent stage in the charge-pump as a voltage supply (V_{DD}) to the inverter. This also lowers potential from the previous stage of the charge-pump to negative supply (V_{SS}) of the inverter. By adopting internal gate biasing techniques, effective on-state and off-state of the switches can be attained [72] by improving the overdrive voltage and an increase in the subthreshold conduction of the transistor. This reduces the negative reverse charge sharing and conduction losses phenomenon. Adopting PMOS transistor can reduce reverse leakage as discussed earlier to improve the pumping efficiency of the charge-pump.

External gate biasing technique adopts a similar concept but through the aid of external peripherals [73]. Clock boosting techniques [74] as external gate control elements can be generated by level shifters [75], *LC*-oscillators [76]–[78], ring-oscillators [64], multiphase-multi voltage level clock generator, or bootstrapping techniques. These techniques provide an improvement in the clock voltage swing of more than 3x of the input supply voltage, reducing conduction losses. Besides, the external clock boosting significantly reduces the number of charge-pump stages required. This reduces the rise time, improves the PCE, and reduces the active chip area [79]. However, external gate biasing requires peripheral circuits that consume additional power which are accounted in the efficiency computation of the charge-pump.

Bulk-biasing or body-biasing is another key technique in charge-pump for EH application [65], [67], [70], [80], [81]. This technique reduces V_{th} through biasing of the transistor's bulk. Deep N-well transistors are required to isolate the bulk and the IC substrate. There are 3 types of body-biasing techniques: forward bulk-biasing, reverse bulk-biasing, and dynamic bulk-biasing. State-of-art charge-pump and peripheral circuits have adopted bulk-biasing to achieve low-startup. However, utilizing forward or reverse bulk-biasing could limit the attainable PCE as reverse sharing and switching losses increases. Alternatively, dynamic bulk-biasing provides V_{th} reduction at forward bias and increases V_{th} during reverse bias to ensure on- or off-state of the transistors according to the operational cycle. Auxiliary transistors which are used for bulk bias are kept at a minimum size to avoid increases in capacitance. Switching losses, body effect, and extreme V_{th} drop are reduced and a significant reduction in conduction losses is achieved.

Reconfigurable techniques in charge-pump are developed to improve the switching performance with the aid of pass transistor switches which configure the circuit's architecture according to predetermine conditions [82], [83]. Optimal charge-pump stage selection [84], series-parallel configuration [83], dual-mode operation [66] and sleep-wake mode [10] are some example of the reconfigurable techniques. Attentive design of the pass transistor as a switching element is required to avoid inadequacy in switching which can increase the prospect for various losses.

In [85], precharge node technique is introduced and adopted at the intermediate nodes of the charge pump. This is to mitigate the rise time and input requirement during wake-up phase of EH systems. This concept improves efficiency by maintaining the node voltage between charge-pump stage equals to the input power by applying precharge current (I_{pc}) into intermediate isolated p-well. Therefore, I_{pc} is greater than the leakage current in which more charges will be fed to the next immediate top-plate capacitor stage. Hence, this technique minimizes the leakage as well as parasitics capacitance at the top-plate of the capacitor. However, auxiliary transistor, as well as triple well CMOS process, are required in this technique.

Last but not least, the adiabatic charge-pump is employed to reduce current peaking and improve the PCE [86], [87]. Assuming that a clock boosting element provides a signal amplitude greater than V_{DD} (i.e.: $2V_{DD}$ or $3V_{DD}$), higher charge transferability can be achieved while simultaneously attaining better PCE performance with lower charge-pump stages. Peak current is evident and can cause reliability issues. Therefore, the clock signals are divided into two steps to attain peak amplitude and vice versa. The charging of capacitors to 3x of V_{DD} in a single step can be mathematically expressed as [60],

$$E_{\text{Single–Step}} = Q * 3V_{DD} \tag{26}$$

The energy delivered by the supply voltage for charging the capacitor to V_{DD} in two steps is,

$$E_{\text{Two–Step}} = Q.\frac{1}{4}3V_{DD} + \frac{1}{2}Q.3V_{DD} = 2.25.QV_{DD} \tag{27}$$

The first term of (27) is obtained through charge sharing. A two-step charging with sharing charge observes a 50% reduction in energy compared to single-step charging. The energy needed to charge/discharge the capacitor at a specific node is given as,

$$E_{\text{source}} = \frac{1}{2}Q.3V_{DD} = \frac{9}{2}C.V_{DD}^2 \tag{28}$$

To summarize the adiabatic technique, energy dissipation is reduced by minimizing the voltage swing [88]. Two-step of gate control are available for the PMOS device to reduce the peak current which reduces half of the power dissipation, improving the PCE of the charge-pump.

C. VOLTAGE CONTROLLED OSCILLATOR (VCO)

The oscillator is considered the main peripheral circuit of the charge-pump. Power consumption, frequency, number of clock phases, and clock boosting voltages are inherent to the performance of an oscillator. Monolithic voltage-controlled-oscillators (VCOs) are classified majorly into two types; *LC*-VCOs and Ring-VCOs (*R*-VCO). The schematic of conventional *LC*- and *R*-VCOs are shown in Fig.7. *R*-VCO can be

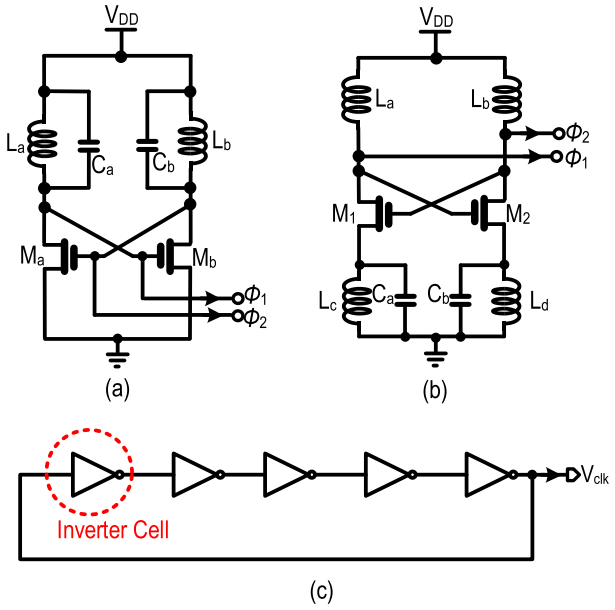

FIGURE 7. (a,b) *LC*-VCO. (c) conventional *R*-VCO.

classified into single-ended *R*-VCO and differential *R*-VCO. *R*-VCOs are best suited for EH applications due to their wide range of operation frequency, low power-loss, and simplicity in design compared to the *LC*-VCO. *LC*-VCOs are rarely used in charge-pump for EH application and will be omitted for discussion in this article.

R-VCO is commonly designed with a feedback loop of odd inverters [Fig.7(c)]. Its operational frequency (f_{vco}) is inversely proportional to the propagation delay (t_{delay}) and the number of inverters stages (N_{inv}) expressed as,

$$f_{\text{vco}} = \frac{1}{2N_{\text{inv}} * t_{\text{delay}}} \tag{29}$$

The frequency can be controlled by altering the number of stages or through the supply voltage. The minimum supply voltage in which *R*-VCO starts to oscillates is known as the start-up voltage and is dependent on the MOSFET's threshold voltage, where the V_{th} is expressed as,

$$\text{V}_{\text{th}} = \text{V}_{\text{th0}} + \gamma(\sqrt{|\text{V}_{\text{sb}} + 2\Phi_{\text{f}}|} - \sqrt{2\Phi_{\text{f}}} \tag{30}$$

V_{th} and V_{th0} are the threshold voltage and threshold voltage at zero source-to-bulk voltage (V_{sb}), respectively. Φ_{f} is the Fermi potential and γ is the body effect parameter. As suggested in (30), a transistor's V_{th} can be reduced through bulk-biasing(V_{sb}), either forward body-biasing or dynamic body-biasing. V_{sb}can be a positive or negative voltage potential to influence V_{th} of the NMOS or PMOS, respectively.

Shift register-based *R*-VCO and *N*-stage frequency divider can be adopted to control the frequency of the VCO for a wide-input operation range [89]. A six-phase differential bootstrapped *R*-VCO is proposed in [64] to deliver a high PCE charge-pump EH circuit. Alternatively, bootstrap single-ended *R*-VCO [90] achieves low start-up but suffers from leakage current and switching loss with a detailed analysis is reported in [91]. Clock booster circuits can provide faster rise time for the charge-pump. An 8 phase bootstrap *R*-VCO with an internal pseudo-differential clocking scheme as reported in[92] has demonstrated the advantages of clock booster circuits. However, a trade-off in design complexity and power dissipation exists and has to be taken into consideration[79].

Low voltage selective-Schmitt trigger inverters are used in the *R*-VCO to achieve 90% swing at 60 mV of input voltage [93]. Another process tolerant *R*-VCO is proposed with a single-cell inverter to provide start-up at 60 mV[94]. In [70], a 5 stage *R*-VCO is reported with two parallel phase shifters operating in subthreshold with a resistive voltage divider to provide bulk biasing for V_{th} reduction. The W/L of the *R*-VCO is kept to a minimal for achieving low V_{th} with the W/L of the buffer maximized [95] to achieve high current drivability as well as maximum clock swing.

IV. DISCUSSION

All the charge-pump techniques reviewed in this article are identified to be suitable for RFEH system in which two or more of these techniques can be fused to attain overall system improvement in PCE and start-up performance. As for the peripheral circuits, *R*-VCO will the most preferred peripheral circuits for RFEH systems as it occupies smaller chip area, achieve low-power consumption and wide-dynamic operational frequency to accommodate variation of the input harvesting voltage compared to the *LC*-VCO. However, it is worth noting that implementing too many peripheral circuits is detrimental to the overall PCE of the harvesting system. Designers should pay attention to the various trade-offs [Fig.8.(a)] that may incur cost, increase parasitic, or leakages that degrade the PCE.

Considering all these design factors of a capacitive-based step-up DC-DC converter (charge-pump), Fig. 8(a) provides a visual illustration of the performance trade-offs. Fig.8(a) outlays all the trade-offs associated in the attempt to attain high PCE and low-input-voltage in designing the charge-pump for RFEH system. The design considerations of a charge-pump are categorized into three layers, namely the core (overall DC-DC converter), intermediate ring (peripherals), and outer ring (second-order effects/losses) for maximizing the PCE and start-up voltage.

The main design aim of the charge-pump is to maximize its PCE. Based on Fig.8(a), the core elements that affects the PCE is the R_{load} [96], *N*-stage [54], [64], [66], [79], [97], [98] and C_{pump} [99]. However, as described in Fig.8(a), there are contradicting trade-offs in achieving the desired specification such as start-up time [79], [85], [100], [101], $V_{\text{out,cp,}}$ and area. However, peripheral circuits also contribute in altering the specification which affects the PCE of the overall charge-pump circuit.

Respective to the design of the peripherals, it is desirable to ensure that the charge-pump achieve its function such as clock generation [64], [70], level shifting [56], [59], [81], and low output voltage ripple [64] with minimal degradation to achieve high-PCE in the overall charge-pump

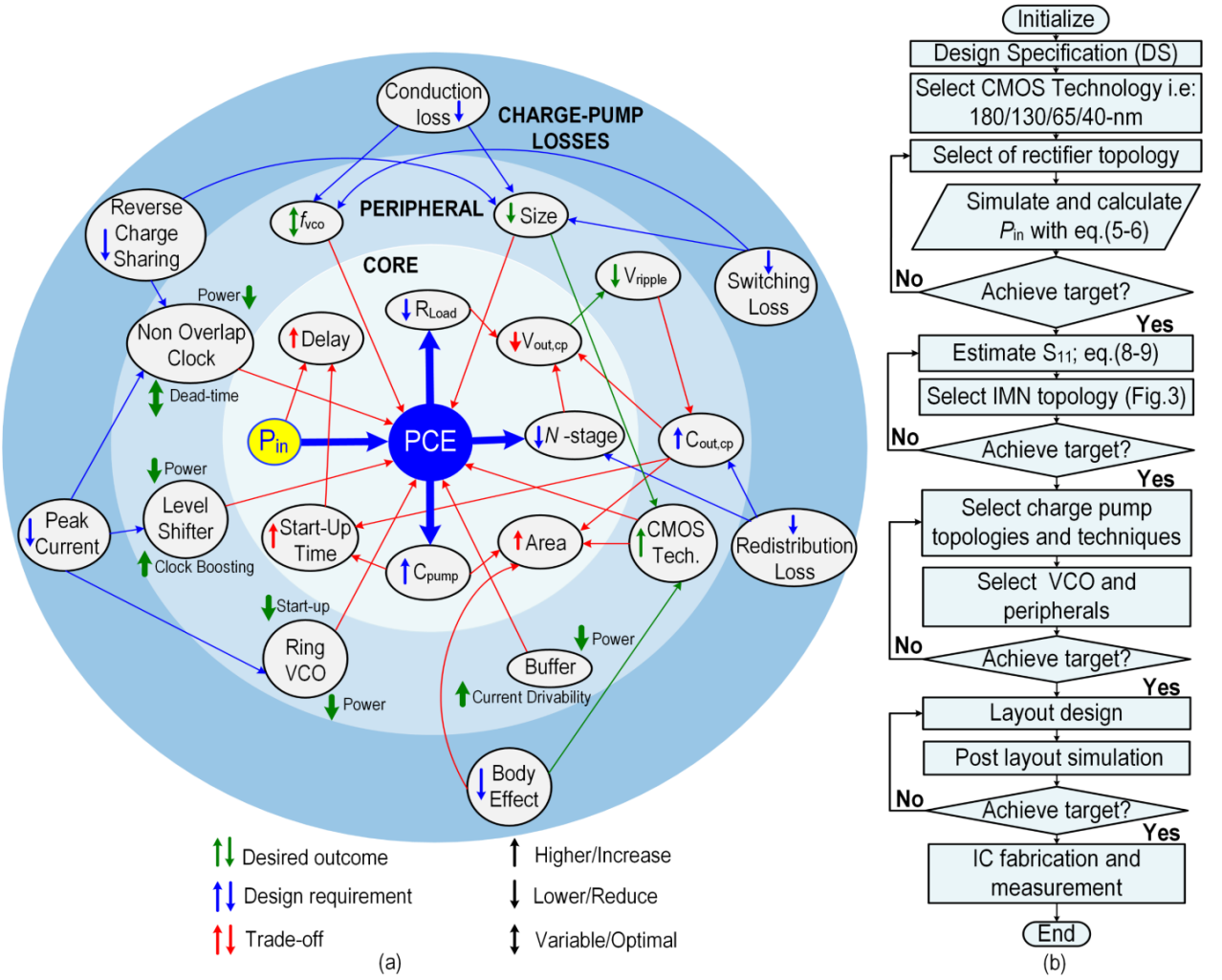

FIGURE 8. Design consideration of RFEH system. (a) Design requirements, performance outcome, and trade-offs of charge-pump circuit. (b) Design flowchart.

circuit. However, designers should be aware of the trade-offs associated with the design in the peripherals as shown in Fig.8(a). As an example, if we alter the transistor size of the charge-pump by increasing its width, this will increase the gate capacitance, thus, affecting the switching loss. Similarly, conduction loss increases when the width of the transistor is minimized, alleviating switching losses where the losses are reflected in the overall PCE of the RFEH system. Therefore, there is an optimal sizing of the transistor for minimal losses [102] and to attain the maximum PCE of the charge-pump, achieving higher power conversion ratio as illustrated in Fig.9. Table II summarized the performance of the state-of-art EH charge-pumps which are a promising option for further enhancement as capacitive-based step-up DC-DC converter for RFEH system.

Eliminating all losses is an impractical endeavour. Intuitive circuit design techniques are required to achieve optimal performance for the targeted application. This will be a significant challenge in the research and development of capacitive-based step-up DC-DC converter for RFEH systems to minimize losses and maximize the PCE. For designing an RFEH system, Fig.8(b) provides a systematic

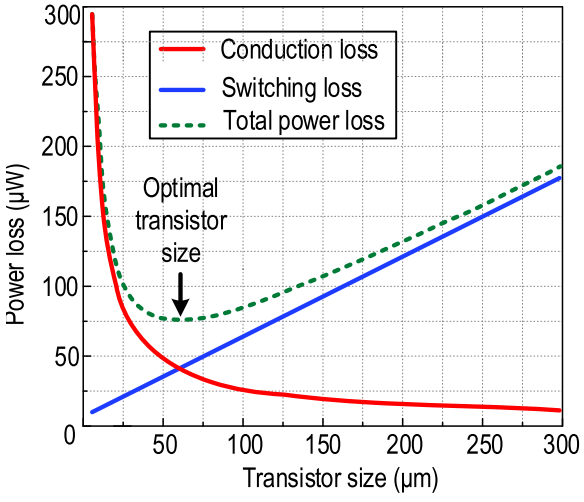

FIGURE 9. Optimal transistor sizing.

approach to Fig. 8(a) for effective design as a guide for designers to understand the trade-offs associated in the charge-pump circuit. Starting with the technology node, rectifier, and IMN, the charge-pump topology and technique are selected according to the design requirements of the RFEH System. The VCO and peripheral circuits are selected according to the requirement of the charge-pump. If the performance of the system could not attain the desired performance specifications, the VCO topology and/or peripheral circuits are reconsidered. Once the performances are met, further optimization in the layout are required prior to IC fabrication and validation.

V. CONCLUSION

In conclusion, this article has provided an overview of the charge-pump circuit for RFEH systems. A summary of state-of-art charge-pump design for EH application, specifically in RFEH systems has been considered. A review of charge-pump circuits has been presented which has discussed various prior state-of-art architectures in the aspect of losses, design techniques for charge-pump in the development for RFEH system utilizing a capacitive-based step-up DC-DC converter. Considering the characteristics for wide range of charge-pump circuit designs, a methodology is proposed to visualize design aspects and performance trade-offs of EH charge-pump in which designers have to consider to realize a highly efficient step-up DC-DC converter in RFEH systems for the next generation of miniaturized IoT devices.

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