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Error Compensation Algorithm for SRF-PLL in Three-Phase Grid-Connected Converters

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ABSTRACT This paper proposes an error compensation algorithm based on synchronous reference frame phase-locked loop for accurate phase estimation of the distorted three-phase voltages including asymmetrical phase voltages, harmonics, and dc offset. These errors cause undesirable periodic ripples with grid frequency in the traditional PLL and significantly degrade the overall performance of the grid-connected converters. In this paper, the effects of the errors are comprehensively analyzed in the stationary and synchronous reference frames. In particular, the errors are estimated and compensated by controlling the α-axis and β-axis components in a PLL to be balanced. The proposed compensation algorithm can be implemented by some integral operations followed by simple Integral-controllers. The performance and robustness of proposed compensation technique are investigated under distorted grid conditions. The proposed technique is numerically and experimentally verified using Matlab/Simulink and Dspace1202 control board platform.

INDEX TERMS Phase-locked loop (PLL), compensation algorithm, dc-offset error, unbalancing error, harmonics, phase angle estimation.

I. INTRODUCTION

The three-phase grid-connected converter is very important for many applications such as renewable energy conversion systems, active power filters, battery charger of electric vehicles, static VAR compensators, uninterruptible power supplies (UPSs), and energy storage systems [1]–[3]. The phase-locked loop (PLL) is one of the most important parts of these systems to achieve a decoupled active and reactive power control for the grid-connected converters. The synchronization between the grid and the converters requires an accurate phase information of the grid voltages.

Among various types of three-phase PLLs, the synchronous reference frame-PLL (SRF-PLL (is mostly used to detect the phase angle of a grid's voltage for its simplicity and robustness [4]. The SRF-PLL can estimate the phase angle of the three-phase system accurately at high speed. However, the errors caused by the offset of the signal measurement and conditioning circuits, the harmonics, or any type of amplitude imbalances seriously influence the performance of PLL, therefore the dynamic performance of the grid-connected converters systems may be degraded [5]. A variety of advanced SRF-PLLs with enhanced disturbance rejection capability can be found in the literature. Most of these techniques based on using filters, which can be either included inside or added before the control loop of the conventional SRF-PLL.

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In this paper, a novel algorithm of error compensation based on SRF-PLL is proposed for accurate phase estimation of the distorted three phase voltages. The errors caused by asymmetrical three-phase voltages, harmonics, and dc-offset are comprehensively analyzed in stationary and synchronous reference frames. Accordingly, the effect of each error is estimated in $\alpha\beta$-domain and then compensated in the conventional SRF-PLL to balance the $\alpha\beta$-axes components (two sinusoids that have the same magnitude and frequency, and are 180° out of phase). In the proposed algorithm, the errors are readily estimated by using integral operations for the synchronous qd-axes voltages according to the estimated phase angle followed by Integral-controllers. The proposed compensation method consists of three compensators: dc offset compensator, phase unbalancing compensator, and harmonics compensator. The compensators are designed to operate in parallel to have faster processing performance.

The proposed compensation algorithm, which is directly embedded in the SRF-PLL, enables a new concept of phase estimation under distorted grid conditions and it can be a suitable candidate to eliminate the distortion errors and improve the performance of traditional SRF-PLLs. The proposed compensation method is numerically and experimentally verified using Matlab/Simulink and Dspace1202 control board platform.

This paper is organized in seven sections and the rest of the paper is organized as follows –Section II summarizes the state of art and relevant publications on the latest PLLs.

Section III analyzes the effects of the errors for distorted grid based on the stationary and synchronous frames. Section IV introduces the proposed error compensation technique and compares it with some advanced PLLs. Section V presents the simulation results using MATLAB/Simulink under several grid disturbances. Section VI documents experimental results in dSPACE control board platform. Section VII concludes the work presented in the paper.

II. STATE OF ART

Moving average filter-PLL (MAF-PLL) has been suggested in [6]. The MAF is added inside the control loop of the conventional SRF-PLL to improve its filtering capability. The MAF-PLL cancels the non-triplen odd harmonics, the dc-offset and the negative sequence component of the PLL three-phase input signals at the fundamental frequency. However, adding the filter considerably slows down dynamic performance of the PLL. The dynamic response of the controller can be improved by using a PID controller [7] and [8], a special lead compensator [9], or a quasi-type-1 PLL (QT1-PLL) structure in implementation [10]. Pre-loop MAF-PLL has been suggested in [11] to be added before the control loop of the conventional SRF-PLL to block disturbance components without significantly affecting the dynamic behavior of the PLL. However, the use of non-adaptive pre-filtering stage within the conventional SRF-PLL requires an additional frequency detector.

Adaptive notch filter-PLL (NF-PLL) has been introduced in [12]. This technique is able to cancel the desired harmonic components in the PLL control loop with small phase delay. However, this advantage is at the cost rather considerable increase in the PLL computational burden. Moreover, the method assumes that the source frequency is known and fixed. Therefore, the parameters of the filter must be changed according to the change in frequency for accurate phase estimation.

Dual SRF filtering-PLL (DSRF-PLL) has been introduced in [13]. This PLL is able to estimate the grid's phase angle under unbalanced grid voltages. However, this technique has imperfect cancellation of harmonic components. The harmonic rejection capability of this technique can be improved by adding more SRFs at the desired harmonic frequencies to the standard structure [13]. This approach, however, increases the computational effort in the PLL. Dual complex-coefficient filter-PLL (DCCF-PLL) has been proposed in [14]. This method has high imbalance and harmonic rejection capabilities.

Recently, delayed signal cancellation-PLL (DSC-PLL) has been proposed and used in the field of grid phase estimation in the three-phase grid-connected converters [15], [16]. This method is the most commonly used method since it has advantages of easy implementation, less computational burden of controller, and it can be easily fitted for different grid conditions. The DSC operator can be added either inside the control loop of the conventional SRF-PLL (dq-frame DSC-PLL) or before the control loop of the conventional SRF-PLL ($\alpha\beta$-frame DSC-PLL). The dq-frame DSC-PLL slows down the dynamic performance of the SRF-PLL. However, the dynamic response can be improved by using a PID controller or a special lead compensator. On the other hand, the $\alpha\beta$-frame DSC-PLL is able to block disturbance components without affecting the dynamic behavior of the PLL. The number of operators in both techniques depends on the harmonic contents of three-phase input signals. These operators must be adapted to the variations in the estimated frequency in order to correct the output phase and amplitude errors and cancel of harmonic components in the presence of frequency change [17]. The adapting process increases the implementation complexity and the computational effort [18]. Moreover, the frequency feedback loop makes the system more nonlinear and difficult to be analyzed from the stability point of view [19].

A second-order generalized integrator-PLL (SOGI-PLL) uses a quadrature signal generator (QSG) with band-pass filter to make a discrimination between the positive and negative sequences of the same frequency [20]. The harmonic filtering capability of this technique can be improved by adding more SOGIs at the desired harmonic frequencies to the standard structure [21]. This approach, however, increases the computational burden in the PLL. An alternative approach is to use the third-order generalized integrator-PLL (TOGI-PLL) [1].

Repetitive regulator-PLL (RR-PLL) has been introduced in [22]. The main advantage of this technique is that its computational burden does not depend on the harmonic content of input signals, but it highly depends on the sampling period of the PLL. Therefore, this method is not recommended for applications where the sampling frequency of the control system is high and/or the three-phase PLL input signals contain a very few harmonics.

Zero-crossing detection-PLL (ZCD-PLL) has been suggested in [23]. This technique is simple in implementation and works well under unbalanced three-phase input signals. However, the harmonic filtering capability of this method is limited.

Space vector Fourier transform-PLL (SVFT-PLL) has been proposed in [24]. This method requires low computational burden when it is implemented in the recursive form. However, the recursive implementation of the SVFT filter makes the system more difficult to be analyzed from the stability point of view. This stability problem can also be solved by using a non-recursive implementation of the SVFT filter. The non-recursive implementation, however, increases the computational effort in the PLL.

Second-order lead compensator-PLL (SOLC-PLL) has been suggested in [25]. This compensator is added inside the control loop of the conventional SRF-PLL to block harmonics without affecting the dynamic behavior of the PLL. Adding the compensator inside the SRF-PLL improves its filtering capability, but it is at the cost of a low noise immunity and slow dynamic performance.

Not all the aforementioned PLLs deal with disturbances caused by the dc offset except that the MAF-PLL. The sources of dc offset in the three-phase input signals

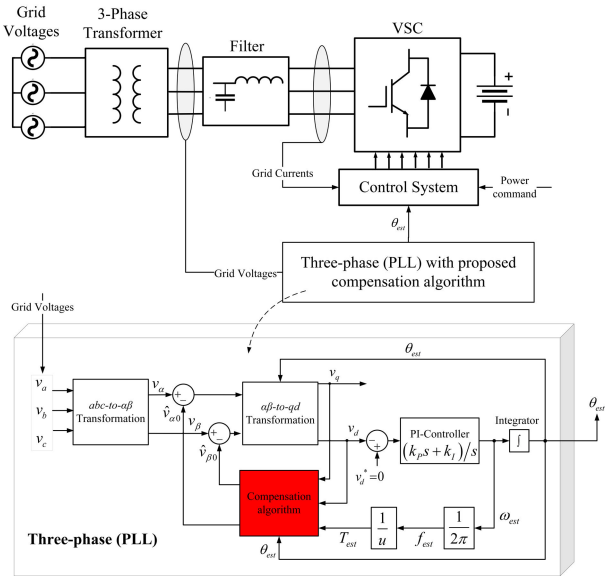


FIGURE 1. Control block diagram of three-phase grid-connected converter.

are grid faults, measurement devices, dc injection from three-phase inverters, geomagnetic phenomena, and rectifiers. The PLLs must be able to reject a high dc offset; otherwise, it will result in dc injection by the grid-connected converter. Different approaches have been proposed in the literature to tackle the problem of dc offset. In [26], an integrator dc offset loop has been added to the standard PLL to estimate and reject the dc components within the three-phase input signals. This technique is simple and effective. In [27], the dc offset has been rejected through a frequency-adaptive correction unit. This approach gives a complete and fast rejection of the dc offset in PLLs. In [28], five other dc offset rejection strategies have been proposed. These strategies include using dq-frame DSC-PLL, $\alpha\beta$-frame DSC-PLL, NF-PLL, CCF-PLL, and a cross-feedback network (CFN) for blocking the dc offset before the PLL input. These techniques can significantly improve the dc offset rejecting capability of the PLL, but at the cost of slowing down its dynamic response due to the added filters to block the dc components.

However, the three compensators in the proposed compensation algorithm are designed to operate in parallel and do not require any additional filter. Therefore, the computation burden is reduced significantly with a faster dynamic response compared to other PLL techniques since each compensator can be easily implemented by using two integral operations according to the estimated phase angle followed by two Integral-controllers without a filtering process. A performance comparison between the proposed algorithm and the advanced PLLs that have been found in the literature will be discussed later in section IV.

III. ERROR ANALYSIS FOR DISTORTED GRID

Fig. 1 shows the block diagram of the three-phase grid-connected converter including conversion circuit and control system, which is used to implement the SRF-PLL with the proposed error compensation algorithm in this paper. The PLL is used to synchronize the grid with the voltage source converter (VSC) to achieve the desired decoupled PQ-control by estimating the grid frequency and phase angle. In reality, the grid voltages may be distorted due to the connection of the grid to a nonlinear load (e.g. rectifier), nonlinear effect of voltage sensors, filters, and A/D converters. The external distortion factors generate asymmetrical three-phase voltages along with harmonic distortion and dc offset in the measured voltages and therefore cause errors in the SRF-PLL system, which may affect the control performance of power converter. In this section, the errors caused by the distortion of the grid voltages are derived. The measured grid voltages considering dc offset, phase unbalancing, and harmonics can be written as:

$$\begin{aligned}
v_{abc} &= \begin{pmatrix} v_a & v_b & v_c \end{pmatrix}^T \\
v_{abc} &= \underbrace{\mu_{abc}}_{\text{DC offset}} + \underbrace{V_{m,abc}\cos\left(\theta + \chi_{abc}\right)}_{\text{Phase unbalancing}} \\
&\quad + \underbrace{\sum_{n=1}\left\{V_{6n-1}\cos\left((6n-1)\left(\theta+\chi_{abc}\right)\right)\right\}}_{\text{Harmonics}} \\
&\quad + \underbrace{\sum_{n=1}\left\{V_{6n+1}\cos\left((6n+1)\left(\theta+\chi_{abc}\right)\right)\right\}}_{\text{Harmonics}}; \\
\theta &= \int \omega\, dt \\
\chi_{abc} &= \begin{pmatrix} 0 & 2\pi/3 & -2\pi/3 \end{pmatrix}^T; \\
\mu_{abc} &= \begin{pmatrix} \mu_a & \mu_b & \mu_c \end{pmatrix}^T; \\
V_{m,abc} &= \begin{pmatrix} V_{m,a} & V_{m,b} & V_{m,c} \end{pmatrix}^T \\
&= \begin{pmatrix} V_m & \rho V_m & \lambda V_m \end{pmatrix}^T;
\end{aligned} \tag{1}$$

where v_{abc} is the grid voltage vector, V_m is the peak value of the measured grid's phase voltage (phase-a), μ_{abc} is a vector that represents the dc offset, and ρ and λ are factors that represents the phase unbalance with respect to phase-a.

The phase voltages can be expressed in stationary reference frame as:

$$v_{\alpha\beta} = \begin{pmatrix} v_\alpha & v_\beta \end{pmatrix}^T = \begin{pmatrix} 2/3 & -1/3 & -1/3 \\ 0 & -1/\sqrt{3} & 1/\sqrt{3} \end{pmatrix} v_{abc} \tag{2}$$

Substituting (1) in (2), yields:

$$\begin{aligned}
v_\alpha &= v_{\alpha 0} + V_m\cos\theta = \underbrace{v_{\alpha,O} + v_{\alpha,U} + v_{\alpha,h}}_{v_{\alpha 0}} + V_m\cos\theta \\
v_\beta &= v_{\beta 0} - V_m\sin\theta = \underbrace{v_{\beta,O} + v_{\beta,U} + v_{\beta,h}}_{v_{\beta 0}} - V_m\sin\theta
\end{aligned} \tag{3}$$

where

- $v_{\alpha,O}$ and $v_{\beta,O}$ are the α-axis and β-axis components due to the dc offset, respectively, which are given by:

$$\begin{aligned} v_{\alpha\beta,\mathrm{O}} &= \begin{pmatrix} v_{\alpha 0,\mathrm{O}} & v_{\beta 0,\mathrm{O}} \end{pmatrix}^T \\ v_{\alpha,\mathrm{O}} &= \frac{1}{3}\left(2\mu_a - \mu_b - \mu_c\right), \\ v_{\beta,\mathrm{O}} &= \frac{1}{\sqrt{3}}\left(-\mu_b + \mu_c\right) \end{aligned} \tag{4}$$

- $v_{\alpha,U}$ and $v_{\beta,U}$ are the α-axis and β-axis components due to phase unbalancing, respectively, which are given by:

$$\begin{aligned} v_{\alpha\beta,U} &= \begin{pmatrix} v_{\alpha,U} & v_{\beta,U} \end{pmatrix}^T \\ v_{\alpha,U} &= \frac{1}{6}H_1\cos\theta - \frac{1}{2\sqrt{3}}H_2\sin\theta, \\ v_{\beta,U} &= -\frac{1}{2}H_1\sin\theta + \frac{1}{2\sqrt{3}}H_2\cos\theta \\ H_1 &= (\rho + \lambda - 2)\,V_m, \quad H_2 = (\rho - \lambda)\,V_m \end{aligned} \tag{5}$$

- $v_{\alpha,h}$ and $v_{\beta,h}$ are the α-axis and β-axis components due to harmonics, respectively, which are given by:

$$\begin{aligned} v_{\alpha\beta,h} &= \begin{pmatrix} v_{\alpha,h} & v_{\beta,h} \end{pmatrix}^T \\ v_{\alpha,h} &= \sum_{n=1}\{V_{6n+1}\cos\left((6n+1)\,\theta\right) \\ &\qquad + V_{6n-1}\cos\left((6n-1)\,\theta\right)\}, \\ v_{\beta,h} &= \sum_{n=1}\{V_{6n+1}\sin\left((6n+1)\,\theta\right) \\ &\qquad - V_{6n-1}\sin\left((6n-1)\,\theta\right)\} \end{aligned} \tag{6}$$

The components, v_α and v_β, can be rewritten in rotating reference frame using the estimated phase angle of the grid, θ_{est}, as:

$$v_{qd} = \begin{pmatrix} v_q & v_d \end{pmatrix}^T = \begin{pmatrix} \cos\theta_{est} & -\sin\theta_{est} \\ \sin\theta_{est} & \cos\theta_{est} \end{pmatrix}\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} \tag{7}$$

The q-axis the d-axis components are derived as:

$$\begin{aligned} v_q &= v_\alpha\cos\theta_{est} - v_\beta\sin\theta_{est} \approx v_{q,O} + v_{q,U} + v_{q,h} + V_m \\ v_d &= v_\alpha\sin\theta_{est} + v_\beta\cos\theta_{est} \approx v_{d,O} + v_{d,U} + v_{d,h} - V_m e \end{aligned} \tag{8}$$

where

- e is the error of the grid's phase angle ($e = \theta - \theta_{\mathrm{est}}$),
- $v_{q,O}$ and $v_{d,O}$ are the synchronous q-axis and d-axis components due to dc offset, respectively:

$$\begin{aligned} v_{q,O} &= v_{\alpha,\mathrm{O}}\cos\theta_{est} - v_{\beta,\mathrm{O}}\sin\theta_{est}; \\ v_{d,O} &= v_{\alpha,\mathrm{O}}\sin\theta_{est} + v_{\beta,\mathrm{O}}\cos\theta_{est} \end{aligned} \tag{9}$$

- $v_{q,U}$ and $v_{d,U}$ are the synchronous q-axis and d-axis components due to phase unbalancing, respectively:

$$\begin{aligned} v_{q,U} &\approx \frac{1}{3}H_1 - \frac{1}{6}H_1\cos\left(2\theta_{est}\right) - \frac{1}{2\sqrt{3}}H_2\sin\left(2\theta_{est}\right) \\ v_{d,U} &\approx -\frac{1}{6}H_1\sin\left(2\theta_{est}\right) - \frac{1}{2\sqrt{3}}H_2\cos\left(2\theta_{est}\right) \end{aligned} \tag{10}$$

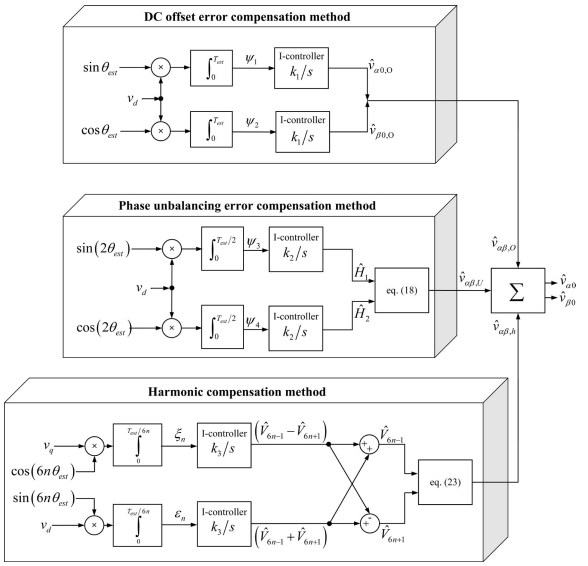


FIGURE 2. The proposed estimation technique.

- $v_{q,h}$ and $v_{d,h}$ are the synchronous q-axis and d-axis components due to harmonics, respectively:

$$\begin{aligned} v_{q,h} &\approx \sum_{n=1}\left(V_{6n-1} + V_{6n+1}\right)\cos\left(6n\theta_{est}\right) \\ v_{d,h} &\approx \sum_{n=1}\left(V_{6n-1} - V_{6n+1}\right)\sin\left(6n\theta_{est}\right) \end{aligned} \tag{11}$$

It is noted in (9), (10), and (11) that the error caused by the offset has the same frequency component with that of the utility voltage, ω, the phase unbalancing produces the error with 2ω frequency component, and the grid harmonics causes the error with the frequency components that are the multiples of six of the grid frequency.

IV. PROPOSED ERROR COMPENSATION METHOD

Fig. 2 shows the block diagram of the proposed compensation technique, which consists of three compensators: dc offset compensator, phase unbalancing compensator, and harmonics compensator.

A. DC OFFSET COMPENSATOR

The main function of the dc offset compensator is to estimate the components of $v_{\alpha,O}$ and $v_{\beta,O}$ as shown in Fig. 2. The procedure of estimating these components is described as follows:

1) Multiplying the synchronous d-axis voltage by sine and cosine functions of the same grid frequency and phase, and integrating the results using the estimated grid angle over the period [0, T_{est}]. The integrated results according to the specific grid angle are given by:

$$\begin{aligned} \Lambda_1 &= \frac{1}{T_{est}}\int_0^{T_{est}} v_d\sin\theta_{est}d\theta_{est} = \frac{1}{2}\left(v_{\alpha,O} - \hat{v}_{\alpha,O}\right); \\ \Lambda_2 &= \frac{1}{T_{est}}\int_0^{T_{est}} v_d\cos\theta_{est}d\theta_{est} = \frac{1}{2}\left(v_{\beta,O} - \hat{v}_{\beta,O}\right); \end{aligned} \tag{12}$$

2) Calculating the error signals ψ_1 and ψ_2 required for Integral-controllers:

$$\psi_1 = 2\Lambda_1; \quad \psi_2 = 2\Lambda_2; \tag{13}$$

3) Applying Integral-controllers on the error signals to estimate the components $v_{\alpha,O}$ and $v_{\beta,O}$:

$$\hat{v}_{\alpha,O} = k_1 \int \psi_1 dt; \quad \hat{v}_{\beta,O} = k_1 \int \psi_2 dt \tag{14}$$

where k_1 is the gain of the I-controller used in the dc offset compensator.

B. PHASE UNBALANCING COMPENSATOR

This compensator is used to estimate the components $v_{\alpha,U}$ and $v_{\beta,U}$. The procedure of estimating these components is described as follows:

1) Multiplying the synchronous d-axis voltage by sine and cosine functions of twice the grid frequency and phase, and then integrating the results over the period [0, $T_{est}/2$]. The integrated results according to the specific grid angle are given by:

$$\begin{aligned}\Lambda_3 &= \frac{2}{T_{est}} \int_0^{T_{est}/2} v_d \sin(2\theta_{est})\, d\theta_{est} \\ &= -\frac{1}{12}\left(H_1 - \hat{H}_1\right); \\ \Lambda_4 &= \frac{2}{T_{est}} \int_0^{T_{est}/2} v_d \cos(2\theta_{est})\, d\theta_{est} \\ &= -\frac{1}{4\sqrt{3}}\left(H_2 - \hat{H}_2\right);\end{aligned} \tag{15}$$

2) Calculating the error signals ψ_3 and ψ_4 required for I-controllers:

$$\begin{aligned}\psi_3 &= H_1 - \hat{H}_1 = -12\Lambda_3; \\ \psi_4 &= H_2 - \hat{H}_2 = -4\sqrt{3}\Lambda_4\end{aligned} \tag{16}$$

3) Applying Integral-controllers on the error signals to estimate the components of H_1 and H_2:

$$\hat{H}_1 = k_2 \int \psi_3 dt; \quad \hat{H}_2 = k_2 \int \psi_4 dt \tag{17}$$

where k_2 is the gain of the I-controller used in the phase unbalance compensator.

4) Calculating the estimated components of $v_{\alpha,U}$ and $v_{\beta,U}$:

$$\begin{aligned}\hat{v}_{\alpha,U} &= \frac{1}{6}\hat{H}_1 \cos\theta_{est} - \frac{1}{2\sqrt{3}}\hat{H}_2 \sin\theta_{est}, \\ \hat{v}_{\beta,U} &= -\frac{1}{2}\hat{H}_1 \sin\theta_{est} + \frac{1}{2\sqrt{3}}\hat{H}_2 \cos\theta_{est}\end{aligned} \tag{18}$$

C. HARMONICS COMPENSATOR

The main function of this compensator is to estimate the components of $v_{\alpha,h}$ and $v_{\beta,h}$ as shown in Fig. 2. The procedure of estimating these components is described as follows:

1) Multiplying the synchronous q-axis and d-axis voltages by cosine and sine functions with the frequency components of $6n\omega$, respectively, and then integrating the results according to the estimated grid angle [0, $T_{est}/6n$]. The integrated results according to the specific grid angle are given by:

$$\begin{aligned}\mathrm{T}_n &= \frac{6n}{T_{est}} \int_0^{T_{est}/6n} v_q \cos(6n\theta_{est})\, d\theta_{est} \\ &= \frac{1}{2}\left[(V_{6n-1} - V_{6n+1}) - \left(\hat{V}_{6n-1} - \hat{V}_{6n+1}\right)\right]; \\ \Gamma_n &= \frac{6n}{T_{est}} \int_0^{T_{est}/6n} v_d \sin(6n\theta_{est})\, d\theta_{est} \\ &= \frac{1}{2}\left[(V_{6n-1} + V_{6n+1}) - \left(\hat{V}_{6n-1} + \hat{V}_{6n+1}\right)\right];\end{aligned} \tag{19}$$

2) Calculating the error signals ξ_n and ε_n required for Integral-controllers

$$\xi_n = 2\mathrm{T}_n; \quad \varepsilon_n = 2\Gamma_n \tag{20}$$

3) Applying Integral-controllers on the error signals to estimate the components of $V_{6n-1} - V_{6n+1}$ and $V_{6n-1} + V_{6n+1}$:

$$\begin{aligned}\hat{V}_{6n-1} - \hat{V}_{6n+1} &= k_3 \int \xi_n dt; \\ \hat{V}_{6n-1} + \hat{V}_{6n+1} &= k_3 \int \varepsilon_n dt\end{aligned} \tag{21}$$

where k_3 is the gain of the I-controller used in the harmonic compensator.

4) Calculating the estimated values of V_{6n-1} and V_{6n+1}:

$$\begin{aligned}\hat{V}_{6n-1} &= \frac{1}{2}\left(k_3 \int \varepsilon_n dt + k_3 \int \xi_n dt\right); \\ \hat{V}_{6n+1} &= \frac{1}{2}\left(k_3 \int \varepsilon_n dt - k_3 \int \xi_n dt\right)\end{aligned} \tag{22}$$

5) Calculating the estimated components of $v_{\alpha,h}$ and $v_{\beta,h}$:

$$\begin{aligned}\hat{v}_{\alpha,h} &= \sum_{n=1} \Big\{\hat{V}_{6n+1} \cos((6n+1)\,\theta_{est}) \\ &\qquad + \hat{V}_{6n-1} \cos((6n-1)\,\theta_{est})\Big\} \\ \hat{v}_{\beta,h} &= \sum_{n=1} \Big\{\hat{V}_{6n+1} \sin((6n+1)\,\theta_{est}) \\ &\qquad - \hat{V}_{6n-1} \sin((6n-1)\,\theta_{est})\Big\}\end{aligned} \tag{23}$$

Finally, the estimated $\alpha\beta$-axes components due to all errors are estimated using (14), (18), and (23) as:

$$\hat{v}_{\alpha 0} = \hat{v}_{\alpha,O} + \hat{v}_{\alpha,U} + \hat{v}_{\alpha,h}; \quad \hat{v}_{\beta 0} = \hat{v}_{\beta,O} + \hat{v}_{\beta,U} + \hat{v}_{\beta,h} \tag{24}$$

and then subtracted from the $\alpha\beta$-axes components of the three-phase voltages to make them balanced for estimating the actual phase angle.

TABLE 1. Comparison of the proposed alogrithm with some advanced PLLS.

PLL	*Imbalance rejection capability*	*Harmonic rejection capability*	*DC-offset rejection capability*	*Filtering capability*	*Dynamic response*	*Computational burden*
In-loop MAF-PLL	----[1]	Yes	----[1]	High	Slow[4]	Low
Pre-loop MAF-PLL	----[1]	Yes	----[1]	High	Fast	Low
NF-PLL	Yes	No	No[2]	Average	Fast	Average
DSRF-PLL	Yes	Yes	No	High	Fast	High
CCF-PLL	Yes	Yes	No[2]	High	Fast	High
dq-frame DSC-PLL	Yes	No	No[2]	High	Slow[4]	Low
αβ- frame DSC-PLL	Yes	No	No[2]	High	Fast	----[5]
SOGI-PLL	Yes	Yes	No	High	Fast	High
RR-PLL	Yes	No	No	High	Average	High
ZCD-PLL	Yes	No	No	Low	Fast	Low
SVFT-PLL	Yes	No	No	High	Fast	High
SOLC-PLL	Yes	No	No	Average	Fast	Average
Proposed technique	**Yes**	**Yes**	**Yes**	**-----[3]**	**Fast**	**Low**

[1] Yes if the MAF's window length is equal to T and No if the window length equals (1/6) T as suggested in [29], where T is the fundamental period of the PLL input signals.
[2] The PLL can be extended to the dc-offset condition.
[3] The proposed technique does not require filtering stage.
[4] The dynamic response can be considerably improved by using the lead compensator, PID controller, or the QT1 structure in the implementation.
[5] Computational burden is low when non-adaptive DSC operators are used, and it is high when DSC operators are adapted to the grid frequency variations using interpolation techniques.

D. PERFORMANCE COMPARISON AND TRANSFER FUNCTIONS

A performance comparison between the proposed algorithm and some of the advanced PLLs given in the literature can be observed in TABLE 1. The comparison results in the table have been reached based on the literature review of PLL techniques given in section II. The comparison is based on imbalance rejection capability, harmonic rejection capability, dc-offset rejection capability, filtering capability, dynamic response, and the computational burden. The proposed algorithm estimates the grid's phase angle accurately at high speed with high harmonic, imbalance, and dc offset rejection capabilities. It should be mentioned that the proposed compensation algorithm does not have a filtering stage and can be easily implemented by some integral operations followed by simple Integral-controllers. Therefore, the computation burden is reduced significantly in comparison with other PLLs since there is a direct relation between the PLL filtering capability and its computational burden.

The transfer functions of inner loop controllers within the three compensators are obtained by taking the Laplace transformations of (12), (13), (14), (15), (16), (17), (19), (20), and (21):

$$\begin{aligned}
\frac{\hat{v}_{\alpha,O}(s)}{v_{\alpha,O}(s)} &= \frac{\hat{v}_{\beta,O}(s)}{v_{\beta,O}(s)} = \frac{k_1}{s+k_1};\\
\frac{\hat{H}_1(s)}{H_1(s)} &= \frac{\hat{H}_2(s)}{H_2(s)} = \frac{k_2}{s+k_2};\\
\frac{\hat{V}_{6n-1}(s)-\hat{V}_{6n+1}(s)}{V_{6n-1}(s)-V_{6n+1}(s)} &= \frac{\hat{V}_{6n-1}(s)+\hat{V}_{6n+1}(s)}{V_{6n-1}(s)+V_{6n+1}(s)} = \frac{k_3}{s+k_3};
\end{aligned} \tag{25}$$

These transfer functions are first order systems with time constants of $T_1 = 1/k_1$, $T_2 = 1/k_2$, and $T_3 = 1/k_3$, respectively. From the viewpoint of control stability, the time constants should be assigned to be much longer than the compensator time delay and shorter than the desired settling time for the closed loop system inside the SRF-PLL.

Assuming that the settling times of three compensators are in the order of 0.1 seconds, the gains of I-controllers should be selected considering that the harmonic compensator has the longest time delay and the dc-offest compensator has the shortest time delay:

$$\begin{aligned}
&T_3 > T_2 > T_1\\
&T_1 = 80\text{ ms}, \quad T_2 = 60\text{ ms}, \; T_3 = 40\text{ ms}\\
&k_1 = 12.5, \quad k_2 = 16.7, \; k_3 = 25
\end{aligned} \tag{26}$$

V. SIMULATION RESULTS

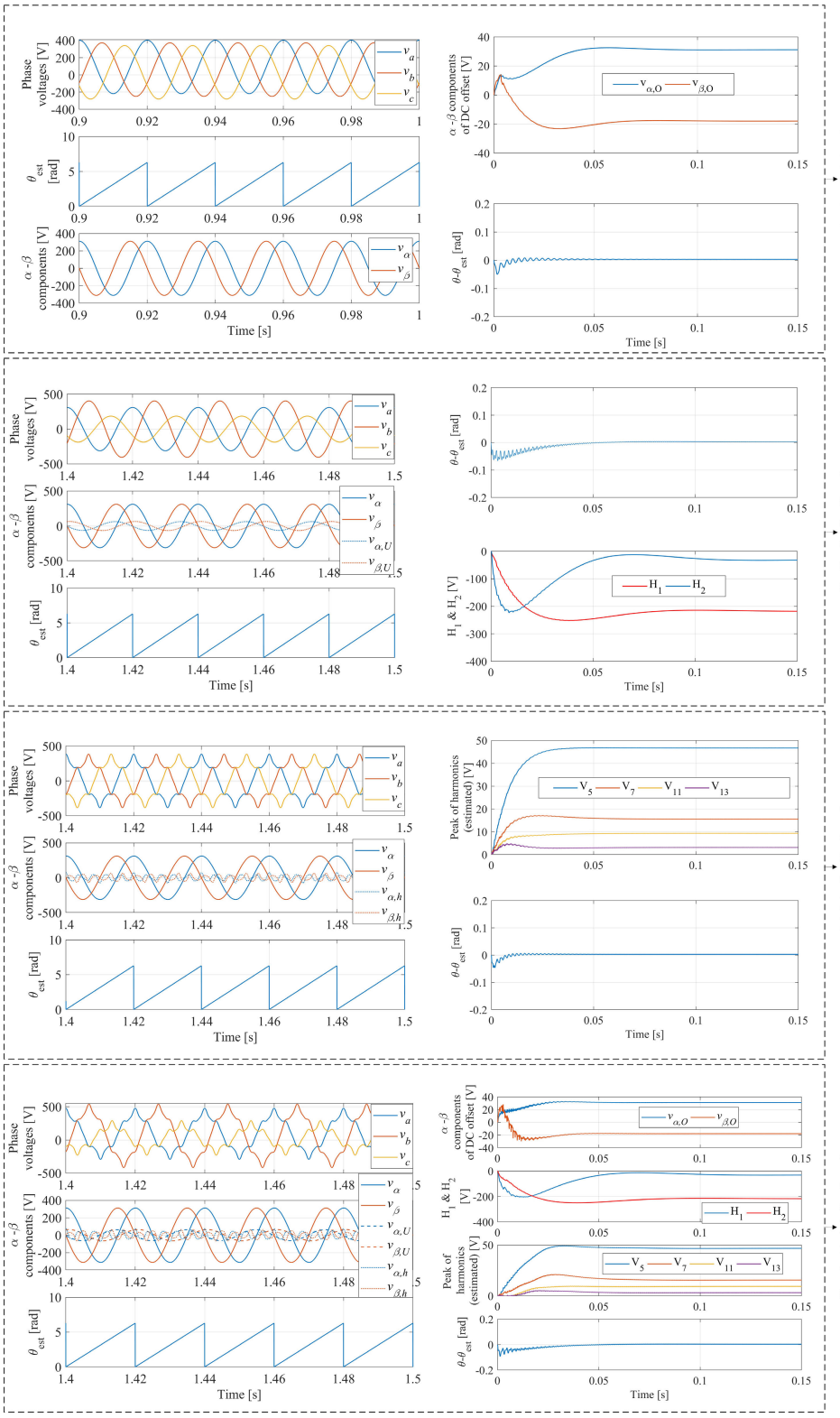
The performance of the proposed PLL is evaluated under several grid disturbances combined with frequency change using numerical simulations. The fourth test combines all the grid disturbances. The nominal grid voltage is 400 V, and the nominal grid frequency is 50 Hz. The grid's frequency is assumed continuously changing within the limits specified by the electricity supply regulations (i.e. ± 2% of nominal grid frequency). The simulation is performed by Matlab/Simulink and the model is sampled at 40 μs. The control gains used for simulation and experiment are given as follows: $k_P = 45.87$, $k_I = 1.27 \times 10^5$, $k_1 = 12.5$, $k_2 = 16.7$, and $k_3 = 25$.

A. TEST 1: DC OFFSET

This test is performed by injecting asymmetrical three phase dc-offsets with $\mu_a = 0.3$, $\mu_b = 0.2$ and $\mu_c = 0.1$ as shown in Fig. 3 (Test 1). It is clear that v_α and v_β are balanced, which means the dc offset compensator continuously generates accurate values of $v_{\alpha,O}$ and $v_{\beta,O}$ to eliminate the dc offset in the PLL loop (remove the ripples) and producing a zero steady state angle error as shown in Fig. 3 (Test 1).

B. TEST 2: AMPLITUDE UNBALANCED CONDITION

This test case is performed with asymmetrical three-phase voltages assuming $\rho = 1.4$ and $\lambda = 0.7$ as shown in Fig. 3 (Test 2). The $\alpha\beta$-axes components are balanced, which



Test 1: Phase voltages, estimated phase angle, the $\alpha\beta$-axes components of phase voltages, the estimated $\alpha\beta$-axes components due to the dc offset, and the phase angle error.

Test 2: Phase voltages, the $\alpha\beta$-axes components, the estimated $\alpha\beta$-axes components due to unbalancing, the estimated phase angle, the phase angle error, and the estimated values of H_1 and H_2.

Test 3: Phase voltages, the estimated $\alpha\beta$-axes components, the estimated α-β-axes components due to harmonics, the estimated phase angle, the estimated peak values of harmonics, and the phase angle error.

Test 4: Phase voltages, the $\alpha\beta$-axes components, the estimated α-β-axes components due to unbalancing and harmonics, the estimated phase angle, the phase angle error and the estimated values of $v_{\alpha,O}$, $v_{\beta,O}$, H_1, H_2, V_5, V_7, V_{13}, and V_{15}

FIGURE 3. Simulation results.

means the compensator is able to produce the required values of $v_{\alpha,U}$ and $v_{\beta,O}$ to eliminate the unbalancing effect in the PLL loop as shown in Fig. 3 (Test 2). The controller keeps compensating accurate values of H_1 and H_2 to eliminate the 2ω frequency component and get a zero steady state phase error as shown in Fig. 3 (Test 3).

C. TEST 3: HARMONICS

This test is performed with a 0.15pu of 5th harmonic, 0.05pu of 7th harmonic, 0.03pu of 11th harmonic, and 0.01pu of 13th harmonic as shown in Fig. 3 (Test 3). The compensator eliminates the harmonic effect in the PLL loop by feeding the loop by the estimated values $v_{\alpha,h}$ and $v_{\beta,h}$ as shown

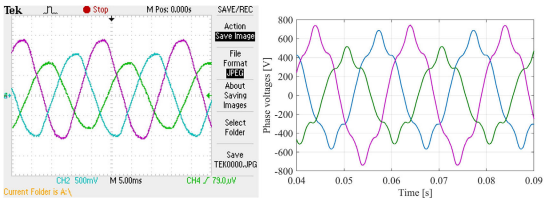


FIGURE 4. Phase voltages.

in Fig. 3 (Test 3). The system is able to estimates continuously the peak value of each harmonic and therefore the phase angle error converged to zero steady state error as shown in Fig. 3 (Test 3), which confirms the robustness of the proposed compensator.

D. TEST 4: ALL DISTURBANCES

In this test, the system is subjected to all previous cases to stress the controller as shown in Fig. 3 (Test 4). The compensator eliminates the effects caused by harmonics and unbalancing in the PLL loop by feeding the loop with the estimated values $v_{\alpha,h}$, $v_{\beta,h}$, $v_{\alpha,U}$ and $v_{\beta,O}$ as shown in Fig. 3 (Test 4). The controller keeps compensating accurate values of $v_{\alpha,O}$ and $v_{\beta,O}$, H_1, H_2, and harmonics to eliminate the low and high frequency components as shown in Fig. 3 (Test 4). The proposed compensation algorithm succeeded to drive the angle error to zero.

VI. EXPERIMENTAL RESULTS

A laboratory prototype is built to verify the validity of the proposed compensation technique. The control loop is implemented on dSPACE 1202 with sampling time equal to 10 μs. The results obtained from experimental test is measured via a 4-Ch Tektronix TDS3054C Digital Oscilloscope through analog output channels of dSPACE. The control algorithm is fed from a variable three-phase AC source with asymmetrical voltages ($\rho = 1.2$ and $\lambda = 0.8$) as shown in Fig. 4. This practical test is performed by injecting a dc offset of 0.15pu to phase-b. The waveform contains a 2.66% of 5th harmonic, 0.78% of 7th harmonic, 0.25% of 11th harmonic, and 0.11% of 13th harmonic. To stress the controller, more harmonics are injected to the waveforms as shown in Fig. 4.

Fig. 5 shows the estimated $\alpha\beta$-axes components due to disturbances, d-axis component of phase voltages, and the estimated phase angle during transient and steady state conditions, respectively. The experimental test elaborates the capability of the compensation technique to adapt the SRF-PLL under various grid conditions. The result also confirms the ability of proposed technique to eliminate the effects caused by harmonics, unbalancing and dc offset in the PLL loop by feeding the loop with the estimated values of the estimated $\alpha\beta$-axes components ($v_{\alpha,0}$ and $v_{\beta,0}$). The control system produces a clean control signals to track the grid's phase angle accurately and achieve a zero steady state phase error between grid and PLL. Fig. 6 shows the simulated results of the estimated and actual $\alpha\beta$-axes components due to disturbances under the same experiment conditions for comparison purposes. The raw data obtained from experimental test is exported from ControlDesk application of dSPACE to Matlab

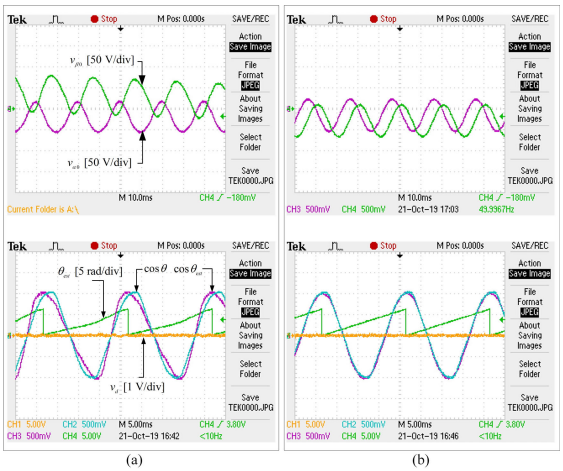


FIGURE 5. Experimental response of the proposed compensation algorithm: transient condition (a) and steady state condition (b).

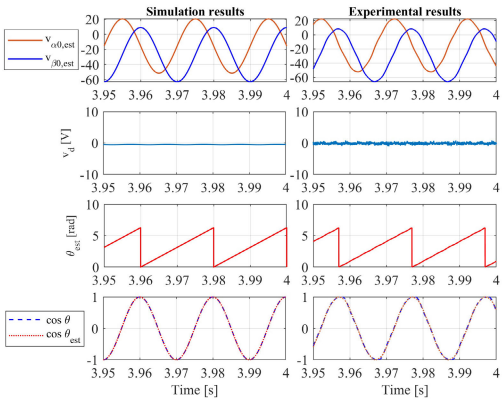


FIGURE 6. Simulation and experimental responses of the proposed compensation algorithm (steady state condition).

environment and then plotted in Fig. 6 to be compared with the simulation results.

VII. CONCLUSION

A new error compensation algorithm for the SRF-PLL of three-phase grid connected converters was proposed. The effects of dc offset, harmonics, and unbalancing were mathematically analyzed based on stationary and synchronous reference frames. The estimated phase angle with the synchronous d-axis and q-axis voltages were directly used for the input signals of the proposed compensator to detect these errors. In the proposed algorithm, the effect of errors are readily estimated in $\alpha\beta$-domain by using integral operations for the synchronous qd-axes voltages according to the estimated phase angle followed by Integral-controllers. The estimated $\alpha\beta$-axes components due to these errors are then compensated in the traditional SRF-PLL to balance the $\alpha\beta$-axes components of the original three-phase voltages. The effectiveness of the proposed algorithm was verified through the several simulation and experimental results under distorted grid conditions. The proposed compensation algorithm succeeded to drive the angle error between the SRF-PLL and the grid to zero.

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