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A Simplified Virtual Vector PWM Algorithm to Balance the Capacitor Voltages of Four-Level Diode-Clamped Converter

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ABSTRACT The voltage balancing problem of dc-link capacitors in multilevel diode-clamped converters limits their applications in industry under some operational conditions. Virtual vector PWM (VVPWM) can attain the capacitor voltage balancing under all operational conditions but it increases the complexity and computation burden by increasing the number of triangular regions for higher levels as compared to conventional space vector PWM (CSVPWM). In order to solve the dc-link voltage balancing problem in four-level diode-clamped converter, a simplified virtual vector PWM (SVVPWM) algorithm is proposed in this paper. The pair of new virtual vectors is defined in such a way that the space vector diagram of four level converter is transformed into three level space vector diagram that lessens the complexity and computation burden by decreasing the number of triangular regions. The balancing of capacitor voltages can be achieved by using proposed SVVPWM algorithm for the whole range of modulation index load power factor. Steady state and dynamic performance of the SVVPWM algorithm is verified through the simulations and experiments.

INDEX TERMS Capacitor voltage balancing, conventional space vector PWM (CSVPWM), diode-clamped converter, simplified virtual vector PWM (SVVPWM).

I. INTRODUCTION

Three-Level diode-clamped converter (3L-DCC) is one of the most commonly used converter topology amid all multilevel converter topologies because of its simple structure, easy control and high power density [1]–[5]. However, it suffers from an inherent problem of capacitor voltage imbalance. The available solutions in literature to control the capacitor voltages of 3L-DCC can be classified into two categories. The first solution is to use an auxiliary hardware circuit that increases the complexity and the cost of the circuit [6]–[8]. The second solution is to modify the modulation algorithm to balance the voltage of dc-link capacitors, which can be further divided into two types: 1) carrier-based PWM (CBPWM) [9]–[14] and 2) space vector PWM (SVPWM) [15]–[20]. CBPWM technique is the simplest in implementation as compared with SVPWM algorithm. By using CBPWM, duty cycles of the switches can be generated directly from the reference voltage vectors. CBPWM technique can be implemented equivalently as SVPWM by injecting the proper amount of zero-sequence voltages to control the neutral point voltage. In case of SVPWM, the capacitor voltages can be balanced by adjusting the application time of redundant switching states according to the deviation in dc-link capacitor voltages. A similar approach known as discontinuous PWM (DPWM) is presented in [21]–[25] to reduce the switching losses by selecting the application time of redundant switching states between 0 and 1. However, aforementioned techniques may cause of generating a low frequency oscillations in neutral point voltage under some operational conditions [26]. The solution of this problem is proposed in [27], [28] by introducing a new virtual vector based PWM (VVPWM) algorithm for three level inverter. The capacitor voltages can be balanced by using VVPWM algorithm for all operational conditions (modulation index and load power factor) by assuring the addition of

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three-phase currents is equal to zero. Reference [29] presents a closed-loop control to boost up the balancing process under perturbations. A carrier-based equivalent PWM method is presented in [30], [31] to reduce the computation burden and simple implementation. VVPWM technique can attain the capacitor voltage balancing of three level inverter for all operational conditions but it faces few problems such as higher switching frequency of the devices that increases the switching losses, higher dv/dt and increase in THD as compared conventional SVPWM (CSVPWM) [32]. Some hybrid PWM techniques have been presented in [32]–[34] to sum up the advantages of SVPWM and VVPWM techniques.

However, it is very hard to balance the capacitor voltages of the inverters with more than three levels. By using conventional modulation algorithms for multilevel converters, the outer capacitors overcharge and inner capacitors discharge completely and the converter behaves like a three level converter. Theoretical limits for four-level diode-clamped converter (4L-DCC) is presented in [35] and an optimal modulation algorithm is proposed to lessen the switching losses. It has been proven that, by using existing modulation algorithms, the voltage balancing of dc-link capacitors cannot be achieved for large modulation index (m>0.55) and higher power factor.

The voltage balancing capability of 4L-DCC can be enhanced by making a back-to-back connections of converters [36]. Another approach to solve the voltage balancing problem of 4L-DCC is presented in [37] by adding an additional hardware balance circuit, which not only make the system more complex but also increases the cost of the circuit. The model-predictive control (MPC) is an another solution proposed in literature to balance the capacitor voltages of 4L-DCC [38]–[40]. The dynamic behavior of MPC is very fast and it is capable of adding nonlinearities and constraints in its cost function to balance the voltages of dc-link capacitors. Moreover, the control signals can be generated directly by the controller without the modulator. However, the main drawbacks of MPC method include inconstant switching frequency, uncertain weighing coefficients and large computations.

To break the limits presented in [35], VVPWM has been extended to four-level and n-level inverters [41], [42]. However, compared to CSVPWM, VVPWM algorithm increases the complexity and computation burden due to rapid increase in triangular regions in each sector for higher level inverters. For example, there are nine triangular regions in each sector of space vector (SV) diagram of 4L-CSVPWM while the SV diagram of 4L-VVPWM has thirteen triangular regions [41]. So, the subsectors identification and the computation of duty ratios have become more complicated by using VVPWM for higher levels of DCCs [43]. Later on, several carrier-based equivalent implementation of VVPWM applicable to any number of levels have been reported in literature [44]–[47]. Phase duty-ratios are obtained with simple mathematical expressions without identifying the location of the reference vector in space vector diagram. These mathematical expressions only depends upon the length and angle of the reference vector. This significantly reduces the computation time with the expense of increase in THD and switching transitions comparing conventional PWM methods.

Although some simplified methods have been discussed in literature [20], [48], [49] to reduce the computation burden by introducing the coordinate transformation for the multilevel SVPWM algorithms such as 60° coordinate system, 120° coordinate system and imaginary coordinate system. But their purpose is only to simplify the calculation burden of multilevel SVPWM algorithms. The final effect is the same as the CSVPWM. So, these method cannot achieve the neutral point voltage balancing of 4L-DCCs under full range of modulation index load power factor.

Another approach based on a novel carrier-overlapped PWM (COPWM) is presented in [50], which assures the voltage balancing of the dc-link capacitors naturally for 4L-DCC by eliminating the dc currents from the neutral points. In order to solve the voltage balancing problem, a simplified virtual vector PWM (SVVPWM) algorithm was proposed in [51] and the performance of the SVVPWM method is validated in this paper through experiments under steady state and dynamic conditions for the whole range of modulation index and load power factor. SVVPWM algorithm can naturally achieve the voltage balancing of bottom and top capacitor in each fundamental cycle and the voltage balancing of middle capacitor in each switching cycle when operating under steady state and ideal conditions. Under transient and non-ideal conditions, the application time of the redundant switching states can be adjusted to balance the voltage of bottom and top capacitors and the duty ratio of the switching signals can be adjusted to balance the voltage of middle capacitor. Moreover, a comparison based on the computation time between CSVPWM and proposed SVVPWM method is presented in this paper to demonstrate the performance of this method. A digital signal controller TMS320F28335 is used to perform the computations that is programmed by C code. The proposed SVVPWM takes significantly less time as compared CSVPWM.

Additionally, by using the SVVPWM algorithm, the transformation of four level space vector diagram to three level space vector diagram simplifies the duty ratio calculations and subsector identification. This method is suitable for any four-level neutral-point clamped (NPC) topologies such as active NPC [52] and π-Type NPC [53] etc. All of them can be equivalent to a single-pole multi-throw switch so they have the same neutral-point voltage balance problem. The diode-clamped topology in this paper is chosen as an example to demonstrate the effectiveness of this method.

The organization of the paper is as follows. The proposed SVVPWM method for 4L-DCC is explained in Section II. Section III presents the balancing method of the dc-link capacitor voltages based on the proposed SVVPWM algorithm in detail under steady state and transient conditions. Section IV and Section V presents the simulation and

experiment results respectively. Finally, Section VI summarizes the conclusions of the paper.

II. PROPOSED SVVPWM ALGORITHM

Fig. 1 shows the schematic diagram of 4L-DCC. There are six equally rated complementary switches (S_{x1}-S_{x3} and S'_{x1}-S'_{x3}) and six diodes in each leg of 4L-DCC. Capacitors C_1-C_3 are dc-link capacitors and the currents i_{N1} and i_{N2} are the neutral point currents that flowing through the N_1 and N_2 respectively. Table 1 shows the relationship between neutral point currents, switching devices and output voltage levels. Suppose that the value of dc-link voltage is 3E, which is equally distributed among the top, middle and bottom capacitors to attain the four voltage levels. i_x represents the three-phase currents i_a, i_b or i_c.

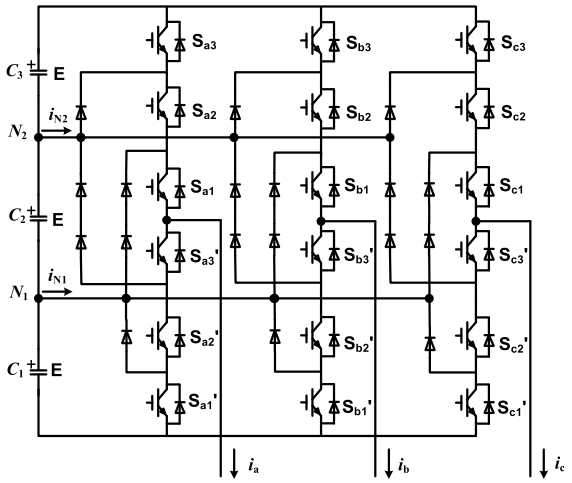

FIGURE 1. Four-level diode clamped converter.

TABLE 1. Switching states of 4L-DCC.

S_{x1}	S_{x2}	S_{x3}	S'_{x1}	S'_{x2}	S'_{x3}	i_{N2}	i_{N1}	Voltage Level
1	1	1	0	0	0	0	0	3E
1	1	0	0	0	1	0	i_x	2E
1	0	0	0	1	1	i_x	0	E
0	0	0	1	1	1	0	0	0

The first sector of the conventional SV diagram of 4L-DCC is shown in Fig. 2. There are ten voltage vectors and nine triangular regions. Each voltage vector is made of one or more switching states depending upon its position in the SV diagram. Fig. 2 also depicts the corresponding neutral point currents i_{N1} and i_{N2} for each switching state. To assure the voltage balancing of dc-link capacitors, the average of these neutral point currents [i_{N1} i_{N2}] should be zero in a certain period. In CSVPWM, for lower modulation indexes (m<0.55), an optimum combination of available redundant switching states can be chosen to make these neutral point current zero but it is not promising for the whole range of load power factors and modulation indexes [35].

To overcome this problem, a new combination of virtual vectors is introduced as shown in Fig. 2 for first sector. This new algorithm is named as a simplified virtual vector PWM (SVVPWM) because it transformed the four level SV diagram to three level SV diagram. The voltage vectors for new virtual SV diagram are defined by

$$\begin{aligned}
V_0 &= (000) = (VVV) = (333) = (0,0)_{\alpha,\beta} \\
V_{S1} &= (V00) = (3VV) \\
&= \frac{1}{2}(100)+\frac{1}{2}(200) = \frac{1}{2}(311)+\frac{1}{2}(322) = \left(\frac{3}{2},0\right)_{\alpha,\beta} \\
V_{S2} &= (VV0) = (33V) \\
&= \frac{1}{2}(110)+\frac{1}{2}(220) = \frac{1}{2}(331) \\
&\quad +\frac{1}{2}(332) = \left(\frac{3}{4},\frac{3\sqrt{3}}{4}\right)_{\alpha,\beta} \\
V_{M1} &= (3V0) = \frac{1}{2}(310)+\frac{1}{2}(320) = \left(\frac{9}{4},\frac{3\sqrt{3}}{4}\right)_{\alpha,\beta} \\
V_{L1} &= (300) = (3,0)_{\alpha,\beta} \\
V_{L2} &= (330) = \left(\frac{3}{2},\frac{3\sqrt{3}}{2}\right)_{\alpha,\beta}
\end{aligned} \tag{1}$$

From (1) it can be seen that virtual vector V_{S1} is obtained by combing two virtual switching states *"V00"* and *"3VV"*. Virtual state "*V00*" is a combination of two adjacent switching states "*100*" and "*200*". Both switching states have different neutral point currents that flowing through the neutral points N_1 and N_2 and cause the unbalancing of the neutral point voltage. So a new virtual switching state is defined by combining these two states that generates the same neutral-point currents i_{N1} and i_{N2}. So these virtual switching state will have no influence on the voltage of the middle dc-link capacitor and the capacitor voltage can be balanced naturally in a carrier cycle. The voltage of the top and bottom capacitors can be balanced by adjusting the application time of the redundant switching states "*V00*" and "*3VV*".

Three nearest virtual vectors in each switching cycle can be used to synthesize the V_{ref} and the on-times of all the virtual vectors can be computed by

$$\left.\begin{aligned} V_{ref}\,T_s &= V_1\,t_1 + V_2\,t_2 + V_3\,t_3 \\ T_s &= t_1 + t_2 + t_3 \end{aligned}\right\} \tag{2}$$

where V_1-V_3 represents the three nearest virtual vectors and t_1-t_3 represents the on-time for the corresponding vectors. The subsector identification is simple as conventional three level SV diagram. Suppose that, the V_{ref} is locating in triangular region 3 as shown in Fig. 2. The duty ratios for the three nearest virtual vectors are:

$$\begin{aligned} d_{V00} &= d_{3VV} = \frac{1}{2}(d_{VS1}) \\ d_{300} &= d_{VL1}, d_{3V0} = d_{VM1} \end{aligned} \tag{3}$$

The switching sequence "*V00-300-3V0-3VV*" of region 3 for three phases is shown in Fig. 3 by using real dc-link

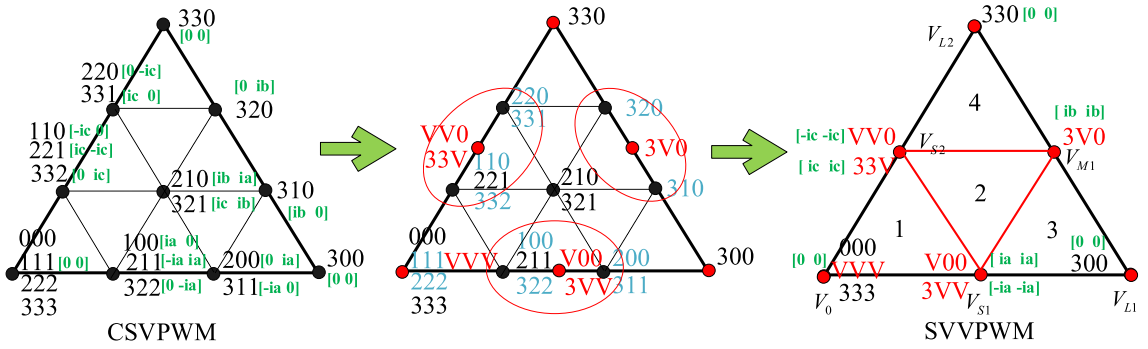

FIGURE 2. Transformation of four level conventional space vector diagram to simplified virtual vector diagram.

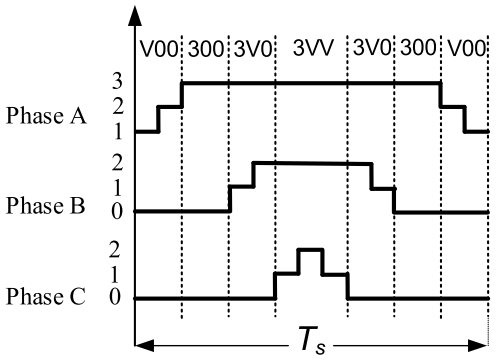

FIGURE 3. Switching sequence for region 3 of the first sector.

connections "1" and "2" instead of using "V" for clear demonstration. The chosen switching states order is such that the sequence of connection of each phase to the dc-link points is the symmetrical. For example, the sequence of connections of phase A is 1-2-3-2-1. The actual switching sequence depends on the duration time of state "V". The ideal sequence for phase B should be 0-(1-2)-(1-2-1)-(2-1)-0, which increases the number of switching transitions. In order to reduce the number of switching transitions, the same voltage levels within a phase are grouped to acquire the simple symmetrical connection 0-1-2-1-0. The average output phase voltage remain unchanged.

III. VOLTAGE BALANCING OF DC-LINK CAPACITORS

Assume that the neutral point currents i_{N1} and i_{N2} are flowing out of the nodes N_1 and N_2 respectively (positive direction) to understand the deviation of capacitor voltages. When the level of output voltage is 2E, the current i_{N2} flows through the node N_2 and causes the discharging of middle capacitor and charging of the top capacitor and when the level of output voltage is E, the current i_{N1} flows through the node N_1 and causes the discharging of the bottom capacitor and charging of middle capacitor. The neutral point currents in terms of capacitor currents can be expressed as:

$$\left.\begin{aligned} i_{N1} &= i_{C2} - i_{C1} \\ i_{N2} &= i_{C3} - i_{C2} \end{aligned}\right\} \tag{4}$$

Suppose that the capacitances of the dc-link capacitors are $C_1 = C_2 = C_3 = C$, the deviation of the capacitor voltages due to neutral point currents in a switching cycle can be expressed as:

$$\left.\begin{aligned} \Delta V_{C1} &= -\frac{2}{3}\cdot\left(\frac{i_{N1}\cdot T_s}{C}\right) - \frac{1}{3}\cdot\left(\frac{i_{N2}\cdot T_s}{C}\right) \\ \Delta V_{C2} &= \frac{1}{3}\cdot\left(\frac{(i_{N1} - i_{N2})\cdot T_s}{C}\right) \\ \Delta V_{C3} &= \frac{1}{3}\cdot\left(\frac{i_{N1}\cdot T_s}{C}\right) + \frac{2}{3}\cdot\left(\frac{i_{N2}\cdot T_s}{C}\right) \end{aligned}\right\} \tag{5}$$

It can be noticed in (5) that the deviation of the middle capacitor voltage is only hinge on the difference between the currents i_{N1} and i_{N2} and the deviation in voltages of the top and bottom capacitors hinge on the addition of the currents i_{N1} and i_{N2}. As shown in Fig. 4, each switching state in new virtual SV diagram has similar neutral point currents i_{N1} and i_{N2} that flows through the node N_1 and N_2. So the difference of these currents will be zero for every switching cycle that certifies the natural balancing of middle capacitor voltage. Similarly, the sum of the neutral point currents will be zero for every fundamental cycle that certifies the natural balancing of top and bottom capacitor voltages which is same as 3L-DCC. For example, when the modulation index is less than 0.5, the reference vector rotates between triangles A1-F1. The sum

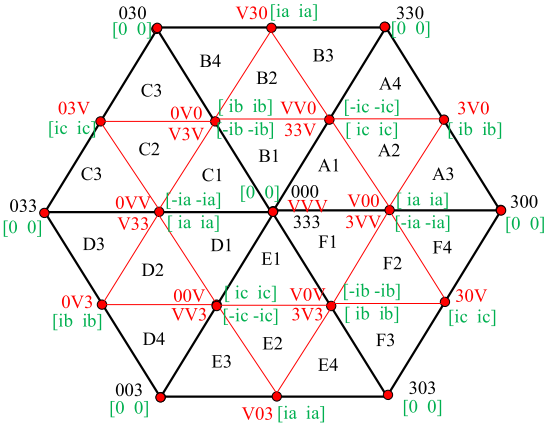

FIGURE 4. Four level simplified virtual vector diagram.

of the i_{N1} and i_{N2} is zero for this fundamental cycle. So, the voltage of the dc-link capacitors can be naturally balanced by using SVVPWM technique under ideal and steady state conditions. However, for non-ideal and transient conditions the capacitor voltages may deviate if a closed-loop control is not used. The balancing of the capacitor voltages can be done in two steps.

A. BALANCING OF THE TOP AND BOTTOM CAPACITOR VOLTAGES

The proposed SVVPWM transforms the four-level SV diagram to three-level SV diagram. So, the voltage balancing process of the top and bottom capacitors becomes similar to three-level NPC converter. The capacitor voltage balancing of three-level NPC converter has been discussed in many papers in literature [16, 32, 54, 55]. The relation between the neutral point currents and voltage ripple caused by the NP currents in top and bottom capacitors can be derived from (5) and expressed as:

$$\Delta V_{C3} - \Delta V_{C1} = V_{C3} - V_{C1} = \frac{(i_{N1}+i_{N2})T_S}{C} = \frac{i_{NP}T_S}{C} \tag{6}$$

which means that the deviation of the top and bottom dc-link capacitor voltages depends on the sum of the two NP currents. In order to eliminate the voltage deviation in the top and bottom DC-link capacitors in a carrier period, according to (6), an average total NP current is expected to be generated. The demanded total NP current can be written as:

$$i_{NP,ref} = \frac{C(V_{C1} - V_{C3})}{T_S} \tag{7}$$

where V_{C1} and V_{C3} are the top and bottom capacitor voltages and C is the capacitance of dc-link capacitors. The average NP current should be zero in each switching cycle to maintain the voltage balancing between top and bottom capacitors. Suppose that the reference vector V_{ref} is locating in region 3 in Fig. 2. The nearest three vectors are V_{S1}, V_{M1}, and V_{L1}. Voltage vector V_{L1} has no influence on the NP current only vector V_{S1} and V_{M1} influence the NP current. The switching sequence (*V00-300-3V0-3VV*) is used to synthesize the reference vector. Small vector V_{S1} is composed of two redundant switching states *"V00"* and *"3VV"*. The switching states "*V00*" and "*3VV*" have similar line to line voltages but opposite neutral point currents that flows through the node N_1 and N_2 as shown in Fig. 4. The non-zero NP current caused by vector V_{M1} can be compensated by adjusting the application time of redundant switching states "*V00*" and "*3VV*". The duty ratio for the states "*V00*" and "*3VV*" can be defined as:

$$\left.\begin{aligned} d_{V00} &= k d_{VS1} \\ d_{3VV} &= (1-k) d_{VS1} \end{aligned}\right\} \tag{8}$$

where d_{VS1} is the duty ratio of the small vector and $k \in [0, 1]$ is sharing factor between two redundant switching states. The calculation of the sharing factor k is similar to 3L-DCC which has been discussed in detail in [32]. Considering the positive direction of phase current ($i_x > 0$), if ($V_{C3} > V_{C1}$) switching state "*3VV*" is used to decrease the top capacitor voltage and increase the bottom capacitor voltage and vice versa for the reverse direction of current. By adjusting the application time of these switching states according to the voltage deviation in top and bottom capacitors, the capacitor voltage can be balanced.

B. BALANCING OF THE MIDDLE CAPACITOR VOLTAGE

The deviation of the middle capacitor voltage is only hinge on the difference between the currents i_{N1} and i_{N2} as shown in (5). The average NP currents of a single phase in a carrier period can be written as follows:

$$\left.\begin{aligned} i_{N1x} &= (d_{x2} - d_{x1}).i_x \\ i_{N2x} &= (d_{x3} - d_{x2}).i_x \end{aligned}\right\} \tag{9}$$

According to (5) and (9), the average current flowing out of the middle dc-link capacitor can be expressed as:

$$i_{C2x} = i_{N1x} - i_{N2x} = (2d_{x2} - d_{x1} - d_{x3}).i_x \tag{10}$$

It means that the voltage of the middle dc-link capacitor can regulate by adjusting the duty ratio (d_{x1}- d_{x3}) of the switching signals for the switches (S_{x1}-S_{x3}) respectively by keeping the sum of the duty ratios unchanged. To understand the voltage balancing process of middle capacitor, consider the switching sequence *"000-V00-VV0-VVV"* of region 1 and switching sequence *"V00-300-3V0-3VV"* of region 3 in Fig. 2 as an example. It can be noticed that in first sequence, phase A is rotating between the connections *"0"* and "*V*" and in second sequence phase A is rotating between connections "*V*" and *"3"*. So, there will be two cases while considering $i_x > 0$ and $V_{C2} < E$ as an example. Where E is the nominal value of the capacitor voltages.

1) when $0 \leq V_{refx} < V$, switch S_{x3} remains off in a carrier cycle. So the duty ratio d_{x3} is always zero. The duty ratio d_{x2} of switching signal for S_{x2} can be decreased by a factor Δdx and the duty ratio d_{x1} of switching signal for S_{x1} can be increased by a factor Δdx to charge the middle capacitor as shown in Fig. 5 (a).

2) when $V \leq V_{refx} \leq 3$, duty ratio of the switching signal for S_{x1} is always 1. The duty ratio d_{x2} of switching signal for S_{x2} can be decreased by a factor Δdx and the duty ratio d_{x3} of switching signal for S_{x3} can be increased by a factor Δdx to charge the middle capacitor as shown in Fig. 5 (b).

The value of factor Δdx is a small value that is limited to 10% of the duty ratios of the switches (S_{x1}-S_{x3}). The duty ratio adjustment of the switches is summarized in Table 2 for $V_{C2} < E$. By this way, the middle capacitor can be charged in each switching period without effecting the average output voltage.

A proportional-integral (PI) regulator is used to obtain the factor Δdx which must saturate to ensure d_{x1}, d_{x2} and d_{x3} no larger than 1 or no less than 0 as shown in Fig. 6. However, the value of the factor Δdx is different for all the three phases but only one PI regulator is required to calculate Δdx. After adjusting the duty ratios (d_{x1} - d_{x3}) of the switching signals for the switches (S_{x1}-S_{x3}) to control the voltage of middle dc-link capacitor, the new duty ratios cam be defined as

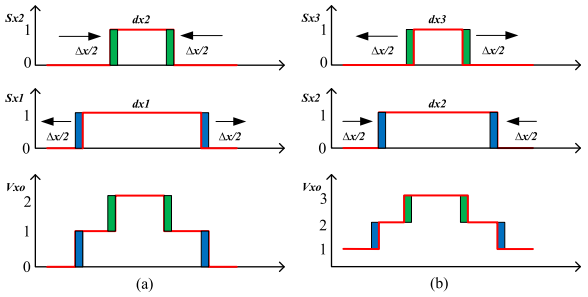

FIGURE 5. Voltage balancing of middle dc-link capacitor: (a) 0 ≤ Vrefx < V, (b) V ≤ Vrefx ≤ 3.

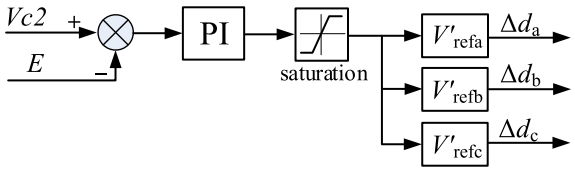

FIGURE 6. The diagram of obtaining the factor Δdx.

TABLE 2. Duty ratio adjustment of the switches for $V_{C2} < E$.

V_{refx}	i_x	d_{x3}	d_{x2}	d_{x1}
$0 < V_{refx} < V$	$i_x > 0$	0	$-\Delta_{dx}$	$+\Delta_{dx}$
	$i_x < 0$	0	$+\Delta_{dx}$	$-\Delta_{dx}$
$V < V_{refx} < 3$	$i_x > 0$	$+\Delta_{dx}$	$-\Delta_{dx}$	0
	$i_x < 0$	$-\Delta_{dx}$	$+\Delta_{dx}$	0

$d_{x1} + d'_{x1}$, $d_{x2} + d'_{x2}$ and $d_{x3} + d'_{x3}$ respectively. The voltage of the middle capacitor can be well balanced by using this method under transient conditions.

IV. SIMULATION RESULTS

MATLAB/Simulink is used to perform the simulations to validate the proposed SVVPWM algorithm. The parameters used in simulations of 4L-DCC by using the proposed modulation algorithm are given in Table 3.

TABLE 3. Parameters used for simulations.

Parameters	Value
DC-link Voltage	Udc=600V
DC-link Capacitors	C_1=C_2=C_3= 1410μF
Switching frequency	5kHz
R-L load	R=22 ohm, L=1mH

The performance of 4L-DCC is shown in Fig. 7 by using SVVPWM algorithm through capacitor voltages, three-phase currents, line voltage and phase voltage under modulation index m = 0.95. It can be seen that the voltages of dc-link capacitors are totally balanced at 200V under this condition of higher power factor and large modulation index. The detailed waveform of line and phase voltages is shown in Fig. 8. It can be observed that there are four levels in the phase voltage

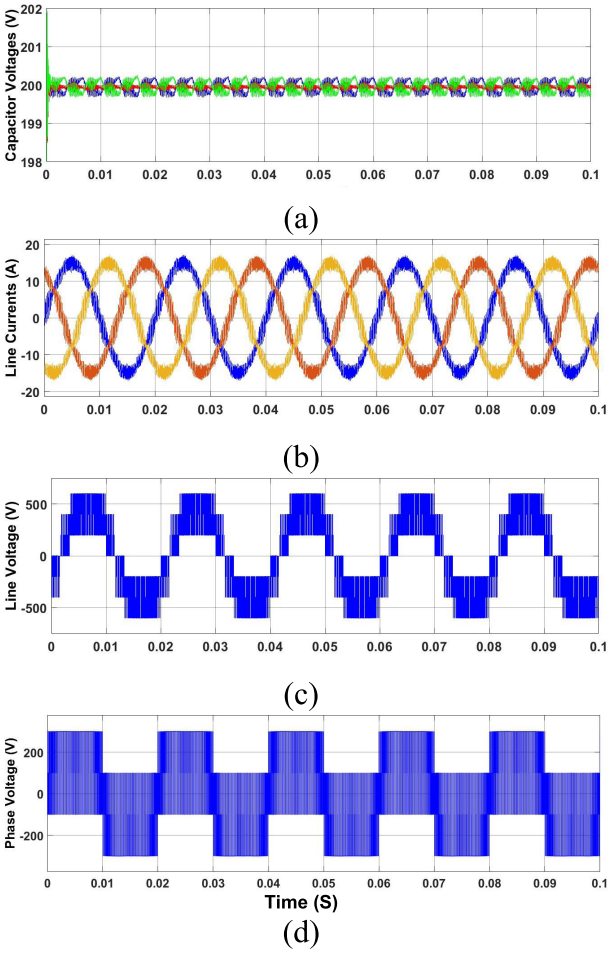

FIGURE 7. Simulation results for m = 0.95: (a) capacitor voltage, (b) three-phase currents, (c) line voltage, (d) phase voltage.

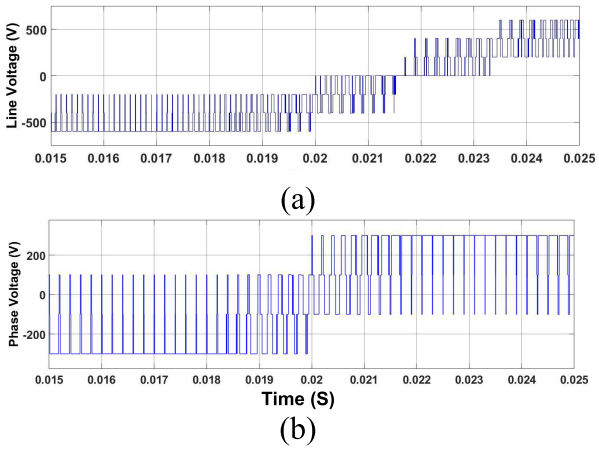

FIGURE 8. Detailed waveform for m = 0.95: (a) line voltage, (b) phase voltage.

and seven levels in the line voltages. The performance of the 4L-DCC is shown in Fig. 9 and Fig. 10 with same power factor under lower modulation index m = 0.4. It can be seen in detailed waveform of phase and line voltages that there are four levels in phase voltage while due to the lower modulation

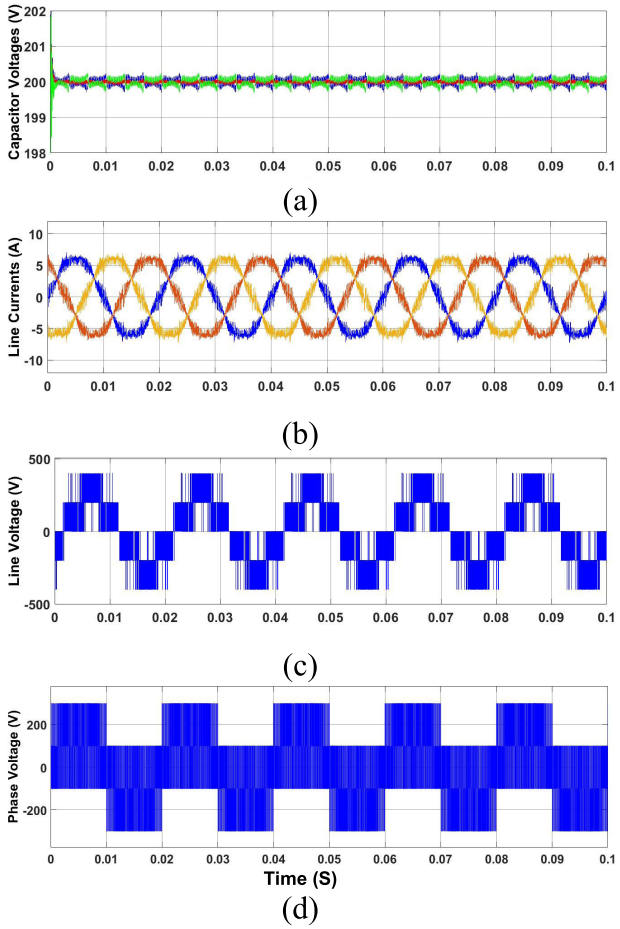

FIGURE 9. Simulation results for m = 0.4: (a) capacitor voltage, (b) three-phase currents, (c) line voltage, (d) phase voltage.

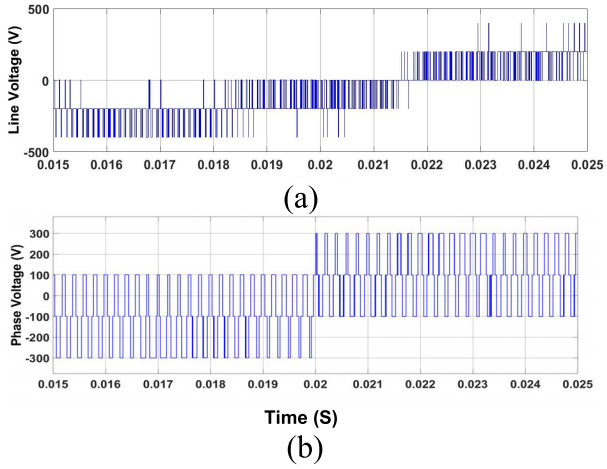

FIGURE 10. Detailed waveform for m = 0.4: (a) line voltage, (b) phase voltage.

index the levels of line voltage are decreased to five levels. The voltages of dc-link capacitors remain well balanced for the whole range of modulation index.

Fig. 11 shows the harmonic spectrums of phase current, line voltage and phase voltage with modulation index

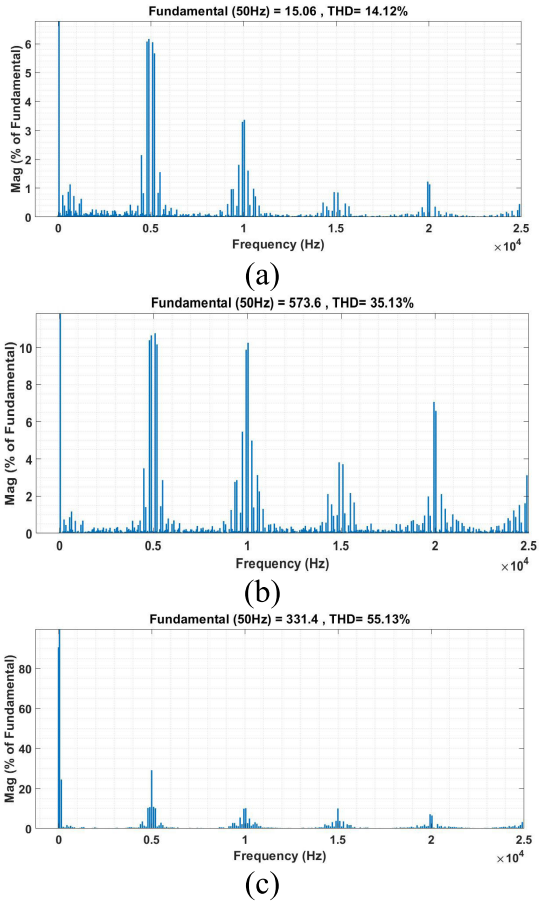

FIGURE 11. Harmonic spectrums for m = 0.95: (a) phase current, (b) line voltage, (c) phase voltage.

m = 0.95. The total harmonic distortions (THDs) of phase current, line voltage and phase voltage is 14.12%, 35.13% and 55.13% respectively. As shown in Fig. 11, the harmonics are around the switching frequency and multiple of the switching frequency. So these harmonics can be filtered out easily.

To authenticate the effectiveness of the proposed algorithm, the simulations are performed under the dynamic conditions by changing the reference value of the capacitor voltages. As shown in Fig. 12, the voltage of all three capacitors are fully controlled at the reference value when $t < 0.3$s. At $t = 0.3$s, the voltages of the top and bottom capacitors are step changed to 10% lower and 10% higher than the reference value respectively. It can be observed that the voltage of the top capacitor are gradually decreased and stabilized at new given value and the voltage of bottom capacitor are increased to new reference value while the voltage of the middle capacitor remains balanced. At $t = 0.6$s, the voltage of the top and bottom capacitor are step changed to their original values.

A similar phenomena is applied to the middle dc-link capacitor. The value of the middle capacitor voltage is step changed to 10% lower than the reference values at $t = 0.3$s. The voltage of the middle capacitor is decreased to new

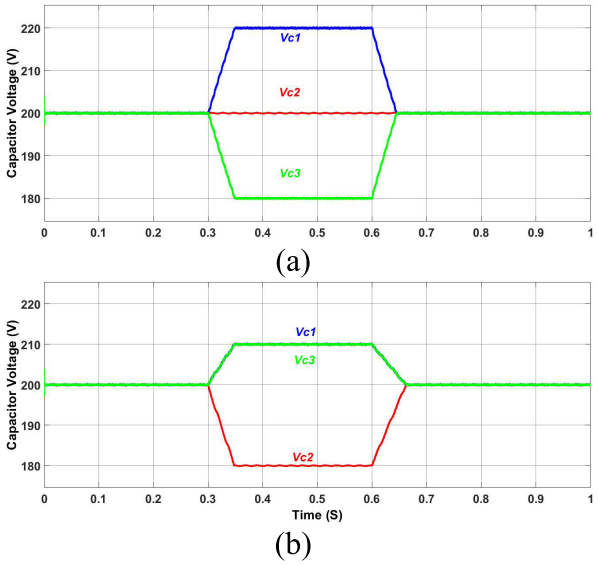

FIGURE 12. Dynamic simulation performance of SVVPWM by step change in reference voltage of: (a) top and bottom capacitor, (b) middle capacitor.

reference value while the voltages of the top and bottom capacitor are fully balanced during this process. At $t = 0.6$s, the value of middle capacitor voltage is set back to its original value.

To further demonstrate the dynamic performance of the proposed algorithm, Fig. 13 shows the simulation results by making a step change in modulation index. When time $t < 0.3$s, inverter is operating at modulation index m = 0.3. At $t = 0.3$s, modulation index is changed from 0.3 to 0.6 and then at $t = 0.35$s, modulation index is changed from 0.6 to 0.9. It can be seen that the capacitor voltages are completely balanced for the whole range of modulation index and the levels in line voltage are changing accordingly.

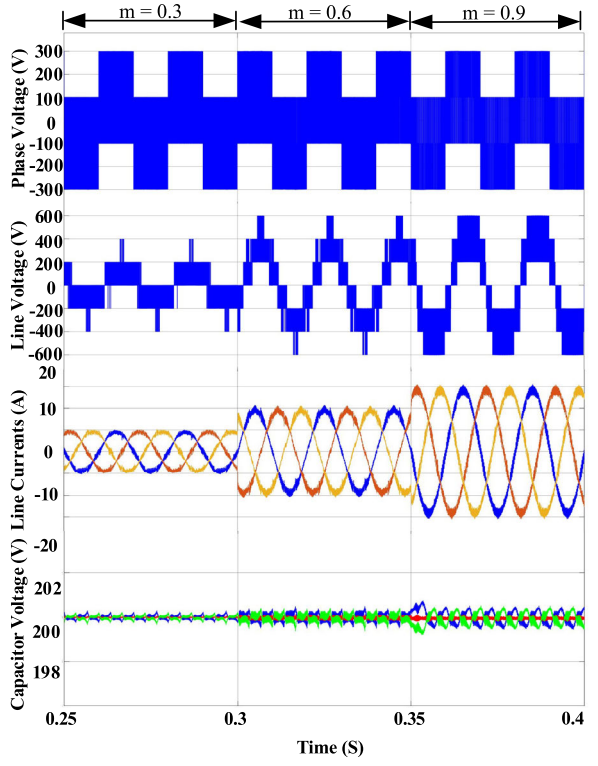

FIGURE 13. Dynamic simulation performance of SVVPWM by step change in modulation index.

In order to demonstrate the performance of proposed algorithm, a simulation based comparison of line voltage THD, switching transitions and computation time has been performed between SVVPWM, carrier-based VVPWM and COPWM for 4L-DCC. Fig. 14 shows the total number of switching transitions of COPWM, carrier-based VVPWM and SVVPWM for m = 0.9. It can be seen that the switching transitions of COPWM, carrier-based VVPWM and SVVPWM are 8,540, 11,700 and 10,000 respectively for 1s time period. The number of switching transitions of SVVPWM is lower than VVPWM and higher than COPWM. Fig. 15 shows the harmonics performance of line voltage for aforementioned three modulation methods. The harmonics performance of SVVPWM is almost similar to COPWM and higher than VVPWM for higher modulation index. The computation time of 50 line cycles is calculated in a personal computer with an Intel core i5 processor at 2.6GHz and 4GB RAM by using MATLAB 9.4. The computation time of SVVPWM, carrier-based VVPWM and COPWM is 38.7s, 11.4s and 9.5s respectively, which depends on simulation environment. The computation time of SVVPWM is larger than carrier-based VVPWM because the phase duty-ratios of VVPWM are obtained with simple mathematical expressions without identifying the location of the reference vector in space vector diagram. These mathematical expressions only depends upon the length and angle of the reference vector. This significantly reduces the computation time with the expense of increase in THD and switching transitions.

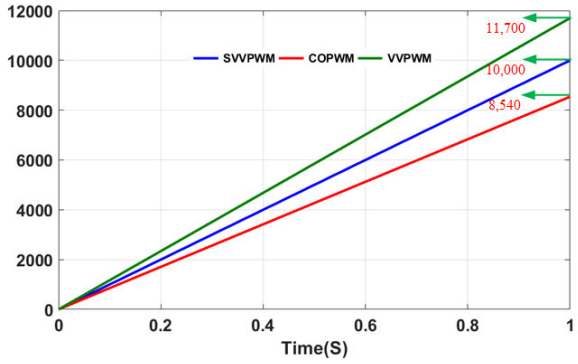

FIGURE 14. The number of switching transitions of COPWM, VVPWM and SVVPWM.

V. EXPERIMENTAL RESULTS

The feasibility of the proposed modulation algorithm has been validated through the experiments also by developing a low power prototype of three-phase 4L-DCC as shown in Fig. 16. The main control board consists of FPGA of Altera

TABLE 4. Parameters used for experiments.

Parameters	Value
DC-link Voltage	Udc=200V
DC-link Capacitors	C_1=C_2=C_3= 1410μF
Switching frequency	5kHz
R-L load	R=22 ohm, L=2mH

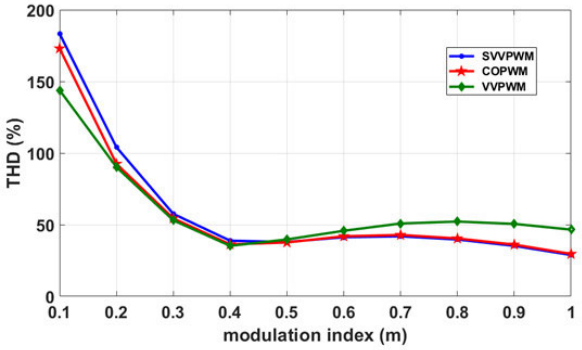

FIGURE 15. The comparison of the harmonic performances of different modulation methods.

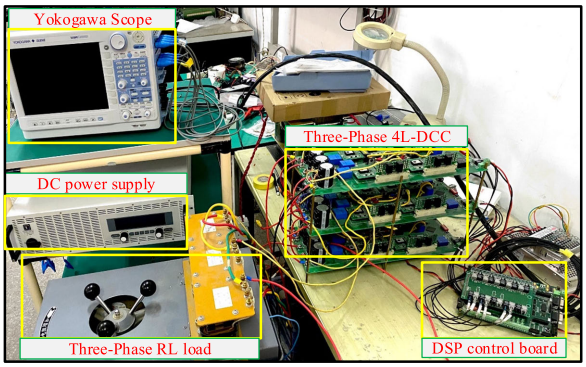

FIGURE 16. Experimental setup for 4L-DCC.

MAX 10 series and a DSP chip TMS320F28335. DSP chip is used to calculate three phase reference signals and to execute the voltage balancing algorithm. CPLD EPM1270T144C5 is used to generate the carriers and PWM signals are produced by comparing the carrier with reference signals. The circuit parameters used to analyze the performance of 4L-DCC using proposed algorithm are illustrated in Table 4. Fig. 17 and Fig. 18 show the experiment results under steady-state conditions for capacitor voltages, three phase currents, line voltage and phase voltage with modulation index m = 0.9 and m = 0.4 for higher power factor PF = 0.999 and lower power factor PF = 0.268 respectively. It can be seen that the voltage of the three dc-link capacitors are totally balanced for the whole range of modulation indexes and power factors that is not possible by using CSVPWM [35]. Fig. 19 shows the detailed waveform of the line and phase voltages. It can be observed that there are seven levels in the line voltages and four levels in the phase voltage similar to simulation results.

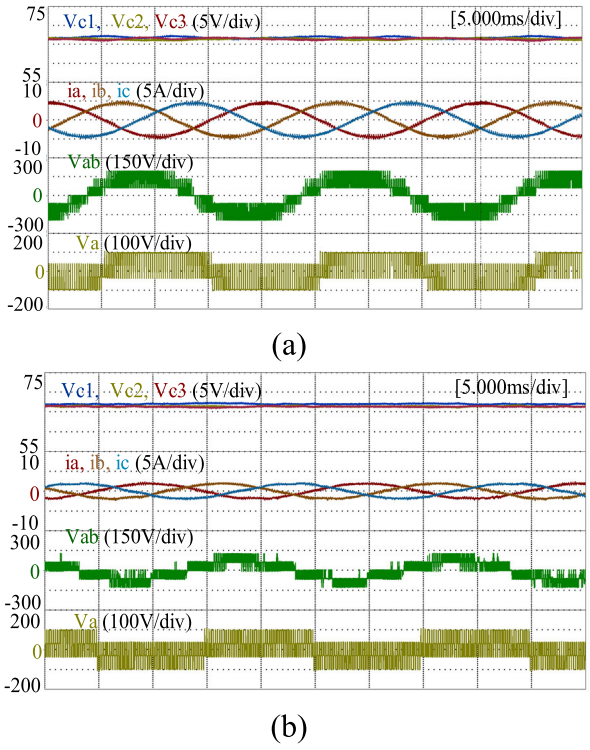

FIGURE 17. Steady state experimental results under higher power factor PF = 0.999 for: (a) m = 0.9, (b) m = 0.4.

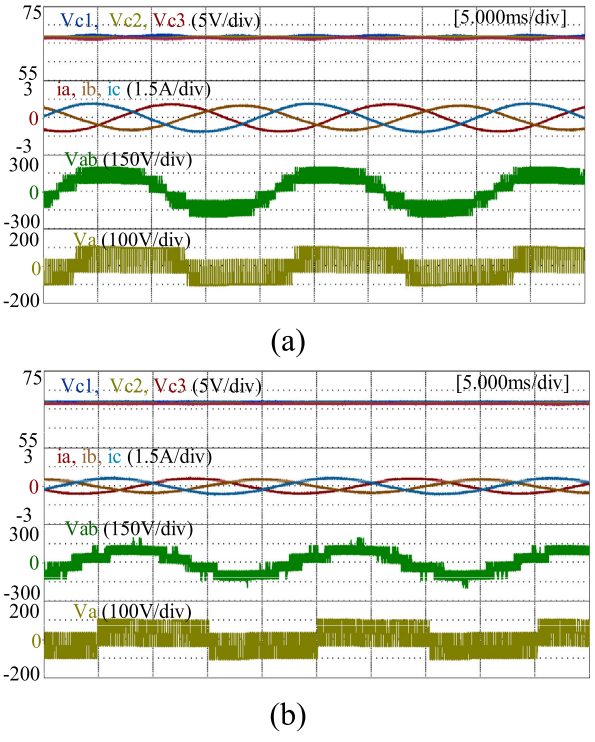

FIGURE 18. Steady state experimental results under lower power factor PF = 0.268 for: (a) m = 0.9, (b) m = 0.4.

To authenticate the effectiveness of the proposed algorithm, the experiments are performed under the dynamic conditions by changing the reference value of the capacitor

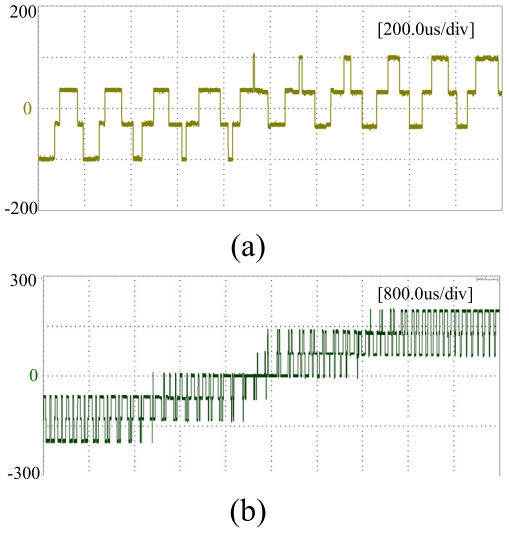

FIGURE 19. Detailed waveform under m = 0.9: (a) phase voltage, (b) line voltage.

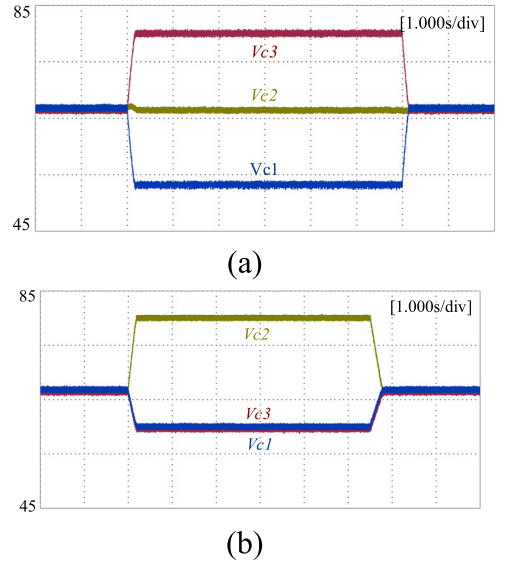

FIGURE 20. Dynamic experimental performance of SVVPWM by step change in reference voltage of: (a) top and bottom capacitors, (b) middle capacitor.

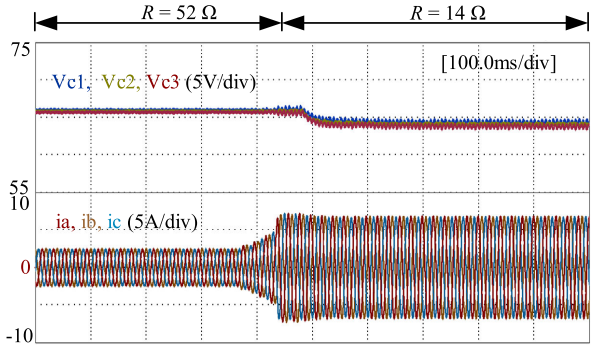

FIGURE 21. Dynamic experimental result under sudden change in load.

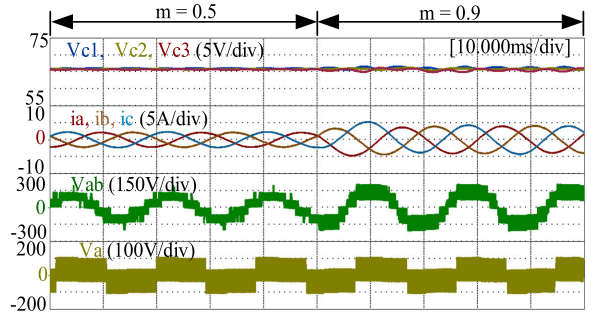

FIGURE 22. Dynamic performance of SVVPWM under pure inductive load by making a step change in modulation index.

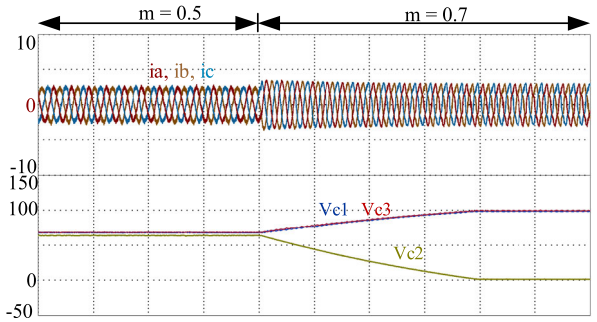

FIGURE 23. Dynamic experimental performance of CSVPWM by step change in modulation index.

voltages. As shown in Fig. 20, the voltage of all three capacitors are fully controlled at the reference value when $t < 2$s. At $t = 2$s, the voltages of the bottom and top capacitors are step changed to 20% lower and 20% higher than the reference value respectively. The voltage of the top capacitor are gradually increased and stabilized at new given value and the voltage of bottom capacitor are decreased to new reference value while the voltage of the middle capacitor remains balanced. At $t = 8$s, the voltage of the top and bottom capacitor are step changed to their original values. A similar phenomena is applied to the middle dc-link capacitor. The value of the middle capacitor voltage is step changed to 20% higher than the reference values at $t = 2$s. The voltage of the middle capacitor is increased to new reference value while the voltages of the top and bottom capacitor are fully balanced during this process. At $t = 7.5$s, the value of middle capacitor voltage is set back to its original value. Fig. 21 shows the voltage balancing performance of SVVPWM with m = 1.0 when the load resistance is suddenly changed from light load to full load. Although there exists a small voltage drift due to the dynamic load change, the three dc-link capacitor voltages remain balanced during the whole process. To prove the voltage balancing ability of the proposed modulation algorithm for pure inductive load, the experiments are also performed under dynamic conditions by making a step change in modulation index from m = 0.5 to m = 0.9 as shown in Fig. 22. It can be seen that the capacitor voltages are completely balanced for the whole range of modulation index. This demonstrates the effectiveness of proposed SVVPWM algorithm under pure inductive load.

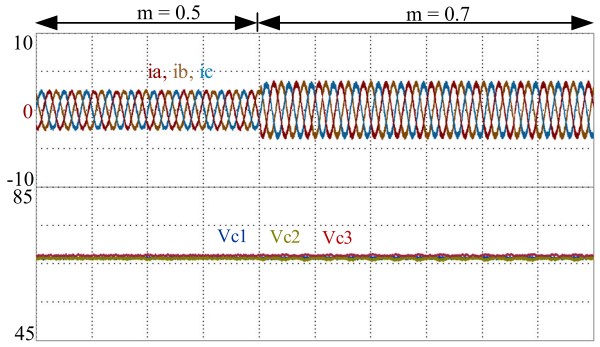

FIGURE 24. Dynamic experimental performance of SVVPWM by step change in modulation index.

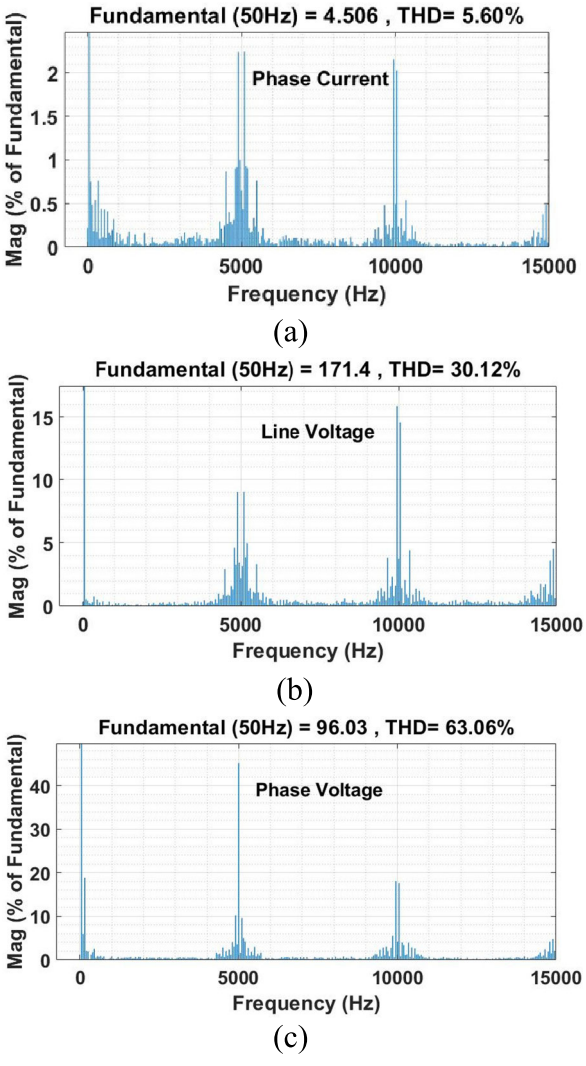

FIGURE 25. Harmonic spectrums for m = 0.9: (a) phase current, (b) line voltage, (c) phase voltage.

The dynamic experimental results for CSVPWM and SVVPWM are also added and compared by making a step change in modulation index. When the modulation index is changed from 0.5 to 0.7, the neutral point voltages lost balance quickly under CSVPWM as shown in Fig. 23, while

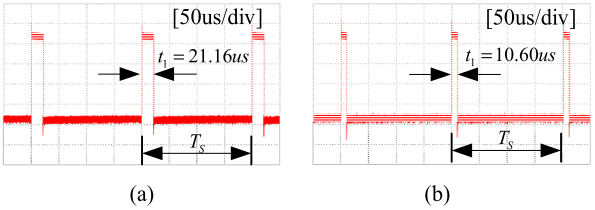

FIGURE 26. The experimental computation time of: (a) CSVPWM, (b) SVVPWM.

remain balanced under SVVPWM as shown in Fig. 24 which demonstrate the effectiveness of proposed SVVPWM algorithm. Fig. 25 shows the harmonic spectrums of phase current, line voltage and phase voltage with modulation index m =0.9. The total harmonic distortions (THDs) of phase current, line voltage and phase voltage is 5.60%, 30.12% and 63.06% respectively. As shown in Fig. 25, the harmonics are around the switching frequency and multiple of the switching frequency. So these harmonics can be filtered out easily.

The performance of the proposed algorithm is also verified by comparing the computation time of SVVPWM technique with CSVPWM technique for 4L-DCC. A digital signal controller TMS320F28335 is used to perform the computations that is programmed by C code. The calculation time is obtained by setting a GPIO pin high at the beginning of the algorithm and low at the end of the algorithm. The calculation time for CSVPWM and SVVPWM is shown in Fig. 26. T_S is the sampling time and t_1 is the time required for the calculations. The computation time for the CSVPWM is 21.16us and the computation time for SVVPWM is 10.60us. The proposed SVVPWM takes significantly less time as compared CSVPWM. The experiment results under steady state and dynamic conditions are validating the proposed SVVPWM algorithm.

VI. CONCLUSION

In order to solve the voltage balancing problem of 4L-DCC, a simplified virtual vector PWM (SVVPWM) algorithm is proposed in this paper. SVVPWM algorithm can naturally achieve the voltage balancing of bottom and top capacitor in each fundamental cycle and the voltage balancing of middle capacitor in each switching cycle when operating under steady state and ideal conditions. Under transient and non-ideal conditions, the application time of the redundant switching states can be adjusted to balance the voltage of bottom and top capacitors and the duty ratio of the switching signals can be adjusted to balance the voltage of middle capacitor. Additionally, by using the SVVPWM algorithm, the transformation of four level space vector diagram to three level space vector diagram simplifies the duty ratio calculations and subsector identification. The simulation and experiment results proves the validity of the proposed modulation algorithm for the whole range of power factor and modulation index. This method is suitable for any four-level neutral-point clamped (NPC) topologies such as active NPC and π-Type

NPC converters and can be extended further for higher level NPC converters.

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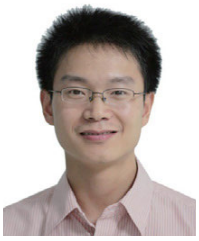

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