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Ka-band Calibration-Free High Image-Rejection Up/Down Mixers With 117% Fractional IF Bandwidth for SATCOM Applications

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ABSTRACT This paper presents two Ka-band calibration-free up/down mixers, each with high image rejection ratio (IRR) for a wide band of IF frequencies covering the satellite modem frequency range (0.95-2.15 GHz). To achieve broadband IRR $>$ 30 dBc, a 3-stage castle-wall polyphase filter (PPF) is used at the IF port to minimize the amplitude and phase errors (AM $<\pm$0.2 dB, PM $<\pm1^\circ$). For local oscillator (LO) quadrature generation, a four-way quadrature divider composed of two broadside 90° couplers and one Marchand balun is used. The single-sideband (SSB) up mixer shows a 4.2-dB conversion gain (CG) with LO power of 4 dBm and an output 1-dB gain compression (OP_{1dB}) of -4.3 dBm. The image-rejection (IR) down mixer achieves a -11.6-dB CG under LO power of 5.5 dBm and an input 1-dB gain compression (IP_{1dB}) of 0 dBm. With a 1.2-V supply voltage, the SSB up mixer and IR down mixer consume 15.6 mW and 12 mW, respectively. The SSB up mixer and IR down mixer demonstrate broad IRR bandwidths at the IF frequencies (IRR $>$ 30 dBc) from 0.6 to 4 GHz (148% fractional IF bandwidth) and from 0.65 to 2.5 GHz (117%), respectively, with no calibration. In addition, the RF bandwidths (IRR $>$ 30 dBc) of the SSB up mixer is 27.7-33.3 GHz (18.36% fractional RF bandwidth), and the IR down mixer is 17.1-20.6 GHz (18.5%). The IRR performances are robust against process, voltage, and temperature (PVT) variations and Monte Carlo simulations for satellite communication (SATCOM) applications.

INDEX TERMS CMOS, image-rejection mixer, polyphase filter (PPF), single-sideband mixer.

I. INTRODUCTION

In the past, the C- and Ku-band transceivers are widely utilized for satellite applications. Since the demand of broadband high-speed transmission, such as 8K UHD video streaming, is significantly increased, the Ka-band is a good candidate for next-generation high throughput satellite (HTS). In Fig. 1(a), the desired RF frequencies in our Ka-band satellite system are 28-30 GHz for uplink and 18.2-20.2 GHz for downlink [1]. To achieve good signal quality in satellite communication, the rejection of the image signal is essential. Therefore, a single-sideband (SSB) up mixer and an image-rejection (IR) down mixer are selected for frequency translation with image rejection function, as illustrated in Fig. 1(b) and (c). The image rejection ratio (IRR) is defined as the ratio of the average power of the desired signal to the average power of the image signal. Having the IRR be above 30 dBc is enough to provide an acceptable system performance [2]. Thus, the IRR bandwidths can be specified for IRR above 30 dBc. At the IF port, the commercial modems are utilized in satellite systems for modulation and demodulation. The frequency range of various commercial modems is from 0.95 to 2.25 GHz [3]–[11] and we select the typical frequency, 0.95-2.15GHz [9], as our design target in Fig. 1(a).

The double quadrature configuration is insensitive to amplitude and phase imbalance in quadrature generation [12], which has been successfully implemented around 5 GHz [13]–[15]. At K-band [16], Ka-band [17], V-band [18] and

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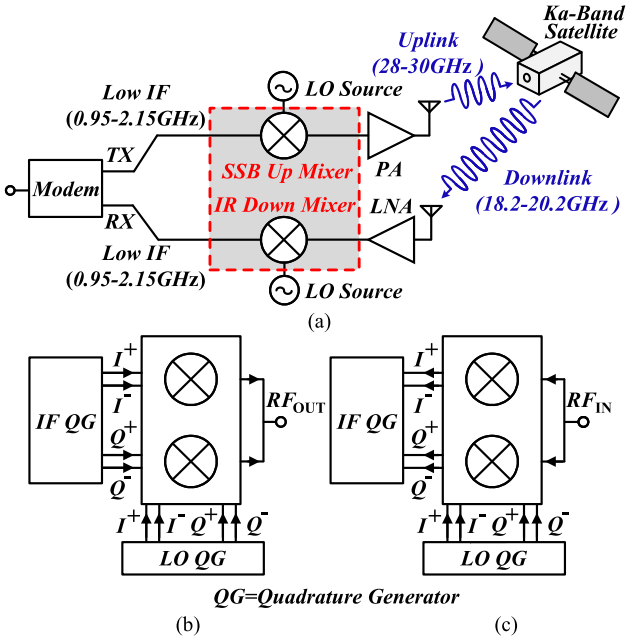

FIGURE 1. (a) Block diagram of our Ka-band satellite system. (b) SSB up mixer and (c) IR down mixer in our Ka-band satellite system.

E-band [19], the single quadrature configuration is more popular due to low complexity. The quadrature signal can be generated by using a polyphase filter (PPF) or couplers [20]. The loss of multi-stage PPFs at 16 GHz in [20] and [21] results in needing a high local oscillator (LO) power of around 12 dBm. On the contrary, at V-band [22] and E-band [19], couplers are utilized at the LO port to generate quadrature signal, which require lower LO power [19], [22]. However, for IF quadrature generation below 3 GHz, couplers are difficult to be integrated into CMOS RFICs due to its size constraint. On the other hand, a PPF at the IF port is suitable for CMOS implementation, especially in a compact area. An accurate quadrature generation is critical for good IRR performance. A calibration mechanism is introduced in [23] to obtain wideband image rejection. Nevertheless, it requires additional power consumption and higher complexity.

This paper presents a Ka-band calibration-free single-quadrature SSB up mixer and an IR down mixer with wide IRR bandwidths at the IF frequencies. In these two mixer designs, the PPFs and the broadside 90° couplers with Marchand baluns are utilized at IF and LO ports for quadrature generation, respectively. These arrangements at the two ports enhance the IRR bandwidths at the IF frequencies and also provide tolerance to process variations and mismatch. To cover the wide operating frequencies of the satellite modem (0.95-2.15 GHz), a 3-stage PPF with castle-wall structure is adopted to minimize the amplitude and phase errors. The quadrature generation is designed at the LO port rather than the RF port to tolerate the process variations and mismatch. For LO quadrature generation, the four-way quadrature divider, including two broadside 90° couplers and one Marchand balun, is utilized. These couplers are selected to have lower LO drive power compared with the PPF. The Marchand balun is also added to provide a differential quadrature signal. Fig. 2 shows the comparison of IRR bandwidths at IF frequencies of published papers [16], [18], [21], [24]–[28]. The proposed SSB up mixer and IR down mixer demonstrate wide IRR bandwidths at the IF frequencies from 0.6 to 4 GHz (148% fractional IF bandwidth) and from 0.65 to 2.5 GHz (117%), respectively. Also, both proposed mixers attain IRR bandwidths for RF frequencies of 27.7-33.3 GHz (18.36% fractional RF bandwidth) and 17.1-20.6 GHz (18.5%), respectively.

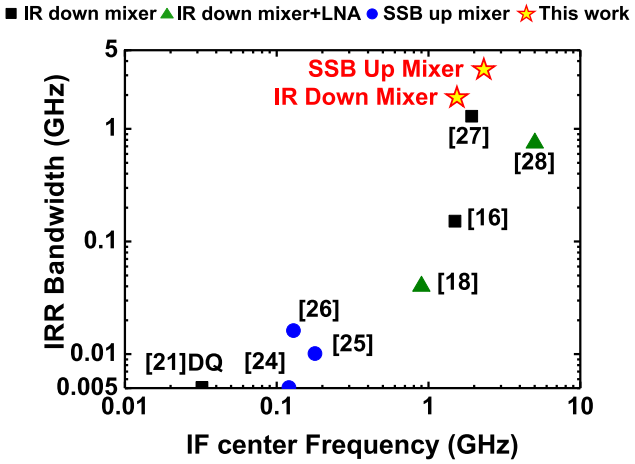

FIGURE 2. Comparison of IRR bandwidths (IRR > 30dBc) at IF frequencies (DQ: double quadrature).

II. PPF DESIGN

The IRR formula derived in [2] only considers the amplitude and phase errors at the LO port and assumes perfect IF amplitude and phase balance, as shown in Fig. 3(a). The effect of both IF and LO errors on IRR performance can be derived from the model shown in Fig. 3(b), where the amplitude/phase errors at IF and LO ports are denoted as α/θ and ε/ϕ, respectively. The imbalanced IF and LO signals can be expressed as

$$IF\_I = (1+\alpha)A_{IF}\cos(\omega_{IF}t+\theta) \tag{1}$$

$$IF\_Q = A_{IF}\sin(\omega_{IF}t) \tag{2}$$

$$LO\_I = (1+\varepsilon)A_{LO}\cos(\omega_{LO}t+\phi) \tag{3}$$

$$LO\_Q = A_{LO}\cos(\omega_{LO}t+90^\circ) \tag{4}$$

The IRR, defined as the average power ratio of desired signal to image signal, can be derived as

$$IRR = \frac{P_{\text{desired}}}{P_{\text{image}}} = 10\log\left[\frac{(1+\varepsilon)^2(1+\alpha)^2+2(1+\varepsilon)(1+\alpha)\cos(\phi+\theta)+1}{(1+\varepsilon)^2(1+\alpha)^2-2(1+\varepsilon)(1+\alpha)\cos(\phi-\theta)+1}\right] \tag{5}$$

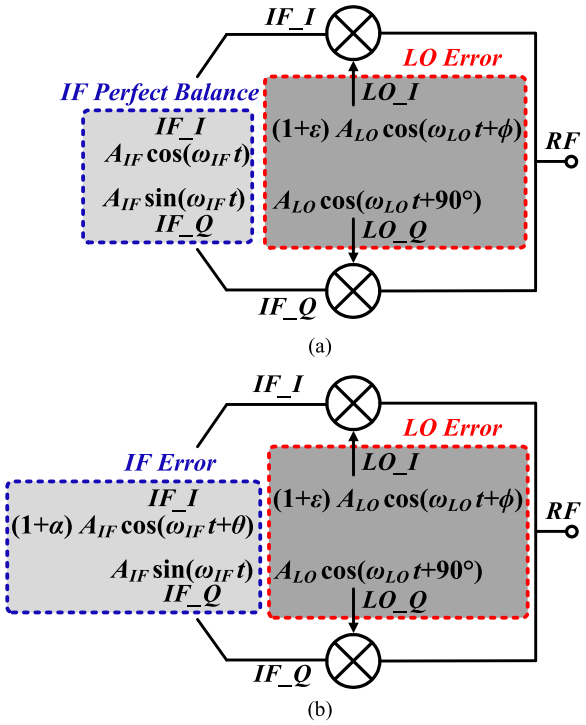

FIGURE 3. (a) Quadrature mixing only with LO error. (b) Quadrature mixing with LO and IF errors.

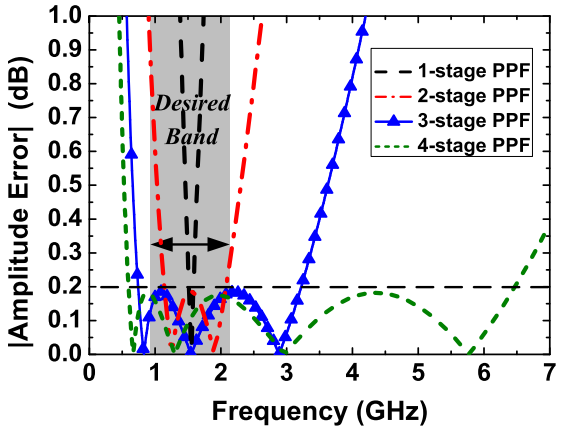

FIGURE 4. Simulated amplitude error of ideal 1∼4-stage PPFs.

According to (5), not only LO imbalance but also IF imbalance is critical to IRR performance. Therefore, the IF quadrature generation should be carefully designed. The PPF can be utilized in the SSB up mixer and IR down mixer to generate a quadrature IF signal. In this satellite system, the operating frequency range of the adopted modem (ViaSat ELiTE-S2) is from 0.95 to 2.15 GHz [9]. For IRR above 30 dBc, the amplitude and phase errors should be restricted within ± 0.2 dB and $\pm 1°$ according to [2]. Based on the constant phase behavior [29] of the adopted PPF, Fig. 4 is shown to choose the appropriate number of stages in PPF for covering the operating frequencies of this modem. Under this IRR requirement, the bandwidths of ideal 1- and 2-stage PPFs are 1.48-1.69 GHz and 1.14-2.07 GHz, respectively, which are too narrow to cover the modem's operating frequencies. The bandwidths of ideal 3- and 4-stage PPFs under this IRR requirement are 0.74-3.23 GHz and 0.6-6.47 GHz, respectively, which are sufficient to cover the operating frequency bandwidth. However, the 4-stage PPF has more insertion loss in comparison with the 3-stage PPF, which degrades the conversion gain (CG) performance of the mixer more. Therefore, a 3-stage PPF is selected for the design of both proposed mixers.

The conventional layout of the PPF shown in Fig. 5(a) suffers from parasitic inductance and capacitance. The parasitic inductance/capacitance are caused by the asymmetric long interconnects (black lines) between node "A" and "B" and the overlapped area between the black and yellow lines. In Fig. 5(b), the optimal layout with L-compensation technique distributes the asymmetric long interconnects on "D" and "E" (black lines) for symmetry and reduces the capacitor value (compensation capacitor in Fig. 5(b)) to alleviate the inductive parasitic effect on the PPF [29]. For more symmetry and less parasitic effect, this paper proposes using a castle-wall PPF which improves amplitude and phase balance to achieve a wide IRR bandwidth at the IF frequency, as illustrated in Fig. 5(c). With the castle-wall arrangement of resistors and capacitors, the paths between resistors and capacitors of each stage are the same. Due to this highly symmetric layout, the parasitic inductance and capacitance can be minimized. Fig. 6 shows the comparison of the conventional and proposed 3-stage PPFs. The simulated amplitude and phase errors of the conventional 3-stage PPF are <0.22 dB and $<1.74°$ (IRR $>$ 34.08 dBc), respectively, over 0.95-2.15 GHz. Compared with a conventional 3-stage PPF, the proposed 3-stage castle-wall PPF has less amplitude and phase errors (<0.06 dB, $<0.21°$; IRR $>$ 48.16 dBc) from 0.95 to 2.15 GHz and can sufficiently cover the operating

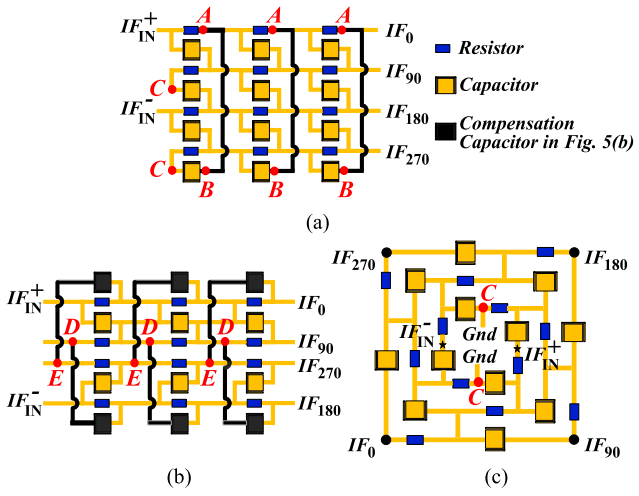

FIGURE 5. (a) Conventional PPF layout. (b) Optimal PPF layout with L-compensation technique [29]. (c) Proposed castle-wall PPF layout.

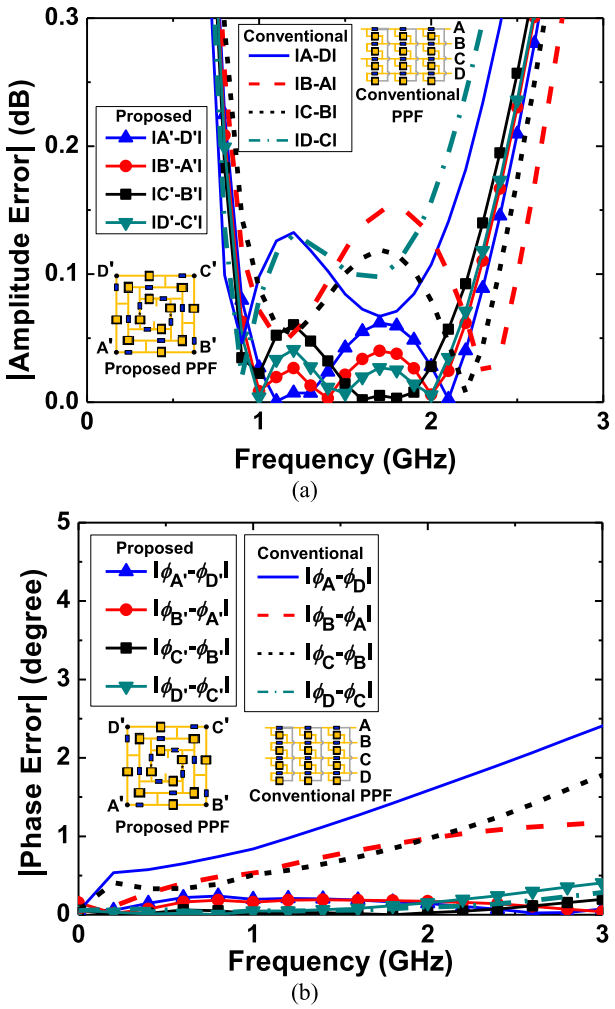

FIGURE 6. Simulated (a) amplitude error and (b) phase error of conventional and proposed PPFs (conventional PPF: line without symbol, proposed PPF: solid line with symbol).

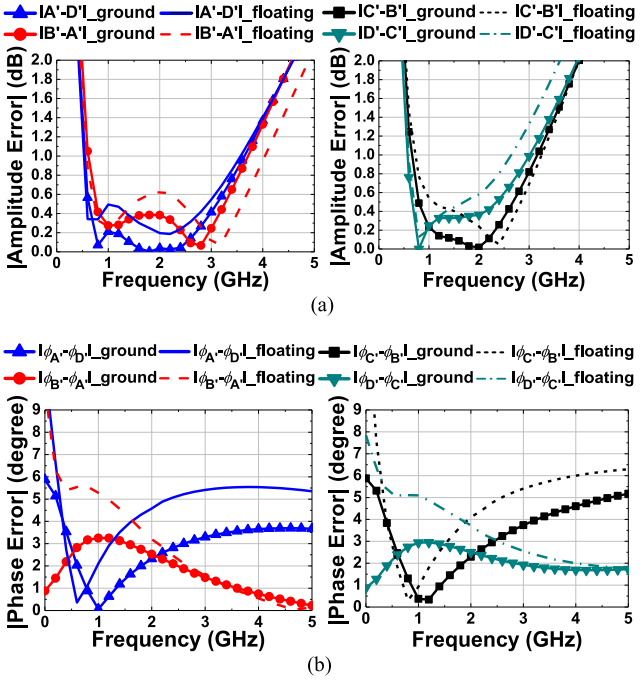

FIGURE 7. Simulated (a) amplitude error and (b) phase error of floating and grounded node C with non-ideal differential input (A', B', C', D' in Fig. 7 are referring to the points shown in Fig. 6).

frequencies of the modem (0.95-2.15 GHz) under an IRR requirement of >30 dBc.

The node C in Fig. 5(a) can be either floating or grounded in PPF design. When the ideal differential input signal is fed into IF_{IN}^{+} and IF_{IN}^{-}, the floating node C is a virtual ground [30]. However, as the input signal is a non-ideal differential, the floating node C will not be a virtual ground, so the amplitude and phase errors of PPF will increase. Fig. 7 shows the simulated amplitude and phase errors of the proposed 3-stage castle-wall PPF with the floating and grounded node C under a non-ideal differential input (amplitude/phase error = 0.5 dB/5°). It is observed that the PPF with the grounded node C (<0.41 dB, <3.25°; IRR > 28.7 dBc) presents less amplitude and phase errors than with the floating node C (<0.65 dB, <5.34°; IRR > 24.47 dBc) over 0.95-2.15 GHz, which means that a PPF with the grounded node C is more insensitive to the non-ideal differential input. Therefore, the node C is grounded in this PPF design, as shown in Fig. 5 (c).

III. DESIGN OF THE SSB UP MIXER AND IR DOWN MIXER

A. DESIGN OF THE SSB UP MIXER

Fig. 8 shows the block diagram of the SSB up mixer, which consists of a 3-stage castle-wall PPF, an LO four-way quadrature divider (two broadside 90° couplers and one Marchand balun), an in-phase mixer (I-mixer), a quadrature mixer (Q-mixer) and a RF buffer amplifier. For a broad IRR bandwidth at the IF frequency, the 3-stage castle-wall PPF is adopted to minimize the amplitude and phase errors over a wide bandwidth. In a 3-stage castle-wall PPF, each stage consists of four identical capacitors and resistors. The value of the capacitors for all three stages is 800 fF, while the resistor values are 101 Ω, 135 Ω and 204 Ω, for the 1st through 3rd stages, respectively. To verify the effect of the proposed castle-wall PPF on the IRR performance of the SSB up mixer,

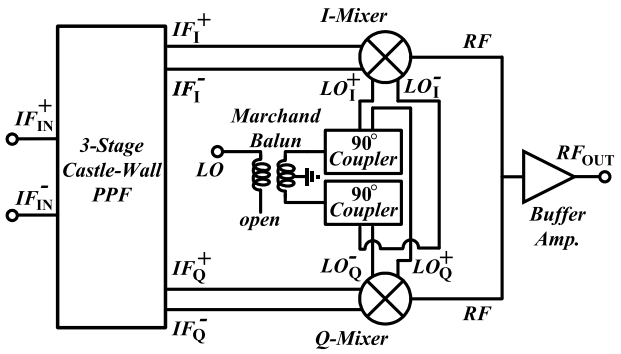

FIGURE 8. Block diagram of the SSB up mixer.

Fig. 9 shows the simulated IRR of the SSB up mixer with conventional and proposed PPFs under ideal LO quadrature signal. With the use of the proposed PPF, the IRR can be improved by about 5 dB to 10 dB from 23 to 34 GHz.

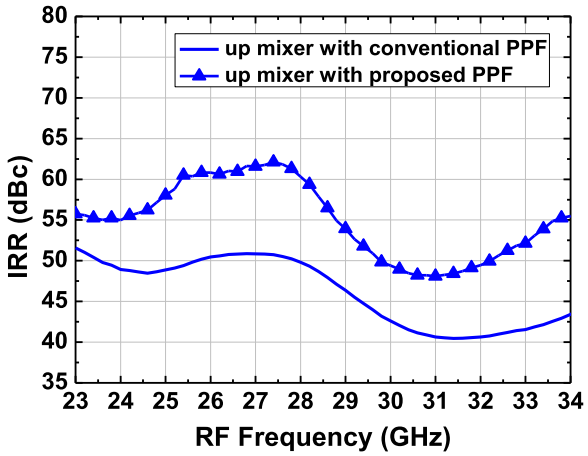

FIGURE 9. Simulated IRR of the SSB up mixer with conventional and proposed PPFs.

Quadrature generation can be used at the RF [18], [24], [31] or LO port [19], [22]. However, under the process variation and device mismatch, the quadrature generation causes load variation of the mixer core which then leads to IQ mismatch. In [2], load insensitive analysis indicates that the load variation at the LO port causes less IQ mismatch than at the RF port, and thus the quadrature generation is adopted at LO port and not at the RF port in our design, as illustrated in Fig. 8. For LO quadrature generation, the four-way quadrature divider composed of two broadside 90° couplers and one Marchand balun is adopted, as shown in Fig. 8. The broadside 90° couplers generate the quadrature signal and are wound into coils to achieve a compact size. The coupled lines are realized in metal 9 (ultra-thick metal) and metal 8 to minimize the metal loss. For proper coupling, the width and spacing of the coupled lines are designed of 4 and 2 μm, respectively. The Marchand balun converts the single-ended LO signal to differential with a wideband response. The top and bottom views of the Marchand balun are shown in Fig. 10. The coils in Marchand balun are broadside coupled for compact size and implemented in metal 9 and 8 (metal width/spacing = 4/2 μm). The double-cross pattern ground in Marchand balun can alleviate the amplitude and phase imbalance over wide bandwidth, as marked by the red solid line in Fig. 10(b). The symmetric layout of the four-way quadrature divider also helps to improve IRR.

Fig. 11 shows the schematic of the Q-mixer with the proposed 3-stage castle-wall PPF. The modified Gilbert-cell mixer architecture [31] is utilized to attain reasonable performance with a low supply voltage. In Fig. 11, the differential IF signal is directed to the 3-stage castle-wall PPF to generate the quadrature signal for the I-mixer and Q-mixer. The IF transconductance stage is composed of

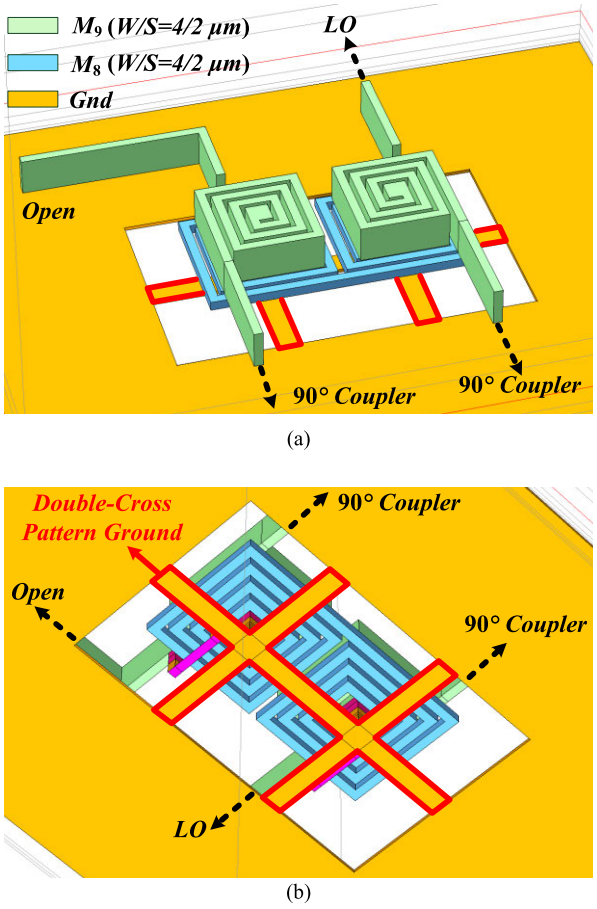

FIGURE 10. (a) Top and (b) bottom views of the Marchand balun.

resistive-feedback inverters (RFIs) which include nMOS transistors (M_5 and M_6), PMOS transistors (M_7 and M_8), and shunt feedback resistors (R_F). Compared with a common source transconductance stage, the RFI boosts transconductance to improve the CG under a low supply voltage [31]. The sizes of the nMOS and pMOS transistors are 16 μm/0.1 μm and 32 μm/0.1 μm, respectively, for moderate gain under low power consumption. By properly choosing R_F = 500 Ω, the transconductance stage provides sufficient gain and resolves the stability issue. The LO switching core (M_1-M_4) up-converts the differential IF input signal to RF bands. However, the LO impedance mismatch between the LO ports of I/Q mixers causes the LO reflection which degrades the IRR performance. Thus, the IRR enhancement networks, consisting of L_{D1}, L_{D2}, L_{S1} and C_{LO}, are used to achieve impedance matching and alleviate the LO reflection for IRR improvement, as marked by the dashed line in Fig. 11. To further improve IRR, the amplitude compensation lines (TL_{cp1} and TL_{cp2}) are adopted to compensate the imperfect symmetry in CMOS layout. For the RF single-ended signal, the Marchand balun is adopted to combine the up-converted RF differential signal. In addition, the RF buffer amplifier is inserted to compensate the loss of PPFs, as shown in Fig. 8.

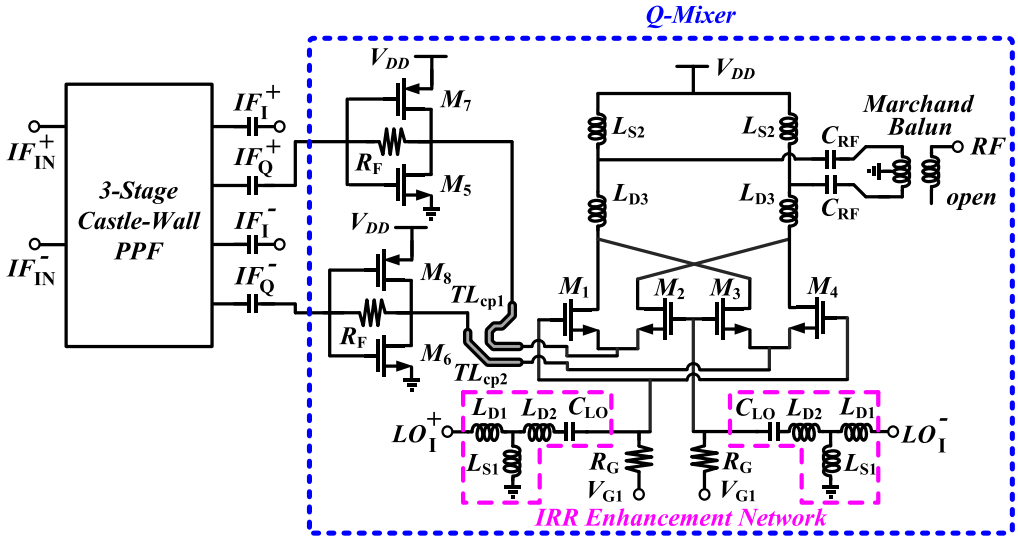

FIGURE 11. Schematic of Q-mixer with the 3-stage castle-wall PPF of the SSB up mixer.

To investigate the IRR sensitivity of the SSB up mixer for bandwidth tolerance, two IRR simulations of PVT variations and the Monte Carlo simulations each were performed, as plotted in Figs. 12 and 13. The PVT variations include the TT, FF, and SS process corners, a voltage range of ±10%, and a temperature range of −40∼+120 °C. Even under the aforementioned PVT variations, the simulated IRR can be better than 30 dBc at an RF frequency from 27.7 to 30.3 GHz, while the IF frequency is from 0.87 to 2.45 GHz, as shown in Fig. 12(a) and (b), respectively. The variations of the transistor, resistance and capacitance are included in the Monte Carlo simulations. With 100 Monte Carlo runs, for IRR above 30 dBc, RF bandwidth is from 27.8 to 30.3 GHz, while the IF bandwidth is from 0.8 to 3 GHz, as shown in Fig. 13(a) and (b), respectively. All four of these frequency ranges are able to cover the respective operating frequencies of the Ka-band satellite transmitter in Fig. 1(a).

B. DESIGN OF THE IR DOWN MIXER

The design in the IR down mixer is similar to the SSB up mixer. The block diagram of the IR down mixer, consisting of a 3-stage castle-wall PPF, an LO four-way quadrature divider (two broadside 90° couplers and one Marchand balun), an I-mixer, a Q-mixer, and IF RFIs, is shown in Fig. 14. To obtain the IR down mixer with broad IRR bandwidth at IF frequency, the 3-stage castle-wall PPF is adopted to achieve both broadband balanced amplitude and phase. In this PPF design, each stage uses four identical capacitors and resistors. The

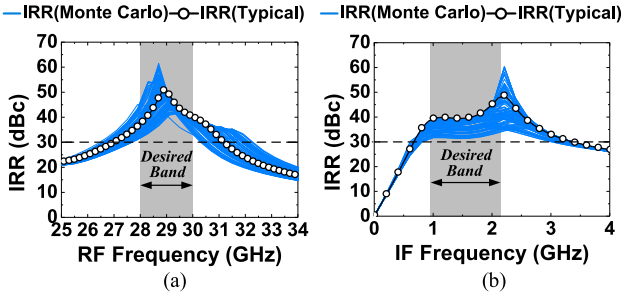

FIGURE 13. IRR Monte Carlo simulations versus (a) RF frequency and (b) IF frequency of the SSB up mixer.

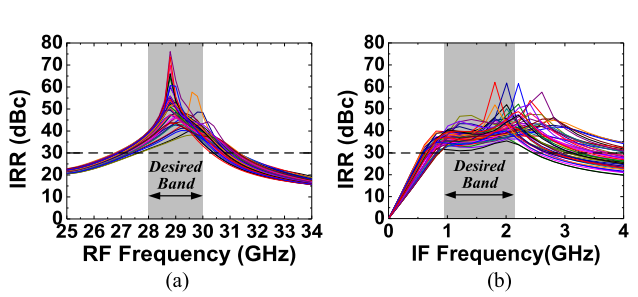

FIGURE 12. Simulated IRR versus (a) RF frequency and (b) IF frequency of the SSB up mixer under PVT variations (process: TT, FF, SS; voltage: 1.2, 1.2±10% V; temperature: −40, 0, 40, 80, 120°C).

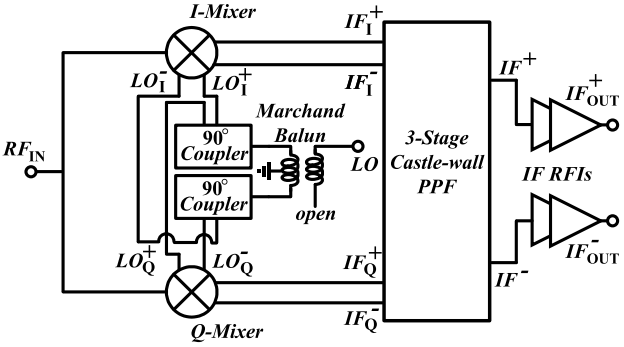

FIGURE 14. Block diagram of the IR down mixer.

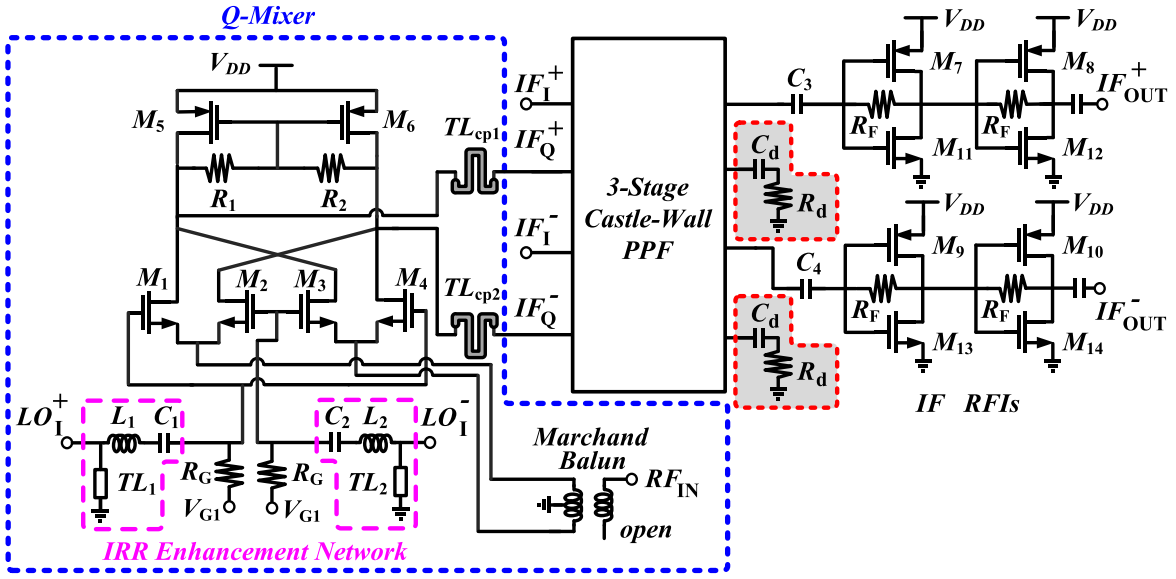

FIGURE 15. Schematic of Q-mixer with the 3-stage castle-wall PPF and IF RFIs of the IR down mixer.

capacitor values of the 1st-3rd stages are chosen as 473 fF, 530 fF, and 745 fF, respectively, while the resistor values of the 1st-3rd stages are selected as 316 Ω, 228 Ω, and 91 Ω, respectively. Since the imbalanced termination of the PPF causes the degradation of image rejection, the unused outputs of PPF are terminated with dummy capacitors (C_d) and resistors (R_d) for balanced termination [32], as marked by the area highlighted in gray in Fig. 15. To tolerate the process variations and mismatch, the quadrature generation is adopted at the LO port instead of at the RF port, as described above and shown in Fig. 14. For LO quadrature generation, the four-way quadrature divider, including two broadside 90° couplers and one Marchand balun, is utilized, as shown in Fig. 14. Similar to the SSB up mixer, the broadside 90° couplers provide the quadrature signal, while the Marchand balun is used to convert the single-ended LO signal to differential. The broadside 90° couplers and Marchand balun are implemented in metal 9 and 8 with a 4-μm width and a 2-μm spacing.

Fig. 15 presents the schematic of the Q-mixer with the proposed 3-stage castle-wall PPF and IF RFIs. The modified Gilbert-cell mixer architecture [31] is adopted to obtain reasonable performance under a low supply voltage. In Fig. 15, the RF input signal (RF_{IN}) is converted to a differential RF input signal through the Marchand balun. The use of this Marchand balun can also reduce the voltage headroom [31]. The differential RF input signal is then down-converted by the LO switching core (M_1-M_4). To alleviate the LO reflection for the IRR improvement, the IRR enhancement networks, composed of TL_1, L_1 and C_1, are utilized to achieve impedance matching between the LO ports of I/Q mixers, as marked by the dashed line in Fig. 15. Using the active load composed of pMOS transistors (M_5 and M_6), it can provide the high output impedance and decrease the ac current flowing through the mixer core [33]. Two resistors (R_1 and R_2) are adopted to ensure that the differential output of mixer core is at the same common-mode dc voltage. With the 3-stage castle-wall PPF, the image rejection mechanism can be realized. To compensate the loss of this 3-stage PPF, the IF RFIs, consisting of nMOS transistors (M_{11}-M_{14}), pMOS transistors (M_7-M_{10}), and feedback resistors (R_F), are used to attain moderate CG. For further IRR improvement, the amplitude compensation lines (TL_{CP1} and TL_{CP2}) are introduced to compensate the imperfect symmetry in CMOS layout. The sizes of nMOS transistors and pMOS transistors are selected as 50 μm/0.1 μm and 100 μm/0.1 μm in these RFIs, respectively. The resistance of feedback resistors (R_F) is 0.3 KΩ for sufficient gain and stability.

In Figs. 16 and 17, two simulations of PVT variations and the Monte Carlo simulations were run for the IRR sensitivity of the IR down mixer. Under the PVT variations, the simulated IRR versus RF frequency above 30 dBc is from 17.8 to 20.5 GHz, while the simulated IRR versus IF frequency better than 30 dBc is from 0.78 to 2.4 GHz, as shown in Fig. 16(a) and (b), respectively. Similarly, from 100 Monte

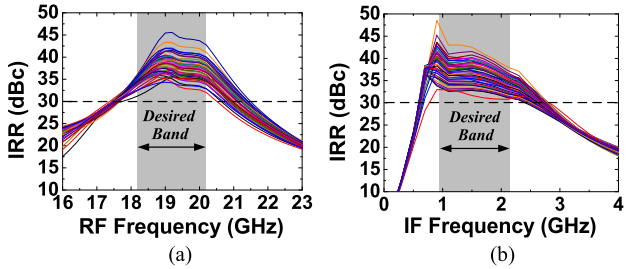

FIGURE 16. Simulated IRR versus (a) RF frequency and (b) IF frequency of the IR down mixer under PVT variations (process: TT, FF, SS; voltage: 1.2, 1.2±10% V; temperature: −40, 0, 40, 80, 120°C).

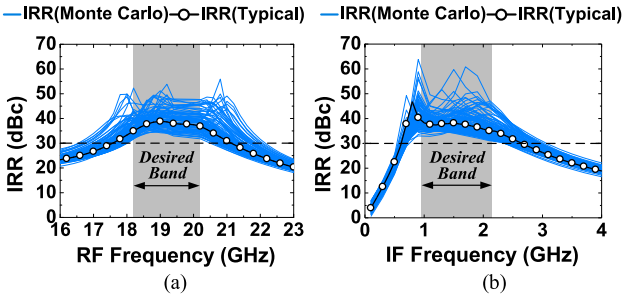

FIGURE 17. IRR Monte Carlo simulations versus (a) RF frequency and (b) IF frequency of the IR down mixer.

Carlo runs, the IRR versus RF frequency above 30 dBc is from 18 to 20.5 GHz, while the IRR versus IF frequency better than 30 dBc is from 0.75 to 2.35 GHz, as shown in Fig. 17(a) and (b), respectively. All four of these frequency ranges are able to cover the respective operating frequencies of the Ka-band satellite receiver in Fig. 1(a).

IV. MEASURED RESULTS

The proposed SSB up mixer and IR down mixer are fabricated using a standard 90-nm low-power CMOS process. All of the DC biasing voltages in both mixers are provided through bondwire to power supplies.

A. SSB UP MIXER CHARACTERISTICS

The chip microphotograph of the proposed SSB up mixer is shown in Fig. 18. The chip size is 1.695 × 1.19 mm^2, including all testing pads. The gate bias of the mixer core is 1.1 V and the gate biases of the common gate and common source in RF buffer amplifier are 0.6 and 1.2 V, respectively. With a 1.2-V supply voltage, the SSB up mixer consumes 15.6 mW. The SSB up mixer was measured via on-wafer probing. A signal generator (Agilent E8257D) is utilized to generate the LO signal and an arbitrary waveform generator (Tektronix AWG7122B) is used to provide the differential IF signal. The RF output signal is measured by a spectrum analyzer (Agilent E4448A). Fig. 19 shows the measured

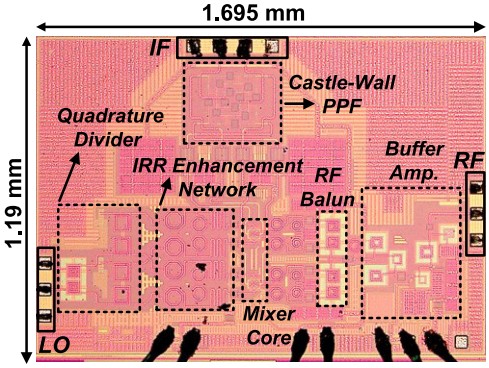

FIGURE 18. Chip microphotograph of the proposed SSB up mixer with chip size of 1.695 × 1.19 mm^2.

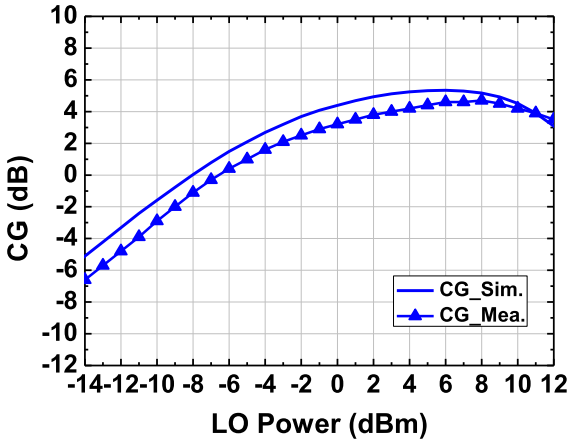

FIGURE 19. Measured and simulated CG versus LO power of the SSB up mixer.

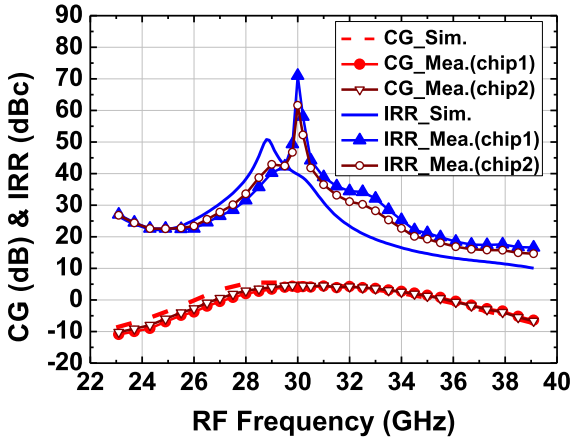

FIGURE 20. Measured and simulated CG and IRR versus RF frequency of the SSB up mixer.

and simulated CG versus LO power with an LO frequency of 28.4 GHz and an IF frequency of 1.6 GHz. For the reasonable LO power, the 4-dBm LO power is selected for all measured data. With the 4-dBm LO power, the measured CG is 4.2 dB. The measured and simulated CG and IRR versus RF frequency at a fixed IF frequency of 1.6 GHz are shown in Fig. 20. The measured CG is from 1.3 to 4.3 dB over the 3-dB RF bandwidth of 27.7-35.2 GHz. The measured IRR is better than 30 dBc over the RF frequency range from 27.7 to 33.3 GHz (18.36% fractional RF bandwidth). Fig. 21 plots the measured and simulated CG and IRR versus IF frequency at a fixed LO frequency of 28.4 GHz. The measured CG is from 2.7 to 5.7 dB over 3-dB IF bandwidth between 0.15 and 2.5 GHz. The measured IRR is above 30 dBc from 0.6 to 4 GHz (148% fractional IF bandwidth). The measured and simulated results of output 1-dB compression point (OP_{1dB}) are shown in Fig. 22. The measured OP_{1dB} performance is −4.3 dBm at a RF frequency of 30 GHz and an IF frequency of 1.6GHz. In Fig. 23, the measured LO-to-RF and LO-to-IF isolations are greater than −33.9 and −57.1 dB from 21.5 to

TABLE 1. Performance summary and comparison of the reported up mixers and transmitter with image rejection.

Ref.	RF Frequency (GHz)	CG(dB)	RF Bandwidth** (GHz)	IF Bandwidth** (GHz)	LO Power (dBm)	OP_{1dB} (dBm)	DC power (mW)	Chip size (mm^2)	Process
[19] SSB up mixer	75-90	-11±0.5	N/A	N/A	9	-4	0	3	0.1 μm GaAs pHEMT
[20] SSB up mixer	14.4-15.4*	3.5±1.5*	IRR= 63 dBc at 15.18GHz	N/A	10	-6	86.4	1.26	0.15 μm AlGaAs/InGaAs pHMET
[24] SSB up mixer	5.76-5.804*	-14.2±1.5*	N/A	0.119-0.124* (4.1%)	4	N/A	N/A	1050	Hybrid
[25] SSB up mixer	43.5-45.5	-11±0.6	N/A	0.175-0.185* (2.78%)	12	-15	0	2.89	0.18 μm GaAs pHEMT
[26] SSB up mixer	2.1-2.93*	-13.1±1.5*	2.62-2.76* (5.2%)	0.122-0.138* (12.3%)	N/A	-8	N/A	1800	Hybrid
[34] SSB up mixer+LO buffer/divider	10-11.5	9.12	IRR=46.9 dBc at 11.5 GHz	N/A	-10	2.65	48.7	0.57	90 nm SiGe
[35] SSB up mixer	48-68*	-2.5±1.5*	50-66 (27.58%)	N/A	N/A	-17	65	1.305	0.18 μm CMOS
[36] SSB up mixer+LO doubler	40.5-43.5*	11.95±0.35*	40.5-42.5* (4.8%)	N/A	0	18	960	2.5	0.15 μm GaAs pHEMT
[37] SSB up mixer	52-61	-10±1	N/A	N/A	9.5	-17*	0	2.1	0.18 μm GaAs pHEMT
[38] Transmitter (SSB up mixer+PLL+PA)	33.5-42.8*	29.5±1.5*	IRR=32 dBc at 40.08GHz	N/A	N/A	-3	260	0.715	90 nm CMOS
[39] SSB up mixer	68-80	-12.66±0.68	68-74.8* (9.5%)	N/A	3	-10*	0	0.3315	65 nm CMOS
This Work SSB up mixer	**27.7-35.2**	**2.8±1.5**	**27.7-33.3 (18.36%)**	**0.6-4GHz (148%)**	**4**	**-4.3**	**15.6**	**2.017**	**90 nm CMOS**

*Graphically estimated; **IRR>30 dBc

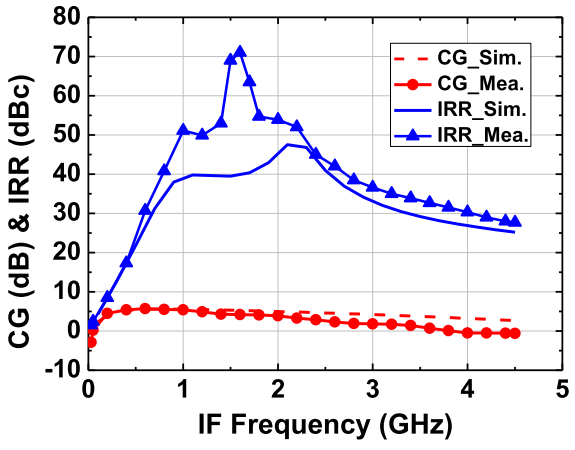

FIGURE 21. Measured and simulated CG and IRR versus IF frequency of the SSB up mixer.

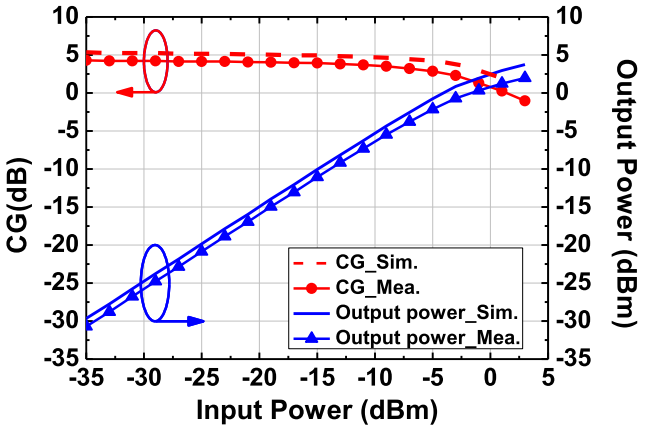

FIGURE 22. Measured and simulated OP_{1dB} performance of the SSB up mixer.

37.5 GHz, respectively. Table 1 summarizes the performances of published up mixers and transmitter with image rejection. Compared with other reports, this work attains a wide IRR bandwidth at the IF frequency.

B. IR DOWN MIXER CHARACTERISTICS

Fig. 24 presents the chip photograph of the proposed IR down mixer with chip area of 1.26×0.97 mm^2, including all testing pads. The gate bias of the mixer core is 0.4 V. The total dc power consumption of the IR down mixer is 12 mW at

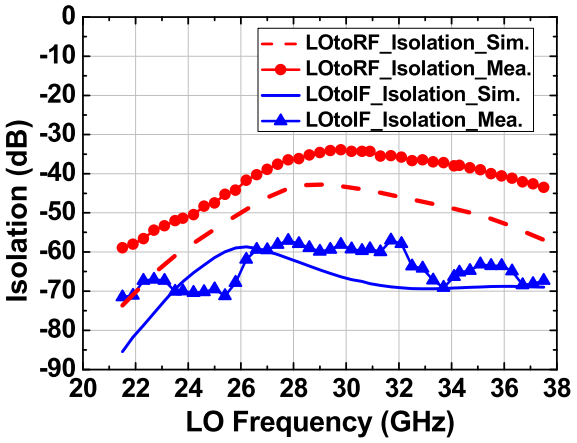

FIGURE 23. Measured and simulated isolations of the SSB up mixer.

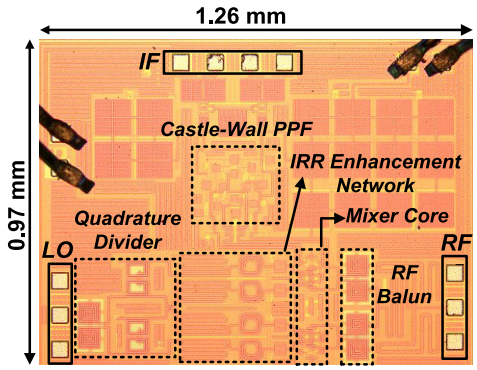

FIGURE 24. Chip photograph of the proposed IR down mixer with chip area of 1.26 × 0.97 mm^2.

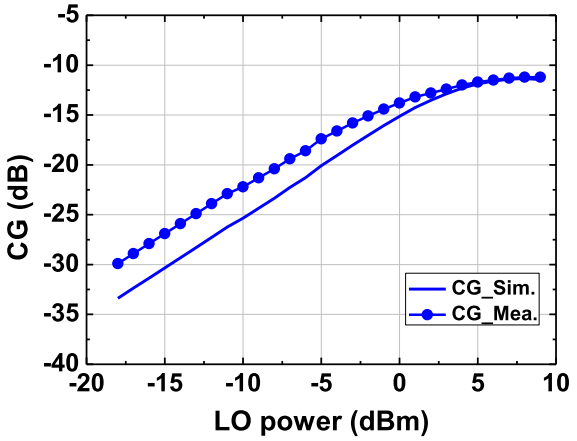

FIGURE 25. Measured and simulated CG versus LO power of the IR down mixer.

1.2-V supply voltage. The IR down mixer was measured via on-wafer probing. During the measurements, the RF signal is provided by the signal generator (Agilent E8257D). The LO source is generated by using another signal generator (Agilent E8257D). The output spectrum of the IR down mixer is observed by a spectrum analyzer (Agilent E4448A). Fig. 25 plots the measured and simulated CG versus LO power with an LO frequency of 17.2 GHz and an IF frequency

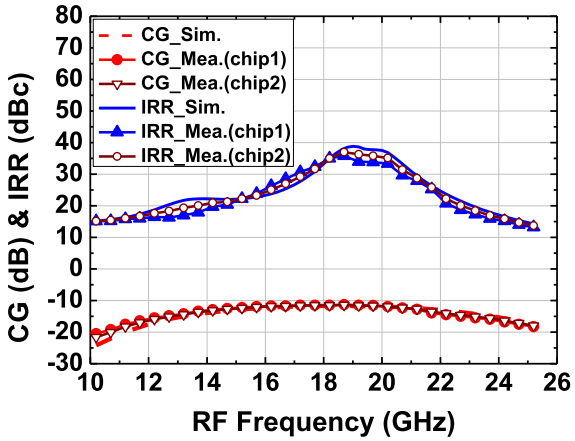

FIGURE 26. Measured and simulated CG and IRR versus RF frequency of the IR down mixer.

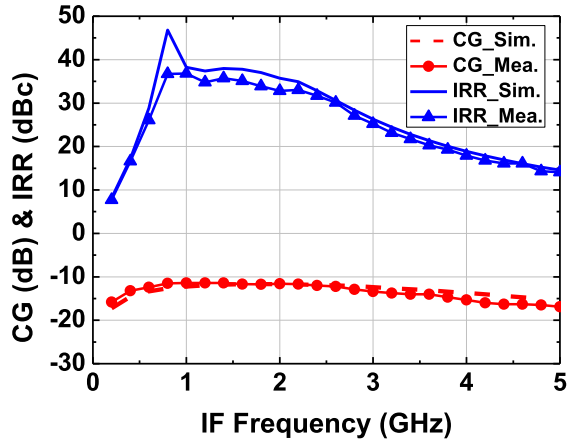

FIGURE 27. Measured and simulated CG and IRR versus IF frequency of the IR down mixer.

of 1.5 GHz. For the reasonable LO power, the 5.5-dBm LO power is selected to present measured results. The measured CG is −11.6 dB at an LO power of 5.5 dBm. Fig. 26 shows the measured and simulated CG and IRR versus RF frequency at a fixed IF frequency of 1.5 GHz. The measured RF 3-dB bandwidth is between 13.1 and 21.9 GHz and the CG is from −11.3 to −14.3 dB. The measured IRR is better than 30 dBc from 17.1 to 20.6 GHz (18.5% fractional RF bandwidth). At a fixed LO frequency of 17.2 GHz, the measured and simulated CG and IRR versus IF frequency are plotted in Fig. 27. The measured CG has a 3-dB IF bandwidth from 0.3 to 3.7 GHz and CG is from −11.3 to −14.3 dB. Since we put the IF bandwidth as the first priority for the satellite applications, there is a trade-off between bandwidth and conversion gain. The measured IRR is above 30 dBc between 0.65 and 2.5 GHz (117% fractional IF bandwidth). In Fig. 28, the measured input 1-dB compression point (IP_{1dB}) is 0 dBm for a RF frequency of 18.7 GHz and an IF frequency of 1.5 GHz. The measured LO-to-RF and LO-to-IF isolations are better than −43.2 dB and −52.3 dB, respectively, as shown in Fig. 29.

TABLE 2. Performance summary and comparison of the reported mixers and receivers with image rejection.

Ref.	RF Freq. (GHz)	CG(dB)	RF Bandwidth** (GHz)	IF Bandwidth** (GHz)	LO Power (dBm)	IP_{1dB} (dBm)	DC power (mW)	Chip size (mm^2)	Process
[16] IR down mixer	21.3-22.7*	-10.3±1.5*	20.05-21.35* (6.3%)	1.43-1.58* (9.96%)	N/A	N/A	N/A	160	Hybrid
[18] LNA+IR down mixer	59.7-64.3*	17±1.5*	54-65* (18.48%)	0.88-0.92* (4.4%)	4.5	N/A	278	6.01	0.15 μm GaAs HEMT
[21] DQ IR down mixer[#]	16.03	1.7	N/A	0.03-0.035* (15.3%)	12	-5	N/A	9.6	0.15 μm mHEMT
[22] IR down mixer	54.5-67*	-11.7±1.5*	IRR=30 dBc at 60 GHz*	IRR=30 dBc at 2.5GHz*	N/A	N/A	N/A	9.24	0.15 μm GaAs pHEMT
[23] LNA+IR down mixer + calibration circuitry	28/37	33*/26*	27-29.3* /35-38* (8.17%) (8.2%)	N/A	N/A	-29.5*/-22*	52.5	1*[§§]	65 nm CMOS
[27] IR down mixer	9.1-10.4	-7	N/A	1.3-2.4 (59.5%)	N/A	1	N/A	1.8	0.18 μm SiGe BiCMOS
[28] LNA+IR down mixer	60	15	N/A	4.61-5.36* (15.9%)	N/A	-22.5	46	0.82	90 nm CMOS
[40] IR down mixer+VCO	10-11.8*	31.5±1.5*	10-11.6* (14.8%)	N/A	8	-30	105	2.86	InGaP/GaAs HBT
[41] LNA+IR down mixer +LO multiplier	56-69	65[##]	50-62*[§] (21.43%)	N/A	-18	N/A	180	3.1	0.13 μm SiGe BiCMOS
[42] LNA+IR down mixer+ LO divider/buffer	24.8-29.8*	32.5±1.5*	25-30 (18.1%)	N/A	N/A	-29	27.5	0.32	65 nm CMOS
This Work IR down mixer	**13.1-21.9**	**-12.8±1.5**	**17.1-20.6 (18.5%)**	**0.65-2.5 (117%)**	**5.5**	**0**	**12**	**1.22**	**90 nm CMOS**

*Graphically estimated; **IRR>30 dBc; [#]DQ: double quadrature; [##]Mean CG; [§]Only IR down mixer; [§§]Core area

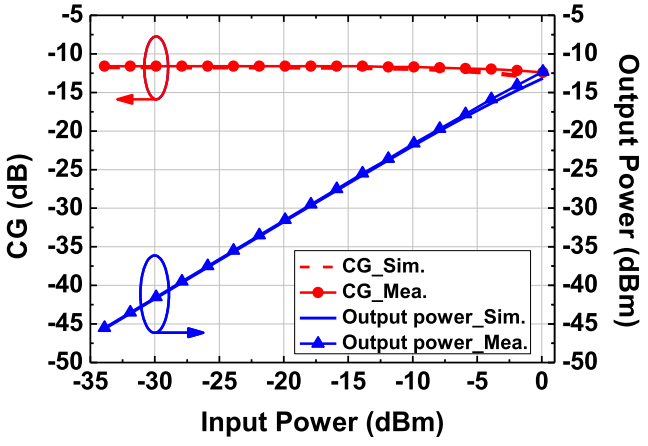

FIGURE 28. Measured and simulated IP_{1dB} performance of the IR down mixer.

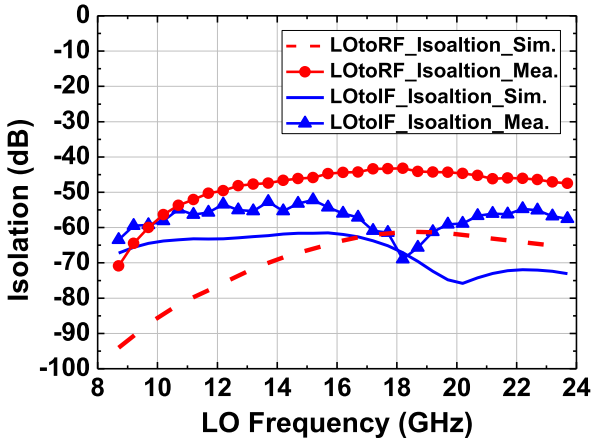

FIGURE 29. Measured and simulated isolations of the IR down mixer.

Table 2 summarizes the performances of reported down mixers and receivers with image rejection. It can be observed that the proposed IR down mixer demonstrates wide IRR bandwidth at the IF frequency compared with other published results.

V. CONCLUSION

The Ka-band SSB up mixer and IR down mixer with wide IRR bandwidths at the IF frequencies for satellite modem (0.95-2.15 GHz) implemented in 90-nm low-power CMOS technology are presented in this paper. By adopting the

proposed 3-stage castle-wall PPF, the amplitude and phase errors can be minimized for broad IRR bandwidth at the IF frequency. At the LO port, the four-way quadrature divider, consisting of two broadside 90° couplers and one Marchand balun, is used for quadrature generation. The SSB up mixer has 4.2-dB CG and OP_{1dB} of −4.3 dBm. The CG and IP_{1dB} of IR down mixer are −11.6 dB and 0 dBm, respectively. With the power consumption of 15.6 and 12 mW, the SSB up mixer and IR down mixer demonstrate wide IRR bandwidths of 0.6-4 GHz (148% fractional IF bandwidth) and 0.65-2.5 GHz (117%) at the IF frequencies without calibration. Also, both mixers achieve IRR bandwidths at the RF frequencies from 27.7 to 33.3 GHz (18.36% fractional RF bandwidth) and from 17.1 to 20.6 GHz (18.5%). The IRR performances are robust against PVT variations and Monte Carlo simulations for SATCOM applications.

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