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Fault Modeling of IIDG Considering Inverter's Detailed Characteristics

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ABSTRACT As more and more inverter interfaced distributed generators (IIDGs) such as PV are connected to the distribution network (DN), the existing relay protection system may malfunction due to the impact of the IIDGs. In order to evaluate that impact, the fault analysis of the DN with IIDGs is needed and the fault modelling of IIDG is of great significant for the fault analysis and the protection system validation and improvement. This paper proposes a new fault modelling method of IIDG that could consider the detailed characteristics of the inverter in different situations including the limitation of the modulation. The symmetrical fault model of PQ controlled IIDG is deduced by the proposed method, based on which the symmetrical fault analysis of the DN with IIDGs is carried out. The proposed model depicts IIDG as a voltage-controlled current source or a voltage-controlled voltage source according to whether the modulation is limited, therefore covers the full characteristics of the inverter under different conditions, improving the modelling accuracy. The case study based on the modified IEEE 13 nodes system shows that the fault analysis results obtained from the proposed model are more consistent with electromagnetic transient simulation than that of the state-of-art fault model, verifying its effectiveness.

INDEX TERMS Inverter interfaced distributed generator (IIDG), stagtewise fault model of IIDG, fault analysis of the distribution network with IIDGs, modulation limitation, fault ride-through.

I. INTRODUCTION

Nowadays, more and more distributed generators utilizing renewable energy resources are connected to the medium and low voltage distribution network (DN) due to the promotion of the energy reform characterized by clean, renewable and sustainable [1]. The inverter (mainly voltage source converter, VSC) interfaced distributed generator, usually referred to as IIDG, enriches the ways of the utilization of renewable energy. However, it also changes the fault characteristics of the DN, which may invalidate the existing relay protection system, such as traditional fault location strategy and overcurrent protection based on fault current, distance protection based on measured impedance [2], [3]. Therefore, the fault analysis is needed to evaluate the impact of IIDGs on the fault characteristics of the DN with IIDGs as well as the protection system validation and improvement.

Analysis based on transient simulation is a direct method and has been adopted by many scholars to study the fault characteristic of IIDG as well as its impact on DN [3], [4]. However, two disadvantages make the transient simulation not very suitable for fault analysis of DN with IIDGs. First, it is cumbersome and high professional quality required to build the dynamic models for transient simulation. Second, it is quite time-consuming to run the transient simulation, especially for the DN with dozens of IIDGs. These two factors make the easy and fast fault analysis infeasible, therefore the quasi-static analysis which is relatively simple and much more time-efficient draws wide attention. Building a quasi-static model of IIDG that could accurately depict its behavior during the fault is the most important part of quasi-static fault analysis. In [4], [5], IIDG is modelled as a constant

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current source whose amplitude is 1.5 ∼ 2 times its rated current, the model is easy to realize and the ordinary power flow calculation algorithm could be adopted to carry out the fault analysis. However, this method doesn't consider the real output of IIDG, diminishing its accuracy. In [6], IIDG is modelled as a voltage source in series with a variable impedance to account for output fluctuation of IIDG. The accuracy is improved but the impedance is complex to calculate and its structure is different from that of the nature VSC. Further studies in [7]–[16] show that the inverter's characteristics and the control strategy are the keys to model IIDG during the fault, and scholars are trying to model the IIDG during the fault under different control strategies (PQ control [7]–[11], V/f control [12], [13] and droop control [12]).

In practice projects, most of the IIDGs adopt PQ control strategy that generates active and reactive power as ordered by the upper layer control system, facilitating the utilization of the renewable energy resources and response to the grid requirement. Therefore the fault modelling of IIDG adopting PQ control strategy draws special attention. In [7], [8], a segmented model composed of a constant power source and a constant current source is proposed to simulate the different behaviors of IIDG before and after its inverter's overcurrent limiter functions. In [9], [10], a model considering the reactive power support behavior of IIDG during the fault is proposed by adding additional reactive current reference stipulated in fault ride-through (FRT) requirement. In [11], [12], a composite sequence model applicable to both symmetric and asymmetric fault analysis for IIDG adopting positive sequence voltage control is proposed. Furthermore, in [13], a unified model applicable to IIDGs adopting flexible PQ control strategies is proposed by deducing the uniform expression of the current reference of the inverter. Based on the fault model of IIDG, fault analysis of DN with several IIDGs are proposed in [14]–[16], which solve network equations and the fault model of IIDGs alternately in an iterative way to calculate nodes' voltage, fault current and the other fault variables, supporting the protection system configuration.

The fault models given above mainly focus on the formulation of FRT control strategy of IIDGs and assume the current of IIDG tracks the reference exactly. However, these models may lose accuracy due to the behavior variation of the inverter, which is a complex nonlinear system with many strong nonlinear links such as current limiter and modulation limiter. When modulation wave is limited, the real current of the IIDG will diverge from the reference value dramatically, corrupting the assumption above. In order to improve the fault model's accuracy under different conditions, we propose a new fault modelling method of IIDG that considers the detailed characteristics of the inverter in different situations including the modulation limitation. The proposed method consists of three steps: The first two steps build the model of the FRT control strategy and the inverter separately, and the third step builds the cascaded model of the two parts to form the whole fault model. Based on the proposed method, the symmetrical fault model of PQ controlled, two-level VSC interfaced IIDG is deduced, and the process of applying it in symmetrical fault analysis of DN with IIDGs is presented. At the end of the paper, a case study based on the modified IEEE 13 nodes system is carried out to verify the effectiveness of the proposed method.

The rest of the paper is organized as follows. Section II illustrates the modelling process of the PQ controlled, two-level VSC interfaced IIDG. Section III presents the process of applying the proposed model in the symmetrical fault analysis of the DN with IIDGs. Section IV carries out the case study and results discussion. Main conclusions and work prospects are drawn in Section V.

II. MODELLING OF PQ CONTROLLED TWO-LEVEL VSC INTERFACED IIDG

IIDG is a type of generation system that connects to the grid with an inverter, which translates the direct current (DC) to the alternative current (AC). Without loss of generality, this paper takes two-level VSC interfaced IIDG that adopts PQ control strategy as an example, as the PQ control strategy is dominating in the practical operation of IIDG and the two-level VSC is widely used in the IIDG rating below 750 kW due to its simple structure and low cost [17].

From the previous work, it is clear that the FRT strategy and the dynamic characteristics of the inverter should be taken into consideration for the IIDG fault modelling. As these two aspects are so distinct from each other both in function and composition, we first model them separately and then merge them. Therefore the fault modelling of IIDG can be divided into the following 3 steps:

Step 1: Modelling of the FTR control. The main objective is to formulate the formula of the FTR control strategy stipulated by grid code. Usually, it takes the form of a function from the fault index to the order of the inverter's control system.

Step 2: Modelling of the inverter. The main objective is to formulate the transfer function of the inverter during the fault. Due to the nonlinear characteristic of the inverter, stagewise model is used here.

Step 3: The model merging. Connecting the model of the FTR control strategy and the inverter, obtaining the fault model of the IIDG.

A. MODELLING OF THE FRT CONTROL

In order to avoid cascading outage of IIDGs, they are required to keep the connection to the grid and supply necessary support power for a required period when the voltage sag occurs during the grid fault. FRT control strategy is designed to fulfill the above requirement and various grid codes stipulating the detailed requirements of FRT such as ride-through time, reactive power support are published across jurisdictions. The reactive power support dominates the behavior of the IIDG during the fault, therefore is mainly considered here. The requirement of reactive power support stipulated in German

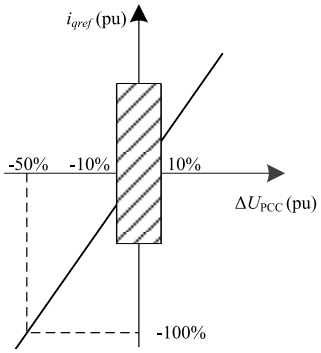

FIGURE 1. Requirements of reactive power support during the fault.

grid code shown in Figure 1 is taken as an example [18], [19], as it is often referred to as a typical grid code in literature.

In Figure 1, ΔU_{PCC} is the index measuring voltage drop and the shaded area indicates the control dead zone which depends on the allowed voltage deviation during the normal operation period. The line outside the dead zone shows that the required supported reactive current increases linearly with the degree of voltage drop. Thus, when the grid voltage diverges from the normal value, the IIDG should generate reactive power as depicted in Figure 1. Meanwhile, the IIDG should try to generate the same active power as pre-fault [9], therefore the active and reactive current order i_{dref} and i_{qref} given by FRT control strategy to inverter control system could be calculated as follows [9], [11], [16].

$$\begin{cases} i_{dref} = P_{ref}/U_{\mathrm{PCC}} \\ i_{qref} = K_q \Delta U_{\mathrm{PCC}} \\ \Delta U_{\mathrm{PCC}} = U_{\mathrm{PCC}} - U_{\mathrm{PCC}_0} \end{cases} \tag{1}$$

where P_{ref} is the pre-fault active power order and is maintained during the fault; $U_{\mathrm{PCC}0}$ and U_{PCC} are the voltage of point of common coupling (PCC) before and during the fault; K_q is the reactive power supportting factor that reflects the requirement of reactive power support and should be not less than 2 in German grid code [18].

Equation (1) is the model of FRT control strategy, which stipulates what the IIDG should do during the fault. However, the order of FRT is executed by the inverter, whether IIDG behaviors as the stipulation given by FRT control depends on the characteristic of the inverter.

B. MATHMATIC MODEL OF VSC AND ITS CONTROL SYSTEM

Figure 2 shows the main circuit topology of two-level VSC and its control system. As the input power given by the primary energy equipment could be seen constant during the fault, they are modelled as a DC voltage source. Here, R and L are the equivalent parameters of the AC filter; e_k, i_k ($k = a, b, c$) are the voltage of the PCC and inverter output current respectively; v_k ($k = a, b, c$) is the inverted voltage and V_{dc} is the magnitude of DC voltage source; v_d, v_q and e_d, e_q are the d and q components of the inverted voltage

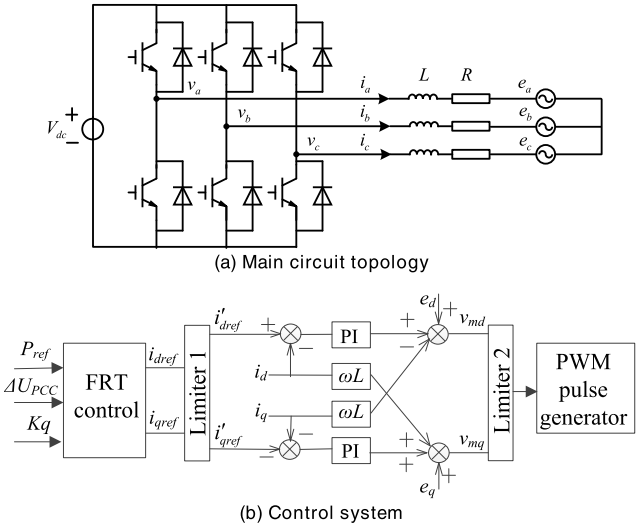

FIGURE 2. Schemes of the two-level VSC.

and the voltage of PCC respectively; i_d, i_q are the d and q components of the inverter's output current and ω is the synchronous angular velocity; v_{md}, v_{mq} are the modulation voltage references. The typical double-layer structure using PI controller and feedforward decoupling is adopted in the control system, which takes the current order from the FRT control and generates the trigger pulses for the switches in the main circuit.

Base on Figure 2, the mathematical model of the inverter as well as its control system could be deduced as in [1]. However, there are two limiters in the control system, which makes the converter's characteristic more complex. Limiter 1 is a current limiter used to prevent the current order from exceeding the safety range of the electronic switches, protecting the inverter from being burned down. Limitation rule with the fixed maximum apparent current is commonly used and takes the expression as:

$$i'_{kref} = \min\left\{ i_{kref}, \frac{i_{kref}}{\sqrt{i_{dref}^2 + i_{qref}^2}} I_{\max} \right\}, \quad k = d, q \tag{2}$$

where $I_{\max}$ is the maximum allowed current of the switches and usually is 1.5∼2 times the rated value. However, in order to meet the reactive power support requirement with high priority, the current limitation rule may be adjusted according to the grid code.

Limiter 2 is used to constrain the amplitude of the modulation waves to avoid nonlinear modulation or control the nonlinear modulation within an acceptable level. If the nonlinear modulation is totally avoided, the limitation rule has the following expression:

$$v'_{mk} = \min\left\{ v_{mk}, \frac{v_{mk}}{\sqrt{v_{md}^2 + v_{mq}^2}} \right\}, \quad k = d, q \tag{3}$$

where v'_{md}, v'_{mq} are the value of v_{md}, v_{mq} after limitation.

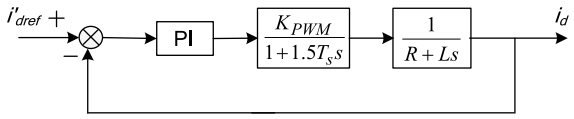

FIGURE 3. The control diagram of decoupled inner current loop.

C. STAGEWISE MODEL OF THE INVERTER

Based on the mathmatic model of VSC and its control system, the inverter model could be obtained. However, the complexity of the inverter model depends on whether the modulation wave is limited by limiter 2: if the modulation wave is not limited, the inverter model will be a linear transfer function and only limiter 1 should be considered; otherwise, the inverter model will be a nonlinear transfer function, in which case the stagewise model is introduced.

1) STAGE SEGMENTATION

According to (3), whether limiter 2 arrives at the turning point depends on the relationship between $\sqrt{v_{md}^2 + v_{mq}^2}$ and 1. For the calculation convenience, inequality (4) which describes the relationship between the invert requirement and the maximum invert capacity could be used instead in the quasi-static analysis.

$$\left(U_{\mathrm{PCC}} - \omega L i'_{qref}\right)^2 + \left(\omega L i'_{dref}\right)^2 \le (MV_{dc})^2 \tag{4}$$

where $M \cdot V_{dc}$ is the maximum inverter voltage (MIV) and M is the voltage utilization ratio which depends on the pattern of the modulation as:

$$M = \begin{cases} 1/2\sqrt{2} & \text{SPWM} \\ 1/\sqrt{6} & \text{SVPWM} \end{cases} \tag{5}$$

If (4) holds, the amplitude limitation of limiter 2 doesn't take action and we call this stage 1; otherwise limitation of limiter 2 must be taken into consideration in the inverter modelling process and we called this stage 2.

2) MODEL OF STAGE 1

If (4) holds, (3) can be simplified to

$$v'_{mk} = v_{mk}, \quad k = d, q \tag{6}$$

Therefore, the inverted voltage could be expressed as

$$v_k = MV_{dc} v_{mk}, \quad k = d, q \tag{7}$$

The control block diagram of the inverter from current order to its real value could be simplified as in Figure 3.

Where K_{PWM} is the equivalent gain of PWM, T_{s} is the total delay time of data acquisition and trigger process. Usually, the "second-order optimal principle" is utilized to design the PI controller [1], then the closed-loop transfer function of the inverter current control could be simplified to

$$W(s) = \frac{1}{4.5T_s^2 s^2 + 3T_s s + 1} \approx \frac{1}{1 + 3T_s s} \tag{8}$$

It is obvious that the process of the current regulation is a first-order process with the time constant equals $3T_s$.

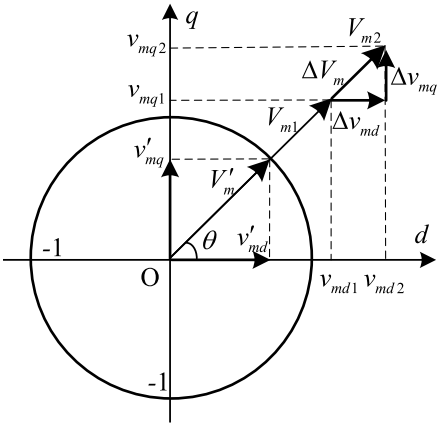

FIGURE 4. Control vector limiting process under SVPWM modulation.

Generally, T_s is around a fraction of a millisecond, much less than the time of the grid fault (hundreds of milliseconds), therefore the current regulation process can be ignored and modelled as a unity gain link. Merging the model of limiter 1 in (2) and unity gain model of the inverter's current control, the inverter model of stage 1 is obtained as a controllable current source shown in (9). Here, the requirement of reactive power support is met with higher priority than that of active power, thus it is slightly different from (2).

$$\begin{cases} i_q = \max\left\{i_{qref}, -I_{\max}\right\} \\ i_d = \min\left\{i_{dref}, \sqrt{I_{\max}^2 - i_q^2}\right\} \end{cases} \tag{9}$$

3) MODEL OF STAGE 2

If (4) doesn't hold, (3) can be simplified to

$$v'_{mk} = v_{mk} \Big/ \sqrt{v_{md}^2 + v_{mq}^2}, \quad k = d, q \tag{10}$$

The limitation described by (10) is the process of control voltage vector truncation when it exceeds the invert capacity of the inverter. The process could be demonstrated in Figure 4 when the space vector pulse width modulation (SVPWM) is adopted to control the VSC. When the modulation vector is placed in the synchronous rotating reference frame, it is a standing vector with angle θ. The uint circle is the maximum allowed modulation vector avoiding nonlinear modulation. If the modulation vector exceeds the unit circle, it will be truncated in its direction and the inverter current can't track its reference because the reference current exceeds the invert ability of the inverter. This is often the case when the voltage of PCC dips, but a large amount of reactive power and active power is required to invert to the grid.

In Figure 4, $\boldsymbol{V}_{\mathrm{m1}}$, $\boldsymbol{V}_{\mathrm{m2}}$ are the modulation vectors at the moment of t_1 and t_2; $\Delta \boldsymbol{V}_m$ is the variation between the two moments with Δv_{md}, Δv_{mq} as its d and q components; $\boldsymbol{V}'_m$, v'_{md} and v'_{mq} are the modulation vector and its dq components after truncated. When IIDG reaches its qusia-steady state, the inverter current i_d, i_q as well as the truncated modulation vector $\boldsymbol{V}'_m$ keeps constant in the synchronous rotating reference frame. Meanwhile, as there is a constant difference

between the inverter current and its reference, the modulation vector $\boldsymbol{V}_{\mathrm{m}}$ will increase steadily in proportion to the time elapse because there is a integrator in the PI controller. In order to maintain the qusia-steady state, $\boldsymbol{V}_{\mathrm{m}}$ and $\Delta\boldsymbol{V}_{\mathrm{m}}$ must be in the same direction and that is

$$\tan\theta = \Delta v_{mq}/\Delta v_{md} \tag{11}$$

where θ is the angle of vector both $\boldsymbol{V}'_m$ and $\boldsymbol{V}_m$. Besides, for the PI controller, the expressions of Δv_{md} and Δv_{mq} in the qusia-steady state are

$$\Delta v_{mk} = k_i\left(i'_{kref} - i_k\right)(t_2 - t_1), \quad k = d, q \tag{12}$$

where k_i is the integral coefficients of the PI controller.

If d axis of the synchronous rotating reference frame is orientated at the direction of the voltage vector of PCC, the relationship between inverted voltage $\dot{V}_{IIDG.f}$, inverter current and voltage of PCC in vector form could be derived from Figure 2 as:

$$\dot{V}_{IIDG.f} = U_{\mathrm{PCC}} + \left(i_d + ji_q\right)(R + j\omega L) \tag{13}$$

Meanwhile, the inverted voltage can be written as

$$\dot{V}_{IIDG.f} = v_d + jv_q = V_{\max}\angle\theta \tag{14}$$

where, $V_{\max}$ is MIV and equals $M\cdot V_{dc}$.

Simultaneously solve (11) - (14) and ignore R, we get

$$\theta = \arcsin\left\{\frac{i'_{dref}X_l V_{\max} - \left(U_{\mathrm{PCC}} - i'_{qref}X_l\right)x}{\left[\left(U_{\mathrm{PCC}} - i'_{qref}X_l\right)^2 + \left(i'_{dref}X_l\right)^2\right]}\right\} \tag{15}$$

where, $x = \sqrt{\left(U_{\mathrm{PCC}} - i'_{qref}X_l\right)^2 + \left(i'_{dref}X_l\right)^2 - V_{\max}^2}$, $X_l = \omega L$

It can be seen from (15) that the inverter model of stage 2 is a controllable voltage source whose amplitude equals MIV and angle equals the solution of (2) and (15).

D. MODEL MERGING

The whole fault model could be obtained by merging the model of FRT control strategy described by (1) and the inverter model described by (9) or (2), (11)-(14). If the current order given by (1) within the invert capacity of the inverter, (4) holds and the inverter model of stage 1 is used. In this case, jointing (1) and (9) we get

$$\begin{cases} i_q = \max\left\{K_q\Delta U_{\mathrm{PCC}}, -I_{\max}\right\} \\ i_d = \min\left\{P_{ref}/U_{\mathrm{PCC}}, \sqrt{I_{\max}^2 - i_q^2}\right\} \end{cases} \tag{16}$$

It is obvious from (16) that the IIDG could be modelled as a voltage-controlled current source where the control variable is U_{PCC}, and the interface variable between IIDG and grid is the injection current of the IIDG. The fault model in stage 1 can also be expressed in the vector form as (17), which is the same as the model used in [16].

$$\dot{I}_{IIDG.f} = i_d + ji_q = f_d(U_{PCC}) + jf_q(U_{PCC}) \tag{17}$$

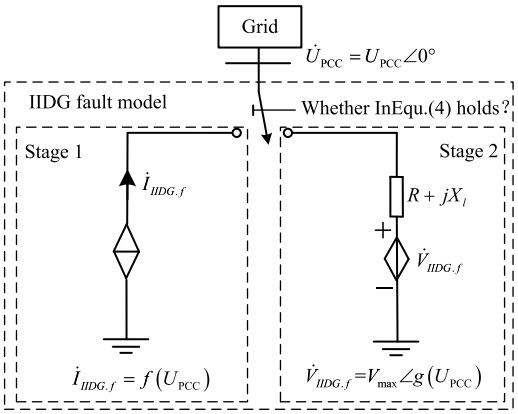

FIGURE 5. Fault model of PQ controlled, two-level VSC interfaced IIDG.

where $\dot{I}_{IIDG.f}$ is the injection current of IIDG in vector form.

If the current order given by (1) goes beyond the invert capacity of the inverter, (4) doesn't hold and the inverter model of stage 2 must be used. In this case, jointing (1), (2) and (11)-(14), the phase angle of the inverted voltage could be solved as in (15), and IIDG could be modelled as a voltage source in series with an impedance. The amplitude of the voltage source is MIV and its phase angle is the function of U_{PCC} as in (18). The series impedance is the equivalent impedance of the AC filter.

$$\dot{V}_{IIDG.f} = V_{\max}\angle\theta = V_{\max}\angle g(U_{PCC}) \tag{18}$$

The whole fault model composed of 2 stages is shown in Figure 5. Firstly, (4) is checked to select the stage model to be used. Then the corresponding equations are solved to determine the parameters of the model. Finally, the multiple IIDG's fault models are simultaneously solved to calculate the nodes' voltage, fault current and the other fault variables of the whole system.

III. PROCESS OF APPLYING PROPOSED MODEL IN FAULT ANALYSIS OF DN WITH IIDGS

Generally, the process of the fault analysis of DN is first to find out the voltage of all buses by the node voltage method and then calculate the other fault variables such as fault current based on the buses' voltage. The buses' voltage could be calculated based on the network equation below:

$$\boldsymbol{Y}\boldsymbol{U}_n = \boldsymbol{I}_s \tag{19}$$

where $\boldsymbol{Y}$ is the node admittance matrix of the DN that taking fault condition such as ground resistance of the fault point into consideration; $\boldsymbol{U}_{\mathrm{n}}$ is the voltage vector of all buses; $\boldsymbol{I}_{\mathrm{s}}$ is the node injection current vector of all buses. The components in $\boldsymbol{I}_{\mathrm{s}}$ equal the equivalent injected currents when there is a power source connecting to the bus, and is zero otherwise.

For DN with IIDGs, the fault analysis has almost the same process as above, except that the influence of IIDGs should be considered as the model presented in Figure 5. That influence mainly includes two aspects: first, the voltage vector Un

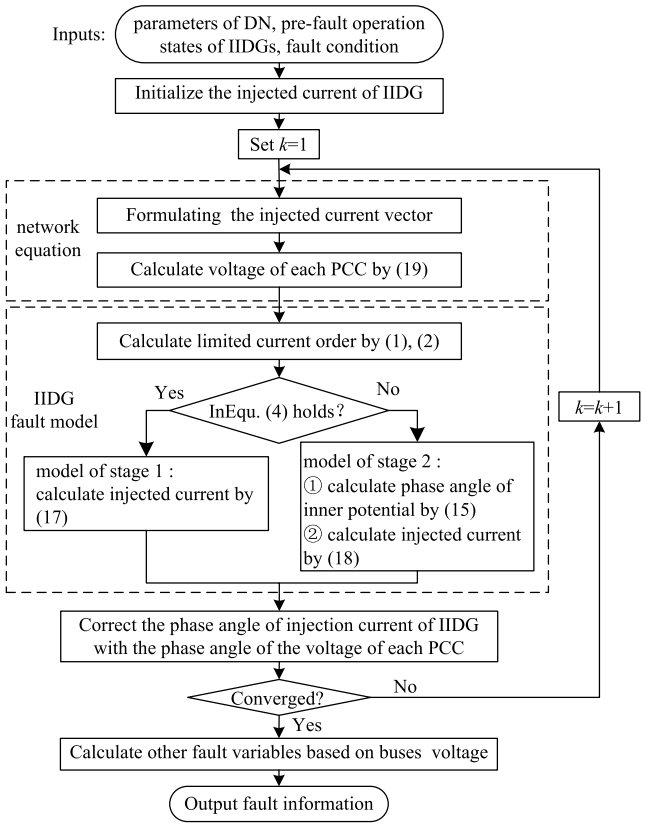

FIGURE 6. Flow chart of the fault analysis of DN with IIDGs.

must be extended to include all the PCCs' voltage of IIDGs; second, equivalent injected currents of all IIDGs should be contained in $\boldsymbol{I}_s$. As parameters of the IIDGs' fault model are the function of PCC voltage, which is further impacted by the IIDGs' equivalent injected current, the IIDGs interact with the grid in a much more complex way than traditional synchronous generator whose inner potential is fixed during the fault. Therefore, it is hard to solve the network equation of DN and the model equation of IIDGs simultaneously. Here, we decouple these two sets of equations by solving them alternatively. Through alternative calculation, the solution finally converges to the real value after several iterations.

The flow chart of the fault analysis of DN with IIDGs is shown in Figure 6. The fault analysis starts from the inputs of the parameters of distribution network, pre-fault operation states of IIDGs as well as the fault condition. Usually, the injected currents of the IIDGs are initialized to the pre-fault value to launch the iteration. Then the network equation of DN is solved to get the voltage of each node including the PCC of IIDGs. The voltage of PCC is the index of the severity of a fault and is used to select the stage model of IIDG according to (4). The selected IIDG fault model is then calculated to get the new equivalent injected currents. The injected currents are rotated from the U_{PCC} frame to the unified frame of DN, and enters the next iteration. In each iteration, the U_{PCC} or the equivalent injected current vector variation are tested to detect the convergence of the iteration. The other fault variables such as fault currents of fault point or specified lines are calculated and output after the calculation converges.

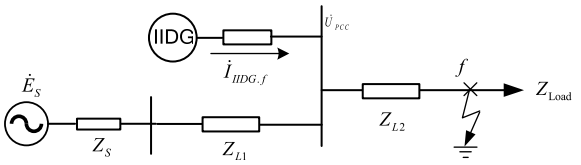

FIGURE 7. Diagram of the system with one IIDG.

IV. CASE STUDY

In order to verify the proposed model, fault analyses of two scenarios are carried out. The first scenario is the system with one IIDG and the model accuracy under different voltage dip degree is analyzed. The second scenario is the modified IEEE 13 nodes system with four IIDGs and the impact of different fault modelling methods of IIDG on the fault analysis as well as on the protection system is analyzed.

A. SCENARIO 1

The system studied is shown in Figure 7 and the parameters are given in appendix A. The system is very simple that a single power source supplies a single load through a transmission line. The IIDG is connected at the one-third length of the line near the load side with rated output power. The rated power and power factor of IIDG is 500kW and 0.98, the switching frequency f_s and the allowed harmonic current $\Delta i_{\max}$ are 5kHz and 5% respectively, the amplitude of DC voltage is 3 times the phase-ground voltage of AC side. The AC filter is designed as in [1] and its reactance is $0.5j$ pu. Besides the step-up transformer of IIDGs with impedance $0.04j$ pu. are considered during the analysis. The FRT control strategy has the form shown in (1) and $K_q = 2$, $I_{\max} = 2$.

Three methods are used in the fault analysis when there is a three-phase short circuit occurs at f point (PCC of the load) in Figure 7. Method 1 ignores the impact of IIDGs by assuming they are disconnected from the grid during the fault period. Method 2 models IIDG as in [15], which only considers FTR control and uses the current source model, and this is actually the stage 1 model in Figure 5. Method 3 considers both FTR control and inverter's characteristic, and models IIDG as a stagewise model in Figure 5. Both method 2 and method 3 adopt the same calculation flow shown in Figure 6. Besides, the simulation results of PSCAD/EMTDC, a commercial software commonly used for electromagnetic transient analysis, are presented as the true values of the fault variables.

The voltage of PCC, current and invert voltage of IIDG calculated by three methods and simulation are shown in Table 1 for different transition resistance. It is obvious that results obtained by method 2 and method 3 are more consistent with the simulation results, especially method 3.

In order to compare the results of different fault modelling method more clearly, the percentage of error vector (referred to as "error" for short) was used to describe the amplitude

TABLE 1. The voltage of PCC, current and invert voltage of IIDG(p.u.).

R_f		Method 1	Method 2	Method 3	Simulation
	V_{PCC}	**0.14∠-48.8°**	**0.23∠-31.8°**	**0.23∠-31.8°**	**0.23∠-32.3°**
0.01	I_{IIDG}	——	2.00∠-82.0°	2.00∠-82.0°	2.00∠-82.2°
	V_{IIDG}	——	1.19∠0.9°	1.19∠0.9°	1.19∠-0.4°
	V_{PCC}	**0.21∠-54.2°**	**0.31∠-41.7°**	**0.31∠-46.7°**	**0.31∠-46.1°**
0.02	I_{IIDG}	——	2.00∠-85.5°	1.92∠-99.6°	1.92∠-96.4°
	V_{IIDG}	——	1.23∠-5.9°	1.22∠-18.5°	1.22∠-16.4°
	V_{PCC}	**0.43∠-50.8°**	**0.53∠-47.4°**	**0.50∠-54.6°**	**0.50∠-53.5°**
0.06	I_{IIDG}	——	2.00∠-65.9°	1.45∠-109.9°	1.43∠-104.3°
	V_{IIDG}	——	1.34∠2.2°	1.22∠-33.3°	1.22∠-31.4°
	V_{PCC}	**0.60∠-42.4°**	**0.69∠-38.3°**	**0.69∠-38.3°**	**0.69∠-39.1°**
0.1	I_{IIDG}	——	1.52∠-55.9°	1.52∠-55.9°	1.52∠-56.2°
	V_{IIDG}	——	1.22∠1.4°	1.22∠1.4°	1.22∠0.9°

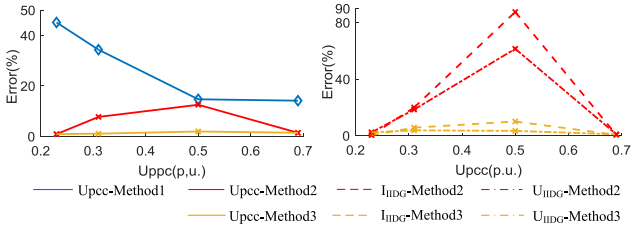

FIGURE 8. Error of the PCC voltage, current and invert voltage of IIDG.

and phase difference of vectors simultaneously. The percentage of error vector defined as $\Delta F_c\% = |(\dot{F}_c - \dot{F})/\dot{F}|$, where $\dot{F}_c$ is the calculated vector and $\dot{F}$ is its true value calculated by simulation. Based on the data in Table 1, the calculation errors of each method under different voltage dip degree are shown in Figure 8.

From Figure 8 it is clear that the calculated PCC voltage error of method 1 is greater than 10% and increases to 50% when the voltage dips deeply. However, that of method 2 and method 3 are much smaller especially when the voltage dip degree at the ends. The error of method 2 is the same as method 3 when the voltage dip degree at the ends, but the former becomes greater than the latter dramatically when the voltage dip degree is medium. This is because the reactive support requirement of FRT exceeds the invert capacity of the inverter in the medium voltage dip degree, then the modulation wave limitation occurs in this situation. Method 3 takes into account this characteristic thus obtains smaller error. From the above comparison, we can conclude that the IIDG should not be ignored in the fault analysis of the DN with IIDGs, especially when the voltage dip degree is high.

B. SCENARIO 2

The original IEEE 13 node test feeder could be found in [20] and it was modified in two aspects: 1) the parameters of the load and the transmission line are averaged between three phases if they are unbalanced to make it suitable for symmetrical fault analysis. The modified parameters are also

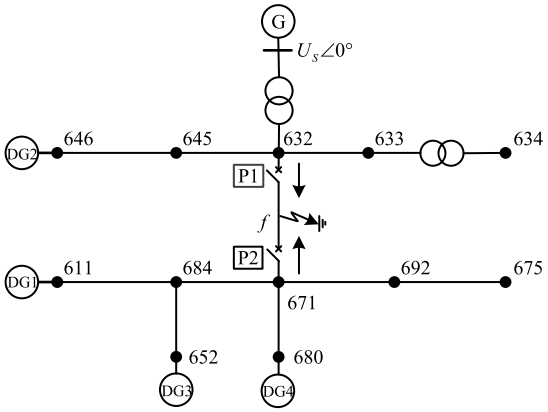

FIGURE 9. Diagram of modified IEEE 13 nodes DA with four IIDGs.

TABLE 2. The fault currents calculated.

position	Method 1	Method 2	Method 3	Simulation
P1	29.5∠-31.3°	28.6∠-27.2	30.0∠-28.3°	29.9∠-28.3°
P2	2.8∠133.0°	2.7∠-48.8°	2.6∠-129.1°	2.2∠-129.0°
f	27.0∠-29.8°	31.2∠-29.1°	29.7∠-33.2°	29.6∠-32.9°

TABLE 3. The fault voltage of the nodes.

Node	Method1	Method 2	Method 3	Simulation
650	0.64∠-2.7°	0.68∠-4.9°	0.65∠-5.6°	0.65∠-5.3°
632	**0.51∠-19.0°**	**0.58∠-19.6°**	**0.55∠-22.6°**	**0.55∠-22.1°**
634	0.50∠-19.6°	0.56∠-20.2°	0.53∠-23.2°	0.53∠-22.6°
646	0.51∠-19.1°	0.58∠-19.3°	0.55∠-22.5°	0.55∠-22.0°
671	**0.46∠-30.7°**	**0.55∠-28.3°**	**0.52∠-33.6°**	**0.52∠-32.8°**
611	0.46∠-30.8°	0.55∠-27.9°	0.53∠-33.5°	0.53∠-32.7°
675	0.46∠-30.9°	0.55∠-28.5°	0.52∠-33.7°	0.52∠-33.0°

given in appendix A; 2) four IIDGs with the same parameters as in scenario 1 are connected to node 611, 646, 652 and 680 as shown in Figure 9 with the total capacity of 2MW, accounting for about 60% of the total load. The output of four IIDGs before the fault are all 1.0 pu and the a three-phase short circuit is assumed to occur at f point (the midpoint of the line between node 632 and 671) in Figure 9 with the transition resistance equals 0.017 pu (0.6 Ω). The same three methods as previous are used, and the calculated fault currents of P1, P2, f point as well as nodes' voltage are given in Table 2, Table 3 and Figure 10.

From Figure 10 we can see that the nodes' voltage error of method 1 is around 10% and the nearer to IIDG larger the error is. The error is decreased to about 7% by method 2 and further decreased dramatically to around 2% by method 3. The error of fault current shows the similar pattern but with much greater value, especially for the current of the IIDG side (P2). These results are similar to the comparison in scenario 1.

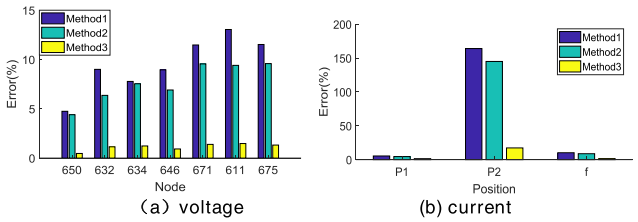

FIGURE 10. Error of fault current and nodes' voltage of three methods.

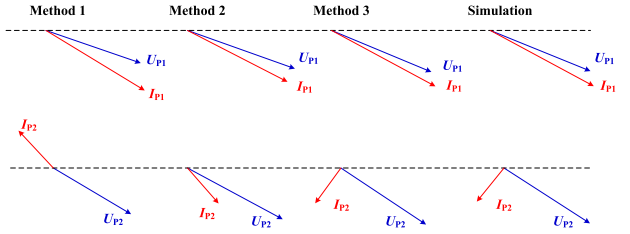

FIGURE 11. Current and voltage phasor of P1 and P2.

Usually, the relative relationship between voltage and current is more likely to be used in fault diagnosis of the multi-power network. Therefore we assume there are protection equipment in P1 and P2 to check the possible impact of the above difference on the protection system. The current and voltage phasor of P1 and P2 could be drawn as in Figure 11 based on the data in Table 2 and Table 3.

It is clear that the relative positions of current phasor and voltage phasor in P1 (gird side) are almost the same for the calculation results of three methods and the simulation. This indicates that the fault current induced by the main power source is almost unaffected by IIDGs. The phase lag and the amplitude of the current is slightly over estimated if ignores the influence of IIDGs. While the relative positions of current phasor and voltage phasor in P2 (IIDG side) are quite different for the three methods and the simulation. For method 1, the current I_{p2} is almost opposite in phase with the voltage U_{p2}, indicates the active power flows from the fault point to the node 671 bus. As the IIDGs are ignored in method 1, this is the typical relationship of a single-power network. For method 2, the current I_{p2} lags U_{p2} with a phase about 20°, indicates the active power flows from node 671 bus to the fault point, coinciding with the pattern of the double-power network. However, for the method 3 and the simulation, the current I_{p2} is almost vertical to U_{p2}, indicates that nearly no active power flow between node 671 bus and the fault point, quite different from the results of method 2. If directional power protection is utilized in this situation, the results of method 2 support its effectiveness but will deviate from the reality and malfunction in practice.

The reason for the above difference is the different modelling method of the IIDG during the fault, which further brings different impact. The injection current and the inverted voltage of IIDG calculated by each method is shown in Table 4. Method 1 assumes the IIDGs are disconnected from the grid during the fault, thus the IIDGs' impact is isolated. Method 2 takes the support of the IIDGs during the fault into consideration and assumes that the injection current of IIDG equals the order given by FRT control. However, the assumption of method 2 may break the limitation of the inverter in IIDG, leading the calculation results to deviate from its real value. As the data in the third column of Table 3, the inverted voltage of IIDGs are greater than the MIV (here is $3/\sqrt{6} = 1.225$) to make sure the injection current track the order given by FRT, which breaks the inverters' limitation. Method 3 takes both the support of the IIDGs and the limitation of the inverter into consideration, fixes the inverted voltage of the IIDG at MIV when it reaches the limit point, thus calculation results of method 3 fits the simulation results best.

TABLE 4. The injection current and inverted voltage of IIDGs.

	Method 1	Method 2	Method 3	Simulation
I_{IIDG1}	——	1.92∠-46.63°	1.41∠-86.78°	1.42∠-84.40°
I_{IIDG2}	——	1.83∠-38.27°	1.39∠-73.00°	1.39∠-71.24°
I_{IIDG3}	——	1.91∠-46.39°	1.41∠-86.46°	1.42∠-84.13°
I_{IIDG4}	——	1.92∠-46.53°	1.41∠-86.63°	1.42∠-84.29°
V_{IIDG1}	——	1.321∠20.14°	1.225∠-11.65°	1.225∠-9.89°
V_{IIDG2}	——	1.297∠26.85°	1.225∠0.46°	1.225∠1.68°
V_{IIDG3}	——	1.319∠20.29°	1.225∠-11.47°	1.225∠-9.85°
V_{IIDG4}	——	1.320∠20.20°	1.225∠-11.55°	1.225∠-9.91°

The difference of IIDGs' voltage and current calculated by each method further leads to the different results of the whole network as in Table 2 and Table 3. The overall amplitude of the nodes' voltage calculated by method 1 is smaller than the simulation results because method 1 omits the support of IIDGs during the fault period. Method 2 increases the overall voltage of the distribution network but goes too far to be greater than the simulation results, as it takes the support of IIDGs into account but omits the limitation of their supportive ability. Method 3 considers the support of IIDGs in accompany with their limitation by utilizing a detailed fault model of IIDG, and therefore achieves the most consistent results with that of the simulation.

V. CONCLUSION

As more and more IIDGs integrated into the distribution network, the fault characteristics of IIDG and its impact should be evaluated properly. This paper proposes a new modelling method of IIDG that first models the FRT control strategy and inverter separately and then merge the two models to form the entire model that could consider each part of IIDG in detail. The PQ controlled, two-level VSC interfaced IIDG was modelled for the symmetrical fault analysis by the proposed method as a two-stage model that composes of a voltage-controlled current source and a voltage-controlled voltage source and are switched depending on whether the modulation wave is limited. The two-stage model could consider the detailed characteristics of the inverter in different situations such as the limitation of the modulation wave.

The comparative study of the three-phase fault analysis using different IIDG modelling method on the simple system

TABLE 5. Line segment data.

E_s	Z_s	Z_{L1}	Z_{L2}	Z_{Load}
1.0	0.1j	0.013+0.0175j	0.0065+0.0088j	1.88+0.470j

TABLE 6. Line segment data.

Node A	632	632	645	650	684	632	671	671	684	692
Node B	645	633	646	632	652	671	684	680	611	675
Length(ft.)	500	500	300	2000	800	2000	300	1000	300	500

TABLE 7. Load and capacitor data.

Node	634	645	646	652	671	675	692	611	Total
P(kW)	400	170	230	128	1255	843	170	170	3466
Q(kVar)	290	125	132	86	776	462	151	80	2102
Cap (KVar)	--	--	--	--	--	600	--	100	700

with an IIDG and the modified IEEE 13 nodes system with four IIDGs demonstrates that:

1) IIDGs should be taken into consideration in the fault analysis otherwise the magnitude of the nodes' voltage will be underestimated and the direction of the fault current from downstream may be opposite to its real direction;

2) modelling IIDGs with a controllable current source that ignores the limitation of the inverter may overestimate the support of IIDGs, resulting in a higher calculated nodes' voltage and an off-direction downstream fault current;

3) modelling IIDGs with the two-stage model proposed can consider the support of IIDGs as well as the limitation of the inverter, the calculated results thus are most consistent with that of the transient simulation.

The paper mainly focuses on the symmetrical fault model of the IIDG, how to extend the proposed method into asymmetrical fault modelling of IIDG is the next work.

APPENDIX A
PARAMETERS OF SYSTEM IN SCENARIO 1

The parameters of system in scenario 1 is show in Table 5. E_s and Z_s are the equivalent potential and equivalent impedance of infinite power system, Z_{L1} and Z_{L2} are the line impedance and Z_{Load} is the equivalent load impedance. All the parameters are in per unit with power base 500 kVA and the voltage base 10kV.

APPENDIX B
PARAMETERS OF MODIFIED IEEE 13 NODE SYSTEM IN SCENARIO 2

The distribution network with IIDGs in scenario 2 is obtained by modifying IEEE 13 node test feeder in [20]. In this network, all lines are modified to three-phase symmetrical lines and the total load is equally divided into three phases.

Node 650 is the low voltage bus of the substation. The amplitude of voltage source that equals the infinite upstream system of substation is 120.75kV and SCR equals 10. The lengths of the line segments are shown in Table 6 and resistance, reactance and susceptance of per mile are 0.1860Ω, 0.5968Ω and 7.2923mS. The load and compensation capacitor data are shown in Table 7. The other data are same as [20].

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