IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received September 7, 2020, accepted September 21, 2020, date of publication September 25, 2020,
date of current version October 13, 2020.

Digital Object Identifier 10.1109/ACCESS.2020.3026744

Discriminating Between Capacitor Bank Faults and External Faults for an Unbalanced Current Protection Relay Using DWT

PRAIKANOK LERTWANITROT AND ATTHAPOL NGAOPITAKKUL, (Member, IEEE)
Department of Electrical Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand
Corresponding author: Atthapol Ngaopitakkul (atthapol.ng@kmitl.ac.th)

ABSTRACT Capacitor faults are a common issue in modern-day power systems. Such systems employ a traditional mechanism that solely relies on unbalanced relays as an indicator of faults in capacitor banks; however, in the case of a relay trip, operators may find it difficult to identify the cause of these faults. To address this issue, this study aims to detect and discriminate between faults in the capacitor bank (i.e., internal faults) and those in the transmission line (i.e., external faults) by employing discrete wavelet transform (DWT). For this purpose, simulations were conducted using PSCAD software and modelled according to the 115-kV system from the Electricity Generating Authority of Thailand (EGAT). Furthermore, case studies involving faults with different phases, side and branch connections, row connections, inception angles, and blown fuses were considered. Moreover, the phase current, unbalanced current, and unbalanced voltage were analyzed to elucidate fault behaviors and the variation in the coefficient obtained via DWT; the unbalanced current and unbalanced voltage were used as design criteria for the proposed detection and relay operation algorithm. Real-world signals were employed to verify the accuracy of the proposed model. The results indicate that the proposed algorithm achieves satisfactory accuracy in terms of fault detection and the operation of relays in capacitor banks. The proposed algorithm is expected to enable an improvement in the performance of protection systems for capacitor banks in the near future.

INDEX TERMS Fault, detection, capacitor bank, discrete wavelet transform, unbalance relay.

I. INTRODUCTION

Currently, economic development has led to an increase in the demand for power. Consequently, it is necessary to increase the capacity of existing power systems, while expanding the power grid to cover all usage areas. However, this would require an increase in the number of substations, which, in turn, would increase the complexity of power systems. Capacitor banks are typically used to increase the voltage and control the reactive power within substations, which improves the efficiency of power transmission. The rating and type of capacitors used in such banks depend on system requirements. A single capacitor bank installed in the bus is termed as an ''isolated capacitor bank.'' Isolated capacitor banks are more suitable for simple systems, as compared to ''back to back capacitor banks,'' which refer to more than two capacitor banks installed in the same bus and are more apt for complex systems [1], [2].

Capacitor banks comprise several capacitor units, and each unit contains capacitor elements (Ce). There are three types of connections for the capacitor units: single wye, double wye, and h-bridge. In addition, the Ce can be connected in four patterns: internally fused, externally fused, fuseless, and unfused. The type of connection depends on the desired capacity and application. For instance, internally fused capacitor banks offer higher capacity than externally fused ones. Moreover, fuseless capacitor banks are capable of alleviating discharge problems. During a fault, the fuse connected to the capacitor unit is blown and the capacitance of the bank is reduced. Therefore, the capacitance of a faulty bank is lower than that of a healthy bank. In such cases, although the current flowing through the faulty unit ceases, the voltage continues to increase [3], [4]. Therefore, if such faults are not resolved quickly, the entire substation would need to be shut down, thereby degrading the reliability of the power system.

The associate editor coordinating the review of this manuscript and approving it for publication was Norbert Herencsar.

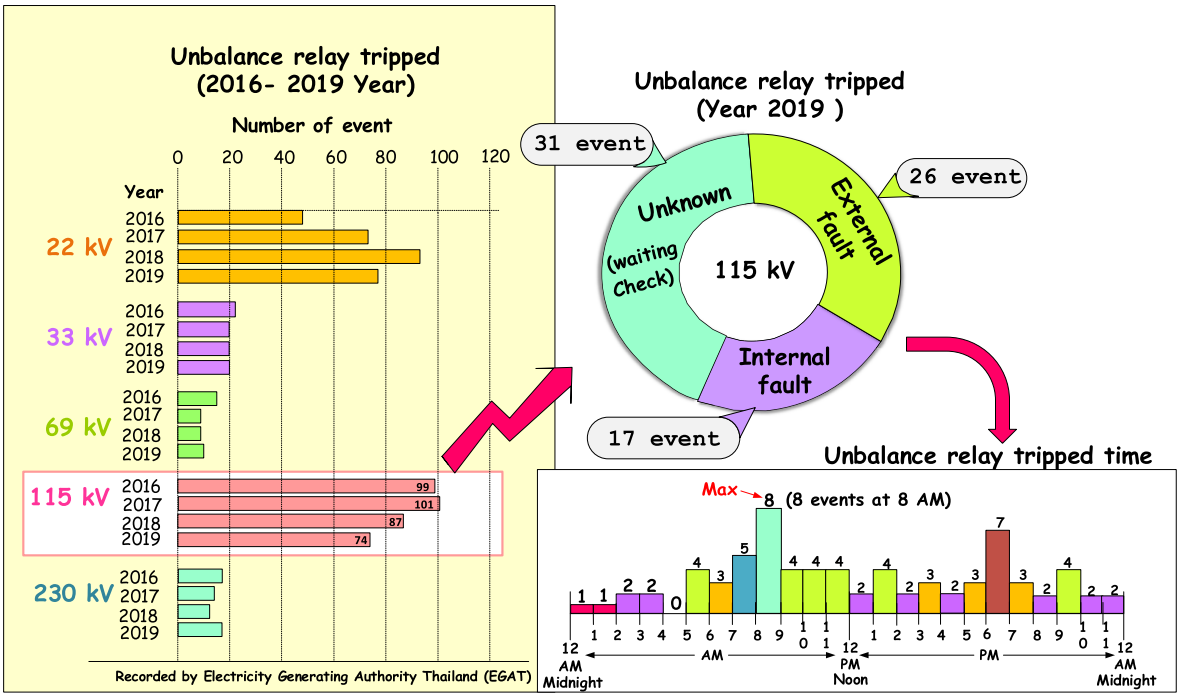


FIGURE 1. Trip events of the unbalance relay from 2016 to 2019 in Thailand.

When a fault occurs within a capacitor unit, the three phase current passing through it is unbalanced. This unbalance occurs due to a reduction in the impedance caused by the fault, which leads to an asymmetric and unbalanced system. Thus, the current for the phase at which the fault occurred decreases, whereas the neutral current increases. Moreover, the capacitance of this faulty phase also decreases. This behavior triggers the operation of the unbalance relay, which is an equipment used for protecting capacitor banks from unbalanced loads. In an unbalance relay, unbalanced current is measured via a current transformer (CT) and compared to the setting (pick-up) value. If the unbalanced current is lower than the pick-up value, the relay does not function (block); otherwise, the relay triggers alarm or trip circuits. Such trip events recorded by the Electricity Generating Authority of Thailand (EGAT) for the period 2016–2019 are presented in figure 1. This figure indicates that such unbalances are unavoidable events that frequently occur in power systems. Considering 2019, it is evident that a total of 74 trip events were recorded for 115 kV. Theoretically, unbalance relay trips occur in the case of faults within the internal zone protection. However, the recorded data of EGAT indicate that, among the 74 trip events observed, 26 events were the result of external faults. Moreover, only 17 events were caused by internal faults; it was unclear whether the remaining 31 events were caused by internal or external faults. These discrepancies indicate that the unbalance relay used was ineffective in terms of detecting and locating faults in the capacitor bank. Therefore, it is necessary to establish a new method to detect faults in capacitor banks.

Based on a literature review [5]–[31], several methods have been proposed for detecting faults in capacitor banks based on parameters such as the phase voltage unbalance phasor [6]–[9], neutral voltage unbalance phasor [10], phase current unbalance phasor [11], and neutral current unbalance phasor [12], [13]–[18]. The method used in [19], [20] employed the superimposed reactance method considering voltage and current; the results proved that the relay algorithm based on measuring unbalance factors was effective and capable of operating even when faults occurred within a short processing time. Previous studies [21]–[23] have also proposed methods based on unbalance factors for detecting faults in capacitor banks, whereby all types of internally fused capacitor banks were considered. These results reveal that the system connected to the ground should analyze unbalance factors based on the neutral current for the purpose of fault detection. Moreover, single wye connections should be analyzed based on voltage differences, whereas double wye and h-bridge connections should be analyzed according to differences in the current. However, these studies were unable to accurately locate fault positions; they could only indicate the phase or zone of faults. When considering a systematic component [24]–[27], the voltage and current of all sequences depend on the unbalanced conditions [24]; however, zero-sequence voltage and current can be used to estimate the fault position in a distribution system [25]. Similarly, the Fourier transform (FT) of zero-sequence voltage and current has been employed to obtain the vectors of voltage and current. In addition, the direction of negative sequences was calculated via Discrete Fourier Transform (DFT) [29].

To summarize the case studies in literature, including the statistical data from EGAT, it is evident that fault detection incapacitor banks is generally achieved by measuring the magnitude and phase angle of the unbalanced voltage or current. Moreover, the traditional unbalance relay, which is solely based on unbalanced current, was inadequate for realizing satisfactory accuracy in identifying the cause of faults in the capacitor banks. Thus, this study focuses on improving the detection of faults in capacitor banks and discriminating between faults in the capacitor bank (i.e., internal faults) and those in the transmission line (i.e., external faults).

The novelty and primary contributions of this study are summarized as follows:

- This study investigates the behavior of the faults in capacitor banks (i.e., internal faults) and those in the transmission line (i.e., external faults) under various conditions.
- The position of the faulty capacitor unit, such as on the side of a wye connection or the branch of a parallel connection; the connection rows; and the number of blown fuses are considered as system parameters. The unbalanced current and voltage are used as the criteria for these system parameters in order to design the proposed algorithm.
- The proposed algorithm, based on the discrete wavelet transform (DWT) methodology, offers considerable benefits, such as quick fault detection, accurate identification of fault causes, and accurate operation of relays, as compared to the conventional method employed by EGAT.
- Real-world signals recorded during the occurrence of faults in capacitor banks were used to verify the efficiency and reliability of the proposed algorithm.

The analysis of system parameters and the design of the proposed algorithm are summarized in figure 2; these consist of the following three steps:

First, this study system, which was based on the power system of EGAT, was simulated using PSCAD software, as discussed in Section II. Subsequently, characteristics of the parameters affected by faults in the capacitor units—unbalanced voltage, and unbalanced current—were analyzed, as presented in Section III.

Second, the fault signals obtained from PSCAD were further analyzed via DWT, which is the basis of the proposed detection algorithm. Characteristics of the wavelet coefficient are discussed in Section IV.

Finally, the proposed algorithm for discriminating between internal and external faults, which is based on the system parameters analyzed in the previous step, is presented. The efficiency of the proposed algorithm, as compared with the traditional protection method (EGAT standard), is presented in Section V. Conclusions of this study are drawn in Section VI.

II. HIGH VOLTAGE CAPACITOR BANK SIMULATION

The characteristics of system signals during the occurrence of faults in the capacitor unit was simulated using PSCAD. The system of the Phangnga1 (PNG1) 115-kV substation of EGAT, as depicted in figure 3(a), was considered as a case study. The PNG1 substation is equipped with three capacitor banks consisting of two 48-Mvar capacitor banks and one 39.6-Mvar detuned capacitor bank.

This study only focuses on capacitor bank no. 1 (i.e., the one with a capacity of 48 Mvar); the second bank was neglected in order to simulate an isolated connection and avoid the phenomenon of inrush current. As shown in figure 3(b), capacitor bank no. 1 comprises one connection per phase; these connections are then further divided into two branches, and each of these branches contains ten capacitor units. Furthermore, as shown in figure 3(b), each capacitor unit comprises an array of 9×4 capacitor elements, and each of these elements is internally fused.

As shown in figure 4(a), the PNG1 substation was modeled using PSCAD in order to generate the fault signals. As discussed previously, this case study focuses on the bay on which capacitor bank no. 1 (CAP1) is installed; the internal connections for capacitor bank no. 1, modeled using PSCAD, are presented in figure 4(b). This capacitor bank featured a double wye connection; it was ungrounded and internally fused. The unbalance detection mechanism was installed at the neutral line and measured the voltage and current. The system parameters for the PNG1 substation of EGAT, i.e., the capacitance (c), current phase (I_{bank}), and voltage phase (V_{bank}), were used to determine the parameters required for the PSCAD simulation.

The capacitance of the 48-Mvar capacitor unit is 26.74 μF. The current and voltage phases are 223.25 A and 66.43 kV, respectively. These parameters are used for the normal condition (i.e., without an internal blown fuse). An internal blown fuse indicates that the fault has occurred within a capacitor unit. When a fault occurs, the first fuse is blown, which affects the voltage of the affected phase (Vln), the current in this affected phase (Iph), and the neutral current (In). These parameters—Vln, Iph, and In—are calculated by using the IEEE Guide for the Protection of Shunt Capacitor Banks [4]. The results thus obtained are summarized in TABLE 1; these results are subsequently used to assess the accuracy of the proposed method.

According to the EGAT protection standard, the unbalance relay triggers a trip event when the voltage on any element exceeds 150% of the normal value or the unbalance current exceeds 250 mA. When a single fuse is blown in the capacitor unit, the voltage of the affected element (Ve) does not exceeds 150%, as shown in TABLE 1. Therefore, the unbalance relay does not trigger any event. A similar behavior is observed when two or three fuses are blown. However, when four fuses are blown, the voltage on the affected element is 107.886 kV, which is more than 150% of the normal value; consequently, the unbalance relay triggers a

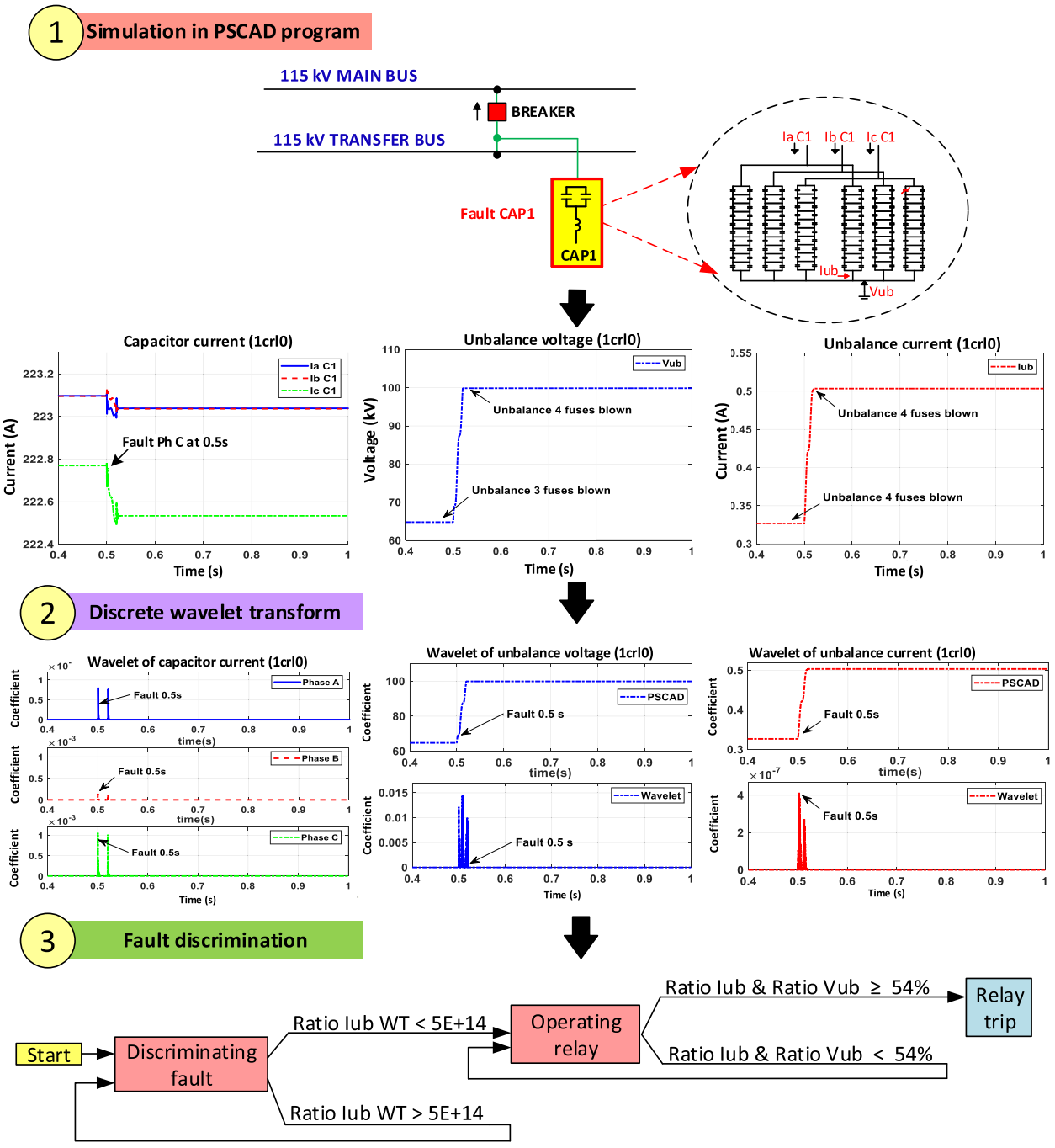


FIGURE 2. Fault classification based on the simulation results from PSCAD.

trip event. In addition, the capacitance of the faulty unit decreases from 26.743 μF to 22.268 μF. Therefore, in the simulation, the capacity of the faulty unit was set as 22.268 μF, whereas the capacity of the healthy unit was set as 26.743 μF.

Additionally, if the relay does not trigger a trip and the fault is not eliminated, the number of blown fuses will continue to increase, causing the capacitance to reduce to zero. As mentioned previously, the voltage and current depend on capacitance. As the capacitance decreases, the current in the affected phase (Iph) also decreases; however, the voltage of the affected phase (Vln) increases. The current of the affected phase directly influences the neutral current (In) and the voltage between neutral and ground (Vng), both of which increase when the fuse is blown.

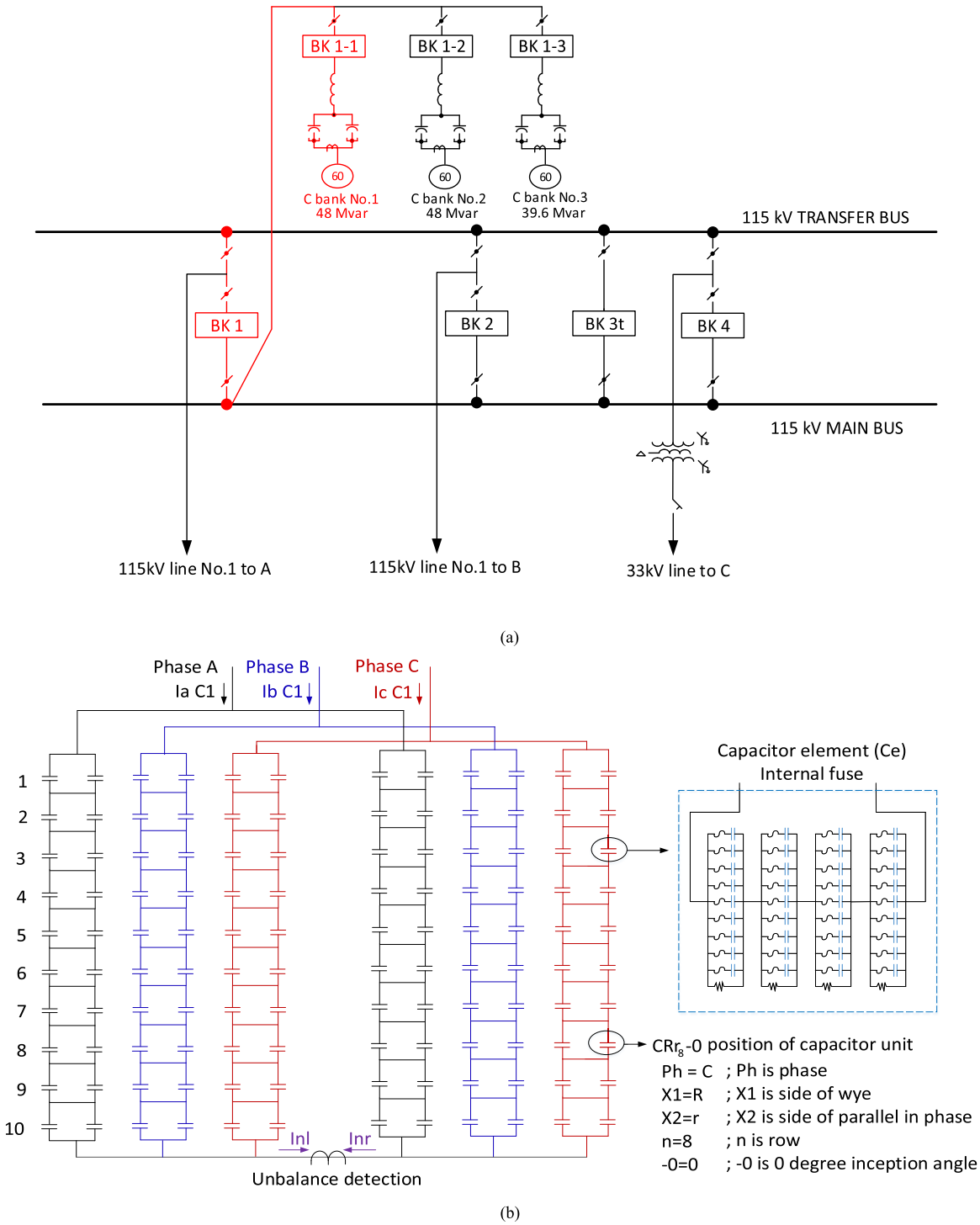
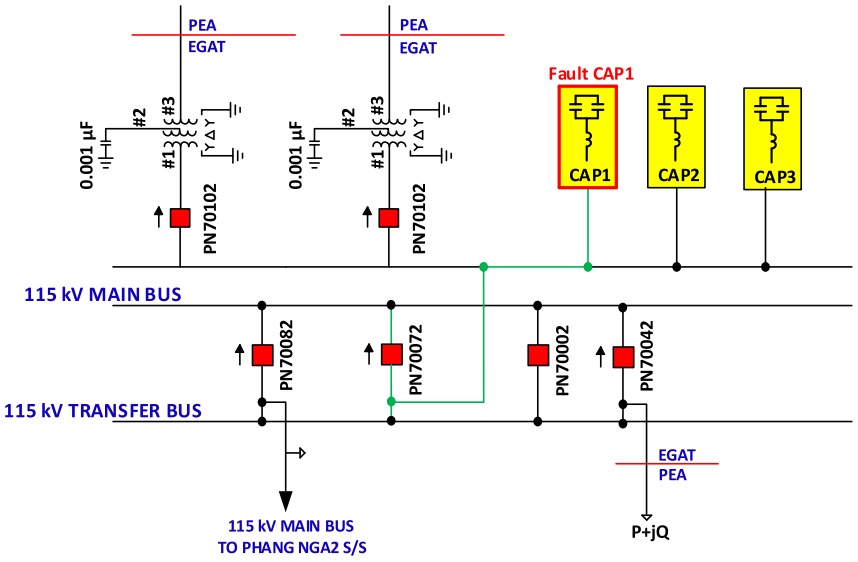


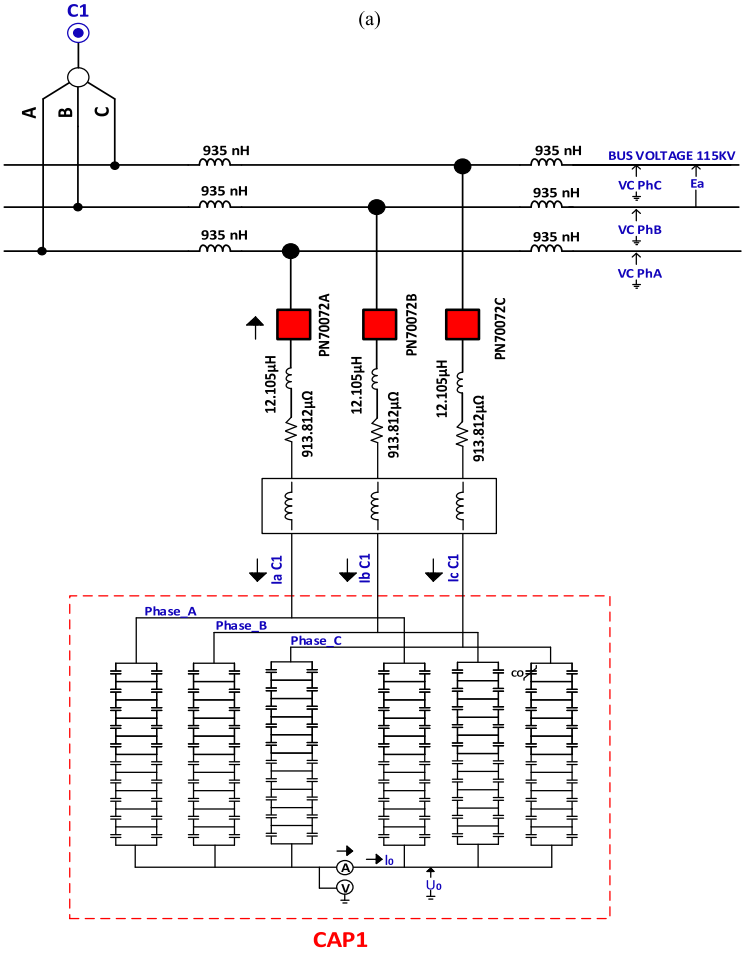
FIGURE 3. (a) PNG1 substation (reference system). (b) Connection in capacitor bank No. 1.

The characteristics of voltage and current under the normal and fault conditions, obtained via the PSCAD simulation, are presented in figure 5 and figure 6, respectively. By considering figure 6, fault occurred in the capacitor unit at phase C, right side of wye connection and left side of branch parallel connection, row number 1 connection with 0 inception angle (CRl_1-0). As recorded by the simulation, which was conducted for 1 s, the capacitor bank energized at 0.15 s, and the fuses were blown at 0.2, 0.3, 0.4, and 0.5 s.

When the power system is operated under the normal condition, the three-phase voltage and current are balanced, as shown in figure 5. When the fault occurs in the capacitor



(a)



(b)

FIGURE 4. (a) Simulation system modeled using PSCAD. (b) Internal connections of capacitor bank no. 1 modeled using PSCAD.

TABLE 1. The fundamental parameters of the capacitor bank.

Internal fuse blown	Capacitor unit (μF)	Voltage neutral to ground (V)	Voltage on affected phase (kV)	Voltage on affected element (kV)	Current in affected phase (A)	Neutral current (A)
0	26.743	0.000	66.430	66.430	223.250	0.000
1	25.933	17.0115	66.447	73.490	223.136	0.086
2	24.960	38.0687	66.468	82.229	222.994	0.192
3	23.772	64.8097	66.495	93.326	222.814	0.327
4	22.286	99.8947	66.530	107.886	222.579	0.504
5	20.376	147.9510	66.578	127.830	222.256	0.746
6	17.829	217.8032	66.648	156.818	221.786	1.098
7	14.263	328.6289	66.759	202.811	221.041	1.657
8	8.914	531.4400	66.961	286.978	219.678	2.679
9	0.000	1022.0000	7.385	490.190	0.969	0.023

bank, characteristics of the voltage under this fault condition are similar to those under the normal condition, as depicted in figure. 5(a) and 6(a). Considering the current shown in figure 6(b), it is evident that all the phase currents were lower than those during the normal condition and that the current of the phase where the fault occurs (i.e., the internal fuse is blown) is lower than those of the other phases. As shown in TABLE 1, as the number of blown fuses continues to increase, the capacitance of the phase is reduced, causing a decrease in the current of the affected phase, which corresponds to the current of phase C in figure 6(b).

In figure. 5(c) and 6(c), which top of the figure was real time signal and bottom of the figure was root mean square (rms) signal. With regard to these figures, for the normal condition, the real-time signal of the unbalanced voltage was a smooth sinusoidal wave, where the rms unbalanced voltage is near zero. On the contrary, both the real-time and rms unbalanced voltage signals continue to increase during the fault condition. Similarly, the real-time and rms unbalanced current signals were near zero in the normal condition, and they continue to increase during the fault condition, as shown in figure 5(d) and 6(d). Both unbalanced voltage and unbalanced current start increasing when the fuse is blown. This effect of phase current result in the unbalance detection point at the neutral line can be detected the unbalance current and voltage.

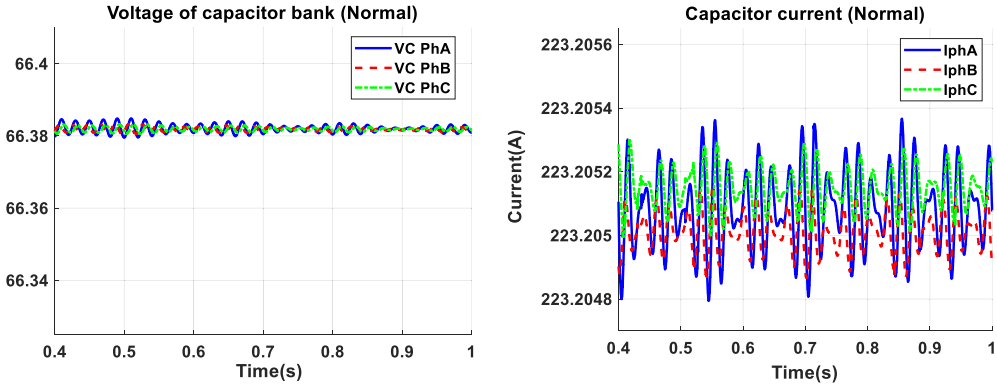
In addition, considering the time of the fault shown in figure 6(b), the current of the affected phase changes when the fuse is blown and shifts toward a new stable state. Thus, when a fault occurs, there is a small delay before the system reaches a new stable state. The unbalanced voltage and unbalanced current also exhibit a similar delay, as shown in figure 6(c) and 6(d), respectively. This delay affected the amplitude value of the unbalance factor from fault occurrence in capacitor bank, so the consideration based on amplitude might measure discrepancies

To clearly differentiate between the faults occurring in the capacitor bank (i.e., internal faults) and those occurring in the transmission line (i.e., external faults), a fault between phase C and the ground on the transmission line was considered as a representative external fault. The parameters in the case of such an external fault, i.e., the voltage phase, current phase, unbalanced voltage, and unbalanced current, are depicted in figures 7(a) to 7(d), respectively.

When a fault occurs between phase C and the ground at time simulation 0.5 s, the phase voltage changes; the voltages of phase B and phase C decrease, whereas the voltage of phase A increases. It is observed that the voltage of phase C is lower than that of phase B.In addition, figure 7(b) indicates that the currents of all the phases increase suddenly when a single line to ground fault occurs, converging to a new stable state that is lower than the normal condition. Based on a comparison between phases, it is found that the currents for phase A and B decrease, whereas the current for phase C, which is the faulty phase, falls below those of the other phases. The unbalanced voltage and unbalanced current in the case of a fault between phase C and the ground are shown in figure 7(c) and 7(d), respectively, where the real-time signals are presented at the top of the figures, whereas the rms signals are shown at the bottom. The unbalanced voltage increases sharply when the fault occurs at 0.5 s. However, the unbalanced current remains zero, similar to that in the normal condition.

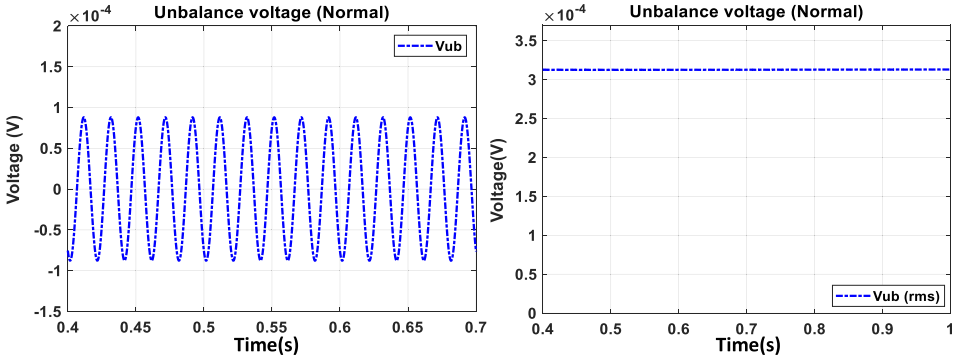
On comparing the internal and external faults, as shown in figure 6 and figure 7, the phase voltage remains unchanged in the case of an internal fault, whereas the phase voltage changes notably after 0.5 s in the case of an external fault. Considering the phase current before 0.5 s, it is evident that the currents of all phases are similar to those in the normal condition in the case of an external fault, whereas the currents in the case of an internal fault are lower than those in the normal condition because three internal fuses were blown.

Furthermore, considering unbalanced voltage and current, in the case of an external fault, the unbalanced voltage was higher than in the case of an internal fault. However, the unbalanced current in the case of an external fault was near zero, whereas the unbalanced current increased in the case of an internal fault. In addition, the delay time was also affected in the case of an external fault (i.e., the fault on the transmission line) as shown in figures 7(a) to 7(c). All the system parameters were changed at 0.5 s and converged to a new stable state, with the exception of the unbalanced current, which was maintained at a value similar to that in the normal condition.

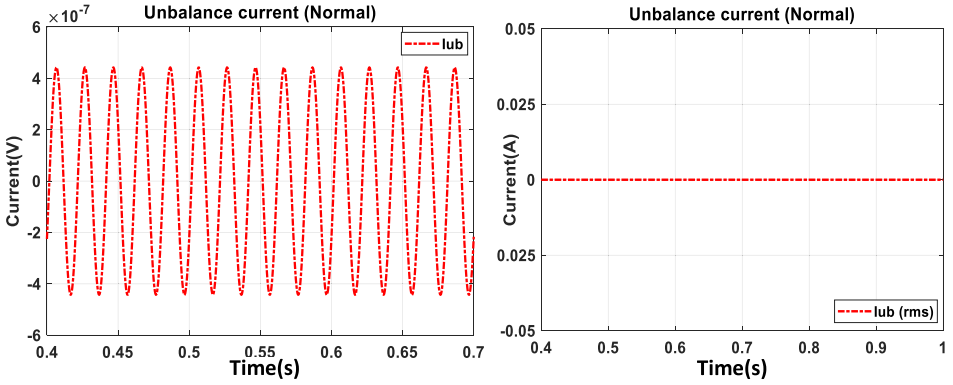


(a) Voltage of the capacitor bank

(b) Current of the capacitor bank



(c) Unbalanced voltage of the capacitor bank

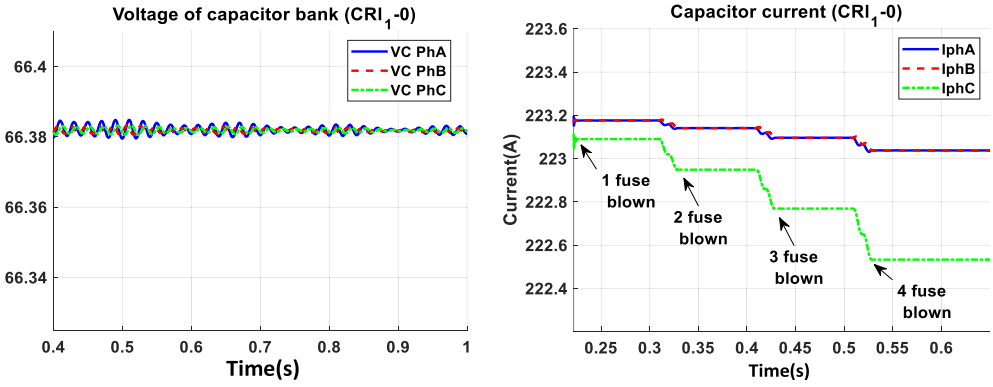


(d) Unbalance current of the capacitor bank

FIGURE 5. Variation in variables under the normal condition.

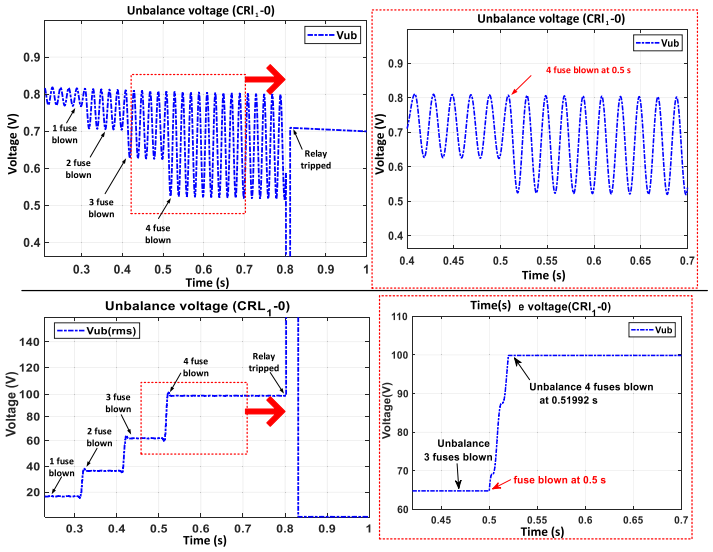
The PSCAD model was verified by comparing the parameters obtained via the PSCAD model to those obtained from the IEEE guide for the Protection of Shunt Capacitor Banks. These parameters were compared under two conditions: the normal and fault conditions; the comparison results are summarized in Table 2. While, the fault in capacitor bank caused each internal fused to continues blown from 1 fuse to 4 fuses. However, the fault condition in this article based on 4 fuse blown at 0.5 s because the voltage on affected element was over than 150% of heathy element and causing the unbalance relay to trips. Thus, the situation of internal fuse blown before 4 fuse blown was not considered.

Considering the data in TABLE 2, the parameters analyzed include reactive power, system voltage (Ea), unbalanced voltage (Vub), unbalanced current (Iub), voltage of the affected phase (Vln), and current of the affected phase (Iph). The results indicate that the PSCAD model generates parameters similar to those obtained via the IEEE calculation, under both normal and fault conditions

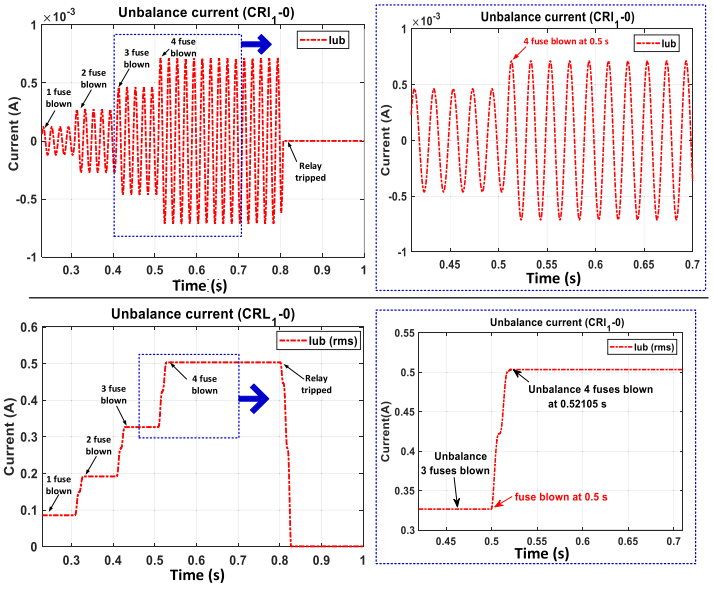


(a) Voltage of the capacitor bank

(b) Current of the capacitor bank

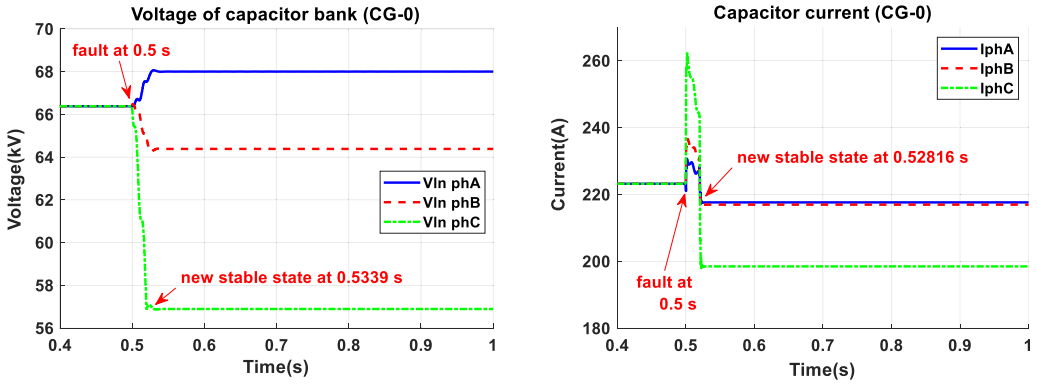


(c) Unbalanced voltage of the capacitor bank



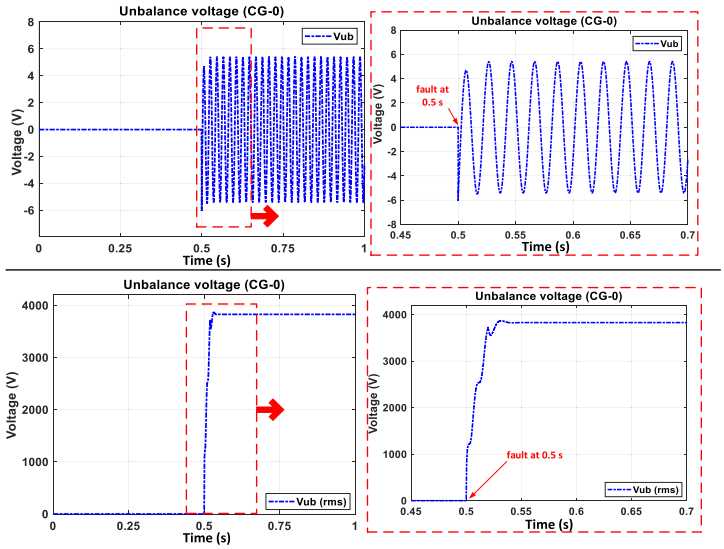
(d) Unbalanced current of the capacitor bank

FIGURE 6. Variations in system parameters when a fault occurs at position CRI_1-0.

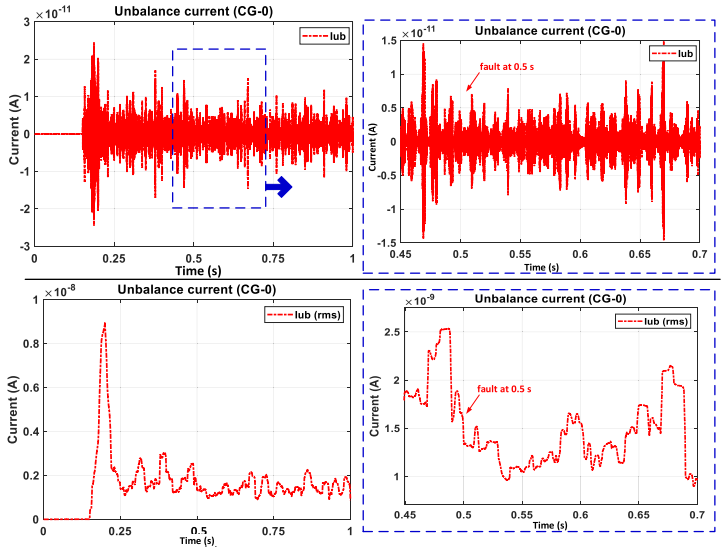


(a) Voltage of the capacitor bank

(b) Current of the capacitor bank



(c) Unbalanced voltage of the capacitor bank



(d) Unbalanced current of the capacitor bank

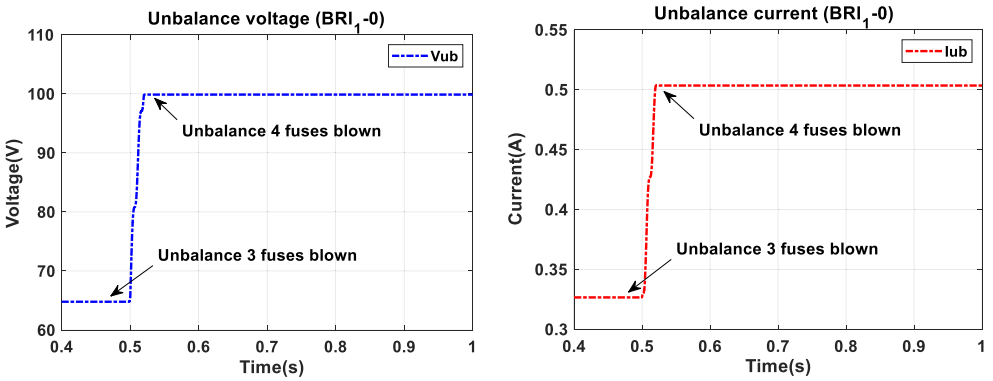
FIGURE 7. **Variation in system parameters when an external fault occurs (SLG:CG).**

III. CHARACTERISTICS OF SYSTEM PARAMETERS

After verifying the accuracy of the PSCAD model, the system parameters were varied in order to validate the proposed algorithm under different conditions. Based on the data from TABLE 1, the unbalance relay triggers a trip event when the voltage on the affected element exceeds 150% of the normal

TABLE 2. Performance between simulation data and calculation data.

Case		Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)	Iph (A)
Normal	PSCAD	44.4503	114.977	0.0013	0.000	66.382	223.205
	IEEE	44.4400	114.970	0.0000	0.000	66.430	223.250
	%Error	0.0232	0.0061	0.13	0	0.0723	0.0202
Fault	PSCAD	44.3880	114.976	94.4220	0.476	66.382	222.577
	IEEE	44.2500	114.970	98.8947	0.504	66.460	222.580
	%Error	0.3119	0.0052	5.4785	5.5556	0.1174	0.0013



a) Unbalanced voltage of the capacitor bank (b) Unbalanced current of the capacitor bank

FIGURE 8. Variations in system parameters for a fault at position BRl_1-0.

value, which occurs when four fuses are blown. Therefore, this section focuses on the characteristics for the condition that a maximum of four fuses are blown. the fault position is varied in terms of the phase, side of the wye connection, branch of the parallel connection, the connection row, inception angle, and number of fuses blown. The reactive power of the capacitor bank, system voltage, unbalanced voltage, unbalanced current, and the voltage and current phase are the system parameters observed.

A. INFLUENCE OF PHASE (ph)

The phase of the fault was varied in order to analyze corresponding changes in the characteristics of the system parameters. Figure 8 presents the change in unbalanced voltage, and unbalanced current when a fault occurred in the capacitor unit at position BRl_1-0. Thus, the unbalance detection pointsinstalled at the neutral line able to detect the unbalance voltage and current which based on the neutral current and voltage as shown in figure 8(a) and 8(b), respectively. Through further analyses and based on a comparison with the position CRl_1-0 shown in figure 6, it was concluded that, even if the fault phase changed from phase C to phase B, the system parameters exhibited a similar trend. This similarity is caused by the capacitor units in both cases, BRl_1-0 and CRl_1-0, having identical values.For a more detailed analysis of the influence of phase on the characteristics of system parameters, the changes with respect to variations in the phase are presented in TABLE 3. Based on the data in TABLE 3, when the fault phase is varied, the position of the fault does not have a significant impact on the system parameters. Moreover, the reactive power depends on the system voltage. The capacity of the capacitor bank was 48Mvar at its rated voltage. As the system voltage was lower than this rated voltage, the capacitance was also lower than 48Mvar.

B. INFLUENCE OF THE SIDE OF FAULT POSITION (X1, X2)

The influence of the fault position can be divided based on the side of the wye connection (X1) and the branch of the parallel (X2) connection; these were varied, both to the left- and right-sides, to analyze their influence on the characteristics of system parameters.

The unbalance voltage and current was observed and compared with the case of a fault at position CRl_1-0, as illustrated in figure 9(a) and 9(b). respectively.

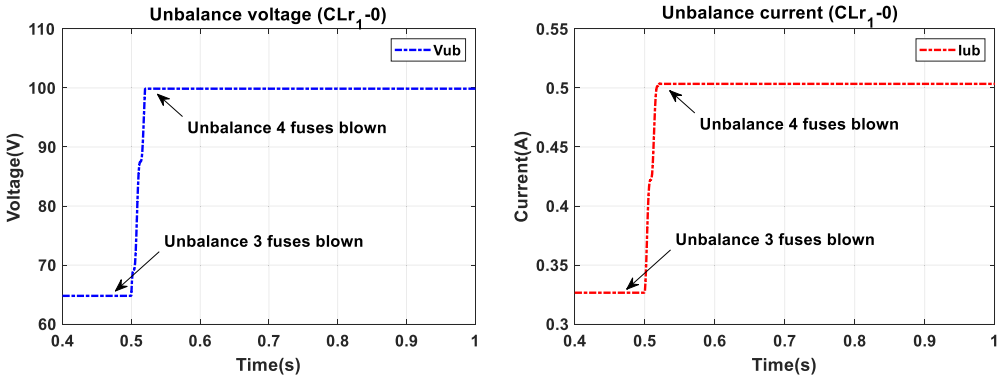
The influence of fault positions on the branch of the parallel connection, the behaviors were the same as those for the side of the wye connection. This is attributed to the capacitor units have the same value, even though the position of the fault was changed. The effects of variations in the side and branch of the fault on the system parameters are displayed in TABLE 4. It can be seen that, even if the side and branch positions of the fault are varied, the system parameters exhibit similar trends because the capacitance value remains unchanged. Therefore, the side or branch positions of a fault do not affect the system parameters.

C. INFLUENCE OF ROW CONNECTION (n)

The row connection was varied to analyze its influence on system parameter characteristics. Figure 10 shows the behavior of unbalance voltage and current when fault occurs

TABLE 3. Behavior of parameter when the fault phase varied.

Case	Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)			Iph (A)		
					phA	phB	phC	phA	phB	phC
Normal	44.4503	114.977	0.0013	0.000	66.380	66.381	66.381	223.205	223.205	223.205
ARl_1-0	44.3885	114.976	94.419	0.476	66.380	66.382	66.381	222.576	223.049	223.047
BRl_1-0	44.3884	114.977	94.494	0.476	66.381	66.381	66.381	223.048	222.578	223.048
CRl_1-0	44.3886	114.976	94.353	0.476	66.380	66.381	66.382	223.047	223.047	222.575



(a) Unbalanced voltage of the capacitor bank

(b) Unbalanced current of the capacitor bank

FIGURE 9. Variations in system variables for a fault at position CLr_1-0.

TABLE 4. Behavior of parameter when side of fault position varied.

Case	Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)			Iph (A)		
					phA	phB	phC	phA	phB	phC
Normal	44.4503	114.977	0.0013	0.000	66.380	66.381	66.381	223.205	223.205	223.205
CRl_1-0	44.3886	114.976	94.353	0.476	66.380	66.381	66.382	223.047	223.047	222.575
CRr_1-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CLl_1-0	44.3886	114.976	94.353	0.477	66.381	66.381	66.382	223.047	223.047	222.575
CLr_1-0	44.3886	114.976	94.353	0.477	66.381	66.381	66.382	223.047	223.047	222.575

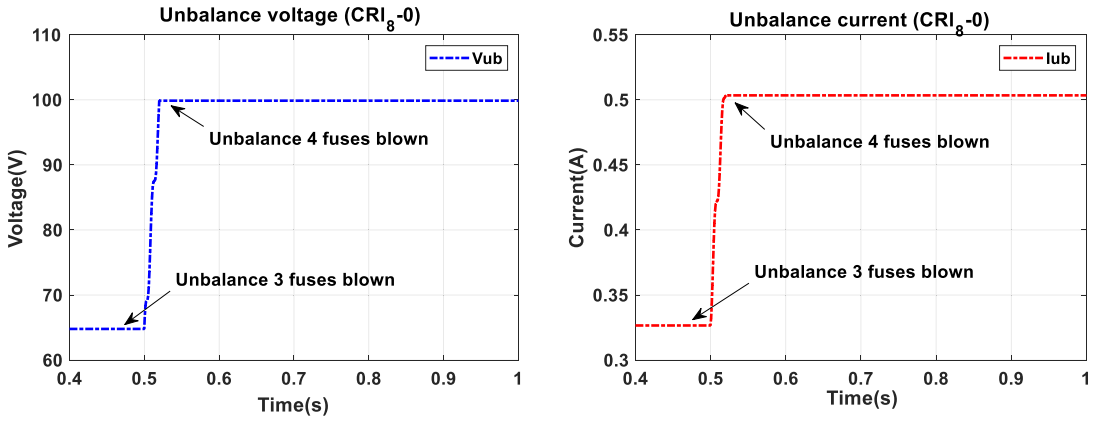
at position CRl_8-0. A comparison between Figures 6 and 10 demonstrate that the characteristics of unbalanced current and voltage were similar to those obtained when fault occurred at position CRl_1-0. The detailed analysis of parameter characteristics when fault position varied from row 1 to row 10 is summarized in TABLE 5. The result demonstrates that the row variation did not influence the system parameters because the capacitance of the capacitor unit for each case was similar.

D. INFLUENCE OF INCEPTION ANGLE (θ)

The inception angle was varied to analyze its influence on the characteristics of system parameters. To this end, position CRl_1-150 was considered and the result is shown in Figure 11 and summarized in TABLE 6. The unbalance voltage and current of figure 11 were compared with that unbalance voltage and current at figure 6 when the inception angle (phase A as reference angle) varied from 0° to 150°.The comparison shown that the characteristic of unbalance factors was the same. In addition, the characteristic of both unbalance factors also same as those obtained for the previous cases when phase, side of fault position and row connection was vaired. To further clarify, the inception angle was varied from 0° to 330°, while the fault position was fixed at CRl_1. Considering the results summarized in TABLE 6, the inception angle was found to have no influence on the system parameters.

E. INFLUENCE OF FUSE BLOWN ($fu\theta$)

Finally, the influence of the number of fuses blown on system parameters was investigated. When fault occurs in a capacitor bank, three fuses were blown within 0.5 s. As previously discussed, the number of fuses blown affected the current, unbalanced voltage, and unbalanced current. Therefore, considering the number of fuses blown to be 1, 2 and 3, the difference in system parameter characteristics was observed. The characteristics of the unbalance factors when three fuses were blown are shown in Figures 12(a) to 12(b), which are similar to those in Figures 6(c) to 6(d), which shows the unbalance voltage and current when four fuses were blown.

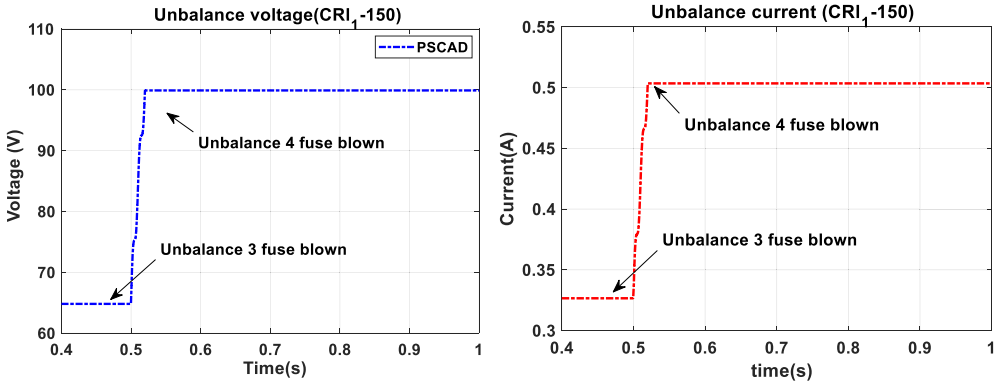


(a) Unbalanced voltage of capacitor bank (b) Unbalanced current of capacitor bank

FIGURE 10. Behavior of the system parameters when fault occurs in the capacitor unit at position CRI_8-0.

TABLE 5. Behavior of parameter when the row of capacitor connection varied.

Case	Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)			Iph (A)		
					PhA	PhB	PhC	PhA	PhB	PhC
Normal	44.4503	114.977	0.0013	0.000	66.380	66.381	66.381	223.205	223.205	223.205
CRI_1-0	44.3886	114.976	94.353	0.476	66.380	66.381	66.382	223.047	223.047	222.575
CRI_2-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_3-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_4-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_5-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_6-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_7-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_8-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_9-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575
CRI_{10}-0	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575

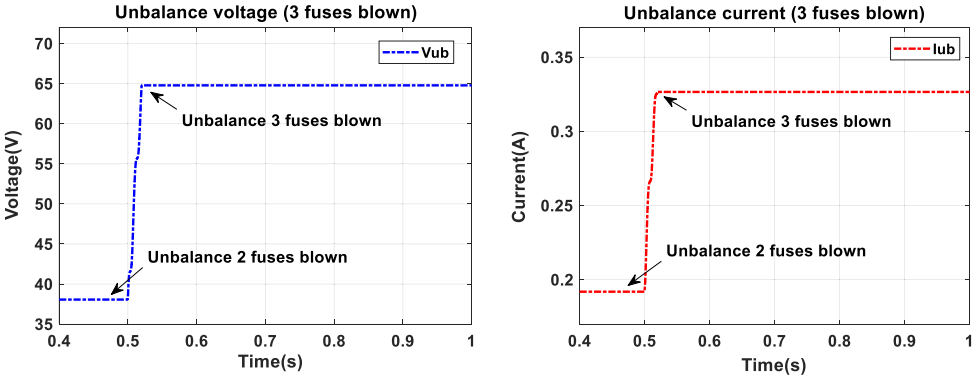


(a) Unbalanced voltage of capacitor bank (b) Unbalanced current of capacitor bank

FIGURE 11. Behavior of the system parameters when fault occurs in the capacitor unit at position CRr_1-60.

These figures prove that the number of fuses blown directly affected only the amplitude of both the unbalanced current and voltage. When the number of fuses blown increased, the capacitance of the capacitor unit decreased. Then, the current decreased relative to that under normal conditions such that the unbalanced current increased. The behavior of the system parameters for different number of fuses blown has been summarized in TABLE 7.

The table lists the average values of the system parameters when fault occurred at positions CRI_1-0 to CRI_{10}-0. As mentioned before, the result demonstrates that when the number of fuses blown increased, the capacitance of the fault



(a) Unbalanced voltage of capacitor bank (b) Unbalanced current of capacitor bank

FIGURE 12. Behavior of the system parameters when the fault blew three fuses of the capacitor.

TABLE 6. Behavior of parameter when inception angle varied.

Case	Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)			Iph (A)		
					phA	phB	phC	phA	phB	phC
Normal	44.4503	114.977	0.00013	0.000	66.380	66.381	66.381	223.205	223.205	223.205
CRl_l-0	44.3886	114.976	94.353	0.476	66.380	66.381	66.382	223.047	223.047	222.575
CRl_l-30	44.3885	114.976	94.350	0.476	66.380	66.381	66.382	223.048	223.046	222.574
CRl_l-60	44.3884	114.976	94.419	0.476	66.380	66.381	66.382	223.048	222.046	223.576
CRl_l-90	44.3883	114.976	94.353	0.476	66.380	66.381	66.382	223.048	223.047	222.578
CRl_l-120	44.3883	114.976	94.493	0.476	66.381	66.381	66.382	223.048	223.048	222.578
CRl_l-150	44.3884	114.976	94.424	0.476	66.381	66.381	66.382	223.047	223.048	222.576
CRl_l-180	44.3886	114.976	94.353	0.476	66.381	66.381	66.382	223.047	223.047	222.575
CRl_l-210	44.3885	114.976	94.350	0.476	66.380	66.381	66.382	223.048	223.047	222.575
CRl_l-240	44.3886	114.976	94.419	0.476	66.380	66.381	66.382	223.048	223.047	222.577
CRl_l-270	44.3886	114.976	94.491	0.476	66.380	66.381	66.382	223.049	223.048	222.578
CRl_l-300	44.3886	114.976	94.493	0.476	66.381	66.381	66.382	223.049	223.049	222.578
CRl_l-330	44.3886	114.976	94.424	0.476	66.382	66.381	66.382	223.048	223.049	222.577

unit decreased. This result is observed when the capacitor is connected to the blown-out fuse, forming an open circuit. In addition, a decrease in the capacitance also results in a decrease in the reactive power.

The results of the above investigations on the characteristic of the system parameters help conclude that the amplitudes of unbalanced voltage, and current were influenced by the fault in the capacitor unit. Considering that the fault occurred at 0.5 s, the system parameters varied and shifted toward a new stable state after 0.5 s, exhibiting a small delay. The difference in the amplitudes during this delay led to a difficulty in the detection process. Thus, this difference was mathematically estimated. The application of a DWT has been discussed in the following section.

IV. DISCRETE WAVELET TRANSFORM (DWT)

Traditionally, the operation of an unbalanced relay depends on the unbalanced current. The above investigations on the characteristics of the system parameters demonstrate that the unbalanced current initially increases when a fuse is blown. This current steadily increases and then attains a new stable state after exhibiting a considerable delay, which can affect the detection performance. The simulation time was extended to 0.8 s before the relay trip in order to clearly observe the fault characteristics. Owing to this extension, the current characteristic could also be clearly observed, compared with that of voltage. This characteristic demonstrated that the factors considered in the wavelet method when a fault occurred were unbalanced voltage, and unbalanced current.

Wavelet transform in one of the mathematic method that can be viewed as the projection of a signal into a set of basis functions named wavelets. The wavelet based on the dilation and translation of the ‘‘mother function. The mother function define an orthogonal basis as follow:

$$\emptyset\,(s, l)\,(x) = 2^{\frac{-s}{2}}\emptyset(2^{-s}x - l) \tag{1}$$

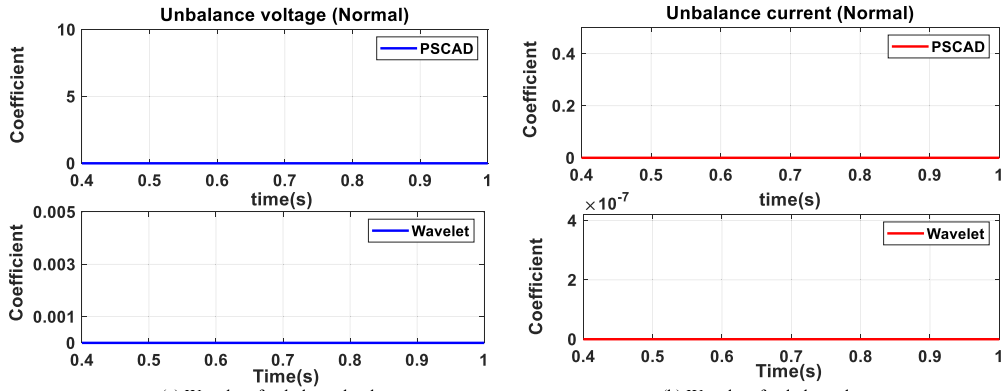
When the variables s and l are integers that scale and dilate the mother function $\emptyset$ to generate wavelet such as Daubechies wavelet (Db). The scale index s indicates the wavelet's width and the location index l show the position.

Discrete wavelet transform (DWT) able to provide high frequency resolution at low frequencies and high time resolution at high frequencies so to span the data domain to different resolution, the analyzing wavelet is used in a scale equation as follow:

$$W\,(x) = \sum\nolimits_{K=-1}^{N-2} (-1)^k B_{k+1}\emptyset(2x + k) \tag{2}$$

TABLE 7. Behavior of parameter when the number of blown fuses varied (fault unit at CRl_1-0 position).

Internal fuse blown	Capacitance (μF)	Reactive power (Mvar)	Ea (kV)	Vub (V)	Iub (A)	Vln (kV)			Iph (A)		
						phA	phB	phC	phA	phB	phC
0	26.743	44.4503	114.977	0.0001	2.38E-09	66.380	66.381	66.381	223.205	223.205	223.205
1	25.933	44.4500	114.977	17.031	0.086	66.462	66.381	66.380	223.193	223.208	222.996
2	24.960	44.4500	114.977	39.418	0.198	66.462	66.381	66.380	223.178	223.213	222.817
3	23.772	44.4500	114.977	64.820	0.306	66.462	66.381	66.380	223.159	223.220	222.760
4	22.286	44.3886	114.976	94.353	0.477	66.380	66.381	66.381	223.047	223.047	222.575



(a) Wavelet of unbalanced voltage (b) Wavelet of unbalanced current

FIGURE 13. Unbalance factors obtained mathematically under normal conditions.

When $W(x)$ is the scaling function for the mother wavelet function $\emptyset$ and B_k is the wavelet coefficient which k is coefficient index. The useful features of wavelet were able to choose the defining coefficient for a given wavelet system to be adapted for a given problem such as multiresolution analysis (MRA).

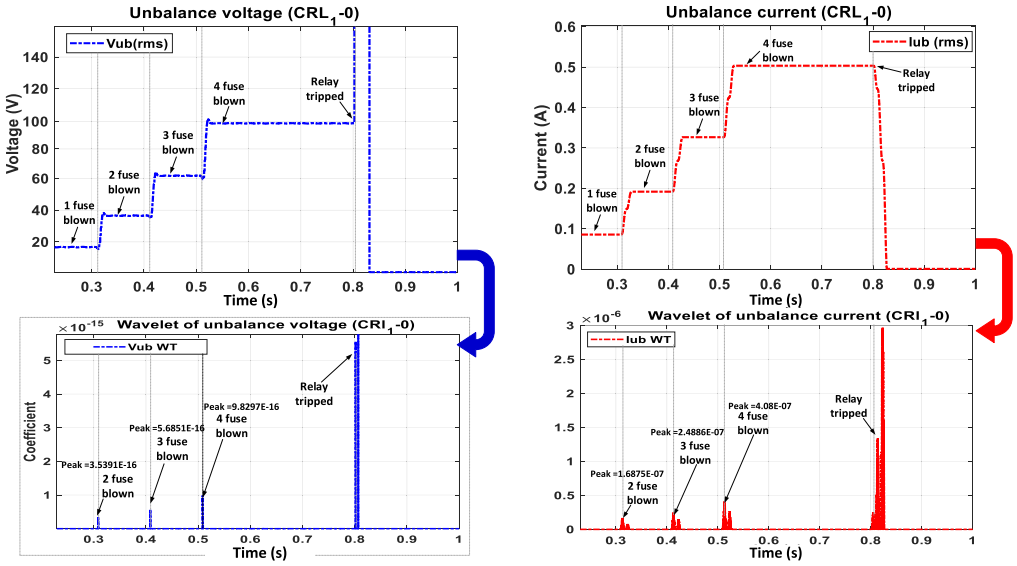
This method was implemented using Daubechies wavelet order 4 (db4) as a mother wavelet due to its commonly used for solving the power system transient issue [32]–[40]. Consequently, the results obtained from the DWT are shown in Figures 13 and 14.

Considering the unbalanced voltage under normal and fault conditions, as shown in Figures 13(a) and 14(a), the coefficient of the unbalanced voltage signal that applied DWT abruptly varies when the fuse is blown. A comparison between the unbalanced signal and the coefficient demonstrated that the delay time of the unbalanced voltage signal was longer than that of the DWT, which instantaneous varied during the occurrence of a fault. In terms of the coefficient of the DWT, only the first peak that was observed when a fuse was blown will be considered; the other peaks were neglected by algorithm.

Similarly, considering the unbalanced current, as shown in Figures 13(b) and 14(b), the wavelet coefficient cannot by obtained under normal conditions because the fuse was not blown and the system was balanced. When a fault occurred and four fuses were blown, the wavelet coefficient suddenly increased the instant the fuse blown, exhibiting a similar trend to that of the unbalanced voltage. This abrupt variation can be used as an index for fault detection in the algorithm. In addition, considering the relay trip at 0.8 s, the wavelet coefficients of unbalanced voltage and unbalanced current suddenly increased, which was observed owing to the abrupt variation of the initial signal at 0.8 s.

The wavelet of the unbalanced voltage, as shown in Figures 14(a) and 15(a), demonstrates the influence of the inception angle; the coefficient of the unbalanced voltage at CRl_1-0 and CRl_1-150 was 9.8297E-16 and 1.2536E-12, respectively. However, the inception angle has a relatively small influence of the coefficient of unbalanced current, which was approximately 10^{-7} at CRl_1-0 and CRl_1-150.

Considering the details summarized in TABLE 8, the study cases of normal and fault occurrence were demonstrated. In which the fault occurrence cases considered the factors such as phase (ph), side and branch of fault position (X1, X2), row (n), inception angle (θ), and number of fuse blown (fu). According to the characteristics of the PSCAD signal previously obtained, the variation in the unbalanced voltage, and unbalanced current cannot be obtained. This is because when fault occurs at different phases and inception angles, the signals obtained are similar. This is in turn because unbalanced voltage, and unbalanced current only depend on the capacitance of the capacitor unit. While, applied DWT and considered in term of DWT coefficient, it can be seen that the coefficient was clear emphasis than the characteristic of signal generated by PSCAD which the changing of and both unbalanced factors can be detect when phase and inception angle variation.



(a) Wavelet of unbalanced voltage

(b) Wavelet of unbalanced current

FIGURE 14. Signal obtained mathematically when fault occurred at position CRI_1-0.

TABLE 8. Wavelet coefficients when fault position variable.

Case					DWT	
Phase	Side (X2)	Branch (X2)	Row (n)	Inception angle	Vub WT	Iub WT
Normal					0.0000	3.48E-22
C (fu=4)	Right	Left	1	0	0.0122	4.16E-07
B (fu=4)	Right	Left	1	0	0.0179	2.26E-07
C (fu=4)	Left	Left	1	0	0.0122	4.16E-07
C (fu=4)	Right	Right	1	0	0.0122	4.16E-07
C (fu=4)	Right	Left	8	0	0.0122	4.16E-07
C (fu=4)	Right	Left	1	150	0.0122	4.13E-07
C (fu=3)	Right	Left	1	0	0.0079	5.51E-06

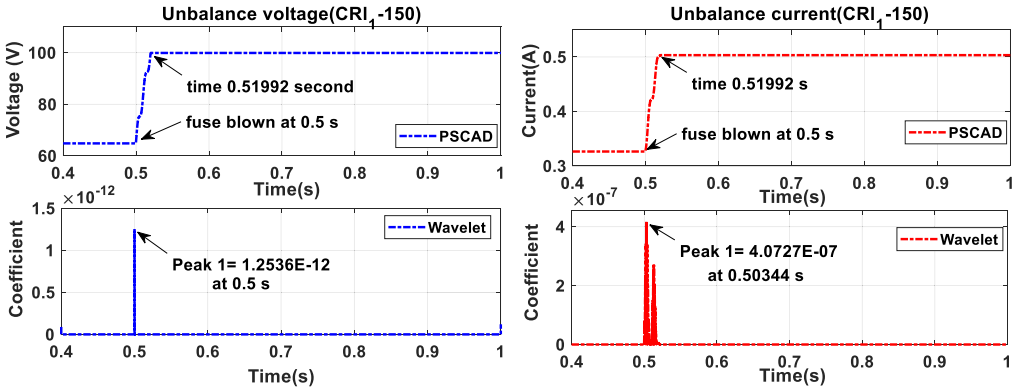
Moreover, when considered the coefficient of both unbalance factors compared to the coefficient of these unbalance in normal conditions, it can be seen that the coefficient of unbalance voltage morependulous than the unbalance current, which the coefficient value of unbalance current was close to the coefficient of unbalance current in case of normal condition but the coefficient value of unbalance voltage was higher than the coefficient of unbalance voltage in case of normal condition.

In summary, the DWT evidently exhibited faster detection and analysis compared with the initial signal obtained from PSCAD. Thus, the proposed algorithm will apply DWT before fault discrimination, as discussed in the following section.

V. PROPOSED ALGORITHM FOR ANALYSIS OF FAULTS

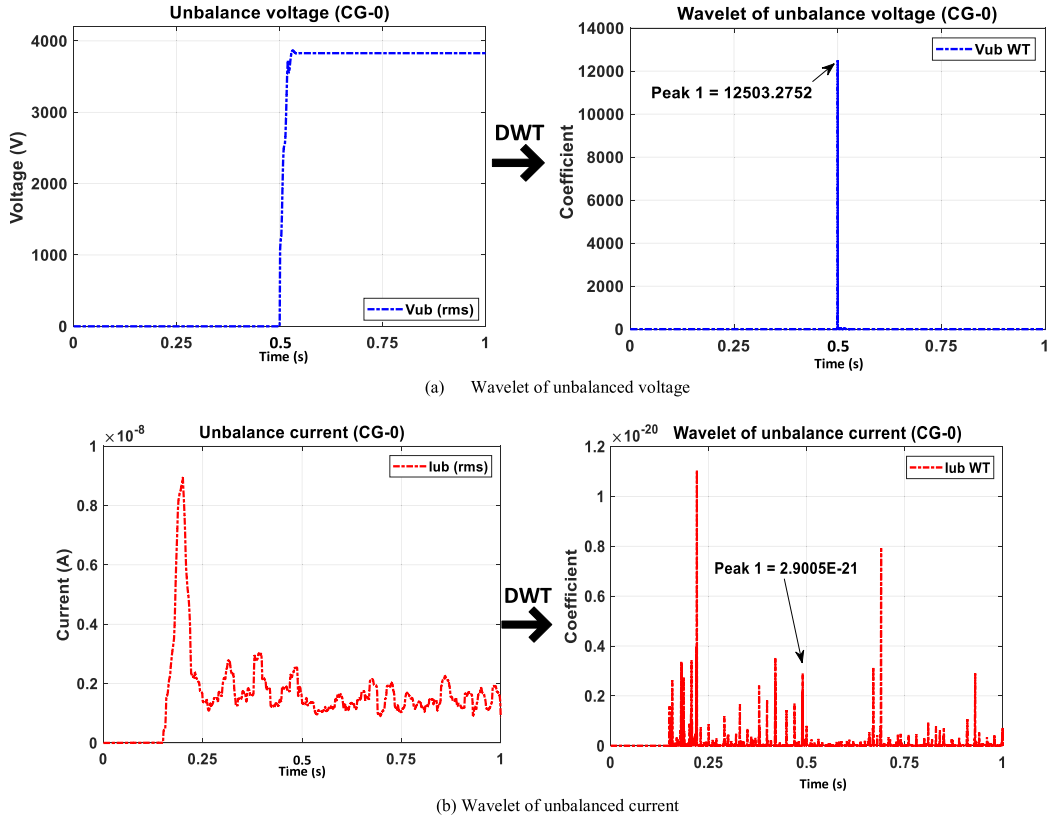
A fault discrimination algorithm based on DWT has been proposed in the capacitor bank. This algorithm has been implemented using DWT to extract the coefficient value that abruptly increased when a fault occurred, thus reducing the delay time, which affected the accuracy of the detection process. To verify the performance of the proposed algorithm, a case study of a fault on the capacitor unit (Internal fault) was considered, as mentioned in the previous section. Moreover, faults in the transmission line (External fault), such as single line to ground fault (SLG), double line to ground fault (DLG), line to line fault (LL), and three phases fault (3P), have also been included. An analysis of the characteristics of the obtained signal demonstrated that the capacitor current as well as unbalanced current and voltage were evidently influenced by the internal fault. Considering an external fault, which is a phase C to ground fault, the behavior of the wavelet obtained from both unbalanced current and voltage is shown in Figure 16.

By considering the unbalanced voltage for both the internal and external faults shown in Figures 14(a) and 16(a), when fault occurred at 0.5 s, the coefficient of unbalanced voltage for both internal and external faults suddenly increased. Moreover, the coefficient for an external fault was considerably higher than that for an internal fault owing to the effect of external fault on the impedance of the system.



(a) Wavelet of unbalanced voltage (b) Wavelet of unbalanced current

FIGURE 15. Signal obtained mathematically when a fault occurred at position CRl_1-150.



(a) Wavelet of unbalanced voltage

(b) Wavelet of unbalanced current

FIGURE 16. Current obtained mathematically when an external fault occurred (SLG:CG).

Similarly, the characteristics of unbalanced current for an external fault were compared with those for an internal fault, as shown in Figures 14(b) and 16(b). The coefficient of the unbalanced current for an external fault was close to zero. The figure shows that the unbalanced current detected at the unbalanced detection point depended on the balance in the capacitance of the capacitor unit. Thus, the external fault did not affect the unbalanced current in the system. This unique characteristic of the unbalanced current was suitable to classify faults the occurred in the capacitor bank.

To demonstrate the difference in the internal and external faults, both unbalanced current and voltage generated by PSCAD and obtained from the wavelet coefficient after applying DWT were compared in TABLE 9.

Considering the unbalanced voltages listed in TABLE 9, the unbalanced voltage for an external fault was observed to be higher than that for an internal fault, except for line to line and three phase faults. This is observed because of the influence of ground in case of line to line fault and the influence of the three phase impedance in case of three phase

TABLE 9. Average values of simulation result.

Case		Phase	PSCAD		DWT	
			Vub	Iub	Vub WT	Iub WT
Internal fault	Fault in capacitor unit	A	94.4195	0.4759	0.141249	3.90E-07
		B	94.4935	0.4756	0.141249	3.96E-07
		C	94.3530	0.4763	0.141249	3.96E-07
External fault	Single line to ground fault (SLG)	AG	3454.87	2.05E-09	21675.63	7.01E-22
		BG	3451.74	2.20E-09	14496.91	7.07E-22
		CG	3508.58	1.54E-09	14420.56	7.50E-22
	Double line to ground fault (DLG)	ABG	3473.35	2.44E-09	13121.87	1.07E-21
		ACG	3470.57	1.49E-09	13170.99	7.59E-22
		BCG	3473.59	1.94E-09	19688.34	6.66E-22
	Line to line fault (LL)	AB	0.000129	2.04E-09	8.43E-17	9.33E-22
		AC	0.000129	1.55E-09	7.66E-17	6.88E-22
		BC	0.000129	1.50E-09	7.87E-17	7.95E-22
	Three phase fault (3P)	ABCG	0.000109	1.66E-09	1.08E-14	6.83E-22

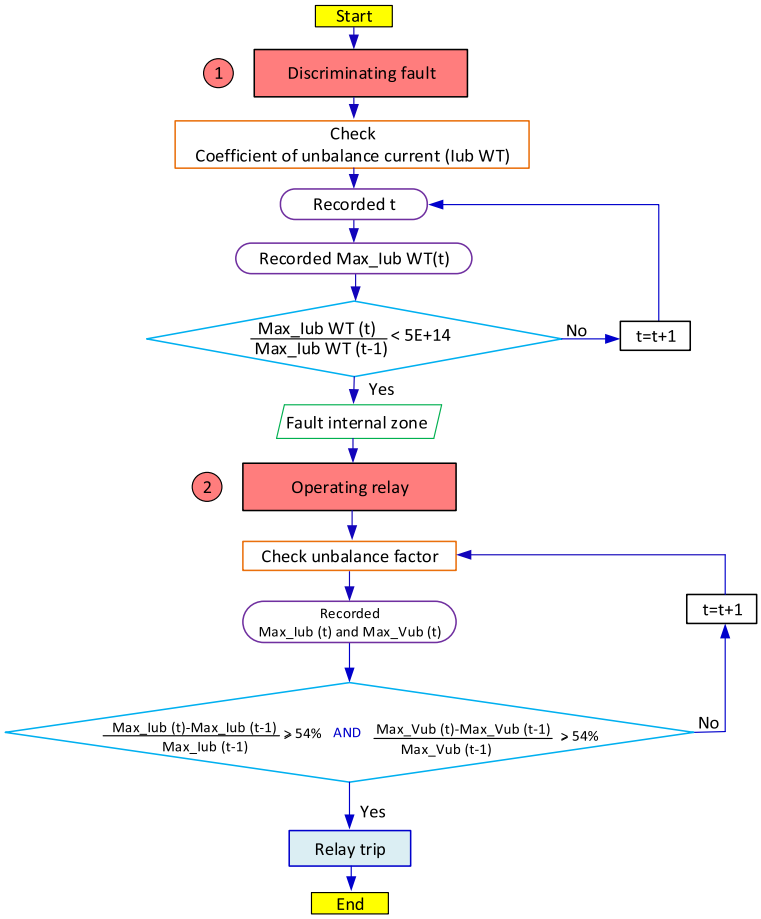
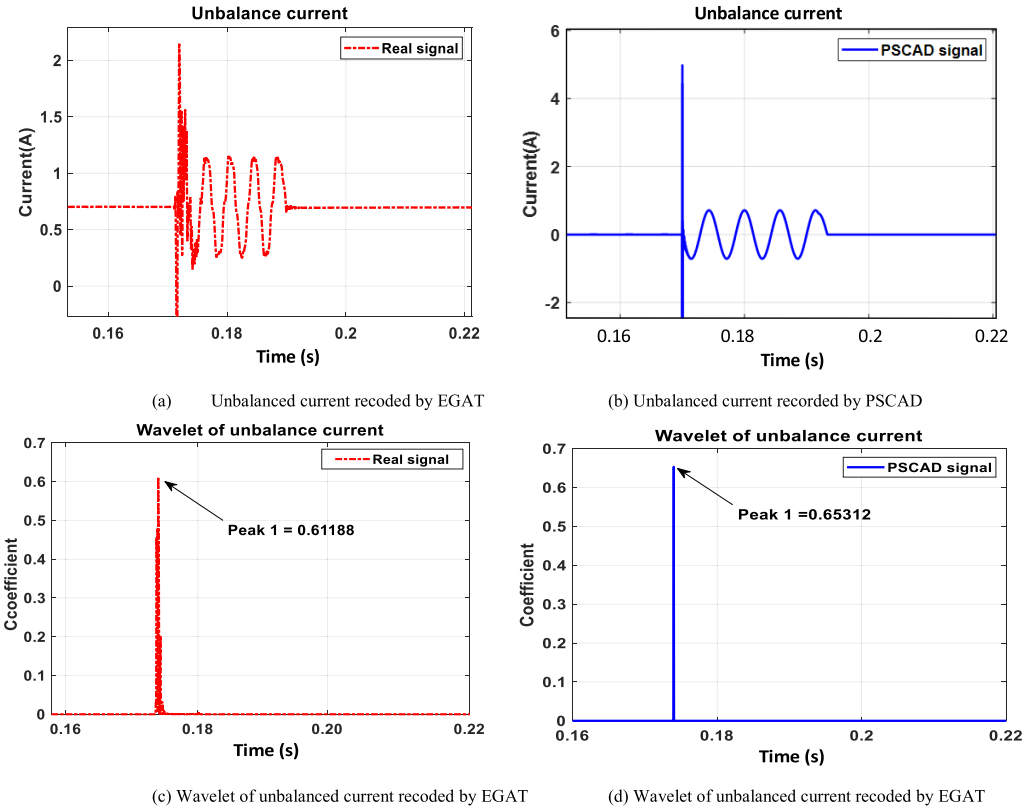


FIGURE 17. Detecting internal fault algorithm.

fault. In addition, by considering the wavelet coefficient of unbalanced voltage, it can be seen that the coefficient was in the same trend as the unbalanced voltage signal. In the same way, when observed the unbalanced current signal, the obtain value shown that the unbalanced current was corresponding to its coefficient from DWT. The unbalanced current for an internal fault was higher than that for an external fault. The difference in the coefficients of the unbalanced current in case of faults occurrence can be used as an index to indicate the fault types between an internal and external fault.

In summary, the coefficient of the unbalanced current exhibits unique characteristics that help discriminate between the internal and external faults. The unbalanced voltage varied with the inception angle and fault type. Thus, the proposed algorithm considered on both unbalanced factors. The proposed algorithm will be applied to an unbalanced relay



(a) Unbalanced current recoded by EGAT

(b) Unbalanced current recorded by PSCAD

(c) Wavelet of unbalanced current recoded by EGAT

(d) Wavelet of unbalanced current recoded by EGAT

FIGURE 18. Unbalanced current when a fault occurred in the capacitor unit.

located in a substation to solve the inability of traditional relays to indicate the occurrence of a fault in the capacitor bank. The proposed algorithm is implemented in two procedures: (1) discriminating between an internal and an external fault based on the coefficient ratio of unbalanced current and (2) relay operation based on both ratios of unbalanced current and unbalanced voltage. The proposed algorithm analyzed by divided the signal into short period time which call ''Moving window''and these ratios were extracted by comparing the value that the currently observed moving window and the previously observed moving window, observed at time t and t-1, respectively, as show in Figure 17.

The figure shows that the proposed algorithm first discriminated faults based on the wavelet coefficient of the unbalanced current. The coefficient ratio of the unbalanced current was extracted by comparing the coefficients obtained at time t and t-1. The results obtained demonstrate that the coefficient ratio of the unbalanced current was lower than 5E+14; thus, the algorithm decided that a fault has occurred in the capacitor unit of the capacitor bank (Internal fault). In contrast, when the wavelet ratio of the unbalanced current was higher than 5E+14, the algorithm decided that a fault has not occurred in the capacitor bank.

The second procedure helps assess the situation and the signal of the relay operation. Here, the unbalanced current ratio, which is the unbalanced current at time T to the unbalanced current at time t-1, was considered as a checking condition. In addition, the ratio of the unbalanced voltage was used as a double-checking condition. The unbalanced relay triggers a trip when both the unbalanced ratios exceeded 54% and results in a block when the unbalanced ratio was less than 54%, provided the voltage of capacitor unit in which the fault occurred exceeded 150% of the voltage of the healthy element used for traditional method (EGAT capacitor protection standard).

The proposed algorithm was applied to the selected case studies as summarized in TABLE 10. Using the data in this table along with the algorithm, the unbalanced factors and the wavelet coefficient of the unbalanced current were obtained as initial parameters.

An internal fault at phase C of the capacitor unit, on the right side, on the left branch, at row 1, for an inception angle of 0° with four fuses blown (CRl_1-0, fu=4) was considered as an example. The wavelet coefficient of the unbalanced current at time t and t-1 was 4.16E-07 and 5.51E-06, respectively. Thus, the coefficient ratio of the unbalanced current at time t to that at t-1 was 0.0754. Therefore, at CRl_1-0, this ratio was lower than 5E+14, which satisfy the first checking condition. Thus, the algorithm detected the analyzed signal as the occurrence of an internal fault. By varying the position of the fault, and not the inception angle or the fault phase, the coefficient ratio was observed to be lower than 5E+14, such that

TABLE 10. Detection faults in the capacitor unit.

Case					Initial parameter									Inference
Phase	Side (X1)	Branch (X2)	Row (n)	θ	Iub WT (t)	Iub WT (t-1)	Ratio Iub WT	Iub (t)	Iub (t-1)	Ratio Iub	Vub (t)	Vub (t-1)	Ratio Vub	
C (fu=4)	Right	Left	1	0	4.16E-07	5.51E-06	0.0754	0.4763	0.306	55.6536%	94.3530	58.4686	61.3738%	Trip
B (fu=4)	Right	Left	1	0	2.26E-07	5.24E-06	0.0431	0.4756	0.2956	60.8931%	94.4935	64.7267	61.6141%	Trip
C (fu=4)	Left	Left	1	0	4.16E-07	5.51E-06	0.0754	0.4763	0.3011	58.1866%	94.3530	64.820	61.3738%	Trip
C (fu=4)	Right	Right	1	0	4.16E-07	5.51E-06	0.0754	0.4763	0.3011	58.1866%	94.3530	64.820	61.3738%	Trip
C (fu=4)	Right	Left	8	0	4.16E-07	5.51E-06	0.0754	0.4763	0.306	55.6536%	94.3530	58.4686	61.3738%	Trip
C (fu=4)	Right	Left	1	150	4.13E-07	5.49E-06	0.0752	0.4759	0.3264	55.5229%	94.4245	64.8189	61.4961%	Trip
C (fu=3)	Right	Left	1	0	5.51E-06	1.88E-06	2.9308	0.3060	0.1987	54.0010%	58.4686	39.4187	48.3264%	Block
A	Single line to ground fault (SLG)			0	2.68	3.48E-22	7.70E+21							Block
A, B	Double line to ground fault (DLG)			0	2.68	3.48E-22	7.70E+21							Block
A, B	Line to line fault (LL)			0	2.69	3.48E-22	7.73E+21							Block
A, B, C	Three phases to ground fault (3PG)			0	2.69	3.48E-22	7.73E+21							Block

TABLE 11. Performance of fault detection algorithm.

No	Case	Event	Check performance (% Accuracy)	
			Traditional method (EGAT standard)	Proposed algorithm
			Iub > 250 mA	
1	Normal condition	12	100%	100%
2	Capacitor unit fault (Internal fault)	1476	97.56%	100%
3	Transmission line fault (External fault)	48	100%	100%
	Total	**1536**	**97.65%**	**100%**

the proposed algorithm decided these signals resulted in the occurrence of an internal fault.

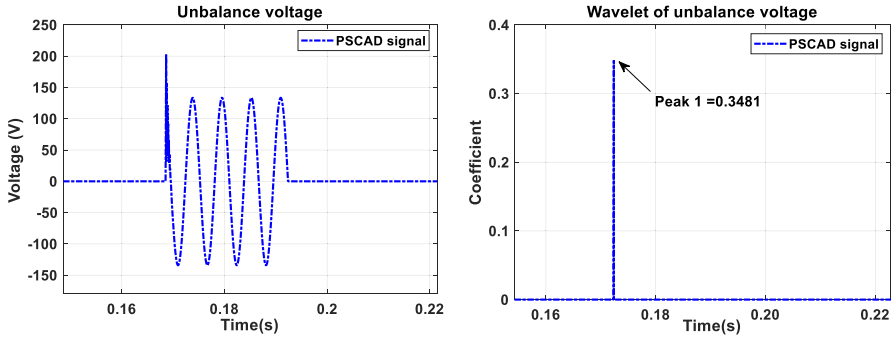
Considering an internal fault that occurred owing to the variation of the fault phase and inception angle, the result of the coefficient ratio in these cases also lower than 5E+14 so the proposed algorithm classified as the internal fault. Considering a single line to ground fault (External fault), the coefficient ratio was observed to be 7.70E+21, which was higher than the checking condition. Therefore, the algorithm neglected the analyzed signal and continued to analyze the initial parameters at time t+1. The coefficient ratio for an external fault was high as the initial signal substantially varied when a fault occurred, which resulted in a high wavelet coefficient. After an internal fault was successfully detected, the relay was operated based on the second checking condition. Considering the data summarized in TABLE 10, the unbalanced current ratio for four blown fuses and that when the position of the faulty capacitor unit varied exceeded 54%. Simultaneously, the unbalanced voltage ratio, which was used as a double-checking condition, also satisfied the criteria. Thus, the algorithm will send a signal to trip the relay. In contrast, considering that three fuses are blown, both ratios of the unbalanced current and voltage were lower than 54%; thus, the algorithm will send a signal to block the relay.

In summary, the proposed algorithm will determine the occurrence of a fault based on whether all initial parameters satisfy the checking conditions. This helps ensure that the unbalanced relay correctly classifies faults and continues to function even when a fault occurs in the capacitor unit.

To validate the proposed algorithm under possible scenarios, it was applied to all case studies considering various factors. The number of case studies considered to verify the effectiveness of the proposed algorithm was 1,536, which consisted of 12 cases under normal conditions, 1,476 cases with a capacitance unit fault, and 48 cases with a transmission line fault. The performance of the proposed algorithm relative to the traditional method which was EGAT capacitor bank protection standard is summarized in TABLE 11. The unbalanced relay under the EGAT protection standard can be operated when the voltage of a faulty element exceeded 150% that of the healthy element, or when the unbalanced current exceeded 250 mA.

The data summarized in TABLE 11 demonstrate that the EGAT protection standard was largely efficient for fault detection. However, there is an error when a fault occurs in the capacitor unit and when three fuses are blown. In such cases, the unbalanced relay should not be operated. This is because, although the value of the voltage element would be less than 150%, the unbalanced current for three blown fuses would be 290 mA, which is higher than the setting value (250 mA). This will result in faulty operation of the relay. In case that relay using proposed algorithm, the result shown that the performance is 100% accurate with correctly detected fault in capacitor bank which was double wye unground 48 Mvar and effective in the relay operation.

To verify the proposed algorithm, the real unbalanced current signal when a fault occurred in the capacitor unit recorded by the unbalanced relay in the RANOD substation of EGAT was observed and compared with the unbalanced current signal generated by PSCAD. Considering the real signal and simulated signal in Figures 18(a) and 18(b), respectively, both signals are observed to show similar characteristics; the signals abruptly varied during the occurrence of a fault and tended to zero within four cycles, due to the unbalanced relay trip. Moreover, considering the wavelet coefficient shown in Figures 18(c) and 18(d), the wavelet coefficient was evident during the occurrence of a fault and exhibits similar characteristics for both signals. However,



(a) Unbalanced voltage (b) Wavelet of unbalanced voltage

FIGURE 19. Unbalanced voltage recoded by PSCAD when a fault occurred in the capacitor unit.

TABLE 12. Detecting faults in the capacitor unit based on real fault signal.

Case	Traditional method (EGAT standard)		Propose algorithm								
	Initial parameter		Initial parameter								
	Iub (mA)		Iub WT (t)	Iub WT (t-1)	Ratio Iub WT	Iub(t) (mA)	Iub(t-1) (mA)	Ratio Iub	Vub(t) (V)	Vub(t-1) (V)	Ratio Vub
RANOD fault	503.3		1.61E-02	9.69E-03	1.6613	0.5033	0.3264	54.1272%	99.9042	64.8193	54.1973%
	Check condition	>250 mA	Check condition 1		<5E+14	Check condition 2		≤ 54%	Check condition 2		≤ 54%
Inference	Trip		Trip								
Operating time	0.027 s		0.017 s								

the EGAT protection standard only analyzes the unbalanced current when a fault occurs in the capacitor bank and the unbalanced voltage was not recorded. However, the proposed algorithm considers both unbalanced current and voltage; the unbalanced voltage and its coefficient of DWT obtained using PSCAD is shown in Figure 19.

Figure 19 shows that the characteristics of the unbalanced voltage and its wavelet were similar to those of the unbalanced current, as shown in Figure 18. This unbalanced voltage increased during the occurrence of a fault, and the wavelet coefficient could be evidently observed when that fault occurred. In addition, the initial parameter when fault occurred in the RANOD substation was testing on the proposed algorithm to verify its accuracy relative to the EGAT standard, as shown in TABLE 12

The RMS value of a practical signal, listed in TABLE 12, has been used as an input for both the proposed and EGAT algorithms. The results obtained reveal that the proposed algorithm can detect faults in the capacitor bank and transmit a signal to the relay to modify operation accurately, similar to the EGAT standard. Therefore, in conclusion, the proposed algorithm can be implemented in practical capacitor bank protection systems, which will help improve the performance of the power system protection in the future. Moreover, by considering the operating time in Figure 20, it can be seen that the unbalance relay detected faults at 0.18 s, and the relay was set to record the pre fault signal for the fault

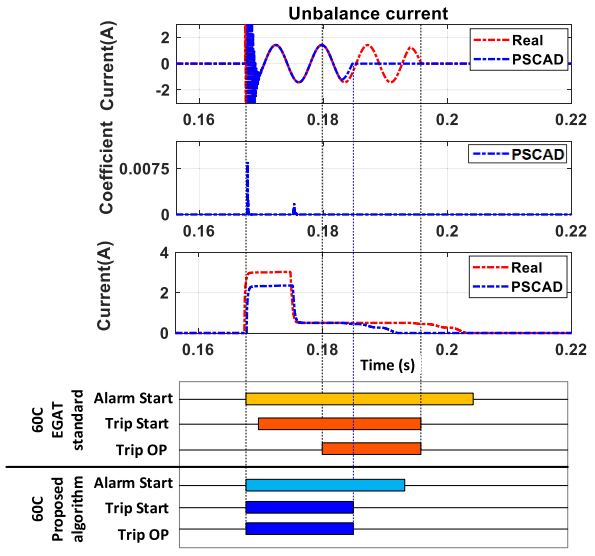


FIGURE 20. Performance of fault detection operated by unbalance relay.

detection processing; thus, the signal started recording at 0.168 s. In term of alarm, the relay alarm sounded when the unbalance current immediately increased, and the relay stopped operating when the fault was eliminated. In the same way, the relay started the trip procedure after the relay alarm sounded. However, when fault occur at 0.168 s, relay

detection process will be operated at 0.18 s and the fault was completely eliminated by breaker at 0.195 s. The duration of the traditional relay process from the fault occur to completely eliminated fault was 0.027 s. Therefore, the operation of unbalance relay based on the EGAT standard showed a time delay before the unbalance relay alarm and trip. This delay issue of traditional relay operation can be solved when the fault decision of the relay is based on wavelet.

By considering the wavelet signal in figure 20, it can be seen that the coefficient of unbalance current occurred at the fault occurrence time. Thus, the relay was trip operating at 0.168 s, and the fault was eliminated by the breaker at 0.185 s. The duration of the time that the fault occurrence and eliminated fault based on wavelet was 0.017 s, which faster than the EGAT standard.

VI. CONCLUSION

This study investigated the characteristics of both internal and external faults. In addition, an algorithm used to detect faults occurring in a capacitor unit was proposed. The simulations in this study were conducted using PSCAD, considering a 115 kV substation with a 48 Mvar capacitor bank, based on tradition method (EGAT standards). The proposed algorithm was implemented via two procedures: one to discriminate the faults and the other to help modify relay operation. The statistical data verified that the proposed algorithm accurately detected faults in the capacitor bank and helped relay operation with 100% accuracy, which is better that the 97.65% accuracy exhibited by the traditional EGAT standard. Moreover, the characteristics of a practical signal from EGAT were used to model the simulated signal, which helped prove that the proposed algorithm can be implemented in practical signal and protection systems. However, the proposed algorithm can only distinguish the cause of the fault, but cannot identify the exact position of the fault. Future studies should consider this limitation.

ACKNOWLEDGMENT

The authors wish to gratefully acknowledge data support for this research from the Electricity Generating Authority of Thailand (EGAT), Thailand.

REFERENCES

[1] R. P. P. Smeets, R. Wiggers, H. Bannink, S. Kuivenhoven, K. M. Tic, S. Chakraborty, and G. Sandolache, "The impact of switching capacitor banks with very high inrush current on switchgear," in *Proc. Cigre Paris Session*, 2012, pp. 1–8.

[2] W. Srisongkram, P. Fuangpian, R. Kem, and T. Suwanasri, "A simulation of electrical transient on 115 kV high voltage equipment in substation caused by capacitor bank switching," in *Proc. Cigre Paris Session, 19th Int. Symp. High Voltage Eng.*, Pilsen, Czech Republic, Aug. 2015, pp. 1–6.

[3] A. Chaudhary, T. Day, K. Fender, L. Fendrick, and J. McCall, "Pull a few strings [complete protection of multistring fuseless capacitor banks]," *IEEE Ind. Appl. Mag.*, vol. 9, no. 6, pp. 34–39, Nov./Dec. 2003.

[4] *IEEE Guide for the Protection of Shunt Capacitor Banks*, IEEE Standard C37.99-2012, Mar. 2013, pp. 1–151.

[5] B. Kasztenny, J. Schaefer, and E. Clark, "Fundamentals of adaptive protection of large capacitor banks—Accurate methods for canceling inherent bank unbalances," in *Proc. 60th Annu. Conf. Protective Relay Eng.*, College Station, TX, USA, 2007, pp. 126–157.

[6] M. D. Sankur, R. Dobbe, A. von Meier, and D. B. Arnold, "Model-free optimal voltage phasor regulation in unbalanced distribution systems," *IEEE Trans. Smart Grid*, vol. 11, no. 1, pp. 884–894, Jan. 2020.

[7] P. Castello, R. Ferrero, P. A. Pegoraro, and S. Toscani, "Effect of unbalance on positive-sequence synchrophasor, frequency, and ROCOF estimations," *IEEE Trans. Instrum. Meas.*, vol. 67, no. 5, pp. 1036–1046, May 2018.

[8] T. Routtenberg, Y. Xie, R. M. Willett, and L. Tong, "PMU-based detection of imbalance in three-phase power systems," *IEEE Trans. Power Syst.*, vol. 30, no. 4, pp. 1966–1976, Jul. 2015.

[9] P. C. Stefanov and A. M. Stankovic, "Modeling of UPFC operation under unbalanced conditions with dynamic phasors," *IEEE Trans. Power Syst.*, vol. 17, no. 2, pp. 395–403, May 2002.

[10] W. Grady and W. Taylor, "Correction of phase voltage measurements referenced to an ungrounded neutral," *IEEE Trans. Power App. Syst.*, vol. PAS-104, no. 7, pp. 1757–1760, Jul. 1985.

[11] S. A. Arshadi, M. Ordonez, W. Eberle, M. A. Saket, M. Craciun, and C. Botting, "Unbalanced three-phase *LLC* resonant converters: Analysis and trigonometric current balancing," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2025–2038, Mar. 2019.

[12] W. Zhou, O. Ardakanian, H.-T. Zhang, and Y. Yuan, "Bayesian learning-based harmonic state estimation in distribution systems with smart meter and DPMU data," *IEEE Trans. Smart Grid*, vol. 11, no. 1, pp. 832–845, Jan. 2020.

[13] Q. Xiong, X. Liu, X. Feng, A. L. Gattozzi, Y. Shi, L. Zhu, S. Ji, and R. E. Hebner, "Arc fault detection and localization in photovoltaic systems using feature distribution maps of parallel capacitor currents," *IEEE J. Photovolt.*, vol. 8, no. 4, pp. 1090–1097, Jul. 2018.

[14] Z. Gajic, M. Ibrahim, and J. Wang, "Method and arrangement for an internal failure detection in a Y-Y connected capacitor bank," U.S. Patent 2013 0 328 569, Dec. 16, 2014.

[15] X. Long, Y. W. Li, W. Xu, and C. Lerohl, "A new technique to detect faults in de-energized distribution feeders—Part II: Symmetrical fault detection," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 1902–1910, Jul. 2011.

[16] R. Horton, T. Warren, K. Fender, S. Harry, and C. A. Gross, "Unbalance protection of fuseless, split-wye, grounded, shunt capacitor banks," *IEEE Trans. Power Del.*, vol. 17, no. 3, pp. 698–701, Jul. 2002.

[17] A. A. Girgis, C. M. Fallon, and D. L. Lubkeman, "A fault location technique for rural distribution feeders," *IEEE Trans. Ind. Appl.*, vol. 29, no. 6, pp. 1170–1175, Nov./Dec. 1993.

[18] R. Montoya-Mira, J. M. Diez, P. A. Blasco, and R. Montoya, "Equivalent circuit and calculation of unbalanced power in three-wire three-phase linear networks," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 7, pp. 1466–1473, Apr. 2018.

[19] H. Jouybari-Moghaddam, T. S. Sidhu, M. R. D. Zadeh, and P. P. Parikh, "Shunt capacitor banks online monitoring using a superimposed reactance method," *IEEE Trans. Smart Grid*, vol. 9, no. 6, pp. 5554–5563, Nov. 2018.

[20] H. Jouybari-Moghaddam, T. S. Sidhu, M. R. D. Zadeh, and P. P. Parikh, "Enhanced fault-location scheme for double wye shunt capacitor banks," *IEEE Trans. Power Del.*, vol. 32, no. 4, pp. 1872–1880, Aug. 2017.

[21] A. Kalyuzhny, J. C. Mccall, and T. R. Day, "Corrective device protection," U.S. Patent 7 973 537, Jul. 5, 2011.

[22] S. Samineni, C. Labuschagne, J. Pope, and B. Kasztenny, "Fault location in shunt capacitor banks," in *Proc. 10th IET Int. Conf. Develop. Power Syst. Protection (DPSP)*, Manchester, U.K., 2010, pp. 1–5.

[23] J. Schaefer, S. Samineni, C. Labuschagne, S. Chase, and D. J. Hawaz, "Minimizing capacitor bank outage time through fault location," in *Proc. 67th Annu. Conf. Protective Relay Eng.*, College Station, TX, USA, Mar. 2014, pp. 72–83.

[24] Q. Huang and V. Vittal, "Integrated transmission and distribution system power flow and dynamic simulation using mixed three-sequence/three-phase modeling," *IEEE Trans. Power Syst.*, vol. 32, no. 5, pp. 3704–3714, Sep. 2017.

[25] Z. Hou, J. Huang, H. Liu, M. Ye, Z. Liu, and J. Yang, "Diagnosis of broken rotor bar fault in open- and closed-loop controlled wye-connected induction motors using zero-sequence voltage," *IET Electr. Power Appl.*, vol. 11, no. 7, pp. 1214–1223, Aug. 2017.

[26] T. Tang, C. Huang, L. Hua, J. Zhu, and Z. Zhang, "Single-phase high-impedance fault protection for low-resistance grounded distribution network," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 10, pp. 2462–2470, May 2018.

[27] *IEEE Guide for Automatic Reclosing of Line Circuit Breakers for AC Distribution and Transmission Lines*, IEEE Standard C37.104-2002, Apr. 2003.

[28] S. Zhang, S. Lin, Z. He, and W.-J. Lee, "Ground fault location in radial distribution networks involving distributed voltage measurement," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 4, pp. 987–996, Feb. 2018.
[29] O. Usta, M. Bayrak, and M. A. Redfern, "A new digital relay for generator protection against asymmetrical faults," *IEEE Trans. Power Del.*, vol. 17, no. 1, pp. 54–59, Jan. 2002.
[30] J. Wang, M. Ibrahim, Z. Gajić, and M. M. Saha, "Internal failure detection and protection on capacitor banks," in *Proc. 13th Int. Conf. Develop. Power Syst. Protection (DPSP)*, 2016, pp. 1–6.
[31] P. Lerley, "Applying unbalance detection relays with motor loads," *IEEE Trans. Ind. Appl.*, vol. 35, no. 3, pp. 689–693, May/Jun. 1999.
[32] S. Verma, "Most suited mother wavelet for localization of transmission line faults," *Int. J. Sci. Technol. Res.*, vol. 4, no. 6, pp. 288–293, Jun. 2015.
[33] S. Zhou, B. Tang, and R. Chen, "Comparison between non-stationary signals fast Fourier transform and wavelet analysis," in *Proc. Int. Asia Symp. Intell. Interact. Affect. Comput.*, Wuhan, China, Dec. 2009, pp. 128–129.
[34] J. P. M. J. Marques, G. C. Junior, and A. P. de Morais, "New methodology for identification of sympathetic inrush for a power transformer using wavelet transform," *IEEE Latin Amer. Trans.*, vol. 16, no. 4, pp. 1158–1163, Apr. 2018.
[35] T. Patcharoen and A. Ngaopitakkul, "Transient inrush and fault current signal extraction using discrete wavelet transform for detection and classification in shunt capacitor banks," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1226–1239, Mar. 2020.
[36] P. E. Argyropoulos and H. Lev-Ari, "Wavelet customization for improved fault-location quality in power networks," *IEEE Trans. Power Del.*, vol. 30, no. 5, pp. 2215–2223, Oct. 2015.
[37] Y. Zhang, T. Y. Ji, M. S. Li, and Q. H. Wu, "Identification of power disturbances using generalized morphological open-closing and close-opening undercimated wavelet," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2330–2339, Apr. 2016.
[38] Y. Gao, F. Villecco, M. Li, and W. Song, "Multi-scale permutation entropy based on improved LMD and HMM for rolling bearing diagnosis," *Entropy*, vol. 9, no. 4, pp. 176–185, 2017.
[39] T. Patcharoen and A. Ngaopitakkul, "Transient inrush current detection and classification in 230 kV shunt capacitor bank switching under various transient-mitigation methods based on discrete wavelet transform," *IET Gener., Transmiss. Distrib.*, vol. 12, no. 15, pp. 3718–3725, Aug. 2018.
[40] Y. Li, X. Yin, and R. Chen, "New method for transient line selection in distribution system based on grounding fault transferred," *J. Eng.*, vol. 2019, no. 16, pp. 2822–2826, Mar. 2019.