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A 40nm CMOS Hysteretic Buck DC-DC Converter With Digital-Controlled Power-Driving-Tracked-Duration Current Pump

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ABSTRACT A fast-transient voltage-mode hysteretic buck converter with digital-controlled power-driving-tracked-duration (PDTD) auxiliary current pump is proposed. The pump injection current duration is digitally controlled by the driving signal of the power stage. It aims at enhancing the transient response time which is limited by the large inductor used in typical buck converters and reducing the multiple undershoot/overshoot effect encountered in conventional current pump injection technique. The converter has been fabricated using TSMC 40nm CMOS technology with the silicon area of $830\mu m \times 620\mu m$. The proposed converter regulates properly in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The measured output ripple is about 30mVpk and the switching frequency is about 1.45MHz. The peak efficiency is 93%. The measured load transient settling time for a 60-to-300mA/300-to-60mA load step change is 369ns/335ns, resulting in 350% faster than that of conventional counterpart without PDTD control scheme. The performance comparison with the representative state-of-art works has shown that the proposed converter shows good balance on performance metrics and the best figure-of-merit (FOM) in transient-response efficiency.

INDEX TERMS DC-DC buck converter, hysteretic control, fast-transient, current pump.

I. INTRODUCTION

In recent years, a rapid growth of portable devices, such as smartphones, tablets, laptops and digital cameras is resulted from the development of system-on-chip (SoC) [1]–[8] which have different energy requirements [6]–[9]. Concurrently, low power consumption is one of the primary design agenda for the battery-powered SoC [10]. Switching converters are widely used due to its high power-conversion efficiency [9]–[11]. Operating under different modes tends to be an effective method of reducing power consumption [12], [13]. As such, the embedded digital systems or microprocessors operating at high speed need to switch between different modes [14], [15]. During the dynamic loading change and the operation mode transfer, a massive load current change can induce a large undershoot/overshoot from the output voltage for a significantly long time owing to the transient regulation latency [12]. The undershoot voltage may cause missing of data and operation distortion under high speed scenario, whereas the overshoot voltage may contribute extra power loss and even damage the ambient devices and the overall chip. The long settling time limits the system mode switching frequency, and thus it may deteriorate the overall system performance and narrow its application scenarios [4]. In this prospective, fast-transient response becomes one of the key requirements for DC-DC converters in high performance applications [11], [16]–[19].

FIGURE 1 shows the block diagram of a DC-DC converter which comprises the power stage and the controller stage. The transient response is mainly constrained by the controller stage delay and the LC limitation of power stage [20]–[23]. Various techniques have been reported to achieve fast-transient response and reliable output voltage.

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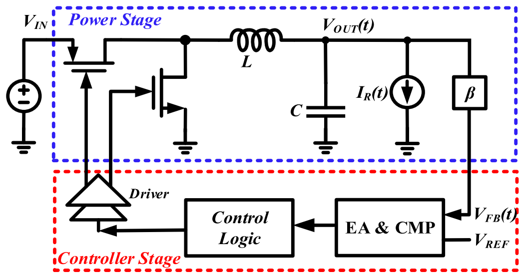

FIGURE 1. The Conceptual Block Diagrams of a DC-DC Converter.

Some of them focus on speeding up the controller stage at the expense of increased system complexity. Although the adaptive bandwidth compensation techniques [24], [25] and the capacitor multiplier techniques [26] aim to extend the compensated bandwidth, their transient responses are still limited by the OTA bandwidth through the frequency compensation in compromising overall closed-loop stability. In addition, V^2 converters are successful by introducing the feedforward path to bypass the slow error amplifier (EA) [12], [18], [27], but this approach may suffer from the subharmonic oscillation [8], [27]. Regarding the hysteretic converters, they offer faster response time and better-guaranteed stability using the compensation-free controller stage [28]–[33]. Moreover, these converters can operate at Pulse Frequency Modulation (PFM) mode automatically under the light load conditions to reduce the frequency-dependent switching loss, thus improving the light load efficiency [27], [34]. However, the transient speed of existing hysteretic converters is still constrained by the inductor. To overcome this limitation, an auxiliary current pump is applied to bypass the inductor, compensating the load current change for enhanced transient response [35]–[39]. The prior reported analog control topology in [4] is applied to achieve an instant current injection and a smooth turning-off, but it requires careful design of compensation network for stability whilst at expense of circuit complexity. Transient improvement of the auxiliary current is degraded by the compensated bandwidth of the error amplifier control loop. Besides, several voltage-triggering current pump sources inject auxiliary current by detecting the output voltage directly, supporting fast auxiliary current injection [36]–[38]. However, without output tracked turning-off control, multiple undershoot/overshoot may be induced when the current pump sources are turned off instantly, thus deteriorating the expected transient performance and the system stability. Although digital slope control scheme can avoid instantly turning-off control for current pump [20], [39], it requires complicated components and topology. In this work, a fast-transient hysteretic buck converter with a digital-controlled Power-Driving-Tracked-Duration (PDTD) scheme for the auxiliary current pump source is proposed. The auxiliary current is injected and hold for a long enough time to optimize the transient improvement of the auxiliary current. The current duration is well-defined to track the output variation through the effective digital control method. Due to hysteretic based design, it can eliminate the need of compensation network as encountered in analog approach whilst it yields low cost design by using simple digital components. It overcomes the above stated drawbacks whilst providing the optimal performance tradeoff arising from the transient enhancement technique.

This paper is organized as follows. Section II presents the respective time-domain transient analysis for the conventional and proposed voltage-mode hysteretic DC-DC converters. Section III presents the system and circuit design of the proposed fast-transient DC-DC converter. Section IV shows the circuit and system implementation. Section V discusses the measurement results and the performance comparison with the representative reported works. Section VI gives the concluding remarks.

II. LOAD TRANSIENT RESPONSE ANALYSIS

In this Section, the undershoot transient response for the voltage-mode hysteretic converter is analyzed at the output node shown in Fig. 2(a) and Fig. 2(b). The current-voltage relationships in Fig. 2(a) are obtained as follows:

$$I_R(t) = I_L(t) + I_C(t) \tag{1}$$
$$V_{out}(t) = V_C(t) - I_C(t)R_C \tag{2}$$

The transient behavior of the inductor current $I_L(t)$ and the load current $I_R(t)$ are assumed as

$$I_R(t) = \begin{cases} m_1 t & 0 < t < t_{Edge} \\ I_R & t_{Edge} < t < t_{\mathrm{Recover}} \end{cases} \tag{3}$$

$$I_L(t) = \begin{cases} m_2 t & 0 < t < t_{Max} \\ -m_3 t + (m_2 + m_3)t_{Max} & t_{Max} < t < t_{\mathrm{Recover}} \end{cases} \tag{4}$$

where m_1 and m_2 are the ramp-up slopes of $I_R(t)$ and $I_L(t)$, respectively and $m_1 \gg m_2$. -m_3 is the falling slope of $I_L(t)$. V_{OUT} is the designed dc output voltage and $I_R = V_{OUT}/R$ is the corresponding load current at V_{OUT}.

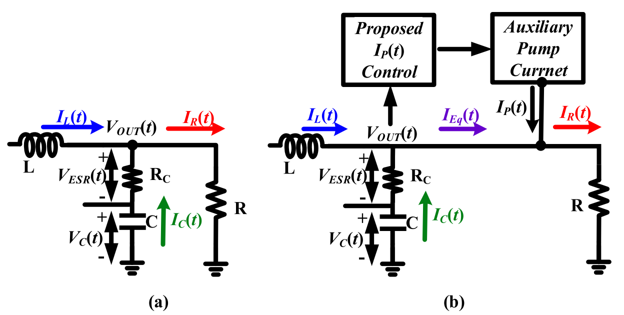

FIGURE 2. Output Node of the Voltage-mode Hysteretic DC-DC Converter (a) without $I_P(t)$ (b) with PDTD $I_P(t)$.

A. WITHOUT I_P (T)

The analysis is based on Fig. 2(a). and the case A timing waveforms are shown in Fig. 3. The key response waveforms are shown in Fig. 4.

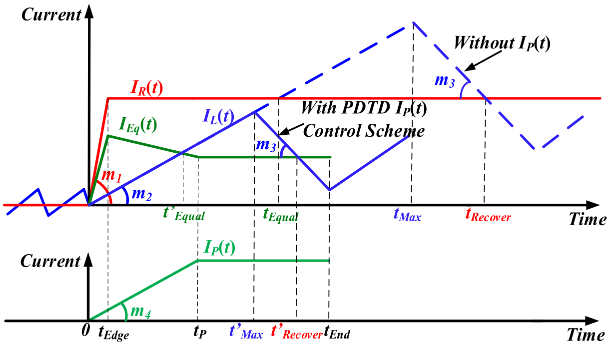

FIGURE 3. Timing Diagrams of $I_R(t)$, $I_L(t)$ [dotted line] for Case A and $I_R(t)$, $I_L(t)$ [full line], $I_{Eq}(t)$ and $I_P(t)$ for Case B.

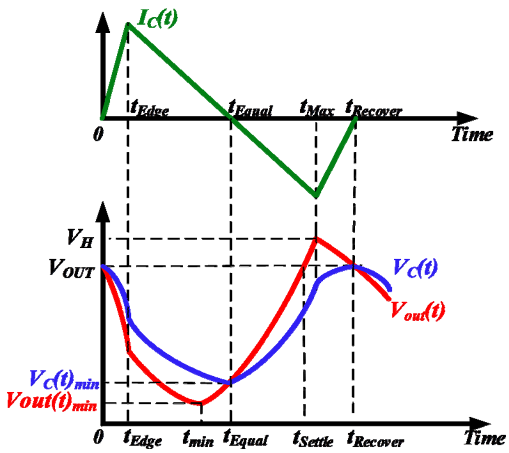

FIGURE 4. Response Waveforms for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ in Case A.

1) REGION_A1: $0 < t < t_{edge}$

In this region, assuming $V_C(0) = V_{out}(0) = V_{OUT}$, we have

$$I_C(t) = \Delta m \times t \tag{5}$$

$$V_C(t) = -\frac{1}{2C}\Delta mt^2 + V_{OUT} \tag{6}$$

$$V_{out}(t) = -\frac{1}{2C}\Delta mt^2 - \Delta mR_C t + V_{OUT} \tag{7}$$

where $\Delta m = m_1 - m_2$.Since $I_C(t) > 0$, the output capacitor C is discharged and a negative $V_{ESR}(t)$ is induced across R_C. As a result, both $V_C(t)$ and $V_{out}(t)$ decrease within $[0, t_{Edge}]$, causing large undershoot variation. If $I_R(t)$ ramps very rapidly where $\frac{t_{Edge}}{2C} \ll R_C$ can be easily fulfilled, then

$$V_{out}(t) \approx -\Delta mR_C t + V_{OUT} \tag{8}$$

The output variation $\Delta V_{out}(t) = V_{OUT} - V_{out}(t)$ mainly consists of the negative $V_{ESR}(t)$ and hence $V_{out}(t)$ decreases linearly.

2) REGION_A2: $t_{Edge} < t < t_{Max}$

$$I_C(t) = -m_2 t + I_R \tag{9}$$

$$V_C(t) = \frac{1}{2C}m_2t^2 - \frac{I_R}{C}t + \frac{I_R^2}{2m_1C} + V_{OUT} \tag{10}$$

$$V_{out}(t) = \frac{1}{2C}m_2t^2 + (m_2R_C - \frac{I_R}{C})t - I_RR_C + \frac{I_R^2}{2m_1C} + V_{OUT} \tag{11}$$

$I_C(t)$ is decreasing, and $I_C(t) = 0$ when $I_L(t) = I_R$. Solving $dV_C(t)/dt = 0$ to yield $t_{Equal} = I_R/m_2$. Hence, at $t = t_{\text{Equal}}$, we have

$$V_C(t)_{\min} = V_{OUT} - \frac{\Delta mI_R^2}{2m_1m_2C} \tag{12}$$

Similarly, solving $dV_{our}(t)/dt = 0$ to yield $V_{out}(t)_{min}$ at the time $t_{min} = I_R/m_2\text{-}CR_C$, we have

$$V_{out}(t)_{\min} = V_{OUT} - \frac{\Delta mI_R^2}{2m_1m_2C} - \frac{m_2R_C^2C}{2}t \tag{13}$$

The undershoot variation ΔV_{UN} is obtained as follows:

$$\Delta V_{UN} = V_{OUT} - V_{out}(t)_{\min} = \frac{\Delta mI_R^2}{2m_1m_2C} + \frac{m_2R_C^2C}{2} \tag{14}$$

Since $V_{out}(t)$ of the voltage-mode hysteretic converter is regulated by itself, when $t > t_{min}$, $V_{out}(t)$ rises continuously until $V_{out}(t)$ reaches the high-side boundary of the window comparator V_H. The settling time t_{Settle} is assumed when $V_{\text{out}}(t) = V_{OUT}$. As such, the settling time expression is obtained as

$$t_{Settle} = \sqrt{\frac{2C\Delta V_{UN}}{m_2}} + \frac{I_R}{m_2} - R_C C \tag{15}$$

When, $V_{out}(t) = V_H$, we have

$$t_{Max} = \sqrt{\frac{2C(\Delta V_{WIN} + \Delta V_{UN})}{m_2}} + \frac{I_R}{m_2} - R_C C \tag{16}$$

ΔV_{WIN} is the hysteretic window, given by $\Delta V_{WIN} = V_H - V_{OUT}$.

3) REGION_A3: $t_{Max} < t < t_{Recover}$

In this region, the $I_L(t)$ ramps down and we have

$$I_C(t) = m_3 t + [I_R - (m_2 + m_3)t_{Max}] \tag{17}$$

In this case, $I_C(t) < 0$ and it continuously charges up C. When $t = t_{Recover}$, $I_C(t) = 0$ and $V_{out}(t_{Recover}) = V_C(t_{Recover})$. At this juncture, $I_C(t)$ finishes one complete discharging and charging cycle after the change of load current.

Table 1 summarizes the time domain expressions for key parameters. Both ΔV_{UN} and t_{Settle} are highly dependent on the load current magnitude I_R. The transient performance can be improved by reducing I_R. Of particular noted, the I_R is the magnitude value over $[t_{Edge}, t_{Recover}]$. This gives the proposed improvement by means of adding the current pump $I_P(t)$, as illustrated in Fig. 2(b), to bypass L so as to compensate the change of $I_L(t)$. In order to enhance the transient performance, the $I_P(t)$ in this work is designed to be hold until t_{End} as indicated in Fig. 3.

TABLE 1. Transient parameters for Case A and Case B.

Parameters	**Case A [Without $I_P(t)$]**	**Case B [With $I_P(t)$]**
$V_C(t)_{min}$	$V_{OUT}-\frac{\Delta m I_R^2}{2m_1m_2C}$	$V_{OUT}-\frac{\Delta m' I_R^2}{2m_1m_2'C}$
$V_{out}(t)_{min}$	$V_{OUT}-\frac{\Delta m I_R^2}{2m_1m_2C}-\frac{m_2C\cdot R_C^2}{2}$	$V_{OUT}-\left[\frac{I_R^2}{2m'_2C}+\frac{m'_2R_C^2C}{2}\right]+\frac{m_1t_{Edge}^2}{2C}$
ΔV_{UN}	$\frac{\Delta m I_R^2}{2m_1m_2C}+\frac{m_2C\cdot R_C^2}{2}$	$\frac{\Delta m' I_R^2}{2m_1m_2'C}+\frac{m_2'C\cdot R_C^2}{2}$
t_{Settle}	$\sqrt{\frac{2C\Delta V_{UN}}{m_2}+\frac{I_R}{m_2}}-R_CC$	$\sqrt{\frac{2C(V_{OUT}-k)}{m_2}+(\frac{I_{Eq}}{m_2})^2+(R_CC)^2}+\frac{I_{Eq}}{m_2}-R_CC$
k	N.A.	$k=-\frac{m_4}{2C}t_P^2+\frac{m_1t_{Edge}^2}{2C}+V_{OUT}$

B. WITH PDTD I_P (T)

The analysis is based on Fig. 2(b) and the Case B timing waveforms in Fig. 3. The key response waveforms are shown in Fig. 5. In this case, the $I_P(t)$ in $[0, t_{End}]$ is described as

$$I_P(t)=\begin{cases} m_2t & 0<t<t_P \\ I_P & t_P<t<t_{End} \end{cases} \tag{18}$$

1) REGION_B1: $0<t<t_{Edge}$

$$I_C(t)=\Delta m' t \tag{19}$$

$$V_C(t)=-\frac{1}{2C}\Delta m' t^2+V_{OUT} \tag{20}$$

$$V_{out}(t)=-\frac{1}{2C}\Delta m' t^2-\Delta m' R_C t+V_{OUT} \tag{21}$$

If $\frac{t_{Edge}}{2C} \ll R_C$, we have

$$V_{out}(t)\approx-\Delta m' R_C t+V_{OUT} \tag{22}$$

where $\Delta m' = m_1 - m_2 - m_4$ and $\Delta m' < \Delta m$.With the injected $I_P(t)$, a smaller $I_C(t)$ is required to compensate the change of $I_L(t)$ while $V_C(t)$ and $V_{out}(t)$ become larger. This is because $I_P(t)$ helps to compensate the change of $I_R(t)$, reducing the discharge current $I_C(t)$. Consequently, $V_C(t)$ decreases with a smaller rate and ΔV_{ESR} becomes smaller, leading to reduced ΔV_{UN}.

2) REGION_B2: $t_{Edge}<t<t_P$

In this region, $I_R(t) = I_R$ while $I_P(t)$ keeps on increasing. As a result, $I_{Eq}(t) = I_R$-m_4t is reducing and the same goes for $I_C(t)$. The corresponding transient relationship for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ can be obtained as follows:

$$I_C(t)=-m'_2t+I_R \tag{23}$$

$$V_C(t)=\frac{1}{2C}m'_2t^2-\frac{I_R}{C}t+\frac{m_1t_{Edge}^2}{2C}+V_{OUT} \tag{24}$$

$$V_{out}(t)=\frac{m'_2t^2}{2C}+\frac{m'_2R_CC-I_R}{C}t+\frac{m_1t_{Edge}^2-2I_RR_CC}{2C}+V_{OUT} \tag{25}$$

where $m'_2 = m_2 + m_4$. Solving $dV_C(t)/dt = 0$ to yield $t = t'_{Equal} = I_R/m'_2$, we have

$$V_C(t)_{\min}=-\frac{I_R^2}{2m'_2C}+\frac{m_1t_{Edge}^2}{2C}+V_{OUT} \tag{26}$$

Solving $dV_{out}(t)/dt = 0$, it yields $t_{\min} = t'_{Equal} - R_CC$, assuming $t_{min}> t_{Edge}$ we have

$$V_{out}(t)_{\min}=-[\frac{I_R^2}{2m'_2C}+\frac{m'_2R_C^2C}{2}]+\frac{m_1t_{Edge}^2}{2C}+V_{OUT} \tag{27}$$

$$\Delta V_{UN}=[\frac{I_R^2}{2m'_2C}+\frac{m'_2R_C^2C}{2}]-\frac{m_1t_{Edge}^2}{2C} \tag{28}$$

Comparing with Case A, $I_C(t)$ decreases with a larger slope in this region. $V_C(t)_{min}$ becomes larger. Equation (27) indicates $V_{out}(t)_{\min}$ varies with respect to m'_2, in which $m'_2 = m_2 + m_4$, and it gives $\frac{\delta V_{out}(t)_{min}}{\delta m_4}$ over $[0, \frac{I_R}{R_CC} - m_2]$. Assumed that $t_{min}>t_{Edge}>0$, we have $m_4<\frac{I_R}{R_CC} - m_2$. Hence, $V_{out}(t)_{min}$ increases with respect to m_4 over $[0, \frac{I_R}{R_CC} - m_2]$ and becomes larger in Case B, and hence the ΔV_{UN} is reduced through $I_P(t)$.

3) REGION_B3: $t_P<t<t'_{Max}$

In this region, $I_P(t) = I_P$ and the equivalent output current $I_{Eq}(t) = I_{Eq} = I_R - I_P$. The corresponding transient relationship for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ can be obtained as follows:

$$I_C(t)=-m_2t+I_{Eq} \tag{29}$$

$$V_C(t)=\frac{m_2}{2C}t^2-\frac{I_{Eq}}{C}t-\frac{m_4t_P^2}{2C}+\frac{m_1t_{Edge}^2}{2C}+V_{OUT} \tag{30}$$

$$V_{out}(t)=\frac{m_2}{2C}t^2-\frac{I_{Eq}}{C}t+m_2R_Ct-I_{Eq}R_C-\frac{m_4}{2C}t_P^2+\frac{m_1t_{Edge}^2}{2C}+V_{OUT} \tag{31}$$

In this region, $I_C(t) < 0$, C is charged up. Both $V_C(t)$ and $V_{out}(t)$ rise with an increasing slope over $[t_P, t'_{Max}]$. As such, the transient settling time will be significantly reduced.

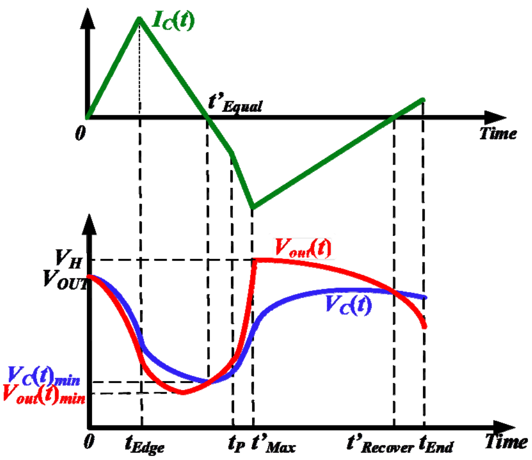

FIGURE 5. Response Waveforms for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ in Case B.

This gives

$$t'_{Settle} = \sqrt{\frac{2C(V_{OUT}-k)}{m_2}+(\frac{I_{Eq}}{m_2})^2+(R_C C)^2}+\frac{I_{Eq}}{m_2}-R_C C \tag{32}$$

When $V_{out}(t) = V_H$, the time becomes

$$t'_{Max} = \sqrt{\frac{2C(V_H-k)}{m_2}+(\frac{I_{Eq}}{m_2})^2+(R_C C)^2}+\frac{I_{Eq}}{m_2}-R_C C \tag{33}$$

where k is a constant and $k = -\frac{m_4}{2C}t_P^2 + \frac{m_1 t_{Edge}^2}{2C} + V_{OUT}$. Comparing with Case A, we have $I_{Eq} < I_R$, and it can be proved that $t'_{Settle}{<}t_{Settle}$ with $I_P{<}I_R$.

4) REGION_B4: $T'_{Max} < t < t_{End}$

In this region, $I_L(t)$ decreases. $I_C(t){<}0$ and it is given as

$$I_C(t) = m_3 t + [I_{Eq} - (m_2 + m_3)t'_{Max}] \tag{34}$$

The $I_C(t)$ continuously charges up C. When $t = t'_{Recover}$, $I_C(t) = 0$ and $V_{out}(t'_{Recover}) = V_C(t'_{Recover})$. At this juncture, $I_C(t)$ finishes one complete discharging and charging cycle after the change of load current. The transient parameters in Case A and Case B are summarized in Table 1. It proves that both ΔV_{UN} and t_{Settle} can be reduced through holding on the $I_P(t)$.

III. CIRCUIT AND SYSTEM IMPLEMENTATION

Fig. 6 illustrates the whole system architecture of the voltage-mode hysteretic buck converter with the proposed PDTD control stage. The output capacitor is required to have a large ESR value to provide sufficient output voltage ripple $\Delta V_{out}(t)$. As suggested in [31], [40], the required minimum ESR value can be estimated by

$$R_C > \sqrt{\frac{L(V_H - V_L)}{C}\left(\frac{1}{V_{IN}-V_{OUT}} + \frac{1}{V_{OUT}}\right)} \tag{35}$$

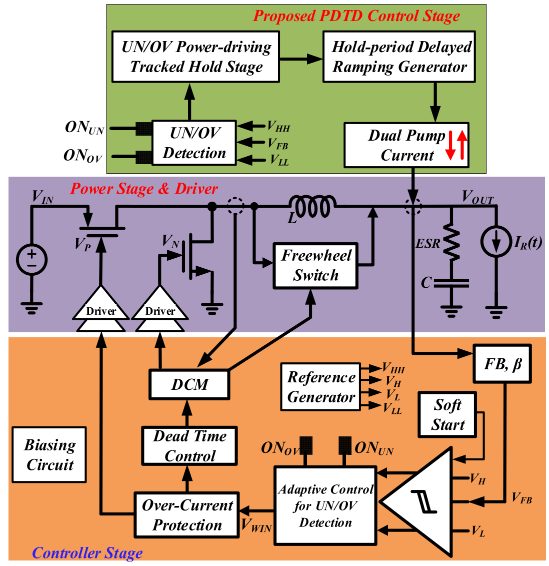

FIGURE 6. Overall system of the proposed PDTD buck converter.

where V_L is the low-side boundary of the window comparator and the other symbols have been defined before. With the large ESR, $V_{out}(t)$ is dominant by the $V_{ESR}(t)$ and it is fed to the hysteretic comparator, generating the voltage signal V_{WIN} as well as the adaptive control signals of undershoot/overshoot detection circuit, ON_{UN} and ON_{OV}. V_{WIN} is used to regulate $I_L(t)$ through controlling the power transistors. The PFM control is added to improve the light load efficiency. Dual current pump sources are employed to compensate the large current difference between $I_R(t)$ and $I_L(t)$. They are triggered on by the undershoot/overshoot detection signal. The $I_P(t)$ turning-on duration is modulated by the power-driving-tracked-hold stage whereas the turning-off mechanism is controlled by the hold-period delayed ramping generator. The detailed circuit implementation of the proposed transient enhanced stage will be described in the following sub-sections.

A. UNDERSHOOT/OVERSHOOT DETECTION STAGE

In this work, the undershoot/overshoot is detected through a pair of adaptively-biased comparators [41]. As shown in Fig. 7, the adaptive biasing signals ON_{UN} and ON_{OV} are generated through the hysteretic comparator. They are added to reduce the standby power consumption of the undershoot and overshoot detection comparators. Once V_{FB} is larger than the overshoot detection reference V_{HH}, the OV goes to high. When V_{FB} is smaller than the undershoot detection reference V_{LL}, UN goes to high.

B. POWER-DRIVING-TRACKED-HOLD STAGE

In this work, the $I_P(t)$ hold-on duration is designed to track $V_{out}(t)$ variation such that a sufficient hold-on duration is guaranteed to enhance the transient response. In the meantime, once $V_{out}(t)$ settles down, $I_P(t)$ will be turned off to save power.

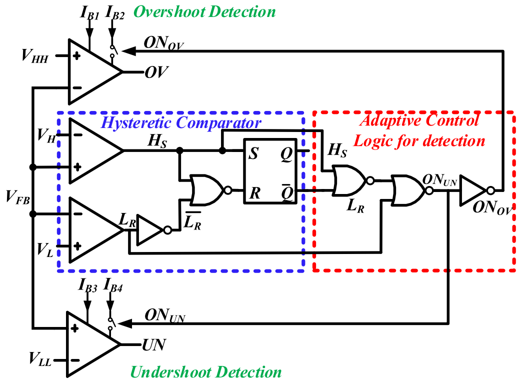

FIGURE 7. Undershoot/overshoot detection stage.

This methodology is realized through the power-driving-tracked-hold stage in Fig. 8. It consists of two sub-stages: (1) wide pulse trigger stage with an exclude stage logic which is formed by the cross-coupled NAND gates and (2) pulse duration control stage.

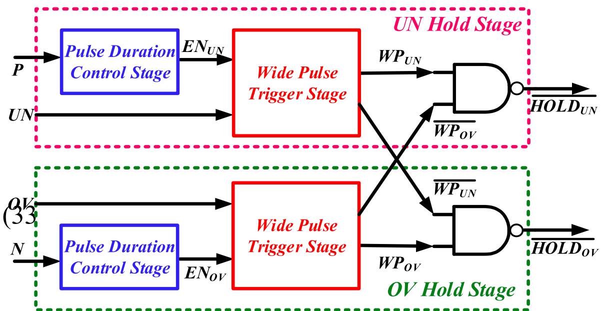

FIGURE 8. Power-driving-tracked-duration hold stage.

The wide pulse trigger stage is to extend the undershoot/overshoot detection signal *UN*/*OV* such that it provides a long enough turning-on duration for $I_P(t)$. The endpoint of wide pulse signal WP_{UN}/WP_{OV} is determined by the pulse duration control stage, which detects $V_{out}(t)$ by monitoring the power transistor driving voltage P and N. The exclude stage logic is to guarantee that *UN* and *OV* are exclusively extended. $\overline{WP_{UN}}/\overline{WP_{OV}}$ is the inverting signal of WP_{UN}/WP_{OV}. EN_{UN} and EN_{OV} is the pulse duration control signal for undershoot and overshoot wide pulse trigger stage, respectively. $\overline{HOND_{UN}}/\overline{HOND_{OV}}$ is the output signal of the dual pulse hold stage for undershoot/overshoot.

C. WIDE PULSE TRIGGER STAGE

In Fig. 7, the *UN*/*OV* state of output signal changes whenever V_{FB} crosses V_{HH}/V_{LL}, giving fast detection speed. However, this narrow *UN*/*OV* pulse output causes insufficient turning-on duration for the $I_P(t)$. To guarantee fast detection as well as sufficient turning-on duration, the turning-on and turning-off mechanism of $I_P(t)$ is separated in this work. This is realized through the wide pulse trigger stage as illustrated in Fig. 9.

When $EN_{UN} = 1$, the equivalent wide pulse trigger stage is shown in Fig. 10(a). When $V_{FB} < V_{LL}$, the narrow detection pulse *UN* goes to high, setting $\overline{WP_{UN}}$ to 0 and WP_{UN} to high. When $V_{FB}>V_{HH}$, *UN* drops to 0. Due to the feedback logic, $\overline{WP_{UN}}$ will be latched to 0 by itself and the WP_{UN} is kept at high. In this case, a wide pulse WP_{UN} can be triggered by the narrow *UN* pulse and the pulse duration of WP_{UN} is independent of *UN*. When $EN_{UN} = 0$, the equivalent circuit is shown in Fig. 10(b). In this case, EN_{UN} will cut off the logic path and reset the wide pulse WP_{UN} to 0 regardless of *UN* state. The narrow trigger pulse *UN* is extended to a wide pulse WP_{UN} to provide sufficient hold-on duration for current pump $I_P(t)$. The rising edge of WP_{UN} is only triggered by *UN* when $EN_{UN} = 1$. On the other hand, the falling edge of WP_{UN} is only controlled by the falling edge of EN_{UN}. In this way, the turning-on and turning-off mechanism of $I_P(t)$ is then separated. The falling edge of EN_{UN} is realized through the pulse duration control stage.

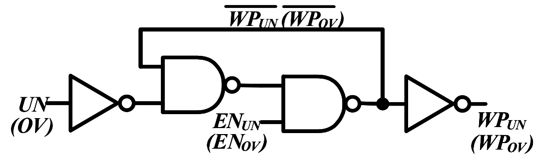

FIGURE 9. Wide pulse trigger stage.

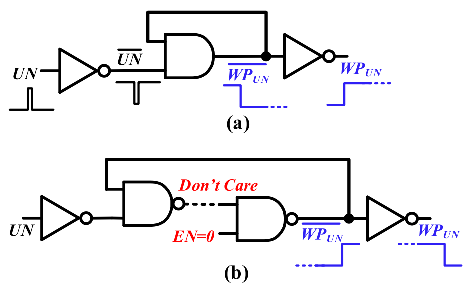

FIGURE 10. Equivalent Circuit for Wide Pulse Trigger Stage (a) $EN_{UN} = 1$, (b) $EN_{UN} = 0$.

The exclude stage logic circuit, which consists of the cross-coupled NAND gates, is added after the wide pulse trigger stage. It is to ensure the wide pulse WP_{UN}/WP_{OV} cannot be passed at the same time. As such, it avoids turning on the dual auxiliary current pump simultaneously. Hence, it helps to protect the overall system and reduce the power loss.

D. PULSE DURATION CONTROL STAGE

To improve the transient response of the voltage-mode hysteretic DC-DC converter, $I_P(t)$ is required to be hold for a long enough time. After $V_{out}(t)$ recovers back, $I_P(t)$ is required to be turned off to save power. In this work, the endpoint of $I_P(t)$ duration is designed to be at t_{End} in Fig. 3. In the voltage-mode hysteretic buck converter, a large ESR value is required to keep $V_{out}(t)$ in phase with $I_L(t)$ and $I_L(t)$ is directly controlled by the power PMOS/NMOS transistor. Hence, the endpoint t_{End} can be determined by monitoring the power PMOS/NMOS transistor driving voltage P/N. This is realized through the circuit as depicted in Fig. 11.

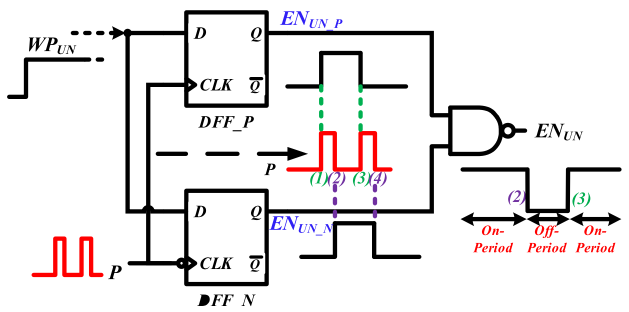

FIGURE 11. Pulse duration control stage.

DFF_P and DFF_N represents the positive and negative edge triggering D flip flop, respectively. WP_{UN} is the wide pulse triggered by the undershoot detection signal UN. P is the power PMOS transistor driving voltage. Edges (1) and (3) are the positive edges and edges (2) and (4) are the negative edges. EN_{UN_P} and EN_{UN_N} are generated when WP_{UN} goes through the flip flops DFF_P and DFF_N, respectively. EN_{UN} is the pulse duration control signal. When EN_{UN} is high, the wide pulse trigger stage is activated, and if UN is triggered, the wide pulse WP_{UN} will be generated. On the other hand, when EN_{UN} is low, the WP_{UN} will reset to 0 regardless of the state of UN.

E. HOLD PERIOD DELAYED RAMPING GENERATOR

After the output voltage settles down, $I_P(t)$ is turned off at t_{End}. However, if $I_P(t)$ is turned off instantly, a large current difference between $I_L(t)$ and $I_P(t)$ will be generated, which has the same effect as the change of $I_R(t)$. As observed, multiple undershoot/overshoot effect will be induced [36], [37], deteriorating the transient response and the system stability. This problem can be solved by turning off $I_P(t)$ slowly such that the change of $I_P(t)$ change can be compensated by $I_L(t)$. This is realized by generating a ramping period to slow down the ramping-up speed of $I_P(t)$ control voltage $V_{GS}(t)$, which is illustrated in Fig. 12. $\overline{HOLD}$ and $\overline{V_{RAMP}}$ indicates the power-driving-tracked-hold signal and the $I_P(t)$ control voltage $V_{GS}(t)$, respectively.

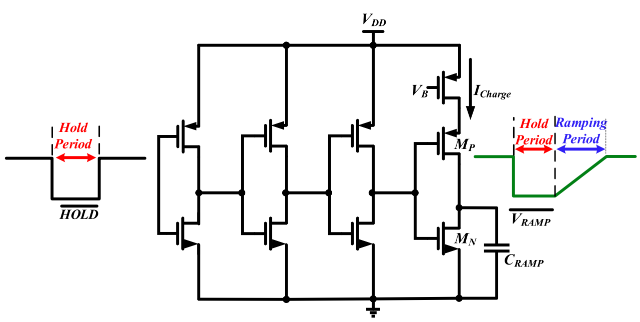

FIGURE 12. Hold period delayed ramping generator.

$\overline{V_{RAMP}}$ is required to go down instantly to enhance the transient response. On the other hand, a relatively slow ramp-up slope is needed to avoid multiple undershoot/overshoot effect. M_N has relatively larger aspect ratio than that of M_P. Once a large undershoot is detected, the $\overline{HOLD}$ will be triggered to logic 0, discharging the capacitor C_{RAMP} rapidly through the large size M_N. As a result, $\overline{V_{RAMP}}$ is pulled down instantly whereas $I_P(t)$ is triggered on instantly to enhance the transient response. After $V_{out}(t)$ recovers back, $\overline{HOLD}$ is reset to high at t_{End} instantly to cut off $I_P(t)$. Different from the $\overline{HOLD}$, a ramping period is generated in $\overline{V_{RAMP}}$ by a relatively small constant current I_{Charge} to slow down the $I_P(t)$ changing rate. If $I_L(t)$ can compensate the change of $I_P(t)$, the multiple undershoots/overshoots will be significantly reduced or even eliminated. The ramp-up rate of $\overline{V_{RAMP}}$ is given as follows:

$$\frac{d\overline{V_{RAMP}}(t)}{dt} = \frac{I_{Charge}}{C_{RAMP}} \tag{36}$$

F. DUAL CURRENT PUMP SOURCE

As shown in Fig. 13, either the current pump I_{P_UN} or I_{P_OV} is injected to the output node directly. Both I_{P_UN} and I_{P_OV} are designed to be supply independent through the constant biasing current I_1 to I_4. S_1 to S_7 are controlled by the ramping voltage for undershoot or overshoot. Hence, I_{P_UN}/I_{P_OV} can be instantly turned on to enhance the transient response and slowly turned off to reduce the multiple undershoot/overshoot. During the steady state, S_1 to S_5 are turned on, pulling V_{P1}, V_{P2} and V_{P3} up to V_{DD} while pulling V_{N1} and V_{N2} down to ground. In this way, I_{P_UN} and I_{P_OV} can be totally off to save power. I_1 and I_3 are always on to speed up the current pump start-up process. I_2 and I_4 are adaptively controlled by S_6 and S_7 to reduce the quiescent current.

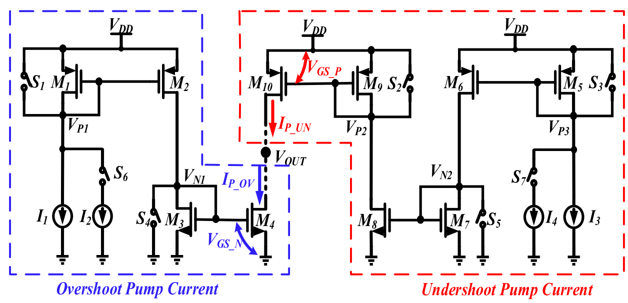

FIGURE 13. Dual current pump source.

G. DCM OPERATION

The DCM control algorithm is added to eliminate the reverse current, thus improving the light load efficiency [5].The reverse current detection is realized by the common gate comparator [42]. A large size free-wheel switch (FWS) transistor is added to reduce the ring effect when both NMOS and PMOS are turned off [43].

IV. RESULTS AND DISCUSSIONS

The proposed converter has been fabricated using TSMC 40nm CMOS process which is suitable for low-voltage SoC applications, the micrograph is shown in Fig. 14. The occupied silicon area is 830μm$\times$620μm. Other support blocks

TABLE 2. Performance comparison with the reported works.

	[11] JSSC 2015	[27] TCASI 2015	[33] ISSCC 2015	[6] JSSC 2015	[44] TVLSI 2016	[20] ISSCC 2017	[21] TVLSI 2018	[22] TPE 2018	[23] TCASII 2019	This Work
Process (nm)	350	350	350	40	350	130	350	28	65	**40**
V_{in} **(V)**	2.7-4.2	2.7-4.2	2.7-4.5	2.7-3.6	2.4-3.6	3.3	2.6-4.0	3.3	3.3	**1.2-2.5**
V_{out} **(V)**	0.8-2.4	1.2	2	0.8-2.1	0.2-3.3	1.2-1.8	1.2	1.05	1~2.5	**0.6-2.1**
I_L **(mA)**	<2000	18-700	N.A	<900	600	1250	600	0.3-1.7	900	**450**
ΔV_{out} **(mV$_{pk}$)**	10#	15	15#	30#	15	12#	45	6	40#	**30**
L **(μH)**	1	2.2	4.7	4.7	4.7	0.09	4.7	1	4.7	**4.7**
C **(μF)**	4.7	10	10	4.7	10	0.94	10	4.7	4.7	**4.7**
Freq. (MHz)	1.25	1	1	1	1	30	1	2.5	1	**1.45**
ΔI_L **(mA)**	500	300	400	100	450	1250	300	1400	450	**240**
$t_{L\text{-}H}$ **(μs)**	0.9	3	4.8	15	2.1	0.22	2.5	4	2	**0.369**
ΔV_{UN} **(mV)**	25	48	35	30	>120	72	167	75	65	**73**
$t_{H\text{-}L}$ **(μs)**	0.9	5	3	15	3.5	0.15	2.8	5	3	**0.335**
ΔV_{OV} **(mV)**	35	30	38	30	>160	33	180	90	70	**72**
η_{peak} **(%)**	90	95.7	95.5	89	91	83.6	90	94	92	**93**
FOM (10^{-6})	0.254	2.364	0.757	4.5	1.853	0.08	3.261	1.246	0.375	**0.106**

$$\mathrm{FOM} = \frac{\Delta t(\mu\mathrm{s}) \times \Delta V_{spike}(mV) \times C(\mu\mathrm{F})}{L(\mu\mathrm{H}) \times \Delta I_L(mA)} \quad \text{where } \Delta t = \frac{\Delta t_{L\_H} + \Delta t_{L\_H}}{2} \text{ and } \Delta V_{spike} = \frac{\Delta V_{UN} + \Delta V_{OV}}{2}$$

#-extracted from data

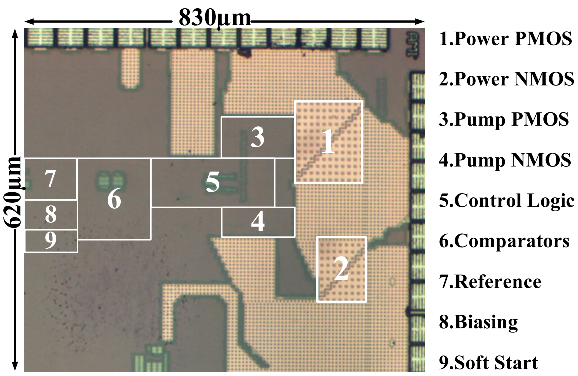

FIGURE 14. Micrograph of the proposed fast-Transient converter.

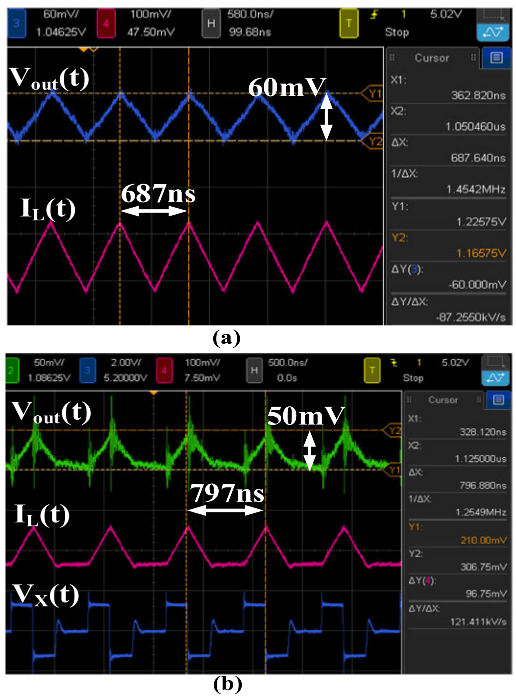

FIGURE 15. Steady state waveforms in (a)CCM; (b)DCM.

such as dead time control, over-current protection and soft start circuits are also realized in the DC-DC converter in order to protect the overall system and maintain the power efficiency. The fabricated fast-transient DC-DC buck converter has been tested with the input voltage of 2.5V and the nominal output voltage of 1.2V. The output capacitor is 4.7μF and the inductor is 4.7μH.

A. STEADY-STATE MEASUREMENT

The steady-state measurement results for CCM and DCM are illustrated in Fig. 15(a) and Fig. 15(b), respectively. Fig. 15(a) shows the steady-state waveforms of the output voltage $V_{out}(t)$ and the inductor current $I_L(t)$ at the load current of 60mA. It has validated that the proposed converter can regulate properly in CCM. The output ripple is about 30mV$_{\text{pk}}$ whereas the switching frequency is about 1.45MHz. It also shows that the $V_{out}(t)$ is in phase with the $I_L(t)$ because of the large ESR in the voltage-mode hysteretic converter as discussed in Section III. Fig. 15(b) shows the waveforms of the output voltage $V_{out}(t)$, the inductor current $I_L(t)$ and the switching node voltage $V_X(t)$ at the load current of 20mA. It has confirmed the design methodology of the DCM operation. During the light load condition, the reverse current can be detected and eliminated. The ringing at the output node can be significantly reduced by applying the FSW control. As a result, the light load efficiency is improved. The efficiency at different load currents is plotted in Fig. 16. The peak efficiency η_{peak} is 93% at 60mA at $V_{out} = 1.2$V. Finally, due to the PFM control of hysteretic converters under DCM, the light load efficiency at 20mA is close to 90%.

B. TRANSIENT RESPONSE MEASUREMENT

For the conventional hysteretic buck converter without the $I_P(t)$, the undershoot and overshoot transient response

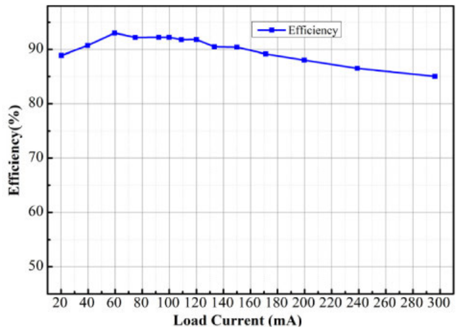

FIGURE 16. Power Efficiency at Different Load Currents at $V_{out} = 1.2V$.

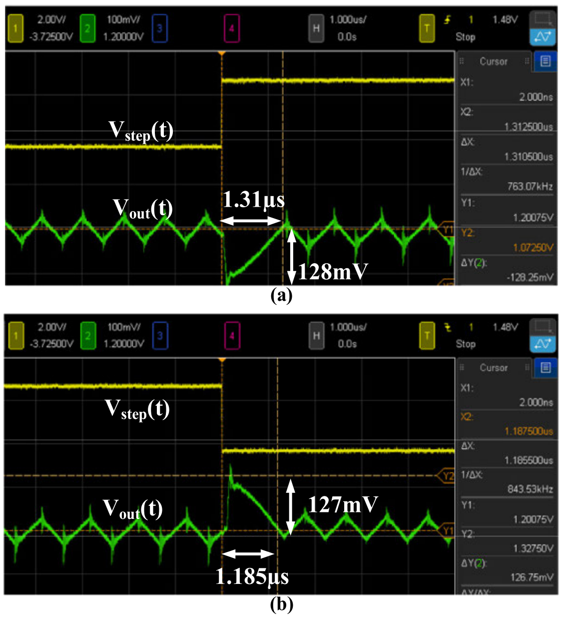

FIGURE 17. Output Transient Reponses for (a) Step-Up Load Change, (b) Step-Down Load Change without $I_P(t)$.

for the 60-to-300mA and 300-to-60mA load current change under the load current control signal $V_{step}(t)$ is illustrated in Fig. 17(a) and Fig. 17(b), respectively. The edge time of the current load step is about 5ns. The undershoot/overshoot variation $\Delta V_{UN}/\Delta V_{OV}$ is 128mV/127mV whereas the undershoot/overshoot transient settling time t_{L-H}/t_{H-L} is 1.31μs/1.185μs.

For the hysteretic buck converter with PDTD $I_P(t)$, the undershoot/overshoot transient response for the 60-to-300mA/300-to-60mA load current change is depicted in Fig. 18(a) and Fig. 18(b), respectively. In comparison to the conventional counterpart, the undershoot/overshoot variation $\Delta V_{UN}/\Delta V_{OV}$ is reduced to 73mV/72mV whereas the transient settling time t_{Settle} is improved to 369ns/335ns. This suggests that the proposed work offers 350% faster than that of the conventional counterpart, validating the effectiveness of the PDTD control scheme.

C. PERFORMANCE COMPARISON

Table 2 shows the performance comparison of the converter with the reported state-of-art works. In order to

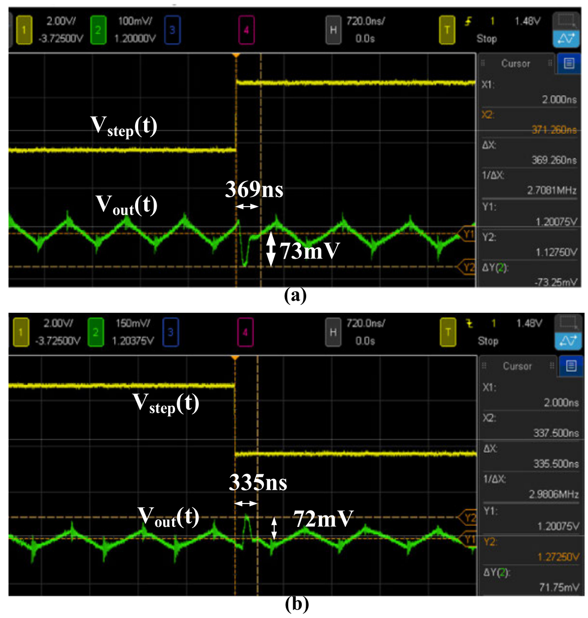

FIGURE 18. Output Transient Reponses for (a) Step-Up Load Change, (b) Step-Down Load Change with Proposed PDTD $I_P(t)$.

compare the transient-response effectiveness under different settings and load transient steps, a normalization based FOM is established. It includes the LC components value, the average setting time Δt, the average voltage ΔV_{spike} and the load transient step ΔI_L. This FOM takes both transient settling time and transient spike voltage into consideration. It also normalizes the LC component effect under different load steps. The smaller FOM gives better transient response performance. The proposed method has achieved an excellent FOM value and peak efficiency simultaneously. It has demonstrated the converter provides fast transient response together with balanced performance metrics.

V. CONCLUSION

The analysis, design and circuit implementation of the voltage-mode hysteretic DC-DC buck converter using the digital-based PDTD control scheme for generating well-defined digital-controlled auxiliary current pump are presented. The measurement results have shown that the converter regulates properly in both CCM and DCM. With freewheel switch control, the ringing at the output node can be significantly reduced. Through the PDTD control scheme, the transient response time of the voltage-mode hysteretic DC-DC buck converter can be significantly reduced with respect to most of representative prior-art topologies. Not only does it provide sufficient turning-on duration of the current pump to speed up the transient response, it also reduces the multiple undershoot/overshoot significantly whilst maintaining reasonable ripple voltage and efficiency at low output voltage to yield the balance performance metrics. Compared with conventional converter without PDTD control scheme, it improves the transient response time by 350%.

Hence, the proposed digital-based PDTD current pump technique is very useful for realizing fast-transient response in DC-DC buck converters.

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REFERENCES

[1] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC–DC converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, Jan. 2004, doi: 10.1109/JSSC.2003.820870.

[2] P. Y. Wu and P. K. T. Mok, "A monolithic buck converter with near-optimum reference tracking response using adaptive-output-feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2441–2450, Nov. 2007, doi: 10.1109/JSSC.2007.907169.

[3] S. Zhou and G. A. Rincon-Mora, "A high efficiency, soft switching DC-DC converter with adaptive current-ripple control for portable applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 4, pp. 319–323, Apr. 2006, doi: 10.1109/TCSII.2005.859572.

[4] K.-I. Wu, B.-T. Hwang, and C. C.-P. Chen, "Synchronous double-pumping technique for integrated current-mode PWM DC–DC converters demand on fast-transient response," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 849–865, Jan. 2017, doi: 10.1109/TPEL.2016.2537214.

[5] B. Sahu and G. A. Rincn-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 312–321, Feb. 2007, doi: 10.1109/TCSI.2006.887472.

[6] W.-C. Chen, Y.-P. Su, T.-C. Huang, T.-W. Tsai, R.-H. Peng, K.-L. Lin, K.-H. Chen, Y.-H. Lin, C.-C. Lee, S.-R. Lin, and T.-Y. Tsai, "Single-inductor quad-output switching converter with priority-scheduled program for fast transient response and unlimited load range in 40 nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1525–1539, Jul. 2015, doi: 10.1109/JSSC.2015.2422071.

[7] R. W. Erickson, and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2001.

[8] B. Choi, *Pulsewidth Modulated DC-to-DC Power Conversion*. Hoboken, NJ, USA: Wiley-IEEE Press, 2013.

[9] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003, doi: 10.1109/JSSC.2003.811976.

[10] Y.-H. Lee, Y.-Y. Yang, K.-H. Chen, Y.-H. Lin, S.-J. Wang, K.-L. Zheng, P.-F. Chen, C.-Y. Hsieh, Y.-Z. Ke, Y.-K. Chen, and C.-C. Huang, "A DVS embedded power management for high efficiency integrated SoC in UWB system," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2227–2238, Nov. 2010, doi: 10.1109/JSSC.2010.2063610.

[11] S.-H. Chien, T.-H. Hung, S.-Y. Huang, and T.-H. Kuo, "A monolithic capacitor-current-controlled hysteretic buck converter with transient-optimized feedback circuit," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2524–2532, Nov. 2015, doi: 10.1109/JSSC.2015.2464720.

[12] C.-H. Tsai, S.-M. Lin, and C.-S. Huang, "A fast-transient quasi-V^2 switching buck regulator using AOT control with a load current correction (LCC) technique," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3949–3957, Aug. 2013, doi: 10.1109/TPEL.2012.2230649.

[13] F.-F. Ma, W.-Z. Chen, and J.-C. Wu, "A monolithic current-mode buck converter with advanced control and protection circuits," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1836–1846, Sep. 2007, doi: 10.1109/TPEL.2007.904237.

[14] X. Zhou, P.-L. Wong, P. Xu, F. C. Lee, and A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1172–1182, Nov. 2000, doi: 10.1109/63.892832.

[15] S. Bandyopadhyay, Y. K. Ramadass, and A. P. Chandrakasan, "20 μA to 100 mA DC–DC converter with 2.8-4.2 v battery supply for portable applications in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2807–2820, Dec. 2011, doi: 10.1109/JSSC.2011.2162914.

[16] P. Y. Wu, S. Y. S. Tsui, and P. K. T. Mok, "Area-and power-efficient monolithic buck converters with pseudo-type III compensation," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1446–1455, Jul. 2010, doi: 10.1109/JSSC.2010.2047451.

[17] W.-H. Ki, K.-M. Lai, and C. Zhan, "Charge balance analysis and state transition analysis of hysteretic voltage mode switching converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 1142–1153, May 2011, doi: 10.1109/TCSI.2010.2089557.

[18] F. Su and W.-H. Ki, "Digitally assisted quasi-V2 hysteretic buck converter with fixed frequency and without using large-ESR capacitor," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 446–447, doi: 10.1109/ISSCC.2009.4977500.

[19] K.-H. Chen, H.-W. Huang, and S.-Y. Kuo, "Fast-transient DC–DC converter with on-chip compensated error amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 12, pp. 1150–1154, Dec. 2007, doi: 10.1109/TCSII.2007.905884.

[20] L. Cheng and W. Ki, "10.6 A 30 MHz hybrid buck converter with 36 mV droop and 125ns 1% settling time for a 1.25 A/2ns load transient," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2017, pp. 188–189, doi: 10.1109/ISSCC.2017.7870324.

[21] J.-J. Chen, Y.-S. Hwang, J.-H. Chen, Y.-T. Ku, and C.-C. Yu, "A new fast-response current-mode buck converter with improved I^2 -Controlled techniques," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 903–911, May 2018, doi: 10.1109/TVLSI.2018.2796088.

[22] W.-H. Yang, C.-J. Huang, H.-H. Huang, W.-T. Lin, K.-H. Chen, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "A constant-on-time control DC–DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6187–6198, Jul. 2018, doi: 10.1109/TPEL.2017.2746659.

[23] J.-D. Suh, J. Seok, and B.-S. Kong, "A fast response PWM buck converter with active ramp tracking control in a load transient period," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 467–471, Mar. 2019, doi: 10.1109/TCSII.2018.2865643.

[24] Y.-H. Lee, S.-C. Huang, S.-W. Wang, and K.-H. Chen, "Fast transient (FT) technique with adaptive phase margin (APM) for current mode DC-DC buck converters," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 10, pp. 1781–1793, Oct. 2012, doi: 10.1109/TVLSI.2011.2163093.

[25] C.-Y. Hsieh and K.-H. Chen, "Adaptive pole-zero position (APZP) technique of regulated power supply for improving SNR," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2949–2963, Nov. 2008, doi: 10.1109/TPEL.2008.2003014.

[26] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008, doi: 10.1109/TPEL.2007.911776.

[27] K.-Y. Hu, S.-M. Lin, and C.-H. Tsai, "A fixed-frequency quasi-V^2 hysteretic buck converter with PLL-based two-stage adaptive window control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2565–2573, Oct. 2015, doi: 10.1109/TCSI.2015.2466791.

[28] S. Dietrich, R. Wunderlich, and S. Heinen, "Stability considerations of hysteretic controlled DC–DC converters," in *Proc. PRIME*, 2012, pp. 79–82.

[29] P. Li, D. Bhatia, L. Xue, and R. Bashirullah, "A 90–240 MHz hysteretic controlled DC-DC buck converter with digital phase locked loop synchronization," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2108–2119, Sep. 2011, doi: 10.1109/JSSC.2011.2139550.

[30] S. C. Huerta, A. Soto, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Advanced control for very fast DC-DC converters based on hysteresis of the C_{out} current," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 4, pp. 1052–1061, Apr. 2013, doi: 10.1109/TCSI.2012.2209308.

[31] R. Redl and J. Sun, "Ripple-based control of switching regulators—An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009, doi: 10.1109/TPEL.2009.2032657.

[32] Y. Zheng, H. Chen, and K. N. Leung, "A fast-response pseudo-PWM buck converter with PLL-based hysteresis control," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 7, pp. 1167–1174, Jul. 2012, doi: 10.1109/TVLSI.2011.2156437.

[33] S. H. Lee, J. S. Bang, K. S. Yoon, S. W. Hong, C.-S. Shin, M.-Y. Jung, and G.-H. Cho, "A 0.518 mm^2 quasi-current-mode hysteretic buck DC-DC converter with 3 μs load transient response in 0.35 μm BCDMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 58, Feb. 2015, pp. 1–3, doi: 10.1109/ISSCC.2015.7063002.

[34] C. Huang and P. K. T. Mok, "An 84.7% efficiency 100-MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhanced light-load efficiency," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2595–2607, Nov. 2013, doi: 10.1109/JSSC.2013.2274826.

[35] Y.-H. Lee, S.-Y. Peng, C.-C. Chiu, A. C.-H. Wu, K.-H. Chen, Y.-H. Lin, S.-W. Wang, T.-Y. Tsai, C.-C. Huang, and C.-C. Lee, "A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1018–1030, Apr. 2013, doi: 10.1109/JSSC.2013.2237991.

[36] P.-J. Liu, Y.-K. Lo, H.-J. Chiu, and Y.-J. Emery Chen, "Dual-current pump module for transient improvement of step-down DC–DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 985–990, Apr. 2009, doi: 10.1109/TPEL.2008.2010322.

[37] P.-J. Liu, H.-J. Chiu, Y.-K. Lo, and Y.-J.-E. Chen, "A fast transient recovery module for DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2522–2529, Jul. 2009, doi: 10.1109/TIE.2009.2017555.

[38] Z. Shan, C. K. Tse, and S.-C. Tan, "Classification of auxiliary circuit schemes for feeding fast load transients in switching power supplies," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 930–942, Mar. 2014, doi: 10.1109/TCSI.2013.2284174.

[39] Y. Wen and O. Trescases, "DC–DC converter with digital adaptive slope control in auxiliary phase for optimal transient response and improved efficiency," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3396–3409, Jul. 2012, doi: 10.1109/TPEL.2011.2181871.

[40] B. C. Bao, G. H. Zhou, X. Zhang, J. P. Xu, and J. Yang, "Effect of output capacitor ESR on dynamic performance of voltage-mode hysteretic controlled buck converter," *Electron. Lett.*, vol. 49, no. 20, pp. 1293–1294, Sep. 2013, doi: 10.1049/el.2013.2043.

[41] R. Prakash, "A 110nA quiescent current buck converter with zero-power supply monitor and near-constant output ripple," in *Proc. IEEE Dallas Circuits Syst. Conf. (DCAS)*, Oct. 2014, pp. 1–4, doi: 10.1109/DCAS.2014.6965326.

[42] Y. Gao, S. Wang, H. Li, L. Chen, S. Fan, and L. Geng, "A novel zero-current-detector for DCM operation in synchronous converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2012, pp. 99–104, doi: 10.1109/ISIE.2012.6237066.

[43] M. Du, H. Lee, and J. Liu, "A 5-MHz 91% Peak-Power-Efficiency buck regulator with auto-selectable Peak-and valley-current control," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1928–1939, Aug. 2011, doi: 10.1109/JSSC.2011.2151470.

[44] W.-C. Chen, C.-C. Chen, C.-Y. Yao, and R.-J. Yang, "A fast-transient Wide-Voltage-Range digital-controlled buck converter with cycle-controlled DPWM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 1, pp. 17–25, Jan. 2016, doi: 10.1109/TVLSI.2015.2405548.

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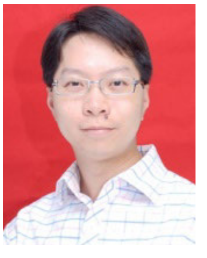

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