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A Front-End Amplifier With Current Compensation Feedback Input Impedance Booster for Neural Signal Applications

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ABSTRACT In integrated circuit form, the front-end amplifier (FEA) determines the fidelity of the biosignal detection, signal-to-noise ratio, power consumption and detector size for the future multi-channel neural signal recording systems and applications. Especially for the high-density implantable applications, a higher input impedance reduces the signal attenuation (with respect to the high-impedance miniature electrodes), and lowers the current into the tissue (to avoid the overheating damage). In this paper, an input impedance booster with current compensation feedback technique is proposed, it neutralizes any currents generated at input of FEA without affecting the gain. It substantially yields a high input impedance across process and device mismatches. The proposed front-end circuit is implemented on a 0.18μm CMOS process, it achieves an input impedance of approximately 60 GΩ, and CMRR of 61 dB with 57 dB PSRR. The input-referred noise is approximately 5.6 μv/$\sqrt{}$Hz while consuming 7.6 μW in 0. 025mm^{2}chip area.

INDEX TERMS Analog integrated circuits, biomedical signal processing, CMOS integrated circuits, biomedical monitoring, input impedance booster, preamplifiers.

I. INTRODUCTION

Growing research interests in biomedical applications demand neural interfacing systems which are capable of simultaneously monitoring the activity of large numbers of neurons [1]–[4]. Especially for wearable and implantable applications, two most significant evaluations of integrated front-end circuity are the power consumption and die area. A higher power efficiency increases the system lifetime to avoid battery changing, and to protect the tissue from overheating damage. A smaller form factor allows more high-density recording channels [5], [6]. Neural signals, such as electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) shown in Fig.1, are low in both amplitude and frequency [7]. To monitor and record such signals, a front-end amplifier (FEA) with relatively wide percentage bandwidth, low noise, high input impedance and low power consumption is required. It determines not only the fidelity of the neural signals, but also impacts the power consumption and detector size of multi-channel systems.

Capacitive feedback (CF) technique is widely used in neural signal recording FEAs. As shown in Fig.2(a), the gain is configured by the ratio of capacitors, and the tissue/electrode DC offset is simultaneously rejected by input coupling capacitor [1]. Chopper stabilization (CS) technique reduces the noise of CF FEAs. It modulates the signal to higher frequency, to avoid the amplification of the low frequency noise (such as the flicker noise) [6], [8]–[10]. However, the input impedance of CF and CS FEA is limited by the input capacitor. The impedance of different types of interface and electrode invariably form a voltage divider [8], [11]–[14]. The higher the input impedance of the FEA, the lower the attenuation caused by the interface. Moreover, a higher input impedance lowers the current into the tissue, to avoid the overheating damage (especially for long-term implantable applications).

The input impedance of CF and CS FEA can be increased by the input impedance (Z_{in}) boosters, such as capacitive path (CP) and auxiliary path (AP) technique. As shown in Fig.2(b),

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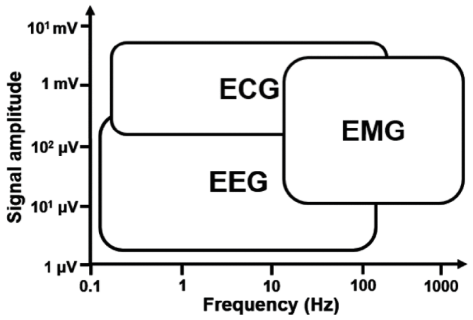


FIGURE 1. Amplitude and frequency range of typical neural signals.

CP boosters uses a precisely-chosen capacitor to match with the input capacitance [15]. However, any manufacturing and operating variations will lead to a mismatch between these capacitances, which reduces the input impedance and destabilizes such positive feedback [16].

AP booster yields a pre-charged voltage buffer and input capacitor, as shown in Fig.2(c), to neutralize the chopped currents [17]. The input impedance of AP booster is limited by the need for satisfying the gain of FEA. The feedforward axillary path (FFAP) technique can further increase the impedance. As depicted in Fig.2(d), FFAP adds a current feedback stage to reduce the input capacitor [18].

Hence, the input capacitor limits the impedance of FEAs, due to the need for the gain and suppress DC offset. In this paper, a new current compensation feedback input impedance booster for FEA is proposed, it neutralizes any current generated by the input capacitor, without affecting the gain.

II. PROPOSED CURRENT COMPENSATION FEEDBACK TECHNIQUE

A. FEA WITH CURRENT COMPENSATION FEEDBACK Z_{in} BOOSTER

The circuit schematic of the proposed FEA with current compensation feedback (CCF) Z_{in} booster is depicted in Fig.3. The amplifier A is a low noise transconductance amplifier (OTA), and the dimension of input transistors are large to lower the noise (details are discussed in Section B). The input signal is AC-coupled by capacitor C_{in} to remove the tissue and electrode DC offsets, and biased by the resistor R_b. The resistors R_1, R_2 and R_b are pseudo resistors (PRs), their tune voltages are feedback controlled to constantly provide a large and linear resistance, (details are discussed in Section C). Such that, R_b and C_{in} achieve a sub-Hz cut-off frequency.

In Fig.3, the midband gain is controlled by the ratio of the capacitors (ignoring the much larger resistance of R_1 and R_2),

$$A_{CCF} = \frac{V_{out}}{V_{in}} \approx \frac{Z_{C_1||R_1} + Z_{C_2||R_2}}{Z_{C_2||R_2}} \approx \frac{C_2}{C_1} \tag{1}$$

The input current I_{in} can be written as,

$$I_{in} = I_+ + I_b - I_{ccf} \tag{2}$$

where, I_+ is the leakage current into the '+' terminal of A, I_b is the current into the bias network [given in equation (3)]

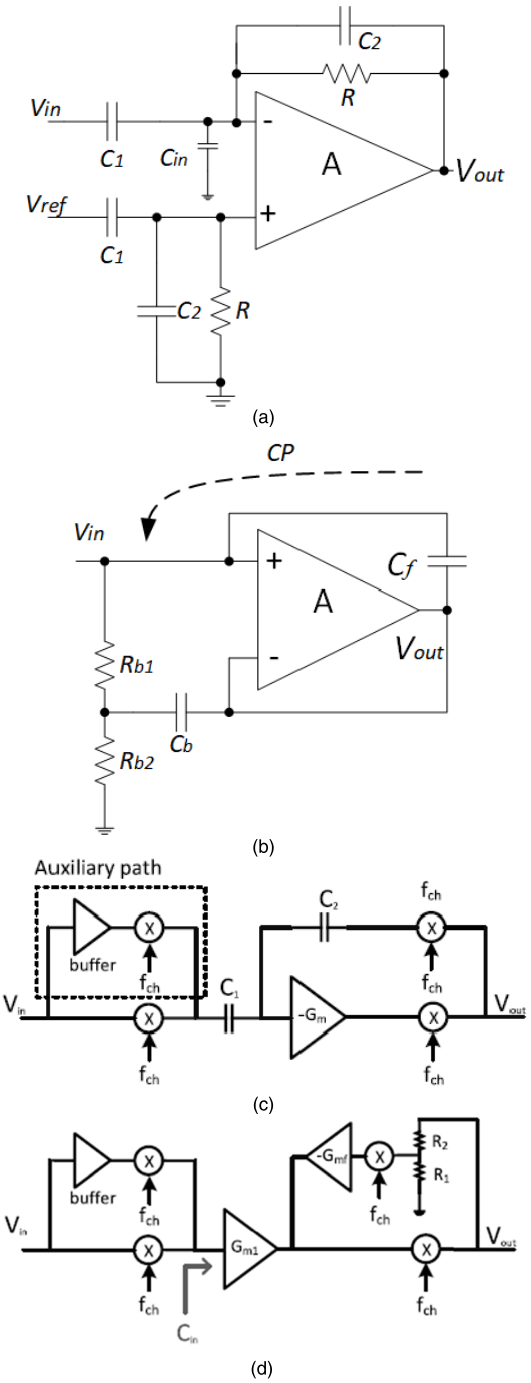


FIGURE 2. Circuit schematic of (a) CF FEA [1]. (b) CP Zin booster [15]. (c) AP Zin booster [17]. (d) FFAP Zin booster [18].

and I_{ccf} is the compensation current [given in equation (4)].

$$I_b = \frac{V_+}{Z_{C_b||R_b}} \approx \frac{V_+}{Z_{C_b}} \tag{3}$$

$$I_{ccf} \approx \frac{V_{out} - V_{in}}{Z_{C_c}} \tag{4}$$

The output voltage V_{out} ensures that the current (I_1) into C_1 and R_1 delivers the current into the '−' terminal of A and the

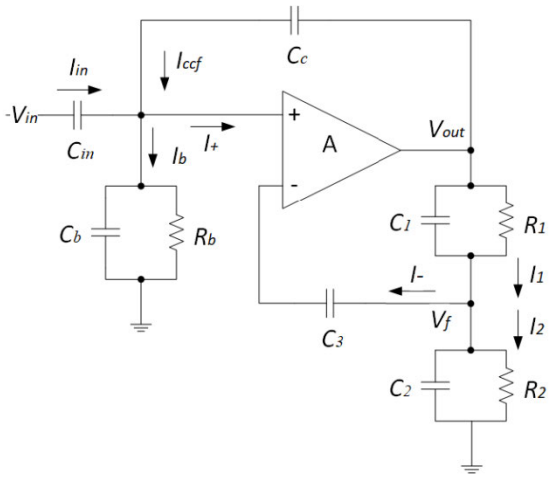


FIGURE 3. Circuit schematic of proposed FEA with CCF Zin booster.

current into C_2 and R_2,

$$I_1 = I_- + I_2 = \frac{V_{out} - V_f}{Z_{C_1}} \tag{5}$$

where, I_- is the leakage current into the '−' terminal of A (leakage currents are approximately the same $I_+ \approx I_-$, due to V_f tracking V_{in} and $C_{in} = C_3$), and I_2 can be written as,

$$I_2 = \frac{V_f}{Z_{C_2||R_2}} \approx \frac{V_{in}}{Z_{C_2}} \tag{6}$$

By setting $C_b = C_2$, equation (3) becomes,

$$I_b \approx \frac{V_+}{Z_{C_b}} \approx \frac{V_f}{Z_{C_2}} \approx I_2 \tag{7}$$

Meanwhile, by setting $C_c = C_1$, equation (4) becomes,

$$I_{ccf} \approx \frac{V_{out} - V_f}{Z_{C_1}} \approx I_1 \tag{8}$$

The input current in equation (2) can be re-written as,

$$I_{in} \approx I_+ + I_b - I_1 \approx I_+ + I_b - (I_- + I_2) \approx 0 \tag{9}$$

Therefore, as shown in equation (9), the feedback current I_{ccf} adaptively compensates for any currents generated by input capacitor, bias network and leakage current into the amplifier. The gain of this FEA, as given in equation (1), is configured by the feedback capacitors only. The proposed Z_{in} booster neutralizes any current generated by the input capacitance, without affecting the gain. The input impedance of this Z_{in} booster can be further increased by a better matching between the capacitors ($C_{in} = C_3$, $C_b = C_2$ and $C_c = C_1$, e.g. dummy capacitor), and a higher open-loop gain of amplifier A.

B. LOW-NOISE OTA

The circuit schematic of OTA is depicted in Fig.4, it comprises a bias circuit and a two-stage differential amplifier with Miller compensation. The bias circuit is formed by transistors M_{B1}-M_{B6} and resistor R_B, and transistors M_{S1}-M_{S5} yield

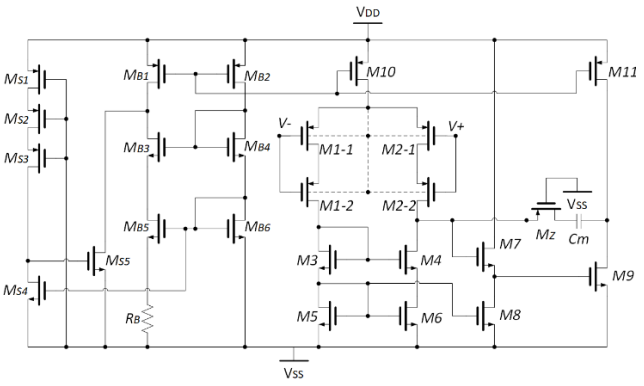


FIGURE 4. Circuit schematic of OTA.

the start-up circuit. Cascoded structure M_{B3}-M_{B6}reduces the channel length modulation effect to provide a better matching of bias currents.

The two-stage differential amplifier uses the cascoded PMOS differential pairs (*M1-1, M1-2, M2-1, M2-2*) as input device, due to the inherent lower 1/f noise over NMOS. A floating N-well back gate connection is applied on the input differential pairs, to improve the matching and to reduce the leakage current. Other transistor bulks (back gates) are connected to the appropriate rails (not explicitly shown for clarity). The Miller compensation is formed by capacitor C_m and transistor M_Z, to stabilize the amplifier. Transistors *M7* and *M8* dynamically reduce the overdrive voltage of *M9*, to increase the output swing and transconductance. The open-loop gain and gain bandwidth of the amplifier is,

$$A_{op} = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m9}}{g_{ds9} + g_{ds11}} \tag{10}$$

$$\omega_{GB} = \frac{g_{m1}}{C_m} = \frac{\sqrt{2k_p(\frac{W}{L})_1 I_{SD1}}}{C_m} \tag{11}$$

where, W and L are the width and length of a corresponding transistor, k_p is the process-dependant constant, I_{SD} is the source-to-drain current, g_m and g_{ds} are the transconductance and output conductance of the corresponding transistors respectively. Here, g_{ds4} is the equivalent output conductance of the cascoded transistor *M4* and *M6* (the equivalent length of the transistors is the sum of the corresponding cascoded gates).

The noise of the amplifier consists of the thermal noise ($\overline{V^2_{n,thermal}}$) and flicker noise ($\overline{V^2_{n,flicker}}$),

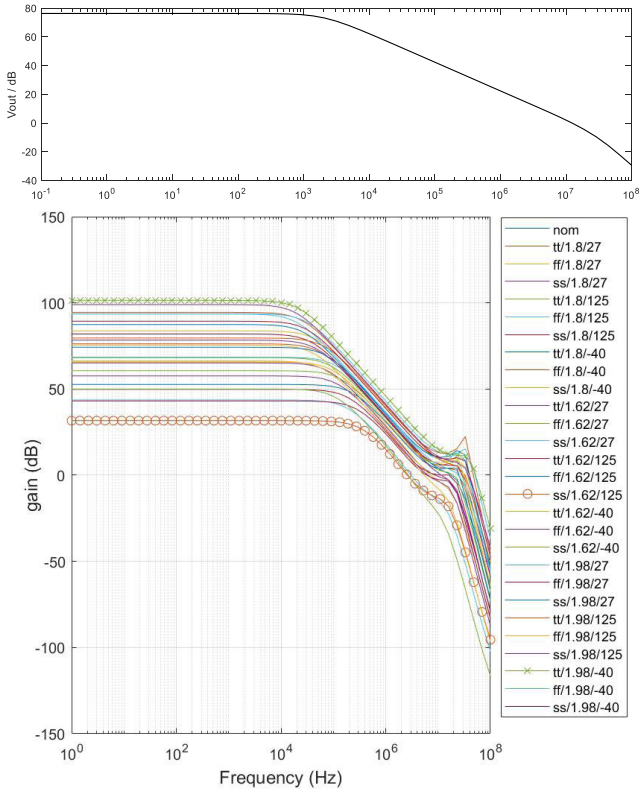
$$\overline{V^2_{n,op}} = \overline{V^2_{n\_thermal} + V^2_{n\_flicker}} \tag{12}$$

where,

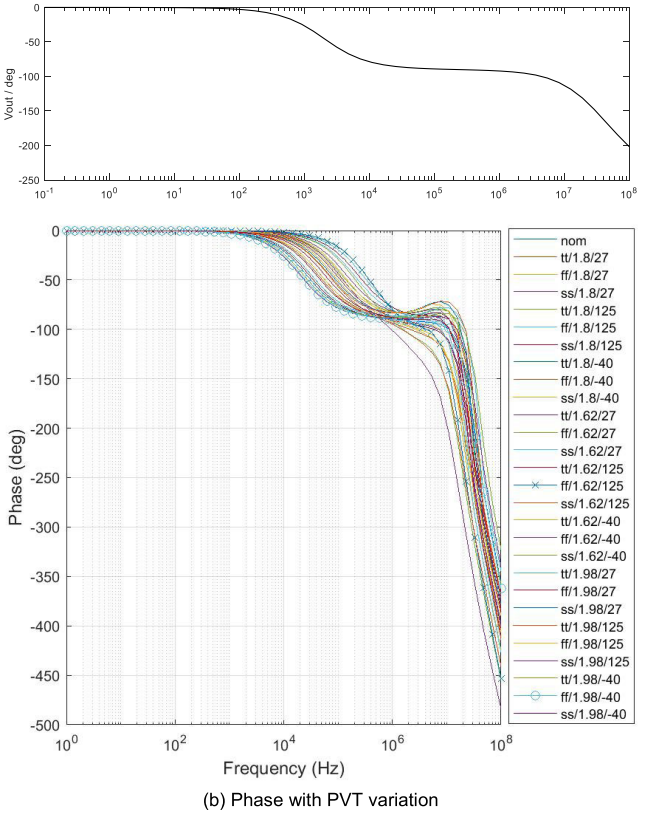
$$\overline{V^2_{n,thermal}} \approx \frac{16kT}{3}\frac{1}{g^2_{m1}}(g_{m1} + g_{m3}) \tag{13}$$

$$\overline{V^2_{n,flicker}} \approx \frac{2}{c_{ox}f}[\frac{k_p}{W_1L_1} + \frac{\mu_n k_n L_1}{\mu_p W_1 L_3^2}] \tag{14}$$

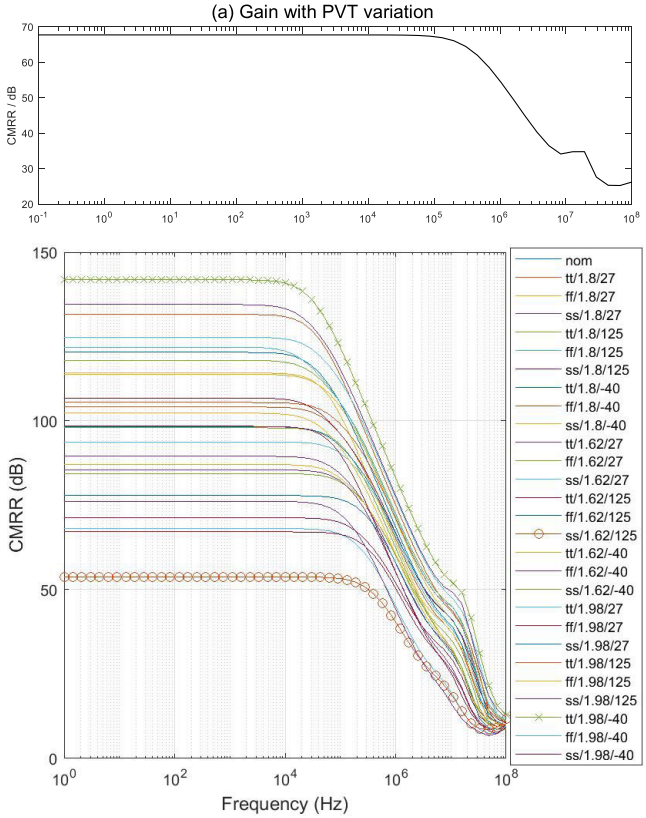
where, k is the Boltzmann constant, T is the absolute temperature, μ_p and μ_n is the mobility of PMOS and



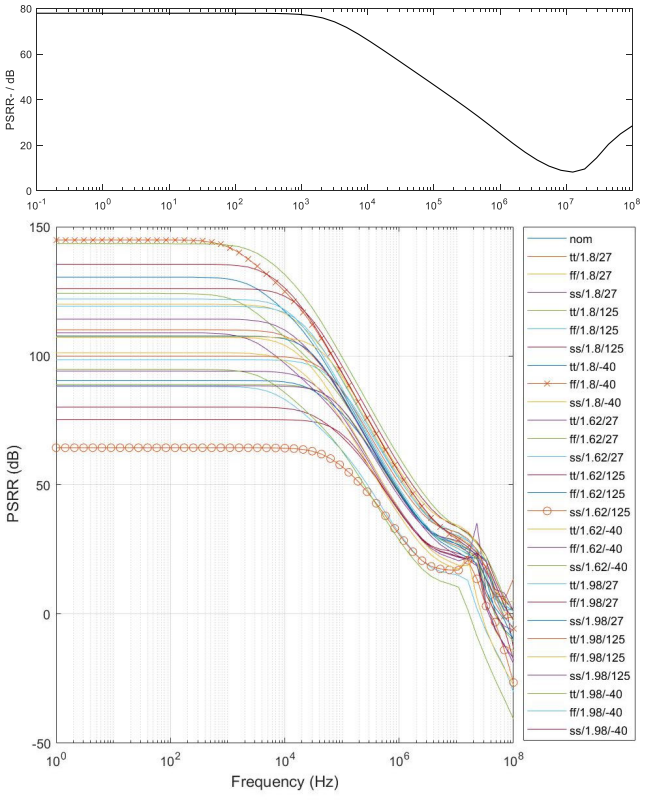
(a) Gain with PVT variation



(b) Phase with PVT variation



(c) CMRR with PVT variation



(d) PSRR with PVT variation

FIGURE 5. **Simulation analysis of OTA.**

TABLE 1. Device dimensions.

Device	Size
M1-1, M1-2, M2-1, M2-2	$2 \times {}^{36um}/_{2um}$
M3–M6	$1 \times {}^{20um}/_{25um}$
M7, M8	$1 \times {}^{4um}/_{2um}$
M9	$1 \times {}^{5um}/_{5um}$
M10	$2 \times {}^{5um}/_{4um}$
M11	$1 \times {}^{5um}/_{4um}$
Mz	$1 \times {}^{1um}/_{1um}$
M_{S1}–M_{S3}	$1 \times {}^{0.5um}/_{17um}$
M_{S4}, M_{S5}	$1 \times {}^{18um}/_{0.5um}$
M_{B1}–M_{B4}	$1 \times {}^{8.5um}/_{5um}$
M_{B5}, M_{B6}	$1 \times {}^{7.5um}/_{5um}$
M_{B7}	$1 \times {}^{12um}/_{5um}$
M_{B8}	$1 \times {}^{7.5um}/_{5um}$
C_m	$1.9pF, 2 \times {}^{30um}/_{30um}$
C_1, C_c	$100fF, 1 \times {}^{9.5um}/_{9.5um}$
C_2, C_b	$400fF, 1 \times {}^{19.3um}/_{19.3um}$
R_1, R_2, R_b (PMOS in PR)	$2 \times {}^{10um}/_{10um}$

NMOS respectively. Hence, as shown in equation (13), the thermal noise can be reduced by increasing the transconductance of *M1*. For the 1/f noise, associated with equation (14), is determined by *M1* and *M3*. In fact, flicker noise is the major contributor to the input-referred noise for neural signal applications, thus, a relatively wider *M1* and longer *M3* are chosen. The dimension of transistors and capacitors of in fig.2 and 3 are given in table 1. The simulation curves and Process, Voltage and Temperature (PVT) variations of OTA are given in Fig.5. The open-loop gain of the amplifier, as given in Fig.5(a), is approximately 76dB at typical conditions. The gain is reduced at high temperatures, especially at slow corner and low voltage. The phase margin, as given in Fig.5(b), is 62° at typical conditions. The pole is split at low temperatures, as well as the phase margin. At typical conditions, the common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) of OTA are circa 68dB and 78dB respectively. CMRR and PSRR are both reduced at high temperatures.

C. FEEDBACK CONTROLLED PSEUDO RESISTOR

Pseudo resistors, as shown in Fig.3, are used in the proposed circuit. Conventional PR comprises two transistors back-to-back to force them into sub-threshold region, which provides large resistance with a small die area [19]–[21]. The impedance of conventional PR is,

$$Z_{PR} = \frac{n\emptyset_t(1-e^{-V_{DS}/\emptyset_t})}{1 + I_{st}(n-1)e^{-V_{DS}/\emptyset_t}} \tag{15}$$

subthreshold slope, V_T is the threshold voltage, $\emptyset_t$ is the thermal voltage, V_{GS} is the gate-to-source voltage and V_{DS} is the drain-to-source voltage. Hence, as given in equation (15), linearity of conventional PR is poor as its impedance is

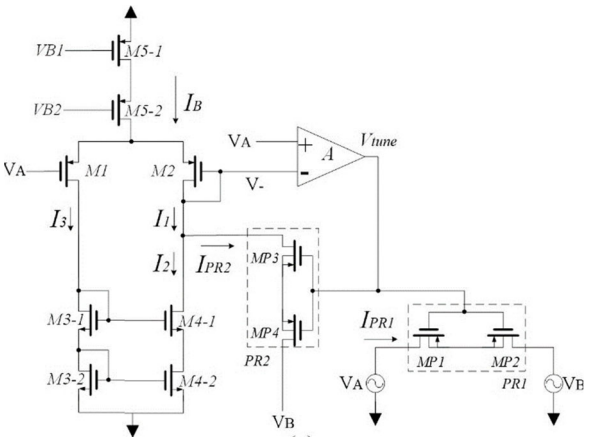


FIGURE 6. Circuit schematic of feedback controlled PR.

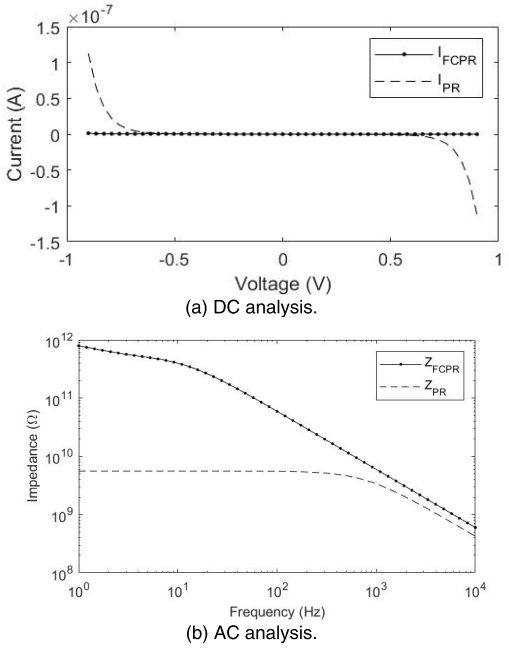


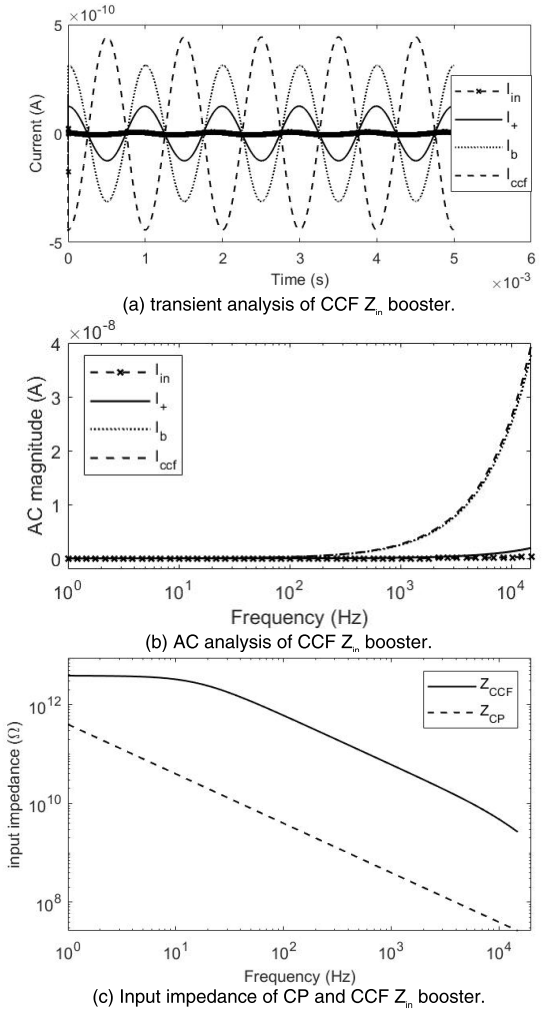
FIGURE 7. Simulation analysis of PRs.

exponentially and asymmetrically decreased by the input signal (V_{DS}). In order to increase the impedance and linearity of PR, a feedback loop is applied [19]. As given in Fig.6, *PR1* comprises two PMOS transistors *MP1* and *MP2*, V_A and V_B are two input node voltages.

The tune voltage is generated by a voltage buffer and inverter-based differential amplifier *A*. The positive input terminal of the buffer and amplifier are connected to V_A. The '−' terminal (*M2*'s gate) is connected to the output of this single-stage amplifier, to yield a voltage buffer. Another PR (*PR2*) formed by *MP3* and *MP4* is connected to the output of the buffer, the current at output is,

$$I_1 = I_2 + I_{PR2} \tag{16}$$

where, I_{PR2} is the current into *PR2*. The note voltages of *PR2* are V_B and $V-$. $V-$ is the '−' terminal voltage of both the

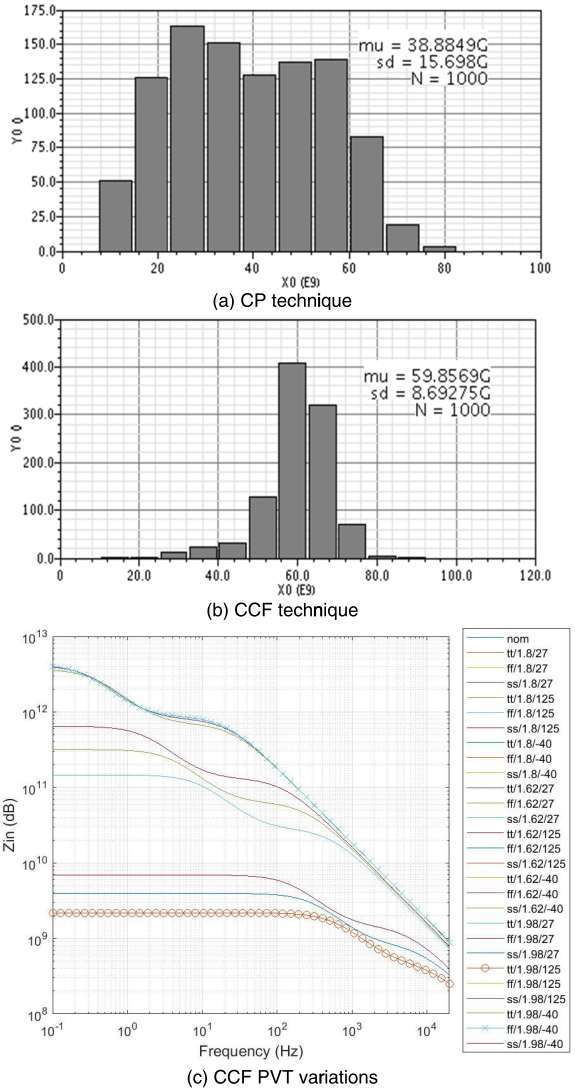


(a) transient analysis of CCF Z_{in} booster.

(b) AC analysis of CCF Z_{in} booster.

(c) Input impedance of CP and CCF Z_{in} booster.

FIGURE 8. Simulation analysis of Zin booster.



(a) CP technique

(b) CCF technique

(c) CCF PVT variations

FIGURE 9. Monte Carlo analysis of input impedance for (a) CP technique. (b) CCF technique. (c) PVT variations of CCF technique.

buffer and amplifier, written as,

$$V_- = \frac{A_{buf}}{A_{buf} + 1} V_A \tag{17}$$

where, A_{buf} is the open-loop gain of the buffer. The turn voltage of both *PR1* and *PR2* is determined by amplifier,

$$V_{tune} = A_A \left(V_A - V_-\right) \tag{18}$$

where, A_A is the open-loop gain of A. The tune voltage will be whatever necessary to decrease the voltage difference between at amplifier's terminals,

$$I_1 \approx I_2 \approx \frac{I_B}{2} \tag{19}$$

The size of both PRs is the same, and node voltages of PRs are approximately the same, hence, the current into PR is minimized by this feedback,

$$I_{PR1} \approx I_{PR2} \approx 0 \tag{20}$$

DC analysis of conventional and feedback controlled PR are given in Fig.7. I_{PR} is the current into conventional PR, which is exponentially increased when the input voltage is greater than threshold voltages. The impedance and linearity is increased by applying the feedback, the current into such PR, I_{FCPR}, yields a near constant resistance–voltage characteristics across a rail to rail DC sweep. The impedance of conventional PR is approximately 5 GΩ, and the feedback controlled PR achieves circa 890 GΩ.

III. RESULTS

The transient analysis of the CCF Z_{in} booster is shown in Fig.8(a). The input amplitude and frequency are 100 mVpp and 1kHz respectively. The current $I_+$is leakage current into the low power OTA. I_b is the current into bias network. The input current (I_{in}) is minimized as the compensation current (I_{ccf}) neutralizes all the currents generated at input. Similarly, the AC currents at the input stage of the CCF booster are shown in Fig.8(b), the input current (I_{in}) is

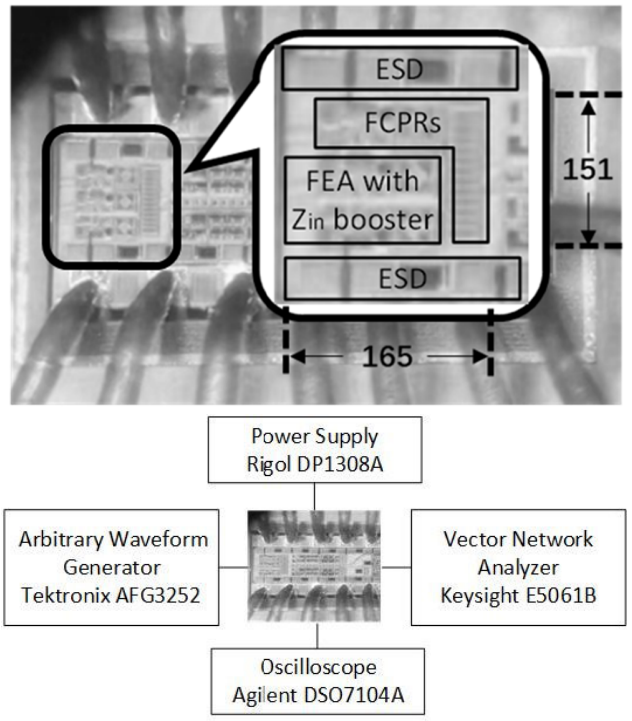


FIGURE 10. Chip photograph of the fabricated FEA with CCF Zin Booster and test conditions.

suppressed by the feedback compensation current I_{ccf}, to boost the input impedance of FEAs. The input impedance of CCF Z_{in} booster is depicted in Fig.8(c), it provides approximately 60GΩ at 100Hz. The Monte Carlo analysis of the input impedance of two boosters are given in Fig.9. The average and deviation of CP technique is approximately 39 and 15.7 GΩ, whereas the CCF achieves circa 60 and 8.7 GΩ respectively. The PVT variations of the input impedance of the CCF is reduced at high temperatures, due to the reduction of the gain for OTA. CCF Z_{in} booster constantly enhances the input impedance of neural recording amplifier. Especially in IC platform, the proposed CCF booster is less susceptible to the process and device mismatches.

The proposed CCF Z_{in} booster is designed and implemented on a 0.18μm CMOS process. The die photograph and testbench are given in Fig.10. The measured voltage gain of the proposed FEA with CCF Z_{in} booster is depicted in Fig.11. As given in Fig.3 and equation (1), the gain of the FEA is configured by the ratio of the feedback capacitors. It achieves a voltage gain of approximately 14dB at 1kHz. The gain can be simply adjusted by the capacitors. The bandwidth of this FEA is circa 0.01Hz to 23kHz. The input-referred noise is approximately 5.6 μv/$\sqrt{}$Hz at 100Hz, the noise effect factor (NEF) can be calculated as

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi V_T \cdot 4kT \cdot BW}} \tag{21}$$

where, $V_{ni,rms}$ is the input-referred noise, I_{tot} is the total current of the proposed amplifier, V_T is the thermal voltage,

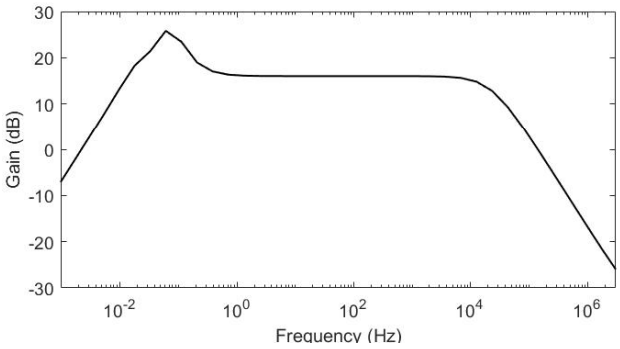


FIGURE 11. Measured voltage gain of FEA with CCF Zin booster.

TABLE 2. Properties Comparison of proposed technique with existing similar FEAs.

	[5]	[10]	[17]	[18]	This work
Process (nm)	350	180	40	180	180
Supply voltage (V)	2	1.5	1.2	1.2	1.8
Power (μW)	0.36	0.855	2.8	2.6	7.6
Gain (dB)	39.8	47.6	25.7	41-59	14
Bandwidth (Hz)	0.2-200	0.64-500	0.1-5k	0.5-5k	0.01-23k
Input impedance (Ω)	20M (200Hz)	250M	800M (100Hz)	500M (100Hz)	60G [a] (100Hz)
Input-referred noise (μv/√Hz)	2.05	2.24	5.3	2	5.6
CMRR (dB)	>70	125	-	70	61
PSRR (dB)	>65	-	-	-	57
NEF	2.26	3.8	AP 4.4 LFP 7.4	AP 3.2 LFP 9.9	AP 4.7 LFP 9.6
THD	<1% 15mV 20Hz	-	-76 dB	1.7% 1mV 1kHz	-49 dB 1mV 1kHz
Size (mm^2)	0.18	-	0.069	0.08	0.025

[a] Simulated results

k is the Boltzmann constant, T is the absolute temperature and BW is the bandwidth. The NEF of the proposed FEA is circa 4.7 and 9.6 for action potential (AP) band (200 Hz-5k Hz) and local filed potential (LFP) band (1 Hz-200 Hz).

The results are summarized in Table 2, with the comparison to other existing similar designs. The proposed FEA with CCF booster achieves a relatively high input impedance and a wide bandwidth to support different neural signal recording applications, both continues-time and chopped topology. The gain can be easily configured by feedback capacitors while the input impedance remains high by matching the capacitors [equation (7) and (8)]. As given in Table 2, the power consumption is relatively high with respect to other state-of-arts, it can be further reduced by lowering the supply voltage or bias current of OTA [22], [23], however, it may

reduce the open-loop gain of the amplifier leading to the reduction of input impedance. NEF is relatively high due to the current within the OTA design is high. The size of the proposed FEA (without ESD protection and PAD) is small. A chopper technique can be further implemented to reduce the 1/f noise, however, the complexity and area of circuit is increased.

IV. CONCLUSION

In this paper, a new input impedance booster with current compensation feedback technique is proposed for neural signal recording FEA. By placing the matched capacitors at negative feedback of the amplifier, CCF constantly compensates for any currents generated at input terminal (such as input capacitor, and leakage current into the amplifier and bias network). The current into input coupling capacitor (remove tissue and electrode DC offset) is substantially neutralized without affecting the gain, across the process and device mismatches. This topology supports both continues-time and chopped recording. The proposed FEA with Z_{in} booster is targeted at IC implementation on a standard 0.18μm CMOS process. It approximately provides an input impedance of 60GΩ (at 100Hz) and 5.6 $\mu v/\sqrt{Hz}$ input-referred noise while consuming 7.6 μW. In order to measure such ultra-high impedance, testing Pads can be placed between the feedback capacitor C_C, to measure the voltage drop across it and the high-pass cut-off frequency. The power consumption of the proposed FEA is determined by the OTA design. It can be further reduced by lowering the supply voltage and bias current of the amplifier, such that to maximize the gm/Id current efficiency. The power consumption can also be reduced by lowering the bias current of the inverted-based amplifier within the pseudo resistors design.

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